Minimization of Crosstalk Noise, Delay and Power Using a Modified Bus Invert Technique

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Abstract

Previously reported bus encoding approaches reduce crosstalk delay but they ignore the effects of inductive coupling between the bus lines, i.e. crosstalk noise. Aiming to solve this issue, this paper presents a modified bus-invert technique which minimizes crosstalk noise, as well as delay and power, at the expense of a small area overhead.

1 Introduction

Crosstalk problems affect the reliability of digital systems especially when the technology scales down and the frequency increases. Consequently several techniques such as shielding, crosstalk aware routing, buffer insertion and differential signaling have been proposed for reducing the crosstalk effects. Although these techniques effectively reduce crosstalk noise and delay they have significant drawbacks such as the increased complexity of the drivers/receivers, the significant routing overhead they insert and the high power consumed in the bus lines.

Bus encoding is another approach which addresses the problem of interconnect crosstalk while overcoming the aforementioned problems. The bus invert technique [1], was used for minimizing the power consumption in the bus lines. Further attempts, such as the coupling driven encoding scheme proposed in [2], aim to consider the coupling effects between lines as these increase the amount of power consumed on the bus. Although a few bus encoding techniques aim to reduce crosstalk delay in the bus lines due to capacitive coupling, none of them aims to reduce crosstalk noise which becomes more severe when the inductive effects are significant. This paper presents a modified bus invert technique for minimizing crosstalk noise, while taking into account both capacitive and inductive effects.

2 Crosstalk noise

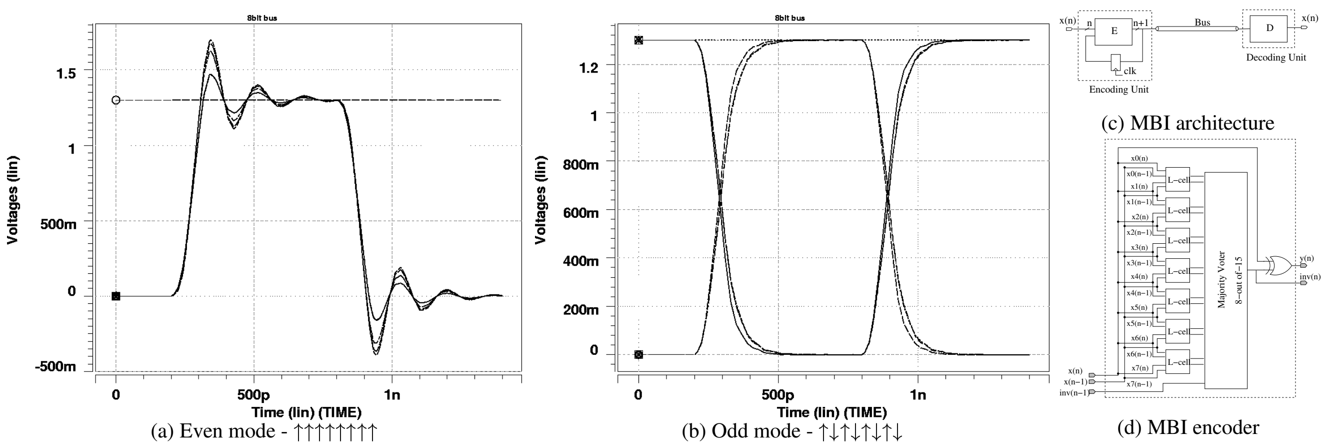
In order to analyze the effect of inductive coupling between bus lines at high frequencies, we modeled an 8-bit coplanar interconnect structure as a distributed RC and RLC model [3]. HSPICE simulations for both cases showed that the noise induced in the lines was much higher when the inductance was included for a $1GHz$ frequency. Therefore, in high-speed designs inductance should be considered when encoding data for crosstalk noise minimization, which represents the motivation of this paper.

In order to find the relation between data patterns and crosstalk noise, the two extreme cases were examined for the RLC model. When all the signals switch in the same direction (even mode - Figure 1(a)), the ringing in the bus lines is significantly higher than the case where the signals switch in the opposite direction (odd mode - Figure 1(b)). An explanation for that comes from the fact that the current flows in opposite directions in adjacent lines for the odd mode thus canceling the magnetic fields and reducing crosstalk noise. A similar reduction in crosstalk noise can be also observed between the even and odd mode when one line stays stable.

3 Proposed bus invert technique

Based on the observation that opposite skews can reduce crosstalk noise, we propose a modified bus invert (MBI) technique. The basic idea is to selectively invert data patterns such that the number of transitions in the same direction is minimized. MBI eliminates also the patterns which result into the worst case delay in the bus. Such patterns (e.g $\uparrow\uparrow\uparrow\downarrow\uparrow\uparrow\uparrow\uparrow$) have most of the lines switching in the same direction (aggressors) and few lines (victims) switching in opposite directions.

The encoding architecture inserts only one extra line which carries the "invert signal" and is used by the decoder (D) in order to restore the original data (Fig. 1(c)). In the encoder (E) the bus lines are partitioned into pairs and each pair of adjacent lines as well as their values from the previous clock cycle drive the inputs of a logic cell (L-cell - Figure 1(d)). The L-cells encodes the types of events occurring on the pair of bus lines. If the transitions happen in the same direction then the 2-bit output of the L-cell becomes: *11*. In cases when both lines are idle the output is: *00*, while for the patterns where either only one line switches, or both lines switch in opposite directions the output is: *01*. The L-cell assigns higher weights (*11*) to transitions which happen in the same direction and lower weights to the remaining transition types. The majority voter takes the outputs of the



(a) Even mode - ↑↑↑↑↑↑↑↑ (b) Odd mode - ↑↓↑↓↑↓↑↓ (d) MBI encoder

Figure 1. Simulations with the RLC model (a), (b), The proposed MBI encoding scheme (c), (d)

		NoEnc	BI%	CBI%	MBI%
PDF file	MaxRing (V)	0.676	23.88	-9.08	**28.89**
	MaxSpike (V)	0.598	21.67	-9.32	**25.01**
	MaxDelay (ps)	55.3	**13.40**	7.80	11.12
	AverRing (V)	0.534	24.67	-7.14	**28.14**
	AverSpike (V)	0.479	22.15	-5.18	**25.11**
	AverDelay (ps)	50.7	**10.53**	5.24	8.32
	Power (mW)	2.21	**16.38**	9.21	8.36
Video file	MaxRing (V)	0.713	26.41	-7.29	**31.67**
	MaxSpike (V)	0.641	20.73	-9.02	**24.10**
	MaxDelay (ps)	55.3	**14.08**	6.55	10.93
	AverRing (V)	0.559	26.97	-6.64	**30.39**
	AverSpike (V)	0.506	21.20	-6.15	**23.75**
	AverDelay (ps)	51.2	**11.26**	4.93	8.98
	Power (mW)	2.34	**17.54**	9.46	8.92
All-Trans	MaxRing (V)	0.720	27.36	-4.50	**33.33**
	MaxSpike (V)	0.663	21.11	-9.14	**24.33**
	MaxDelay (ps)	55.6	**14.49**	8.28	12.05
	AverRing (V)	0.541	25.14	-4.51	**29.08**
	AverSpike (V)	0.513	21.96	-5.44	**24.12**
	AverDelay (ps)	50.9	**10.94**	6.21	9.12
	Power (mW)	2.44	**19.13**	11.21	9.71

Table 1. Crosstalk noise, delay and power comparison (8-bit bus)

logic cells and the previous invert signal and sets the invert signal to 0 when the count of $1's$ on the majority voter inputs is less than n and in 1 otherwise.

4 Experimental results

The validity of the proposed encoding scheme was certified with HSPICE simulations for a typical 8-bit bus in the $0.18um$ technology [1]. The line length set to $2000um$ and the width-spacing characteristics of the interconnects are $W = 2.5um$ and $S = 1.25um$. Drivers of 50Ω and receivers of $100fF$ are used for a $1.3V$ Vdd and $1GHz$ frequency.

We applied PDF and Video files and a pattern sequence containing all the possible transitions for an 8-bit bus (All-Trans) to BI [1], CBI [2] and the proposed MBI encoding scheme. Table 1 presents the % reduction in crosstalk noise (ringing and spikes), delay and power consumption on the bus lines with respect to the unencoded data.

[1]For the extraction of the RLC values the 3-D filed solvers FastHenry and FastCap were used. The RLC model we used is described in [3].

As we can see MBI provides the greatest reduction in crosstalk noise while compared with BI and CBI and also improvement in delay while compared with the unencoded data. BI has the best performance in delay as it reduces the maximum transition activity on the bus by half. CBI seems to increase crosstalk noise which is a result of the extra line inserted. It should be noted that in [2] the authors have used redundancy in time, as opposed to our experimental setup based on redundancy in space.

In terms of power BI has the best performance but MBI also reduces the average power dissipation on the bus by almost 10%. MBI requires less area overhead when compared with the CBI but more area overhead when compared with the BI. However an analog implementation of the majority voter [4] can reduce significantly the area overhead and also the propagation delay of the encoder, such that it can operate at frequencies higher than $1GHz$.

5 Conclusion

This work has shown the importance of considering inductance when examining crosstalk problems on high speed buses. A modified bus-invert technique has been proposed which targets crosstalk noise minimization, while considering inductive effects. Experimental results show that this technique achieves the highest reduction in crosstalk noise, while performing comparably in terms of delay and power with other bus-invert techniques.

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