MOOSE: A Physically Based Compact DC Model of SOI LDMOSFETs for Analogue Circuit Simulation

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***Abstract*—In this paper, we present a compact model for silicon-on-insulator (SOI) laterally double diffused (LD) MOSFETs. The model is complete insofar as it uses no subcircuits, and is intended to predict device operation in all regions of bias. The device current is described by two main equations handling the MOS channel and the drift region, both of which are smooth and continuous in all operating regimes. Attention is also given to the modeling of inversion at the back oxide to ensure correct behavior is predicted for a source follower in power control applications ("high side operation"). A surface-potential-based formulation is used for the inversion/accumulation channel giving smooth transitions between different regions of operation, and care has been taken to ensure all expressions are smooth and infinitely differentiable to achieve the best possible convergence performance. Self (and coupled) heating effects exert a major influence over the behavior of power SOI devices, and these issues are incorporated in the model core in a consistent fashion.The model has been installed in a commercial SPICE-type circuit simulator and evaluated against individual devices and complete circuits fabricated in an industrial smart power SOI process. Accuracy is significantly improved with respect to the existing LDMOS models, and convergence behavior in switching and linear circuit simulations is comparable with industry standard models of this complexity.**

***Index Terms*—Analogue circuits, compact models, laterally double diffused (LD) MOSFET, MOS devices, silicon-on-insulator technology, simulation.**

I. Introduction

As THE scaling down of smart power ICs is gaining in importance, silicon-on-insulator (SOI) technology is becoming more attractive. Compared with a bulk technology, SOI offers a far better isolation scheme [1] leading to improved circuit density, and exhibits a significantly lower on-resistance for source-high conditions [2].

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The LDMOS transistor is one of the key devices in high voltage (HV) ICs, and a good model is indispensable in order to perform accurate circuit design. Some subcircuit models for bulk and SOI LDMOS devices are available, but, when certain specific aspects of device behavior become critical, they are not always sufficient. Moreover, they also suffer from a higher degree of complexity, compared with a compact model and, hence, an increase in computation time and a more complex parameter extraction procedure. The need for an accurate, robust compact model is therefore apparent.

In the general class of SOI LDMOS devices with a constant doping profile in the drift region, two different structures can be distinguished, each designed for a different range of drain voltages. The first type does not contain a field oxide, and the thin gate oxide extends over the drift region all the way to the drain. This device is illustrated in Fig. 1(a) and will be referred to as the low voltage (LV) SOI LDMOS. In the second type, a thicker oxide (field oxide) is grown on the drift region to bend back the equipotential lines and reduce the fringing fields at the edge of the polysilicon gate. This construction is shown in Fig. 1(b) and will be referred to as the medium voltage (MV) LDMOS. Note that the model can also be used for the offset drain structure, being the MV structure with the thickness of the field oxide being zero. HV LDMOS transistors often have a graded doping profile in the drift region to fullfill the conditions of the RESURF principle [3], [4], or use superjunction techniques [5]. At present, these HV devices are very technology dependent, and it would be difficult to develop one general model for this type of device; this task is left for a succeeding research project.

Compact models for SOI LDMOS transistors have received much attention in the literature [6]–[10]. The main difference between SOI and bulk structures is to be found in the drift region; for SOI, the lightly doped drift region rests on a thick oxide, while, in a bulk device, it sits on top of a P-type substrate. The modeling of the MOS channel part with the doping gradient in the inversion channel is similar for both technologies. The vertical and lateral bulk DMOS models from the University of Florida [6]–[9] take this lateral doping gradient in the channel into account, albeit only partly. In the Motorola LDMOS model [10] this gradient can be accounted for by partitioning the channel into regions of constant doping, and thus creating more internal nodes; this is accurate, but increases the computation time considerably.

Our model aims to describe in particular LV and MV SOI LDMOS transistors, which have a constant doping concentration in the drift region. Particular emphasis has been placed on

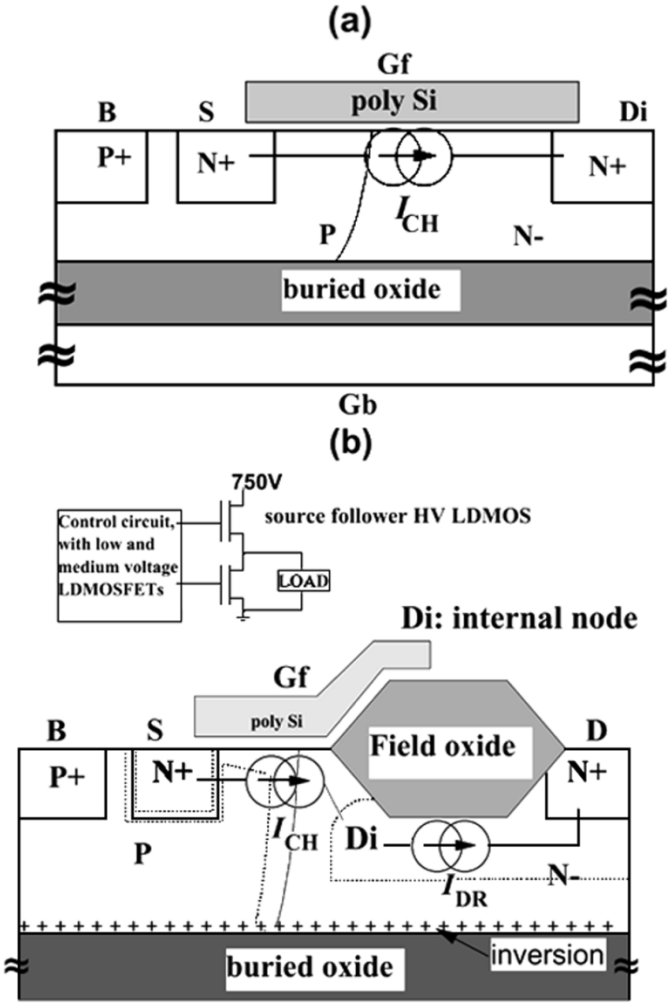

Fig. 1. Definition of the dc currents: (a) LV LDMOS and (b) MV LDMOS working under high side conditions.

the behavior and circuit-level modeling issues related to high-side drive applications, and on the self- and mutual heating. For the N-type LDMOS, high-side operation increases the on-resistance and demands specific modeling effort. To describe accurately the behavior of the MV SOI LDMOS, we use two current equations, both of which are smooth and continuous in all regions of operation. These two current expressions have been matched consistently with the help of limiting procedures and an accurate prediction of the internal node voltage. MOOSE can be made to converge more quickly than a compound subcircuit model, since the internal node voltage is set automatically to some reasonable initial estimate, calculated within the model.

Although it is not intended to be the main focus of this paper, a comparison between the two types of models was made by constructing subcircuit models and comparing their performance with the MOOSE compact model when running single device and test circuit simulations [11]. That subcircuit models are subject to a higher risk of convergence failure was indeed confirmed. Furthermore, the subcircuit models were found to be somewhat limited in the types of physical effects that could be modeled. For instance, accurate modeling of self-heating effects was not possible, unless a separate thermal node was added to each device model. Charge modeling was also problematic. Additionally, more parameters were required, and these tended to be less physical than in a compact model, and more difficult to extract. Despite these drawbacks, the subcircuit models still managed to provide good agreement with DC measurements, and reasonable matching for transient and AC results. The issue of poor convergence speed could not however be resolved using these models; we now turn our attention to the development of our compact model.

In Section II, we develop the first current expression $(I_{\rm CH})$, which describes the LV LDMOS part, including the drift region under the thin gate oxide. The formulation for the current under the thin gate oxide is surface potential based, and models both the drift and diffusion currents in all operating regions. Care has been taken to use only continuous and infinitely differentiable expressions. Furthermore, the model ensures a smooth transition between subthreshold and strong inversion and between triode and saturation. Both the lateral doping gradient in the channel and the overlap of the thin gate oxide over the drift region are accounted for in a compact and physical manner.

In Section III, we explain the second expression $(I_{\rm DR})$, which models the drift region under the field oxide and includes high-side behavior. By using both the potential in the drift region and the surface potential at the surface of the buried oxide, we ensure a purely physical prediction of the unique high-side behavior observed in the SOI LDMOS. Fig. 1 illustrates where $I_{\rm CH}$ and $I_{\rm DR}$ are applicable in the LV and MV SOI LDMOS structures.

The MOOSE model combines an electrical model with a thermal network to model self- and coupled heating effects in a consistent manner. In Section IV, the implementation of the internal thermal netlist is discussed.

The model has been implemented in the SPICE circuit simulator and careful formulation and coding has led to a very robust SOI LDMOS model, which converges easily without the frequent need for node setting commands. The model has been thoroughly evaluated, both qualitatively, using a set of simulations based on the SEMATECH tests [12], and quantitatively, verifying single device characteristics against measurements for different geometries. Some key results are presented in Section V.

II. Current Under Thin-Gate Oxide $(I_{\rm CH})$

To derive $I_{\rm CH}$, we define first the surface potentials with respect to the P-body (B), in all regions of operation. The different symbols used in this section are defined in Fig. 2. We consider three regimes, these being strong inversion, subthreshold, and saturation. Using a logarithmic smoothing function to join the various components, we arrive at the following expression [13]:

$$\psi_{\rm s0} = \phi_{\rm t} \ln\left(1 + \frac{\exp\left(\frac{\psi_{\rm si0}}{\phi_{\rm t}}\right)}{1+\exp\left(\frac{\psi_{\rm si0}-\psi_{\rm ss0}}{\phi_{\rm t}}\right)}\right) \tag{1}$$

$$\psi_{\rm sL} = \phi_{\rm t} \ln\left(1 + \frac{\exp\left(\frac{\psi_{\rm siL}}{\phi_{\rm t}}\right)}{1+\exp\left(\frac{\psi_{\rm siL}-\psi_{\rm sLsatf}}{\phi_{\rm t}}\right)}\right) \tag{2}$$

$$\psi_{\rm sdi} = V_{\rm DiB} + \phi_{\rm bid} \tag{3}$$

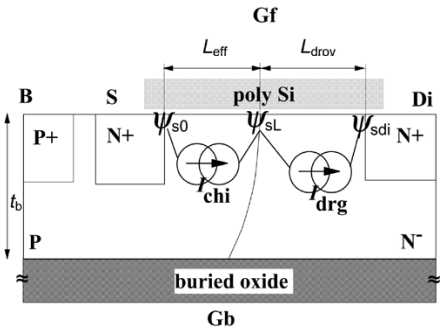

Fig. 2. Symbols used for the calculation of I_{CH}.

where ϕ_{t} is a smoothing parameter equal to the thermal voltage, $\phi_{\text{t}} = (kT/q)$. The expression for ψ_{sLsatf} is developed in Section II-D. It is shown that $\psi_{\text{sLsatf}} = \psi_{\text{ss0}}$ in the subthreshold region and $\psi_{\text{sLsatf}} = \psi_{\text{sLsat}}$ in the saturation regime. For more details about the physical background, refer to [14].

A. Inversion-Channel Current

Using standard assumptions for MOSFETs [14], the inversion-channel current can be expressed using the classic charge-sheet model [15]. Using the electron continuity equation [16] and neglecting recombination and generation currents yields

$$I_{\text{chi}} = \frac{W}{L_{\text{eff}}}\left(-\int_{\psi_{\text{s0}}}^{\psi_{\text{sL}}} \mu_{\text{s}}(y) q_{\text{cinv}}(y)\cdot d\psi_{\text{s}} + \phi_{\text{t}}\int_{q_0}^{q_{\text{L}}} \mu_{\text{s}}(y)\cdot dq_{\text{cinv}}\right) \quad (4)$$

where $q_{\text{cinv}}(y)$ is the channel charge density, ψ_{s} the surface potential at position y, $\mu_{\text{s}}(y)$ the surface mobility, and L_{eff} the effective length of the channel, defined by the length of the underdiffusion of the P-well minus the underdiffusion of the N^+ source well ($L_{\text{eff}} = L - L_{\text{D}}$). q_{cinv} is denoted by q_0 at $y = 0$ and by q_{L} at $y = L_{\text{eff}}$.

The mobility is initially assumed to be constant along the channel. Using the depletion approximation, which assumes that the depletion region under the gate is free of mobile carriers [17], the inversion channel charge can be obtained as

$$q_{\text{cinv}}(\psi_{\text{s}}, y) = -C_{\text{of}}\cdot(V_{\text{g}} - \psi_{\text{s}} - \gamma(y)\sqrt{\psi_{\text{s}}}) \quad (5)$$

with $V_{\text{g}} = V_{\text{GfB}} - V_{\text{FB}}^{\text{f}}$, C_{of} the thin-gate oxide capacitance per unit area, and the body factor $\gamma(y)$ is given by $(\sqrt{2q\,\epsilon_{\text{si}}N_{\text{A}}(y)})/(C_{\text{of}})$.

In order to get an analytic closed-form expression for the saturation voltage when including high field effects (see Section II-D), the body charge is linearized using a Taylor expansion for the square root term [18]

$$q_{\text{b}} = C_{\text{of}}\gamma\sqrt{\psi_{\text{s}}} \quad (6)$$

$$\cong C_{\text{of}}\gamma\cdot\left(\sqrt{\psi_{\text{s0}}} + \delta\cdot(\psi_{\text{s}} - \psi_{\text{s0}})\right) \quad (7)$$

with $\delta = (1)/(2\sqrt{1+\psi_{\text{s0}}})$.

The LDMOS has a nonuniformly doped channel region, starting at the end of the N^+ source diffusion and ending where the P-implant equals the N-type background doping. Thus, the doping concentration along the channel has a maximum near the source ($N_{\text{A}}(0) = N_{\text{As}}$) and decreases sharply toward the drain ($N_{\text{A}}(L_{\text{eff}}) = N_{\text{Ad}}$). The lateral doping gradient in the channel ($k_{N_{\text{A}}}$) is brought in by means of $\gamma(y)$, which is a function of $N_{\text{A}}(y)$ and thus of the position y along the channel. In order to perform the integration of (4), q_{cinv} is needed in terms of ψ_{s} only, or in other words, we have to transform $\gamma(y)$ to $\gamma(\psi_{\text{s}})$. This can only be done under certain assumptions, which are set out below.

The doping profile is assumed to be exponential ($N_{\text{A}} = N_{\text{As}}\exp(-k_{N_{\text{A}}}(y)/(L_{\text{eff}}))$) [9], [8] and hence

$$\gamma(y) = \gamma_0\exp\left(-\frac{k_{N_{\text{A}}}y}{2L_{\text{eff}}}\right) \cong \gamma_0\cdot\left(1 - \frac{k_{N_{\text{A}}}y}{2L_{\text{eff}}}\right) \quad (8)$$

with $\gamma_0 = (\sqrt{2q\epsilon_{\text{si}}N_{\text{As}}})/(C_{\text{of}})$. To transform $\gamma(y)$ into $\gamma(\psi_{\text{s}})$, ψ_{s} is assumed to be a linear function of y, i.e.,

$$\psi_{\text{s}} = \psi_{\text{s0}} + \frac{y}{L_{\text{eff}}}(\psi_{\text{sL}} - \psi_{\text{st0}}). \quad (9)$$

This yields

$$\gamma(\psi_{\text{s}}) = \gamma_0\cdot\left(1 - \frac{k_{N_{\text{A}}}}{2(\psi_{\text{sL}} - \psi_{\text{s0}})}(\psi_{\text{s}} - \psi_{\text{s0}})\right). \quad (10)$$

In a standard MOSFET with a constant doping in the channel, the linearity of ψ_{s} with y is accurate for low drain biases, but deteriorates toward higher drain biases. However, a decreasing doping concentration in the channel causes a *reduced field effect*, giving a reasonable linearity for higher drain biases. This has been confirmed using ATLAS simulations [11]. Furthermore, the MOS part of the LDMOS never reaches very deep saturation because the main part of the applied voltage drops over the drift region.

Using (10) and (7), the inversion channel density can be expressed as a function of ψ_{s} only. Substituting this expression into (4) results in a closed-form continuous equation, which can be used for the inversion-channel current in all regions of operation

$$I_{\text{chi}} = \beta\cdot\left(g\cdot(\psi_{\text{sL}}^2 - \psi_{\text{s0}}^2) + f\cdot(\psi_{\text{sL}} - \psi_{\text{s0}})\right) \quad (11)$$

with

$$\beta = \frac{W}{L_{\text{eff}}}\mu_{\text{s}}C_{\text{of}} \quad (12)$$

$$g = -\frac{1}{2}\eta_{\text{s}} + \gamma_0\delta\cdot\left(\frac{1}{6}k_{N_{\text{A}}} - \frac{1}{2}\right) \quad (13)$$

$$f = f_1 + f_2 \quad (14)$$

$$f_1 = V_{\text{g}} - \gamma_0\sqrt{\psi_{\text{s0}}}\left(1 - \frac{k_{N_{\text{A}}}}{4}\right) + \left(1 - \frac{k_{N_{\text{A}}}}{3}\right)\gamma_0\delta\psi_{\text{s0}} \quad (15)$$

$$f_2 = \phi_{\text{t}}\cdot\left(\eta_{\text{s}} + \gamma_0\delta - \frac{1}{2}\gamma_0 k_{N_{\text{A}}}\delta\right) \quad (16)$$

where η_s accounts for the influence of the fast surface states at the silicon-oxide interface [16]. Note that β can be recognized as the inversion layer gain factor.

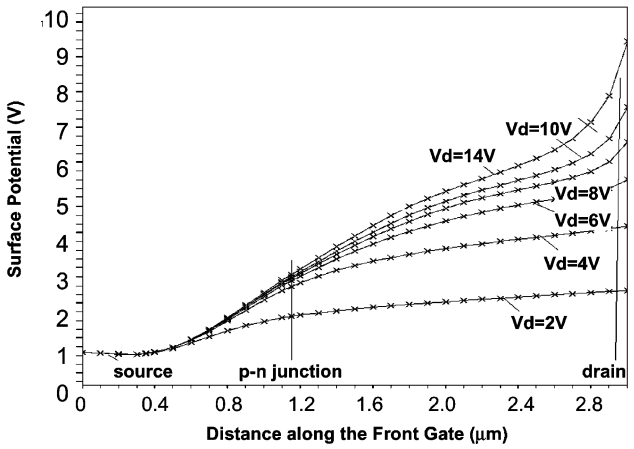

Fig. 3. ATLAS simulation of the depletion layers and the surface potential under the front gate ($V_{\mathrm{GfB}} = 4$ V).

B. Accumulation/Drift Current Under Thin Gate Oxide

In linear region operation, an accumulation layer exists in the drift region under the thin oxide, and this has a significant impact on device behavior. In bulk and SOI compact models published so far [7], [9], [19] this effect is neglected, or else an additional current source is added [10], slowing down convergence. In this work, we handle the issue analytically without introducing an extra node.

Since the length of this part of the drift region (L_{drov}) is typically comparable with the channel length, we assume that the channel current saturates before the accumulation layer starts to disappear at the drain, and ATLAS [20] simulations confirm the validity of this approach (Fig. 3). Further, when looking at the measured output characteristics of an LV LDMOS (see Fig. 8), it can be observed that the current saturates before V_{DiS} reaches $V_{\mathrm{GfS}} - V_{\mathrm{FB}}^{\mathrm{fdr}}$.

Neglecting the diffusion current and assuming that the surface is completely accumulated, the current in the drift region under the front gate can be expressed by [21]

$$I_{\mathrm{drg}} = -\frac{W}{L_{\mathrm{drov}}} \int_{\psi_{\mathrm{sL}}}^{\psi_{\mathrm{sdi}}} \left(\mu_{\mathrm{dr}} q_{\mathrm{b}}^{\mathrm{dr}} + \mu_{\mathrm{acc}} q_{\mathrm{cacc}}\right) \cdot d\psi_{\mathrm{s}}. \tag{17}$$

where μ_{dr} is the low field mobility in the drift region, μ_{acc} is the surface mobility in the accumulation region, and $q_{\mathrm{b}}^{\mathrm{dr}}$ is the free bulk charge density in the N^- region, and q_{cacc} the surface accumulation charge density:

$$q_{\mathrm{b}}^{\mathrm{dr}} = qN_{\mathrm{D}}t_{\mathrm{b}}f_{\mathrm{v}}, \tag{18}$$

$$q_{\mathrm{cacc}} = C_{\mathrm{of}} \cdot \left(\left(V_{\mathrm{GfB}} - V_{\mathrm{FB}}^{\mathrm{f}}\right) - \psi_{\mathrm{s}}\right) \tag{19}$$

where N_{D} is the doping concentration in the drift region and f_{v} is a fitting parameter taking into account the fact that the current flow is partially vertical. This is due to the current flow lines being longer than L_{drov}, especially when L_{drov} is of the same order as the silicon film thickness t_{b}. When L_{drov} is considerably larger than t_{b} this factor should approach one.

To ensure zero model current when $V_{\mathrm{DiS}} = 0$, we use $\psi_{\mathrm{sdi}} = V_{\mathrm{DiS}} + \psi_{\mathrm{si0}}$ instead of $V_{\mathrm{DiB}} + \phi_{\mathrm{bid}}$. The difference between $\phi_{\mathrm{bid}} = \phi_{\mathrm{F}} + \phi_{\mathrm{Fdr}}$ and $2\phi_{\mathrm{F}}$ is usually negligible (<0.1 V), because, considered on a logarithmic scale, the doping concentrations of the P-body and the N^- drift region are comparable.

After integration of (17) we obtain

$$I_{\mathrm{drg}} = h_1 \cdot (V_{\mathrm{DiS}} + \psi_{\mathrm{si0}} - \psi_{\mathrm{sL}}) + h_2 \cdot \left((V_{\mathrm{DiS}} + \psi_{\mathrm{si0}})^2 - \psi_{\mathrm{sL}}^2\right) \tag{20}$$

with

$$h_1 = \frac{f_{\mathrm{v}}}{R_{\mathrm{ON}}} + \beta_{\mathrm{acc}} \cdot \left(V_{\mathrm{GfB}} - V_{\mathrm{FB}}^{\mathrm{f}} + (\psi_{\mathrm{si0}} - V_{\mathrm{SB}})\right) \tag{21}$$

$$h_2 = -\frac{1}{2}\beta_{\mathrm{acc}} \tag{22}$$

$$\beta_{\mathrm{acc}} = \frac{W}{L_{\mathrm{drov}}} \mu_{\mathrm{acc}} C_{\mathrm{of}} \tag{23}$$

$$R_{\mathrm{ON}} = \left(\frac{W}{L_{\mathrm{drov}}} \mu_{\mathrm{dr}} q N_{\mathrm{D}} t_{\mathrm{b}}\right)^{-1}. \tag{24}$$

This expression completely describes the drift current under the thin gate oxide with a second order equation in the surface potentials ψ_{sL} and ψ_{sdi}. Note that R_{ON} can be recognized as the ON-resistance of the drift region under the thin gate oxide under zero bias conditions, and β_{acc} is the accumulation layer gain factor.

C. Solving for Surface Potential at the End of the Inversion Channel

Having obtained expression for the inversion-layer channel current (I_{chi}) and the drift current under the thin-gate oxide (I_{drg}), an analytical expression for the surface potential at the P-N junction (ψ_{sL}) can be derived. To find ψ_{sL} when the channel is in strong inversion $(\psi_{\mathrm{s0}} = \psi_{\mathrm{si0}}, \psi_{\mathrm{sL}} = \psi_{\mathrm{siL}}^*)$, (11) is equated to (20), $I_{\mathrm{drg}} = I_{\mathrm{chi}}$ and yields ψ_{siL}^* as a function of the known surface potentials ψ_{si0} and ψ_{sdi}

$$\psi_{\mathrm{siL}}^* = \frac{-\frac{B}{2} + \sqrt{\frac{B^2}{4} - AC^*}}{A} \tag{25}$$

with

$$A = g + G \tag{26}$$

$$B = f + F \tag{27}$$

$$C^* = -\left(g\psi_{\mathrm{si0}}^2 + f\psi_{\mathrm{si0}}\right) - F \cdot (V_{\mathrm{DiS}} + \psi_{\mathrm{si0}}) - G \cdot (V_{\mathrm{DiS}} + \psi_{\mathrm{si0}})^2 \tag{28}$$

$$G = -\frac{\beta_{\mathrm{acc}}}{2\beta} \tag{29}$$

$$F = \frac{f_{\mathrm{v}}}{\beta R_{\mathrm{ON}}} + \frac{\beta_{\mathrm{acc}}}{\beta}\left(V_{\mathrm{GfB}} - V_{\mathrm{FB}}^{\mathrm{f}} + (\psi_{\mathrm{si0}} - V_{\mathrm{SB}})\right). \tag{30}$$

D. Inclusion of High Field Effects

1) Vertical Field Mobility Reduction: Using the linearized expression for the body and the channel charge densities [(7) and (5)], the transverse electric field becomes [22]

$$\xi_{\mathrm{x}} = -\frac{\zeta C_{\mathrm{of}}}{\epsilon_{\mathrm{si}}} \left\{ V_{\mathrm{g}} - \psi_{\mathrm{s}} - \gamma_{\mathrm{m}} \cdot \left(1 - \frac{1}{\zeta}\right) \left(\sqrt{\psi_{\mathrm{s0}}} + \delta \cdot (\psi_{\mathrm{s}} - \psi_{\mathrm{s0}})\right) \right\} \tag{31}$$

where ζ is an empirical parameter, taking on the value $(1/2)$ for electrons and $(1/3)$ for holes, and a mean value for the body factor has been defined as $\gamma_{\rm m} = (\gamma_0 + \gamma_{\rm L})/(2)$.

Averaging $\xi_{\rm x}$ over the length of the device and using this average in the expression for the effective mobility for an N-type device (assuming classical diffuse scattering at the Si-SiO_2 surface) yields

$$\mu_{\rm xeff} = \frac{\mu_{\rm s}}{1+\theta\cdot\left(V_{\rm g}+\gamma_{\rm m}\cdot\left(\sqrt{\psi_{\rm s0}}-\delta\psi_{\rm s0}\right)-(1-\gamma_{\rm m}\delta)\frac{\psi_{\rm s0}+\psi_{\rm sL}}{2}\right)} \tag{32}$$

with θ the vertical field mobility coefficient. Note that it is important to include the linearized root terms in HV devices because the doping concentration of the P-body is often higher than for standard CMOS, leading to a higher body factor and hence an increased importance of these terms.

2) Carrier-Velocity Saturation: When the longitudinal field $\xi_{\rm y}$ increases, the carrier velocity increases proportionally to the field strength, until eventually reaching the saturation velocity $v_{\rm sat}$. The critical field for which this happens is given by $\xi_{\rm c} \cong (v_{\rm sat})/(\mu_{\rm s})$. This effect is modeled as [14]

$$\mu_{\rm yeff} = \frac{\mu_{\rm s}}{1+\frac{\mu_{\rm s}}{v_{\rm sat}}\frac{\psi_{\rm sL}-\psi_{\rm s0}}{L_{\rm eff}}}. \tag{33}$$

3) Combined Mobility Model: The two high-field effects give rise to (34), which is shown at the bottom of the page for the high-field effective mobility.

In [6], it is claimed that velocity saturation in LDMOS transistors occurs at the source side because the doping concentration is highest there, but this is not proven. The position of the lateral field maximum also depends on the applied biases and, on whether velocity saturation occurs before channel pinch-off, i.e., for very short channel length devices, the onset position will probably move along the channel. For long channel devices, pinch-off generally happens before velocity saturation, and velocity saturation takes place at the internal drain junction, where the lateral field is highest. Considering the above arguments, characterizing saturation by electron velocity saturation at a fixed position [6] is questionable. To find the saturation-surface potential at $y = L_{\rm eff}$, we search for the value of $\psi_{\rm sL}$ for which the channel current reaches a maximum and avoid the problem of the peak position of the lateral field

$$\left.\frac{\partial I_{\rm chi}}{\partial \psi_{\rm sL}}\right|_{\psi_{\rm sL}=\psi_{\rm sLsat}} = 0. \tag{35}$$

If we consider only the drift part of the channel current, which means neglecting f_2 in (14), we find

$$\psi_{\rm sLsat} = \psi_{\rm s0} + \frac{\psi}{S} \tag{36}$$

with

$$S = \frac{1}{2} + \frac{1}{2}\sqrt{1+\frac{2\psi M_{\rm mob}}{1+\theta\cdot(V_{\rm g}-\psi_{\rm s0})+\theta\gamma_{\rm m}\sqrt{\psi_{\rm s0}}}} \tag{37}$$

$$M_{\rm mob} = -\frac{\theta}{2} + \frac{1}{L_{\rm eff}\xi_{\rm c}} + \theta\gamma_{\rm m}\frac{\delta}{2} \tag{38}$$

$$\psi = -\psi_{\rm s0} - \frac{f_1}{2g}. \tag{39}$$

Let us now have a closer look at the expression for ψ

$$\psi = -\psi_{\rm s0} - \frac{f_1}{2g} \tag{40}$$

$$= \frac{V_{\rm g} - \eta_{\rm s}\psi_{\rm s0} - \gamma_0\sqrt{\psi_{\rm s0}}\left(1-\frac{k_{\rm N_A}}{4}\right)}{2g} \tag{41}$$

$$= \frac{\frac{q_0}{C_{\rm of}} + \gamma_0\sqrt{\psi_{\rm s0}}\frac{k_{\rm N_A}}{4}}{2g}. \tag{42}$$

In the strong inversion case, the term $\gamma_0\sqrt{\psi_{\rm s0}}(k_{\rm N_A})/(4)$ can be neglected, compared with $(q_0)/(C_{\rm of})$. On the other hand, in the subthreshold case, q_0 is zero, and neglecting the abovementioned term means $\psi = 0$. So, under subthreshold conditions, we find $\psi_{\rm sLsat} = \psi_{\rm s0} = \psi_{\rm ss0}$, which is what we want. Rewriting (36) without that term gives the final expression for the saturation surface potential at $y = L_{\rm eff}$

$$\psi_{\rm sLsatf} = \psi_{\rm s0} + \frac{V_{\rm g} - \eta_{\rm s}\psi_{\rm s0} - \gamma_0\sqrt{\psi_{\rm s0}}}{2gS}. \tag{43}$$

E. Calculation of the Saturation Voltage

In the previous section, the saturation surface potential at $y = L_{\rm eff}(\psi_{\rm sLsatf})$ was calculated. To calculate the drain saturation voltage, $V_{\rm dsat}$, we look for $V_{\rm DiS} = V_{\rm dsat}$ for which $I_{\rm chi}(\psi_{\rm sLsatf}) = I_{\rm drg}(\psi_{\rm sLsatf}, V_{\rm DiS})$. This results in

$$V_{\rm dsat} = \frac{1}{G}\left(-\frac{F}{2} + \sqrt{R_{\rm s}}\right) - \psi_{\rm s0} \tag{44}$$

with

$$R_{\rm s} = \frac{F^2}{4} + G\cdot\Big(g\cdot\left(\psi_{\rm sLsatf}^2 - \psi_{\rm s0}^2\right) + f\cdot(\psi_{\rm sLsatf} - \psi_{\rm s0}) + \psi_{\rm sLsatf}\cdot(G\psi_{\rm sLsatf} + F)\Big) \tag{45}$$

and F and G as defined by (30) and (29).

To attain a smooth transition from triode into saturation region a smoothing function is invoked to limit $V_{\rm DiS}$ to $V_{\rm dsat}$ [23]:

$$V_{\rm DiSn} = \frac{V_{\rm DiS}V_{\rm dsat}}{\left((V_{\rm DiS})^{2m} + (V_{\rm dsat})^{2m}\right)^{1/2m}} \tag{46}$$

with m an empirical parameter, which can take integer values only. For a short channel MOSFET, $m = 2$ gives a good fit. For longer channel lengths, larger values of m must be used.

$$\mu_{\rm eff} = \frac{\mu_{\rm s}}{1+\theta\cdot\left\{V_{\rm g} - \frac{\psi_{\rm sL}+\psi_{\rm s0}}{2} + \gamma_{\rm m}\left(\sqrt{\psi_{\rm s0}} + \frac{\delta}{2}(\psi_{\rm sL}-\psi_{\rm s0})\right)\right\} + \frac{\mu_{\rm s}}{v_{\rm sat}}\frac{\psi_{\rm sL}-\psi_{\rm s0}}{L_{\rm eff}}} \tag{34}$$

F. Total Current Expression

All the different aspects of the current under the thin-gate oxide studied in the previous sections can now be joined to give the final formulation as seen in (47), located at the bottom of the page with ψ_{s0} and ψ_{sL} given by (1) and (2). The expression for ψ_{siL} is identical to ψ^*_{siL} (25), with the difference that V_{DiS} is replaced by V_{DiSn} to include the saturation effects.

G. Auxiliary Model

The model also includes short and narrow channel effects, the channel-length modulation (CLM) effect, the DIBL effect, the parasitic bipolar effect, and impact ionization; these are all implemented in the same way as for standard SOI MOSFETs [14]. A couple of points need to be made however.

First, the CLM and DIBL effects in LDMOS transistors are much smaller than in a standard MOSFET because a large part of the drain voltage drops over the drift region. However, for low gate biases, it is important to take the CLM into account because it determines the value of the output conductance in the saturation regime.

Second, in LDMOS technology, it is common to place the body contact parallel with the source contact. This can lead to a relatively high body resistance, which is formed by the pinched region underneath the source junction. This body resistance, together with the impact ionization back gate current, can switch on the lateral parasitic bipolar transistor (BJT), and this can determine the safe operating area of the LV and MV LDMOS [24]. The safe-operating area is reduced further by self-heating; when the device heats up, the effective body source voltage necessary to trigger the parasitic BJT becomes smaller. Furthermore, because the BJT has a positive temperature dependent factor in the expression for the collector current, this effect can lead to early failure of the device.

III. Drift Current Under the Field Oxide

The current flow in the drift region is illustrated in Fig. 4. When the back gate voltage is negative, the surface at the buried oxide can be partially (as illustrated in Fig. 4) or fully inverted, depending on the channel potential ψ.

A. Intrinsic Drift Current

Neglecting the diffusion contribution, the current can be written as in a depletion-type MOSFET with the back gate acting as the gate terminal [21]

$$I_{DR0} = \frac{W}{L_{dr}} \mu_{dr} q N_D \int_{\psi_{Di}}^{\psi_D} (t_{bdr} - d(\psi)) \cdot d\psi \qquad (48)$$

where $d(\psi)$ is the depletion layer thickness extending from the buried oxide into the silicon, and t_{bdr} the silicon thickness under the field oxide. Refer to Fig. 4 for the channel potentials ψ_{Di} and

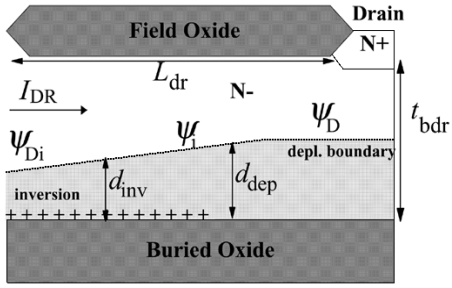

Fig. 4. Current flow in the drift region under high side conditions.

ψ_D. In this section, all potentials are defined with respect to the neutral bulk potential minus ϕ_{bid}.

We consider two definitions for the depletion-layer thickness, before and after inversion. Before inversion this is given by [21]

$$d_{dep} \cong \frac{C_{ob}}{qN_D}(-V_{gb} + \psi) \qquad (49)$$

with $V_{gb} = V_{GbB} - V_{FB}^{bdr}$, and C_{ob} the buried oxide capacitance per unit area. In standard depletion-type MOSFET devices, the possibility of surface inversion is usually excluded for practical devices. However, when an LDMOS is working under high side conditions, the formation of an inversion layer is crucial to limit the further increase in ON-resistance. If the surface at the buried oxide is inverted, the depletion layer thickness d_{inv} can be expressed as

$$d_{inv} = \sqrt{\frac{2\epsilon_{si}(2\phi_{Fdr} + \psi)}{qN_D}} \qquad (50)$$

using the depletion-layer approximation from [17], and where the inversion surface potential is approximated as $2\phi_{Fdr} + \psi$. To obtain closed-form analytical expressions for the saturation potentials in the next section, the square root of the surface potential is linearly approximated with a Taylor approximation around $2\phi_{Fdr}$

$$d_{inv} \cong \sqrt{\frac{2\epsilon_{si}}{qN_D}}(\sqrt{2\phi_{Fdr}} + \delta_{dr}\psi) \qquad (51)$$

with $\delta_{dr} = (1)/(2\sqrt{1 + 2\phi_{Fdr}})$. In Fig. 5, the linearized and ideal depletion layer thicknesses d_{dep} and d_{inv} are compared for typical parameters. Very good agreement is obtained for low values of ψ and V_{GbB}. For higher values, the deviation increases, but remains below 5%.

Using the linearized formulations for $d(\psi)$ the integral in (48) can be rewritten as

$$\int_{\psi_{Di}}^{\psi_D} \big(t_{bdr} - d(\psi)\big) \cdot d\psi = t_{bdr} \cdot (\psi_D - \psi_{Di}) - \int_{\psi_{Di}}^{\psi_i} d_{inv}(\psi) \cdot d\psi - \int_{\psi_i}^{\psi_D} d_{dep}(\psi) \cdot d\psi \qquad (52)$$

$$I_{CH0} = \frac{\beta}{1 + \theta \cdot \left\{ V_g - \frac{\psi_{sL} + \psi_{s0}}{2} + \gamma_m \cdot \left(\sqrt{\psi_{s0}} + \frac{\delta}{2}(\psi_{sL} - \psi_{s0}) \right) \right\} + \frac{\mu_s}{v_{sat}} \frac{\psi_{sL} - \psi_{s0}}{L_{eff}}} \cdot \left(g \cdot \left(\psi_{sL}^2 - \psi_{s0}^2 \right) + f \cdot (\psi_{sL} - \psi_{s0}) \right) \qquad (47)$$

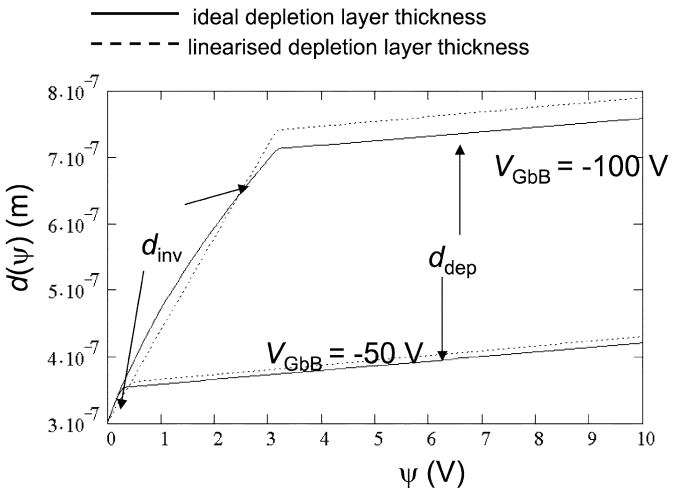

Fig. 5. Comparison of the linearized (dotted line) and ideal (full line) formulation of the depletion layer thickness: $d(\psi)$ versus ψ for $V_{\mathrm{GbB}} = -50$ V and -100 V.

where ψ_{i} is the potential at the end of the inversion layer as denoted in Fig. 4. This potential can be calculated from $d_{\mathrm{inv}}(\psi_{\mathrm{i}}) = d_{\mathrm{dep}}(\psi_{\mathrm{i}})$

$$\psi_{\mathrm{i}} = \frac{\gamma^{\mathrm{bdr}}\sqrt{2\phi_{\mathrm{Fdr}}} + V_{\mathrm{gb}}}{1 - \gamma^{\mathrm{bdr}}\delta_{\mathrm{dr}}} \tag{53}$$

with $\gamma^{\mathrm{bdr}} = (\sqrt{2\epsilon_{\mathrm{si}} q N_{\mathrm{D}}})/(C_{\mathrm{ob}})$ being the back gate-body factor in the drift region. The potentials at the internal drain node and at the drain can be expressed in terms of the nodal voltages using $\psi_{\mathrm{Di}} = V_{\mathrm{DiB}}$ and $\psi_{\mathrm{D}} = V_{\mathrm{DB}}$. Substituting (49), (51), and (53) into (52) results in

$$I_{\mathrm{DR0}} = \frac{1}{R_{\mathrm{ON}}^{\mathrm{dr}}}\left\{V_{\mathrm{DB}} - V_{\mathrm{DiB}} - \frac{1}{V_{\mathrm{Pdep}}}\left(\gamma^{\mathrm{bdr}} H_{1\mathrm{t}} + H_{2\mathrm{t}}\right)\right\} \tag{54}$$

with

$$R_{\mathrm{ON}}^{\mathrm{dr}} = \frac{L_{\mathrm{dr}}}{W \mu_{\mathrm{dr}} q N_{\mathrm{D}} t_{\mathrm{bdr}}} \tag{55}$$

$$V_{\mathrm{Pdep}} = \frac{q N_{\mathrm{D}} t_{\mathrm{bdr}}}{C_{\mathrm{ob}}} \tag{56}$$

$$H_{1\mathrm{t}} = \left((V_{\mathrm{DBf0}} - V_{\mathrm{DiB}})\sqrt{2\phi_{\mathrm{Fdr}}} + \frac{\delta_{\mathrm{dr}}}{2}\left(V_{\mathrm{DBf0}}^2 - V_{\mathrm{DiB}}^2\right)\right) \tag{57}$$

$$H_{2\mathrm{t}} = \frac{1}{2}\left((-V_{\mathrm{gb}} + V_{\mathrm{DB}})^2 - (-V_{\mathrm{gb}} + V_{\mathrm{DBf0}})^2\right) \tag{58}$$

and $V_{\mathrm{DBf0}} = \min(V_{\mathrm{DB}}, \max(V_{\mathrm{DiB}}, \psi_{\mathrm{i}}))$. The "min" and "max" functions describe a smooth and continuous minimum and maximum respectively. Note that $R_{\mathrm{ON}}^{\mathrm{dr}}$ can be recognized as the ON-resistance of the drift region under zero bias conditions. V_{Pdep} is the pinch-off voltage when the back surface is not inverted and $V_{\mathrm{gb}} = 0$.

B. Saturation by Pinch-Off

The maximum value for the depletion layer thickness is t_{bdr}. Assume here that $V_{\mathrm{DB}} > V_{\mathrm{DiB}}$; otherwise V_{DB} and V_{DiB} need only be swapped in the current equation. The pinch-off voltage V_{Psat} can be found by equating d_{dep} to t_{bdr} if $V_{\mathrm{DiB}} > \psi_{\mathrm{i}}$ (no inversion at the buried oxide), and d_{inv} to t_{bdr} in the inverse case. It can be shown [11] that V_{Psat} is given by the maximum of

$$V_{\mathrm{Psatdep}} = V_{\mathrm{gb}} + V_{\mathrm{Pdep}}, \tag{59}$$

and

$$V_{\mathrm{Psatinv}} = \frac{V_{\mathrm{Pdep}} - \gamma^{\mathrm{bdr}}\sqrt{2\phi_{\mathrm{Fdr}}}}{\delta\gamma^{\mathrm{bdr}}}. \tag{60}$$

To include saturation by pinch-off in the drift current expression, V_{DiB} and V_{DB} have to be limited smoothly [11] to V_{Psat}.

C. Velocity Saturation

For high drain biases the high field velocity saturation effects must be taken into account. Therefore, the low-field mobility μ_{dr} is replaced with [25]

$$\mu_{\mathrm{dreff}} = \frac{\mu_{\mathrm{dr}}}{1 + \theta_{3\mathrm{dr}}(V_{\mathrm{DB}} - V_{\mathrm{DiB}})} \tag{61}$$

with $\theta_{3\mathrm{dr}} = (\mu_{\mathrm{dr}})/(v_{\mathrm{satdr}} L_{\mathrm{dr}})$, where v_{satdr} is the drift saturation velocity.

To calculate the saturation potential, we solve

$$\left.\frac{\partial I_{\mathrm{DR0}}}{\partial V_{\mathrm{DB}}}\right|_{V_{\mathrm{DB}} = V_{\mathrm{sat}}} = 0. \tag{62}$$

It can be proven [11] that the solution which is valid for all bias situations is shown in (63) at the bottom of the page with

$$V_{\mathrm{DiB}}^{\mathrm{e}} = \max\Bigg(\min(V_{\mathrm{DiBs}}, \psi_{\mathrm{i}}), \psi_{\mathrm{i}} - \sqrt{\frac{2}{\theta_{3\mathrm{dr}}}\,\mathrm{pos}\,(V_{\mathrm{Psatinv}} - \psi_{\mathrm{i}})}\Bigg) \tag{64}$$

where

$$\max(\mathrm{x}, \mathrm{y}, \epsilon) = x - 0.5\big((x - y) - \sqrt{(x - y)^2 + 4\epsilon^2}\big) \tag{65}$$

$$\min(\mathrm{x}, \mathrm{y}, \epsilon) = x - 0.5\big((x - y) + \sqrt{(x - y)^2 + 4\epsilon^2}\big) \tag{66}$$

with ϵ being a fitting parameter. Here, V_{DDi} is limited to $V_{\mathrm{sat}} - V_{\mathrm{DiB}}$.

IV. Modelling Heating Effects

Self-heating effects are a well-known complicating factor for high-power dissipation levels in DMOS [26]–[28] and other HV devices [29]. In a SOI technology, the thermal resistance is much higher than in its bulk counterpart, especially for HV devices where the buried oxide layer can be reasonably thick.

$$V_{\mathrm{sat}} = V_{\mathrm{DiBs}} - \frac{1}{\theta_{3\mathrm{dr}}} + \sqrt{\frac{1}{\theta_{3\mathrm{dr}}^2} - 2\frac{V_{\mathrm{DiBs}}}{\theta_{3\mathrm{dr}}} + 2\frac{V_{\mathrm{Psat}}}{\theta_{3\mathrm{dr}}} + (\psi_{\mathrm{i}} - V_{\mathrm{DiB}}^{\mathrm{e}})^2\,(1 - \gamma^{\mathrm{bdr}}\delta_{\mathrm{dr}})} \tag{63}$$

The finite thermal capacitance prevents the device temperature from following the device power instantaneously, and so it is important to consider self-heating as a dynamic effect both in large and small signal terms [30]–[32]. The increase of the output conductance with frequency due to the thermal time constant (typically in the range of 100 kHz–1 MHz) is of extreme importance for analogue designers, since the output conductance determines the gain of any amplifier.

In ultrathin RESURF SOI LDMOS structures, the distribution of the heat generation in the drift region will be highly nonuniform, but will be reasonably constant in thicker SOI LDMOS devices [33], [34]. In compact models two-dimensional (2-D) heat-flow analysis [35] is too complicated, and it is usually preferred [14], [36] to assume thermal equilibrium and use an average temperature rise ΔT.

A separate circuit is used to model the thermal behavior of a device [37], [38], consisting of a thermal resistance $(R_{\rm T})$ and a thermal capacitance $(C_{\rm T})$. Only one time constant has been embedded in the model, but if more are needed [39], a higher order network can be added externally. The thermal node can also be connected to a thermal interconnection network for the simulation of static and dynamic thermal coupling between devices.

In the case of a first order thermal circuit, the simulated temperature rise is obtained from

$$P = \frac{\Delta T}{R_{\rm T}} + C_{\rm T}\frac{d(\Delta T)}{dt}. \tag{67}$$

The dissipated power in the SOI LDMOS is given by

$$P = I_{\rm CH}V_{\rm DiS} + I_{\rm DR}V_{\rm DDi} \tag{68}$$

from which the simulated temperature rise can be determined via (67). To find the small-signal equivalent, the thermal dissipation must be differentiated with respect to $\Delta T, V_{\rm DiB}, V_{\rm GfB}, V_{\rm GbB}, V_{\rm DB}$, and $V_{\rm SB}$, just as with all the other electrical current expressions in the compact model. The temperature rise is treated as another voltage for which SPICE has to solve, and the local device temperature rise is available to circuit designers as a terminal voltage. Thermal dependence of model parameters is also included [14].

V. Validation

Test chips were fabricated using a commercial HV SOI process containing single LV and MV LDMOS structures with different geometries. In this section, the measured data from the single devices are presented compared with MOOSE simulations. LV LDMOS devices with two different overlap lengths ($L_{\rm drov} = 1.2\ \mu$m and $L_{\rm drov} = 3.2\ \mu$m, with $L_{\rm dr} = 0\ \mu$m) and MV LDMOS devices with three different drift lengths ($L_{\rm dr} = 3.7\ \mu$m, $L_{\rm dr} = 5.7\ \mu$m, and $L_{\rm dr} = 7.7\ \mu$m, with $L_{\rm drov} = 1.7\ \mu$m) were selected for study and represent a comprehensive range of geometries. Other relevant process details are: front gate oxide thickness $t_{\rm of} = 60$ nm, back gate oxide thickness $t_{\rm ob} = 3\ \mu$m, silicon film thickness $t_{\rm b} = 1.5\ \mu$m, silicon thickness under field oxide $t_{\rm bdr} = 1\ \mu$m, and maximum doping concentration $N_{\rm As} = 10^{17}/{\rm cm}^3$.

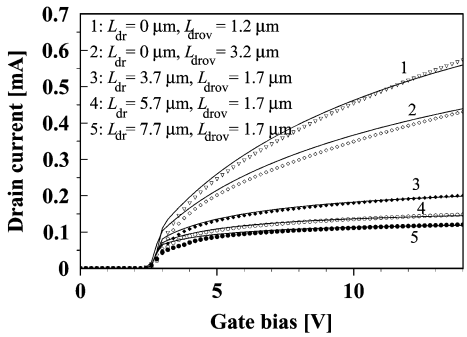

Fig. 6. Measured (markers) and simulated (full line) drain current in the linear region for different geometries and $V_{\rm DS} = 0.1$ V.

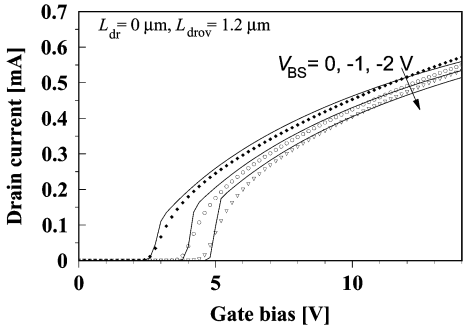

Fig. 7. Measured (markers) and simulated (full line) drain current in the linear region $V_{\rm BS} = 0, -1, -2$ V, and $V_{\rm DS} = 0.1$ V.

The parameter extraction procedure used is very similar to the one used in compound models [40], although less parameters are required, which eases the optimization procedure.

A. Linear Characteristics

The linear characteristic for different geometries is shown in Fig. 6. As can be seen, the MOOSE model matches the measured data very well in almost all regions.

Curves 1 and 2 show the drain-current decrease with increasing $L_{\rm drov}$, and curves 3–5 show the current decrease with increasing $L_{\rm dr}$. The match is very good for gate voltages more than 2 V above the threshold voltage but just above the threshold, the model slightly overestimates the measured current.

Fig. 7 shows the linear characteristic for different body voltages. Similar agreement is observed. The reason for overestimation in the simulated current has its origin in the approximation for the body factor employed in (10). Just above the threshold, the body factor is not exactly a linear function of the surface potential; the lower threshold at the drain end of the channel causes the inversion at the source end to be considerably less than at the drain end, and hence the main part of the drain voltage will drop over the source end of the inversion layer, becoming almost constant toward the point where $y = L_{\rm eff}$. Because of the assumption that γ is a linear function of $\psi_{\rm s}$, the inversion charge in the intergral of (4) will be overestimated just above the threshold for values between $\psi_{\rm s0}$ and $\psi_{\rm sL}$, explaining the slightly overestimated current.

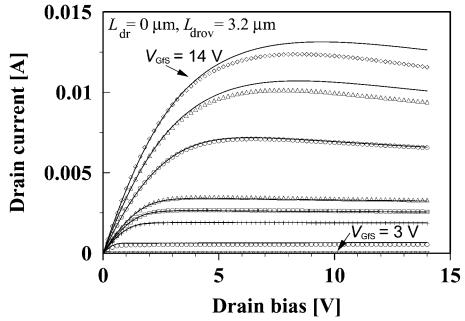

Fig. 8. LV LDMOS with $L_{\rm drov} = 3.2\ \mu$m; measured (markers) and simulated (full line) current vs. $V_{\rm DS}$ for $V_{\rm GfS} = 3.5$ V, 4.5 V, 5 V, 5.5 V, 8 V, 11 V, and 14 V.

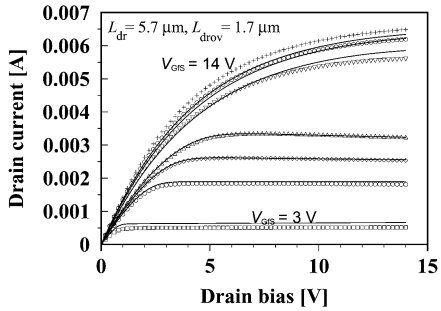

Fig. 9. MV LDMOS with $L_{\rm drov} = 1.7\ \mu$m and $L_{\rm dr} = 5.8\ \mu$m; measured (markers) and simulated (full line) current versus $V_{\rm DS}$ for $V_{\rm GfS} = 3.5$ V, 4.5 V, 5 V, 5.5 V, 8 V, 11 V, and 14 V.

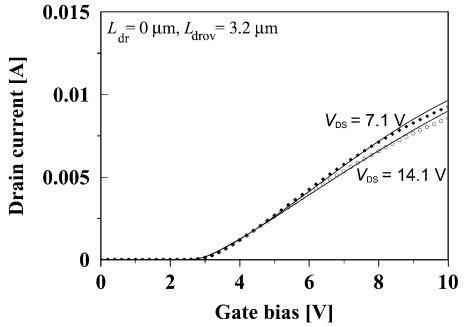

Fig. 10. LV LDMOS with $L_{\rm drov} = 3.2\ \mu$m; measured (markers) and simulated (full line) current versus $V_{\rm GfS}$ for $V_{\rm DS} = 7.1$ V and $V_{\rm DS} = 14.1$ V.

B. Output Characteristics

Output characteristics for the LV and MV LDMOS are shown in Figs. 8 and 9, respectively. In almost all cases, the model yields a good match with the measured data. The onset of saturation is well predicted, proving that pinch-off and saturation effects in the drift region are well modeled. For the LV LDMOS, the drain-saturation current keeps increasing with the gate bias, while for the MV LDMOS the drift region limits the current much more noticeably. The model predicts well the decrease in current due to self-heating, which can lead to a negative output resistance in some bias situations.

This is also shown in Figs. 10 and 11. Self-heating is very noticeable in these curves because, above a certain gate voltage, the curves cross each other, leading to a higher current for the lower drain bias.

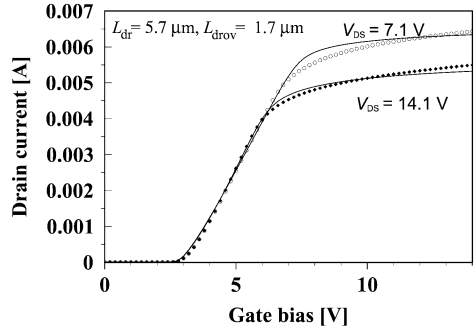

Fig. 11. MV LDMOS with $L_{\rm drov} = 1.7\ \mu$m and $L_{\rm dr} = 5.8\ \mu$m; measured (markers) and simulated (full line) current versus $V_{\rm GfS}$ for $V_{\rm DS} = 7.1$ V and $V_{\rm DS} = 14.1$ V.

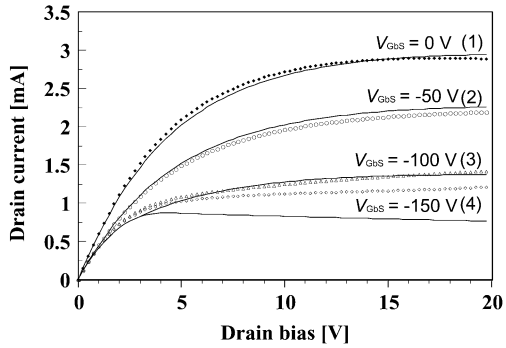

Fig. 12. Measured (markers) and simulated (full line) current for $V_{\rm GfS} = 10$ V and $V_{\rm GbS} = 0$ V, -50 V, -100 V, and -150 V.

C. High-Side Behavior

Fig. 12 shows the device operated under high-side conditions. We observe a current decrease with increasingly negative back gate bias (i.e., substrate bias), but when inversion is established, the back gate voltage no longer influences the drain current. Good agreement is found between the simulated and measured data for curves 1–3. However, measured curve 4 has a positive slope, while the simulated curve 4 has saturated and has a negative slope; this latter effect is due to self-heating and is masked prior to current saturation. One would expect the current for measured curve 4 to also have saturated due to pinch-off of the drift region, so that the current decreases with increasing $V_{\rm DS}$. In reality, 2-D effects in the drift region may change the field distribution when $V_{\rm DS}$ is increased, or else enhanced CLM may occur with increasing back gate bias, thus delaying saturation and keeping the slope of the curve positive.

Fig. 13 shows the influence of a negative back gate on the linear characteristic. As explained in Section V-A, the simulated current just above the threshold slightly overestimates the real current, but the decrease in current due to a negative back gate bias shows good agreement with the measurements. In Fig. 14 we have plotted the current vs. the back gate bias for a fixed front gate bias and two different drain biases. As explained in the previous paragraph, the simulated saturation current is too low for very negative back gate biases. The plot illustrates nicely the decrease in current with increasingly negative back gate bias until the drain voltage-dependent back gate threshold voltage of

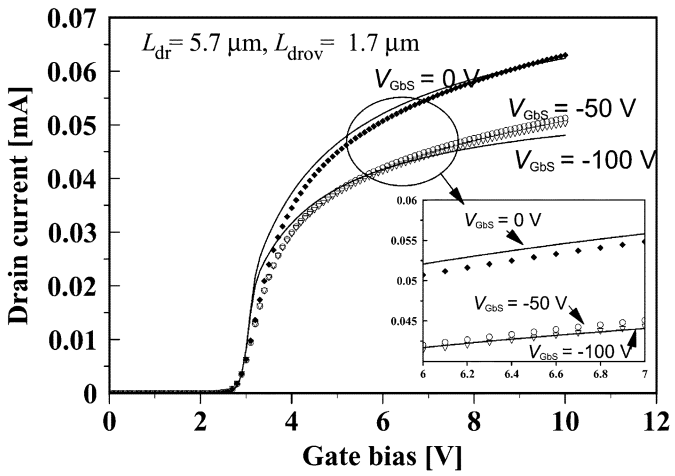

Fig. 13. MV LDMOS with $L_{\rm drov} = 1.7\ \mu$m and $L_{\rm dr} = 5.8\ \mu$m; measured (markers) and simulated (full line) current vs. $V_{\rm GfS}$ for $V_{\rm DS} = 0.1$ V and $V_{\rm GbS} = 0$ V, -50 V, -100 V.

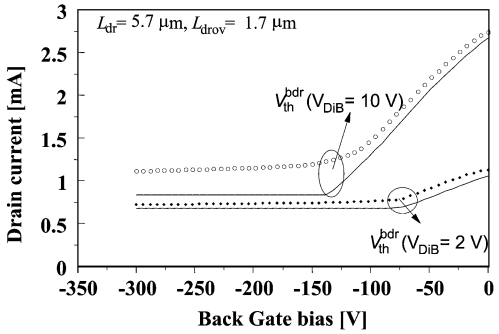

Fig. 14. MV LDMOS with $L_{\rm drov} = 1.7\ \mu$m and $L_{\rm dr} = 5.8\ \mu$m; measured (markers) and simulated (full line) current versus $V_{\rm GbS}$; $V_{\rm GfS} = 10$ V; $V_{\rm DS} = 2$ V, and $V_{\rm DS} = 10$ V.

the drift region is reached ($V_{\rm th}^{\rm bdr}$), at which point the current stays constant.

D. Circuit Simulation Performance: Switching-Power Circuit

In this section, the influence of self-heating on some circuit blocks has been investigated and further insights about the compact model are set out. Obviously, the MOOSE model also includes a full charge description [41], but to observe space restrictions, we will concentrate on the dc aspects of the circuit.

The circuit consists of a simplified horizontal line-driver circuit for plasma displays as shown in Fig. 15. To investigate the self-heating behavior of the circuit, a load resistor was added between the output and the positive supply (see dotted lines in Fig. 15). The output voltage does not go all the way back to 0 V when Y12 is switched on, but reduces to a value determined by Y12 and the load resistor. The measured and simulated results for the MV circuit when $\rm R = 120\ \Omega$ are shown in Fig. 16. Due to self-heating the temperature of Y12 increases with time when it is on. This reduces the current in Y12 and results in a slight rise in the output voltage. In Fig. 17, the output voltage is plotted in detail and one can clearly observe the positive slope. In the same figure, the output voltage is simulated with and without self-heating; it is clear that including self-heating correctly predicts the positive slope while the isothermal result shows a constant value for $V_{\rm out}$. Fig. 18 shows the simulated temperature

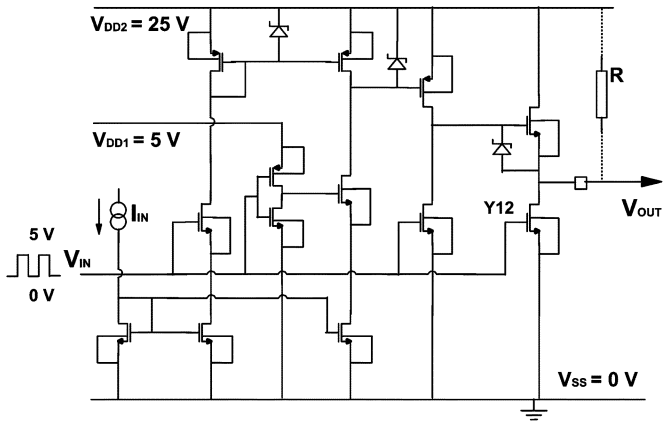

Fig. 15. Circuit schematic for a switching power block.

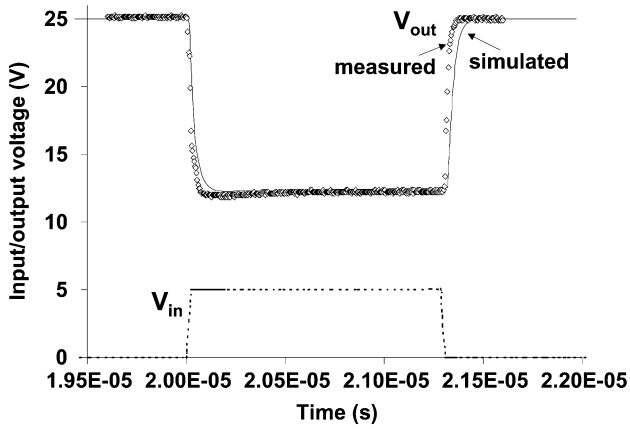

Fig. 16. Simulated (full line) and measured (markers) output voltage of a plasma display driver switching circuit with a resistive load ($\rm R = 73\ \Omega$) to the positive supply voltage (LV circuit).

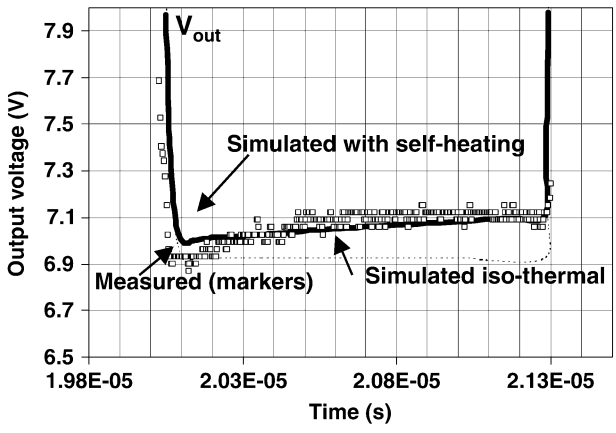

Fig. 17. Detail of the measured (markers) and simulated (with (full line) and without (dotted line) self-heating) positive slope from the switching circuit in Fig. 15.

rise of Y12 during the transient simulation, and for a frequency of 150 kHz and a duty cycle of 20%, a temperature rise of 10 K is observed. Measuring the circuit at higher frequencies with a

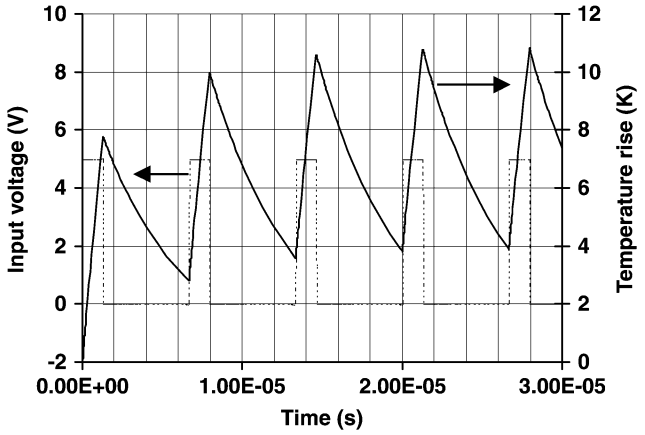

Fig. 18. Simulated temperature rise of the output transistor Y12 in Fig. 15 when $\mathrm{R} = 73\ \Omega$.

higher duty cycle can lead to very high temperatures with the possibility of destroying the circuit.

VI. Conclusion

In this paper, the MOOSE SOI LDMOS dc model was set out. Expressions for the current under the thin gate oxide and under the field oxide were carefully derived, keeping the model approach as physical as possible. The assumptions made were considered critically and verified where necessary.

First, an expression for the current under the thin-gate oxide was developed, describing the current in terms of the surface potentials, whilst taking into account the lateral doping gradient and the overlap of the gate over the N^- drift region. Next, an expression for the current under the field oxide was developed. The impact on the current of the thickness of the depletion layer at the buried oxide was studied rigorously, leading to a good prediction of the unique high-side behavior.

The model simulations match the measured characteristics well for a wide range of geometries, with self-heating effects being accounted for. The accuracy of the MOOSE model has been thoroughly evaluated and compared with measurements from single devices, and the usefulness in practical situations has been demonstrated by comparison with a complete circuit.

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