ADAPTIVE SENSOR RESPONSE CORRECTION USING ANALOG FILTER COMPATIBLE WITH DIGITAL TECHNOLOGY

M. Jafaripanah, B. M. Al-Hashimi and N. M. White

ESD Group, School of Electronics and Computer Science
University of Southampton, SO17 1BJ, UK
{mj01r,bmah,nmw}@ecs.soton.ac.uk

ABSTRACT

An analog adaptive filter for response correction of a load cell sensor is presented. The filter employs only transistors and therefore it can be integrated using digital CMOS technology, which is suitable for System-on-Chip applications. To achieve adaptive compensation over a wide range of measurand, a novel $CMOS$ multiplier was developed. The analog adaptive filter has been simulated using $0.35\mu m$ 3.3V BSim3v3 CMOS foundry models and found to perform effective compensation.

1. INTRODUCTION

Some sensors, such as load cells, have an oscillatory output, which needs time to settle down. It is therefore necessary to determine the value of the measurand while the output is still in oscillation. Load cells are used in a variety of industrial weighing applications such as vending machines and checkweighing systems. Since the measurand contributes to the load cell response characteristics, a compensation filter is required to track variation in measurand whereas a simple, fixed filter is only valid at one specific load value. A number of methods, including digital adaptive techniques [1] and artificial neural network [2] have been reported for sensor compensation, which basically employ digital signal processing chips to implement the required filtering algorithms. Recently, analog adaptive techniques [3, 4] have been used to perform effective sensor response correction, with the main benefits of smaller size, lower complexity and lower power consumption compared to digital techniques.

In recent years, the quest for smaller and cheaper electronic systems has led manufactures to integrate systems onto a single chip (Systems on Chip, SoC). In the sensor research community, efforts have focused on making silicon-based sensors and circuit designers investigate techniques to develop CMOS compatible analog electronic circuits [5, 6, 7] because this is dominant processing technology for integrated circuits and systems. Despite the effectiveness of the op-amp based compensation filter reported in [4], the filter is not compatible with digital CMOS technology since it contains resistors and capacitors. This limits its applications in SoCs, and therefore, the motivation of this research is to develop and implement an analog filter for senor compensation, which is compatible with CMOS technology. It should be noted that traditionally the switched-capacitor technique has been employed extensively to integrate the analog portion of mixed-signal chips. However, switched-capacitors are not fully compatible with the digital CMOS process and as technology advances further, the drawbacks of switched-capacitor are becoming more significant [8]. The switched-capacitor technique requires high quality capacitors usually implemented using two polysilicon layers. The second layer is not required in wholly digital circuits and often it is not available, particularly in deep submicron technology used to fabricate SoCs.

This paper shows that it is possible to design and implement an analog adaptive filter capable of effectively correcting the sensor response without the use of floating capacitors. The proposed filter consists entirely of transistors and therefore it is suitable for integration using standard digital CMOS process (single polysilicon). The filter is designed using switched-current (SI) techniques, which exploit the ability of a MOS transistor to maintain its drain current, when its gate is open-circuited, through the charge stored on the parasitic gate oxide capacitance, and without the explicit need for designed capacitors [9]. SI techniques are increasingly being applied to sensor applications [5, 7]. The application of SI to dynamic sensor compensation has not been addressed in the literature, and is therefore the main aim of this paper.

2. SENSOR RESPONSE CORRECTION

The general principle of sensor response correction, in order to eliminate oscillatory sensor output, involves cascading a filter, having the reciprocal characteristic of the sensor, with it(Fig.1). Therefore, the transfer function of the whole system is *"unity"*, which means that any changes in the input transfer to the output without distortion. It has been shown that the load cell can be modelled as a 2^{nd} order system [1]:

$$G(s) = \frac{X(s)}{F(s)} = \frac{\frac{1}{m+m_0}}{s^2 + \frac{c}{m+m_0}s + \frac{k}{m+m_0}} = \frac{A}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \quad (1)$$

Where m is the mass being weighed, m_0 is the effective mass of the sensor, c is the damping factor, k is the spring constant, and $F(t)$ is the force function. Equation (1) shows that m affects all characteristics of the sensor such as gain factor, A, quality factor, Q, and natural frequency, ω_0. Equation (1) yields a pair of complex conjugate poles $a \pm jb$ where

$$a = -\frac{c}{2(m+m_0)} \quad \text{and} \quad b = \sqrt{\frac{k}{(m+m_0)} - \frac{c^2}{4(m+m_0)^2}} \quad (2)$$

Thus the zeros of the adaptive filter, which are the poles of the sensor, can be found. The parameter m is unknown in the

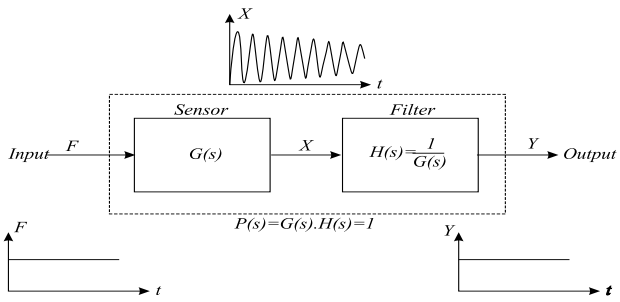

Figure 1: Principle of sensor response correction

first instance when a new measurement begins. Therefore the parameters of the adaptive filter can not be set to appropriate values in order that the filter behaves as an inverse system. Hence, an adaptive rule is required to modify the parameters of the adaptive filter according to the value of measurand, m. Usually, in classic adaptive techniques, an adaptive algorithm, such as least mean squares (LMS) method, updates the parameters of the adaptive filter to minimize a cost function. However, (1) shows that, for a load cell, the suitable filter has a pair of conjugate zeros, $z_{1,2} = a \pm jb$, where, a and b can be considered as the parameters of adaptive filter and the relationship between them and the load is expressed in (2). The adaptive compensation operation is shown in Fig.2.

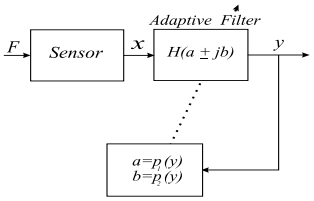

Figure 2: Adaptive sensor response correction diagram

So far the zeros of the 2^{nd} order compensation filter have been examined. In order that the analog filter can be realized, it is necessary to add at least two poles to the filter. The values of these poles can be determined practically. These poles are selected so that the output of the filter quickly reaches its steady-state value with minimum oscillation. The transfer function of the compensation filter is:

$$H(s) = \frac{(m + m_0) \cdot s^2 + c \cdot s + k}{s^2 + 87.5s + 0.0004} \tag{3}$$

The transfer functions of the compensation filter, (3), is a biquadratic function. The problem is how to make it adaptive and from design simplicity point of view, it is necessary to have only one filter component to track changes in m without any influence on the other characteristics of the filter. How to achieve this with $CMOS$ transistor alone circuits is discussed in the next section .

3. ADAPTIVE COMPENSATION FILTER

Amongst the various biquadratic structures, the integrator based biquad [9], shown in Fig.3, has been chosen. It consists of current mirrors, memory cells and switches, which are driven by two non-overlapping clock pulses, ϕ_1 and ϕ_2. With this biquad, it is possible to track variation in the measurand by controlling a single filter parameter. The s-domain transfer function of the biquad circuit is:

$$H(s) = \frac{[\frac{4\alpha_6 + 2\alpha_5 - \alpha_1\alpha_3}{D}]s^2 + [\frac{4\alpha_5}{T.D}]s + [\frac{4\alpha_1\alpha_3}{T^2.D}]}{s^2 + [\frac{4\alpha_4}{T.D}]s + [\frac{4\alpha_2\alpha_3}{T^2.D}]} \tag{4}$$

where $D = 2\alpha_4 - \alpha_2\alpha_3 + 4$, T is the clock period and each α_i is the ratio of two currents in the filter circuit. Comparing (4), with the compensation filter transfer function, (3), gives:

$$\frac{4\alpha_6 + 2\alpha_5 - \alpha_1\alpha_3}{D} = (m + m_0) \tag{5}$$

$$\frac{4\alpha_5}{T.D} = c \tag{6}$$

$$\frac{4\alpha_1\alpha_3}{T^2.D} = k \tag{7}$$

$$\frac{4\alpha_4}{T.D} = 87.5 \tag{8}$$

$$\frac{4\alpha_2\alpha_3}{T^2.D} = 0.0004 \tag{9}$$

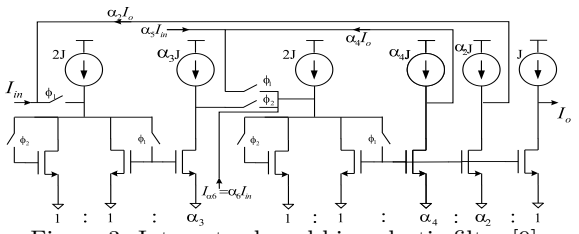

Figure 3: Integrator-based biquadratic filter [9]

Equation (5) confirms that only one filter parameter, α_6, is proportional to m. Examining Fig.3 shows that α_6 is a coefficient for the filter input current ($I_{\alpha_6} = \alpha_6 I_{in}$) and in the adaptive case it should be $I_{\alpha_6} = \alpha_6(m) I_{in}$. In our current-mode filter, the output current, I_o, displays the load cell measurand, m, therefore having α_6 proportional to m is equivalent to control the filter input current by a variable gain proportional to the filter output current. This means that a current multiplier is needed to make an adaptive compensation filter. This is clarified schematically in Fig.4.

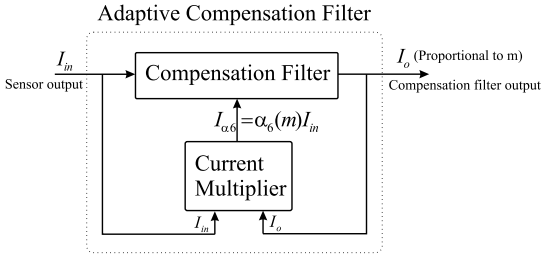

Figure 4: Adaptive compensation filter block diagram

The design procedure involves determining the parameters of a fixed filter, α_i, and then using a current multiplier block (Fig.4) to make it adaptive. From experimental data for a particular load cell [2] the damping factor c, spring constant k, and the effective mass of the load cell m_0, are 3.5, 2700 Pa, and 0.1 kg, respectively. In addition, m is considered to be 1 kg, which is an arbitrary choice. The filter parameters, α_i, are implemented by $[\frac{W}{L}]$ of the transistors in the current mirrors. The clock period, T, affects the spread of the transistor sizes for the filter. With $T = 10^{-2}s$ and using (5) to (9), the parameters of the compensation filter can be calculated as shown in table 1. Choosing $T = 10^{-2}s$ provides parameter spread of 25:1, while for $T = 10^{-5}s$ it is 3000000:1, which is clearly impractical. It is worth noting that the load cell output is oscillatory with low frequency (less than $30Hz$), therefore $T = 10^{-2}s$ is a reasonable choice.

Table 1: Compensation filter parameters, $T = 10^{-2}s$

α_1	α_2	α_3	α_4	α_5	α_6
1	1	0.4	1.4	0.0519	1.556

To find how α_6 is related to m, it is calculated for different values of m from $0.1kg$ to $1kg$ by using (5). Table 2 shows α_6 for different values of m. It is possible to express the values in table 2 as a linear relationship between α_6 and m:

$$\alpha_6 = 1.4816m + 0.074 \tag{10}$$

To ensure the correct operation of the transistors in the filter circuit, it is assumed that a load cell measurand of $m = 1kg$ corresponds to $10\mu A$ output current. Therefore, with reference to Figs.4 and using (10), to have an adaptive compensation filter, a current multiplier with the following relationship between its input and output is required.

$$I_{\alpha_6} = \alpha_6 \cdot I_{in} = (0.14816 I_o + 0.074) \cdot I_{in} \tag{11}$$

Table 2: Filter parameter α_6 for different values of m

$m[kg]$	0.1	0.3	0.5	0.7	0.9	1
α_6	0.222	0.519	0.815	1.111	1.407	1.556

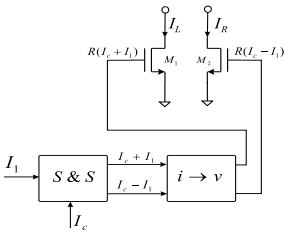

Figure 5: Current gain cell [10]

where I_{in} is input to the filter (output of the sensor), I_o is output of the filter and I_{α_6} is the current required for the second integrator in the filter (Fig.3). The implementation of (11) with $CMOS$ transistors is discussed next.

3.1. Proposed Current Multiplier for Adaptive Filter

One approach to achieve multiplication of two signals x and y is accomplished by evaluating their quadratic terms: $(x+y)^2-(x-y)^2=4xy$. With this base, in [10] a $CMOS$ current gain cell is proposed (Fig.5). It consists of a summer and subtractor (S & S), a linear current to voltage convertor, and two matched MOS transistors M_1 and M_2, which are assumed to perform voltage-to-current conversion with a squaring characteristic. I_1 is the input current to be amplified and I_c is a current for the gain control. These two currents are applied to the input nodes of S & S. After $i \longrightarrow v$ conversion, both voltages, $R(I_c+I_1)$ and $R(I_c-I_1)$ are applied to M_1 and M_2, respectively. Applying square-law characteristic to M_1 and M_2 yields:

$$I_{om}=\frac{\beta}{2}[R(I_c+I_1)-V_t]^2-\frac{\beta}{2}[R(I_c-I_1)-V_t]^2=2\beta R(I_cR-V_T)I_1 \quad (12)$$

Where I_{om} is the output of the current gain cell, V_t is threshold voltage and β is a process dependent constant.
To evaluate this current gain cell, transistor level simulation was performed using MOS models including all high-order effects and realistic parameters of $0.35\mu m$ CMOS process. The following linear relationship of the cell input-output was obtained for $8<I_1<55\mu A$ and $0.2<I_c<8\mu A$:

$$I_{om}=0.087(I_1+33)(I_c+0.263) \quad (13)$$

Out of the above ranges, there is a nonlinear input-output relationship because some of the transistors in the S & S are leaving their saturation region. Whereas, for the adaptive compensation filter, a current multiplier is needed with the input-output relationship of (11) and the input current ranges of $0<I_{in}<20\mu A$ and $0<I_o<10\mu A$, which are correspond to $0<m<1kg$. Since the load cell output (I_{in}) is oscillatory, with the steady-state value of $10\mu A$, its peak could be as much as $20\mu A$. To achieve these features, the block diagram depicted in Fig.6 is proposed, which contains current mirrors (b_1, b_c, b_o and b_{11}) and constant current sources (I_{01}, I_{0c} and I_{0o}). The aim of b_1, I_{01} and I_{0c} are to bring the range of the multiplier input currents to the operating range of the current gain cell. The following equations can be obtained from Fig.6:

$$I_1=b_1I_{in}+I_{01} \quad (14)$$

$$I_c=b_cI_o+I_{0c} \quad (15)$$

$$I_{\alpha 6}=b_oI_{om}-I_{0o}-b_{11}I_o \quad (16)$$

In order to find the appropriate values for b_c, b_0, b_{11} and I_{0o}, the combination of (14), (15), (16) and (13) gives a relationship for $I_{\alpha 6}$, which should be made equivalent to (11).

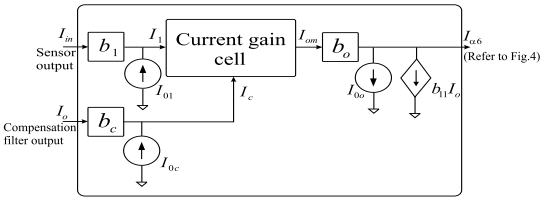

Figure 6: Proposed multiplier for adaptive compensation

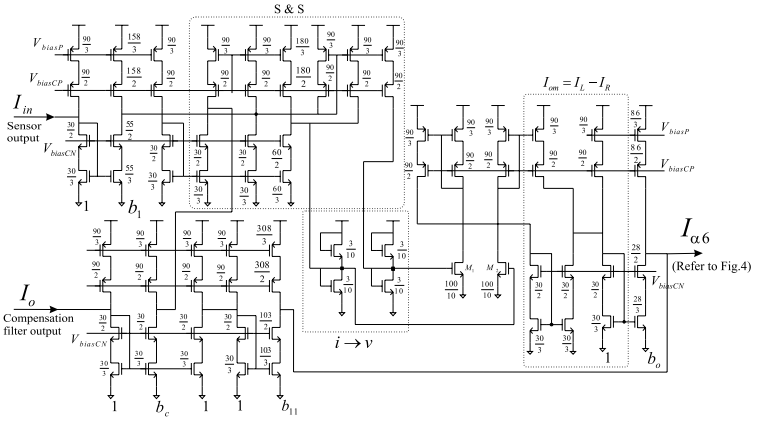

Figure 7: Transistor-level realisation of Fig.6

The $CMOS$ realisation of the block diagram of Fig.6 is shown in Fig.7. The size of squaring characteristic transistors, M_1 and M_2 are equal and it is $\frac{W}{L}=\frac{100\mu m}{10\mu m}$ and $\frac{W}{L}$ of transistors in $i \longrightarrow v$ convertors are $\frac{3\mu m}{10\mu m}$. The other part of the circuit, including S & S, are composed of current mirrors. The structure of the current mirrors and the size of their transistors are designed such that to be compatible with the the compensation filter, which is explained in the next section.

3.2. CMOS Adaptive Compensation Filter

Current mirrors and memory cells in the filter affect the performance of switched-current circuits and numerous designs have been proposed to have improved cells [9]. In this work, to improve transmission errors, due to the finite input conductance and nonzero output conductance of transistors, high compliance cascode memory cell and current mirror have been used. The bias currents for the memory cells and NMOS mirrors are chosen to be $J=100\mu A$, which are provided by PMOS mirrors of the same type and bias voltages (V_{biasP}, V_{biasCP} and V_{biasCN}) can be produced by a separate bias generation circuit. Different bias currents in the all current mirrors can be altered easily by scaling all transistor widths. In addition, the circuit needs to be preceded by a sample-and-hold with multiple scaled output currents. All the filter switches are implemented by $NMOS$ transistors. The complete adaptive compensation filter is shown in Fig.8, in which the box marked " X " denotes the proposed multiplier circuit of Fig.7 needed to achieve adaptive operation. As it can been seen, the adaptive compensation filter consists of entirely of transistors without using capacitors and resistors, which retains the important advantage of being compatible with digital $CMOS$ process. The combination of relatively large size memory transistor and minimum geometry switch transistor is chosen primarily to keep the effect of charge injection errors at a reasonable level. However, the use of a reasonably large memory transistor also has other performance benefits, such as lower output conductance, better matching and improved current mirror resolution. Hence, the aspect ratio of the memory transistors is considered to be $\frac{W}{L}=\frac{30\mu m}{3\mu m}$ and for the $NMOS$ switch $\frac{W}{L}=\frac{2\mu m}{0.35\mu m}$.

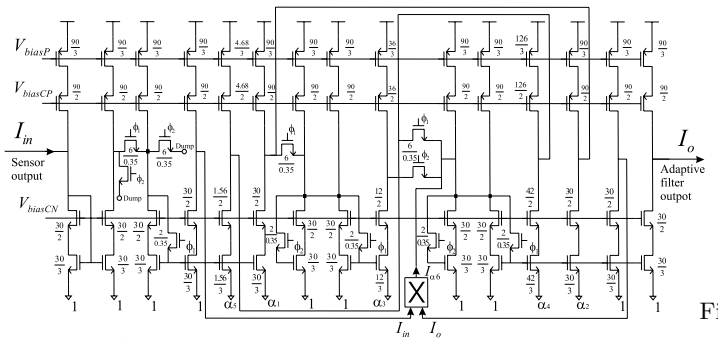

Figure 8: Adaptive compensation filter using only transistors

4. TEST AND RESULTS

To test the compensation filter, the output signal of the load cell is needed. For CMOS transistor level simulation with Cadence, a VerilogA behavioral modelling facility has been used, which can produce load cell oscillatory current. A step excitation current is applied to the load cell model whose output has been applied to the compensation filter and according to the amplitude of excitation current, the value of the $(m+m_0)$ has been changed in the VerilogA model.

The circuit in Fig.8, including the multiplier circuit of Fig.7, was simulated using Cadence with $0.35\mu m$ 3.3V BSim3v3 CMOS foundry models. Fig.9 shows the load cell output and the compensation filter output for $m = 0.1kg$, which corresponds to $1\mu A$ excitation current. To illustrate the capability of the filter in tracking changes in m, Fig.10 shows the results for $m = 1kg$ corresponding to $5\mu A$ excitation current. Clearly these results show that fully $CMOS$ adaptive compensation filter can be used to correct the oscillatory output of the load cell sensor. To indicate the effectiveness of using an adaptive filter, a fixed filter was also used for compensation. When the excitation current is $5\mu A$, a fixed filter suitable for $m = 0.1kg$ have been used and the input and output of the filter are depicted in Fig.11, which shows that the fixed filter is unable to perform the sensor response correction.

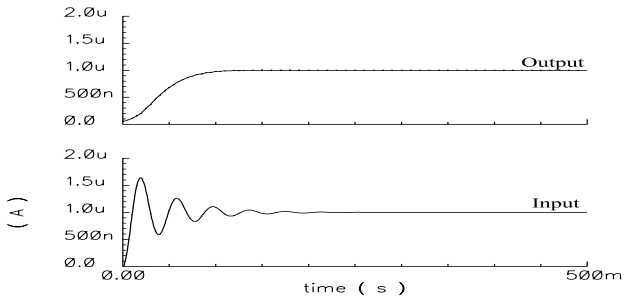

Figure 9: Input and output of the adaptive filter for m=0.1kg

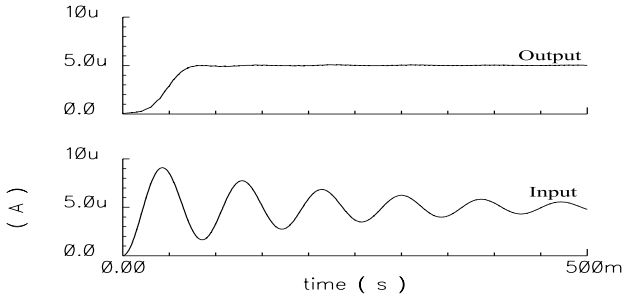

Figure 10: Input and output of the adaptive filter for m=0.5kg

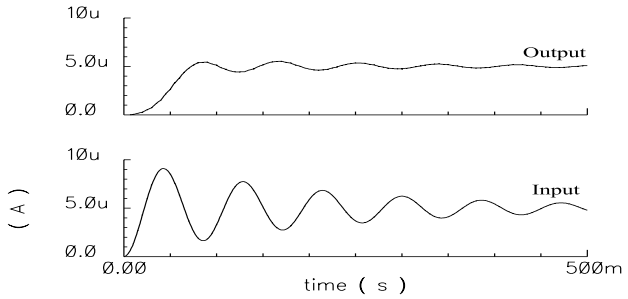

Figure 11: Input and output of non-adaptive filter (m=0.5kg)

5. CONCLUDING REMARKS

This paper has shown that it is possible to perform effective response compensation of dynamic sensors using switched-current techniques. The proposed analog adaptive filter employs only transistors without using passive elements and therefore compatible with digital $CMOS$ process, which makes it suitable for SoC applications. Adaptive response correction is achieved by developing a new $CMOS$ current multiplier circuit. Transistor-level simulations of the adaptive compensation filter, with realistic Spice transistor models, confirm the effectiveness of the proposed technique.

6. REFERENCES

[1] W J Shi N M White and J E Brignell. 'Adaptive filters in load cell response correction'. *Sensors and Actuators A*, A 37-38:280–5, 93.

[2] A A Yasin and N M White. 'The application of artificial neural network to intelligent weighing systems'. *IEE proc.- Science, Measur. and Tech.*, 146:265–9, Nov. 99.

[3] M. Jafaripanah B. M. Al-Hashimi and N. M. White. 'Load cell response correction using analog adaptive techniques'. pages IV752–5, ISCAS, 2003.

[4] M. Jafaripanah B. M. Al-Hashimi and N. M. White. 'Application of analog adaptive filters for dynamic sensor compensation'. *To be appear in IEEE Trans. on Instru. and Measur.*, 54(1), Feb. 2005.

[5] A. Graupner J. Schreiter S. Getzlaff and R. Schuffny. 'CMOS image sensor with mixed signal processor array'. *IEEE J. Solid-State Circuits.*, 38(6):948–57, June 2003.

[6] M. Sergio N. Manaresi F. Campi R. Canegallo M. Tartagni R. Guerrieri. 'A dynamically reconfigurable monolithic CMOS pressure sensor for smart fabric'. *IEEE J. Solid-State Circuits*, 38(6):966–75, June 2003.

[7] C. Rubio S. Bota J. G. Macias J. Samitier. 'Modelling, design and test of a monolothic integrated magnetic sensor in a digital CMOS technology using a switched current interface system'. *Analog Integrated Circuits and Signal Processing*, 29:115–26, 2001.

[8] J. B. Hughes A. Worapishet and C. Toumazou. 'Switched-capacitors versus switched-currents'. pages 409–412. ISCAS, 2000.

[9] C. Toumazou J. B. Hughes and N. C. Battersby, editors. *'Switched-Current: An Analogue Technique for Digital Technology'*. IEE Peter Peregrinus Ltd., London,UK, 93.

[10] Z. Wang. 'Two CMOS large current-gain cells with linearly variable gain and constant bandwidth'. *IEEE Trans. on circ. and syst. I: Fundamental theories and Applications*, 39(12):1021–4, Dec. 92.