Dynamic Sensor Compensation Using Analogue Adaptive Filter Compatible with Digital Technology

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Abstract: *An analogue adaptive filter for dynamic response compensation of a load cell sensor is presented. The filter employs only transistors and therefore it can be integrated using standard digital CMOS technology, which is suitable for System-on-Chip applications. To perform adaptive compensation over a wide range of measurand, a novel CMOS multiplier circuit was developed. The analogue adaptive filter has been designed and simulated using* $0.35\mu m$ *3.3V BSim3v3 CMOS foundry models and found to achieve effective compensation.*

1 Introduction and Motivation

Since information processing and control systems cannot function correctly if they receive inaccurate input data, compensation of the imperfections of sensors is one of the most important aspects of sensor research. The influence of unwanted signals, non-ideal frequency response, parameter drift, non-linearity, and cross-sensitivity are the five major defects in primary sensors. In the new generation of sensors, called intelligent or smart sensors, the

influence of these imperfections has been dramatically reduced by using signal processing techniques, which have resulted from advances in the field of digital systems.

Some sensors, such as load cells, have an oscillatory output, which needs time to settle down. It is therefore necessary to determine the value of the measurand while the output is still in oscillation. Load cells are used in a variety of industrial weighing applications such as vending machines and checkweighing systems. Since the measurand contributes to the load cell response characteristics, a compensation filter is required to track variation in measurand whereas a simple, fixed filter is only valid at one specific load value. A number of methods have been reported for dynamic sensor compensation. These include digital adaptive techniques [1], artificial neural network [2] and estimation with recursive least square procedure [3], which basically employ digital signal processing (DSP) chips or microcontrollers to implement the required filtering algorithms. Recently, analogue adaptive techniques [4, 5] have been used to perform effective sensor response compensation, with the main benefits being smaller size, lower complexity and lower power consumption compared to digital techniques. The sensor compensation analogue technique employs an adaptive biquadratic filter to track the variations in the measurand by changing the position of the filter zeroes. In [5], a discrete adaptive filter prototype consisting of op-amps, resistors and capacitors was produced to validate the compensation analogue technique in practice.

In recent years, the quest for smaller and cheaper electronic systems has led manufactures to integrate systems onto a single chip (Systems on Chip, SoC). In the sensor research community, efforts have focused on making silicon-based sensors and circuit designers investigate techniques to develop CMOS compatible analogue electronic circuits [6, 7, 8, 9, 10] because this is dominant processing technology used for integrated circuits and systems. Despite the effectiveness of the op-amp based compensation filter reported in [5], the filter is not compatible with digital CMOS technology since it contains resistors and capacitors. This limits its applications in SoCs, and therefore, the motivation of this research is to develop and implement an analogue filter for sensor compensation, which is compatible with CMOS technology. This means that the filter should not require floating capacitors or operational amplifiers. It should be noted that traditionally the switched-capacitor technique has been employed exten-

sively to integrate the analogue portion of mixed-signal chips. However, switched-capacitors are also not fully compatible with the digital CMOS process and as technology advances further, the drawbacks of switched-capacitor are becoming more significant [11]. The switched-capacitor techniques require high quality capacitors usually implemented using two layers of polysilicon. The second polysilicon layer used by the switched-capacitor is not required in wholly digital circuits and often it is not available, particularly in deep submicron technology used to fabricate SoCs.

This paper shows that it is possible to design and implement an analogue adaptive filter capable of effectively correcting the sensor response without the use of op-amps and floating capacitors. The proposed filter consists entirely of transistors and therefore it is suitable for integration using standard digital CMOS process (single polysilicon). The filter is designed using switched-current (SI) techniques, which exploit the ability of a MOS transistor to maintain its drain current, when its gate is open-circuited, through the charge stored on the parasitic gate oxide capacitance, and without the explicit need for designed capacitors. SI techniques are increasingly being applied to sensor applications as demonstrated in publications [6, 10, 12]. The application of SI to dynamic sensor compensation has not been addressed in the literature, and is therefore the main aim of this paper. The following contributions are made:

- All previously reported applications of SI to sensors do not require adaptive operation, unlike the load cell, which requires adaptive processing to track variation of the measurand. For example, the magnetic sensor reported in [10] employs a filter with fixed characteristics.

- A novel CMOS multiplier is proposed, which is needed to perform adaptive compensation for different measurand values of the sensor.

- Transistor level of the adaptive compensation filter is designed and simulated using $0.35\mu m$ 3.3V BSim3v3 CMOS foundry models.

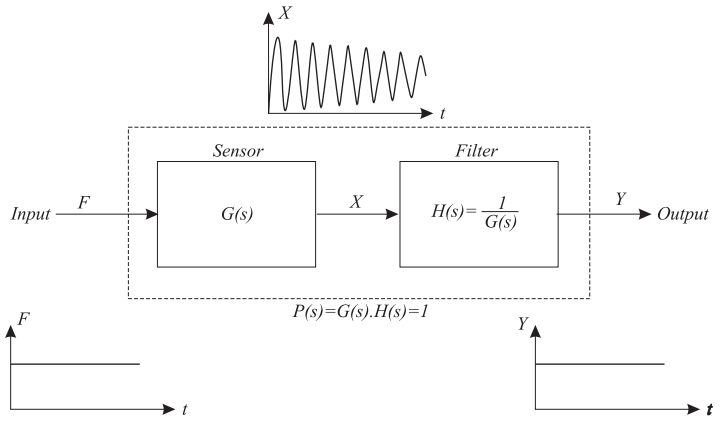

Figure 1: Principle of load cell response correction

2 Sensor Response Correction

The general principle of sensor response correction, in order to eliminate oscillatory sensor output, involves cascading a filter, having the reciprocal characteristic of the sensor, with it (Fig.1). Therefore, the transfer function of the whole system is *"unity"*, which means that any changes in the input transfer to the output without distortion.

It has been shown that the load cell can be modelled as a 2^{nd} order system [1]:

$$G(s) = \frac{X(s)}{F(s)} = \frac{\frac{1}{m+m_0}}{s^2 + \frac{c}{m+m_0}s + \frac{k}{m+m_0}} = \frac{A}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \tag{1}$$

Where m is the mass being weighed, m_0 is the effective mass of the sensor, c is the damping factor, k is the spring constant, and $F(t)$ is the force function. Equation (1) shows that m affects all characteristics of the sensor such as gain factor, A, quality factor, Q, and natural frequency, ω_0.

Equation (1) yields a pair of complex conjugate poles $a \pm jb$ where

$$a = -\frac{c}{2(m+m_0)} \tag{2}$$

and

$$b = \sqrt{\frac{k}{(m+m_0)} - \frac{c^2}{4(m+m_0)^2}} \tag{3}$$

Thus the zeros of the adaptive filter, which are the poles of the sensor, can be found. The parameter m is unknown in the first instance when a new measurement begins. Therefore the parameters of the adaptive filter can not be set to appropriate values in order that the filter

behaves as an inverse system. Hence, an adaptive rule is required to modify the parameters of the adaptive filter according to the value of measurand, m. Usually, in classic adaptive techniques, an adaptive algorithm, such as least mean squares (LMS) method, updates the parameters of the adaptive filter to minimise a cost function. However, (1) shows that, for a load cell, the suitable filter has a pair of conjugate zeros, $z_{1,2} = a \pm jb$, where, a and b can be considered as the parameters of adaptive filter and the relationship between them and the load is expressed in (2) and (3). The adaptive compensation operation is shown in Fig.2.

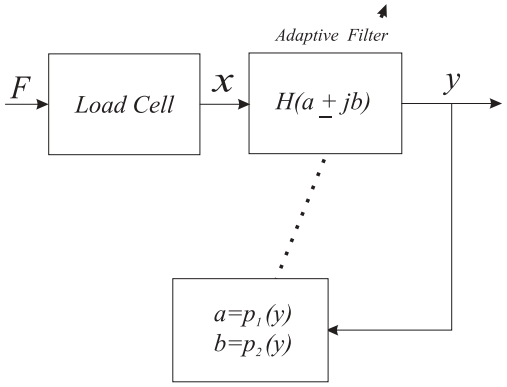

Figure 2: Block diagram of adaptive load cell response correction

Initially the zeros of the filter are set to arbitrary values. Then the output y is calculated. This new value of y is used to calculate the zeros of the filter once again. Repeating these steps results in a rapid approach to obtain the steady state value of y. So far the zeros of the 2^{nd} order compensation filter have been examined. In order that the analogue filter can be realised, it is necessary to add at least two poles to the filter. The values of these poles can be determined practically. These poles are selected as shown in [5] so that the output of the filter quickly reaches its steady-state value with minimum oscillation. The transfer function of the compensation filter is

$$H(s) = \frac{(m + m_0) \cdot s^2 + c \cdot s + k}{10^{-5}s^2 + 0.06s + 1} \tag{4}$$

The transfer functions of the load cell, (1,) and its compensation filter, (4), are biquadratic functions. The problem is how to make a biquad adaptive and from design simplicity point of view, it is necessary to have only one filter component to track changes in m without any influence on the other characteristics of the load cell such as c, and k. How to achieve

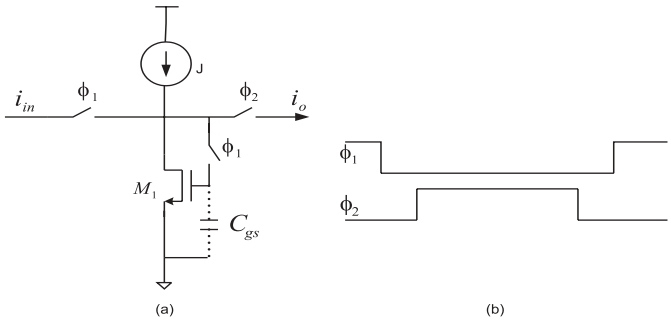

Figure 3: (a)-Current memory cell (b)-Clock waveforms

this with $CMOS$ transistor alone circuits is discussed in section 4 after an introduction to switched-current design, which is given next.

3 Switched-Current Design Principles

The basic element in switched-current (SI) design is a memory cell shown in Fig.3-a. The SI technique exploits the parasitic capacitance, C_{gs}, at the gate of a MOS transistor to maintain its drain current [13]. The current memory cell of Fig.3-a has one transistor M_1 and three switches, which are driven by the clock waveforms shown in Fig.3-b and operates as follows. On phase ϕ_1, the input current adds to the bias current J and the current $J+i_{in}$ flows initially into the discharged gate-source capacitor C_{gs}. As C_{gs} charges, the gate source voltage rises and when it exceeds the threshold voltage, M_1 conducts. Eventually the whole of the current $J+i_{in}$ flows in the drain of M_1. During the second phase, ϕ_2 , the gate of M_1 is disconnected from the drain so the gate voltage is held on C_{gs} and the input switch is now opened. This forces an output current $i_o = -i_{in}$ to flow throughout this phase. The output current is therefore a memory of the input current.

Fig.4-a shows a delay cell, created by cascading two memory cells. It should be noted that the output current i_{o1} is not available through the first phase, ϕ_1, and when the output current is required throughout the entire clock period then another transistor, M_3, and its associated bias current should be added. To achieve a scaled output current, i.e. $i_{o2}[n] = \alpha i_{in}[n-1]$, the aspect ratio of M_3 is α times that of M_2. This is shown in Fig.4 by putting "1", "1" and "α" under transistors M_1, M_2 and M_3, respectively, which means that $[\frac{W}{L}]_{M_2} = [\frac{W}{L}]_{M_1}$ and

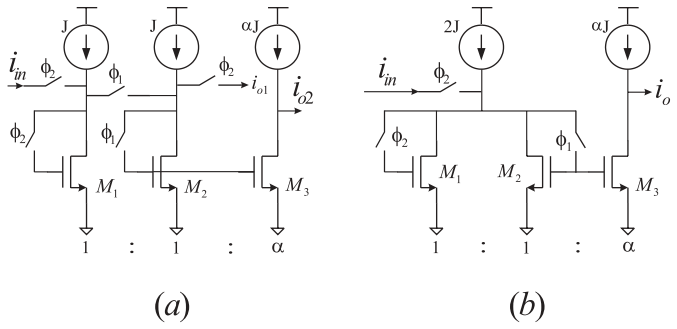

Figure 4: (a)-Delay cell (b)-Integrator

$[\frac{W}{L}]_{M_3} = \alpha \cdot [\frac{W}{L}]_{M_2}$, where W and L are the width and length of the MOS transistors.

A switched-current integrator can be obtained by feeding back the output current of the delay cell, i_{o1}, to the input summing node. This results in two parallel switches, one operating with ϕ_1 and another with ϕ_2, which is equivalent to a short circuit and two parallel bias currents that can be added together. The resulting integrator is shown in Fig.4-b, which can be used as a building block to construct other filter functions [14].

4 Adaptive Compensation Filter

To simplify the implementation of the compensation filter, we have chosen the integrator-based biquad circuit shown in Fig.5. With this choice, as shown later in this section, it is possible to track variation in the load cell measurand by controlling a single filter parameter. This biquad consists of two integrators and two feedback loops ($\alpha_2 I_o$ and $\alpha_4 I_o$) and appropriate signal summations. The s-domain transfer function of the biquad circuit is:

$$H(s) = \frac{[\frac{4\alpha_6+2\alpha_5-\alpha_1\alpha_3}{D}]s^2 + [\frac{4\alpha_5}{T.D}]s + [\frac{4\alpha_1\alpha_3}{T^2.D}]}{s^2 + [\frac{4\alpha_4}{T.D}]s + [\frac{4\alpha_2\alpha_3}{T^2.D}]} \tag{5}$$

where $D = 2\alpha_4 - \alpha_2\alpha_3 + 4$, T is the clock period and each α_i is the ratio of two currents in the filter circuit. Comparing (5), with the compensation filter transfer function, (4), gives:

$$\frac{4\alpha_6 + 2\alpha_5 - \alpha_1\alpha_3}{D} = 10^5(m + m_0) \tag{6}$$

$$\frac{4\alpha_5}{T.D} = 10^5 c \tag{7}$$

$$\frac{4\alpha_1\alpha_3}{T^2.D} = 10^5 k \tag{8}$$

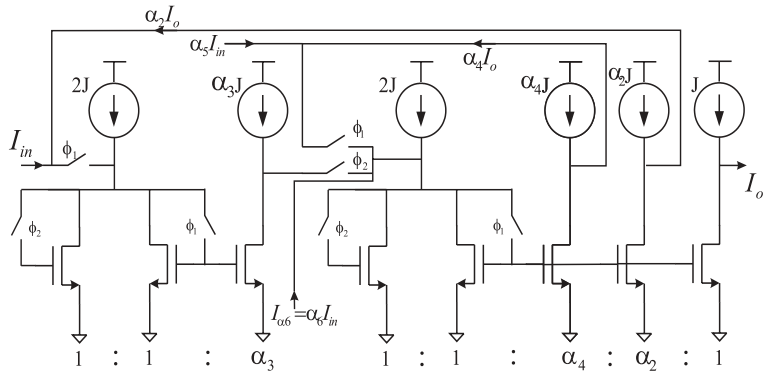

Figure 5: Integrator-based biquadratic filter [14]

$$\frac{4\alpha_4}{T.D} = 600 \tag{9}$$

$$\frac{4\alpha_2\alpha_3}{T^2.D} = 10^5 \tag{10}$$

Equation (6) shows that it is possible to have an adaptive filter, which is capable of tracking variations in m, by controlling only one filter parameter (α_6) without any influence on the other characteristics of the filter. Examining Fig.5 shows that α_6 is a coefficient for the filter input current ($I_{\alpha_6} = \alpha_6 I_{in}$) and in the adaptive case it should be $I_{\alpha_6} = \alpha_6(m) I_{in}$. In our current-mode filter, the output current, I_o, displays the load cell measurand, m, therefore having α_6 proportional to m is equivalent to control the filter input current by a variable gain proportional to the filter output current. This means that a current multiplier is needed to make an adaptive compensation filter. This is clarified schematically in Fig.6.

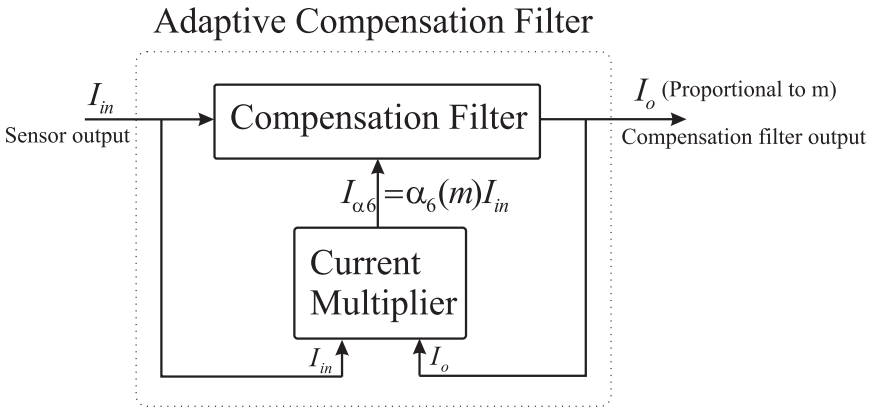

Figure 6: Adaptive compensation filter block diagram

The design procedure of the compensation filter involves determining the parameters ($\alpha_1 - \alpha_6$) of a fixed filter and then using a current multiplier block (Fig.6) to make it adaptive. From experimental data for a particular load cell [2] the damping factor c, spring constant k, and the effective mass of the load cell m_0, are 3.5, 2700 Pa, and 0.1 kg, respectively. In addition, as a starting point, m is considered to be 1 kg, which is an arbitrary choice. The parameters of the compensation filter can be calculated using (6) to (10). As outlined earlier, the filter parameters, α_i, are implemented by $[\frac{W}{L}]$ of the transistors in the current mirrors. The clock period, T, affects the spread of the transistor sizes for the filter. For different clock periods, considering (4) as the transfer function of the compensation filter results in wide ranges for α_i, which seems impractical. In order to achieve reasonable $\frac{W}{L}$ for the transistors in the filter design, the positions of filter poles in (4) is changed and it is scaled in magnitude. Note that the filter poles do not have significant effect on the compensation (refer to section 2). Therefore, the modified transfer function for the compensation filter is:

$$H(s) = \frac{1}{2700} \cdot \frac{(m + m_0) \cdot s^2 + c \cdot s + k}{(4 * 10^{-4})s^2 + 0.035s + 1} \tag{11}$$

With this transfer function, choosing $T = 10^{-2}s$ provides parameter spread of 25:1, while for $T = 10^{-5}s$ it is 3000000:1, which is clearly impractical. It is worth noting that the load cell output is oscillatory with low frequency (less than $30Hz$), therefore $T = 10^{-2}s$ is a reasonable choice. Using the values in the modified transfer function, (11), in (6) to (10) gives the parameters of the compensation filter shown in table 1.

Table 1: Compensation filter parameters, $T = 10^{-2}s$

α_1	α_2	α_3	α_4	α_5	α_6
1	1	0.4	1.4	0.0519	1.556

Load cell response correction for different values of the measurand, m, requires changing the compensation filter zero positions. As discussed earlier in this section, this can be achieved simply by varying the value of the parameter α_6 of the filter. To find how α_6 is related to m, using (6) to (10), the parameters of the filter are calculated for different values of m from $0.1kg$ to $1kg$. It is seen that the parameters α_1 to α_5 have the same values as in table 1, but

the value of α_6 differs for each m, as shown in table 2.

Table 2: Filter parameter α_6 for different values of measurand

$m[kg]$	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
α_6	0.222	0.37	0.519	0.667	0.815	0.916	1.111	1.259	1.407	1.556

It is possible to express the table values as a linear relationship between α_6 and m:

$$\alpha_6 = 1.4816m + 0.074 \tag{12}$$

To ensure the correct operation of the transistors in the filter circuit, it is assumed that a load cell measurand of $m = 1kg$ corresponds to $10\mu A$ output current. Therefore, with reference to Figs.6 and using (12), to have an adaptive compensation filter, a current multiplier block with the following relationship between its input and output is required.

$$I_{\alpha_6} = \alpha_6 \cdot I_{in} = (0.14816I_o + 0.074) \cdot I_{in} \tag{13}$$

where I_{in} is input to the filter (output of the sensor), I_o is output of the filter and I_{α_6} is the current required for the second integrator in the filter (Fig.5). The implementation of (13) with $CMOS$ transistors is discussed next.

4.1 Proposed Current Multiplier for Adaptive Compensation

One approach to achieve multiplication of two signals x and y is accomplished by evaluating their quadratic terms: $(x+y)^2 - (x-y)^2 = 4xy$. With this base, in [15] a $CMOS$ current gain cell is proposed. The principle of operation of this current gain cell is shown in Fig.7. It consists of a summer and subtractor (S & S), a linear current to voltage convertor, and two matched MOS transistors M_1 and M_2, which are assumed to be in saturation region and each performs voltage-to-current conversion with a squaring characteristic. I_1 is the input current to be amplified and I_c is a current for the gain control. These two currents are applied to the input nodes of S & S. After $i \longrightarrow v$ conversion, both voltages, $R(I_c + I_1)$ and $R(I_c - I_1)$ are applied to M_1 and M_2, respectively (R is the conversion factor). Applying square-law characteristic to M_1 and M_2 yields:

$$I_{om} = I_L - I_R = \frac{\beta}{2}[R(I_c + I_1) - V_T]^2 - \frac{\beta}{2}[R(I_c - I_1) - V_T]^2 = 2\beta R(I_c R - V_T)I_1 \tag{14}$$

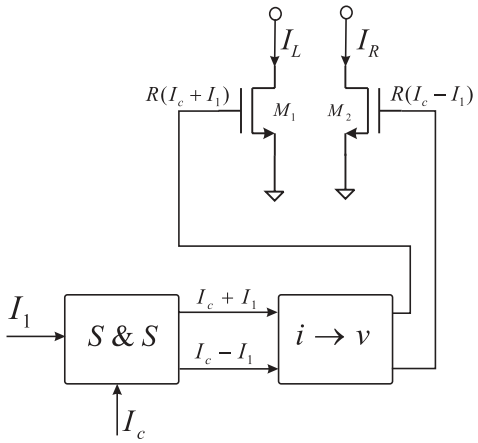

Figure 7: Current gain cell [15]

where I_{om} is the output of the current gain cell and $\beta = \mu C_{ox} W/L$, μ is the mobility of carriers, C_{ox} is the gate capacitance per unit area, V_T is the threshold voltage, and W and L are the channel width and length of the devices, respectively.

To evaluate this current gain cell, transistor level simulation was performed using Cadence with $0.35\mu m$ 3.3V BSim3v3 CMOS foundry models. The following linear relationship of the cell input-output was obtained empirically:

$$I_{om} = 0.087(I_1 + 33)(I_c + 0.263) \quad \text{for:} \quad 8 < I_1 < 55\mu A \quad \text{and} \quad 0.2 < I_c < 8\mu A \tag{15}$$

Out of the above ranges for I_1 and I_c, there is a nonlinear input-output relationship because some of the transistors in the S & S are leaving their saturation region. Whereas, for the adaptive compensation filter, a current multiplier with the following features is needed:

1. Input-output relationship of (13)

2. If we consider that the compensation filter operates for $0 < m < 1kg$, then the range of multiplier input currents should be $0 < I_{in} < 20\mu A$ and $0 < I_o < 10\mu A$. It should be noted that $10\mu A$ current corresponds to $m = 1kg$ and since the load cell output (I_{in}) is oscillatory, with the steady-state value of $10\mu A$, its peak could be as much as $20\mu A$.

To achieve these two features, the block diagram depicted in Fig.8 is proposed, which contains current mirrors (b_1, b_c and b_o), constant current sources (I_{01}, I_{0c} and I_{0o}) and a dependent current source ($b_{11} I_{in}$). The aim of b_1 and constant current sources I_{01} and I_{0c} are to bring

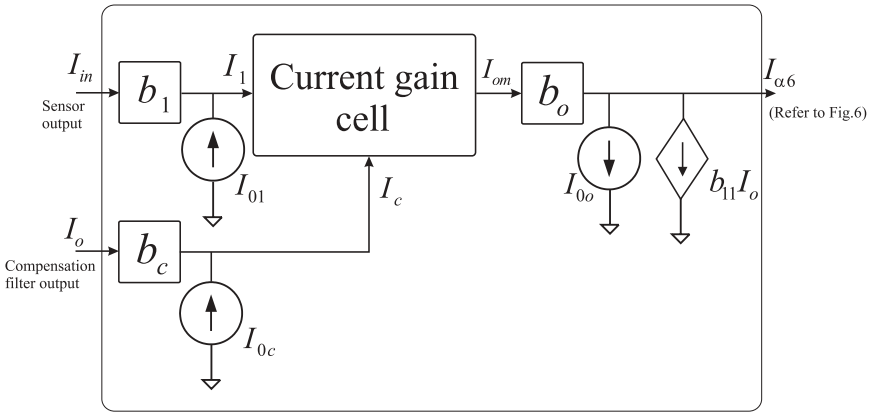

Figure 8: Proposed multiplier block diagram to achieve adaptive compensation

the range of the multiplier input currents to the operating range of the current gain cell. The following equations can be obtained from Fig.8:

$$I_1 = b_1 I_{in} + I_{01} \tag{16}$$

$$I_c = b_c I_o + I_{0c} \tag{17}$$

$$I_{\alpha 6} = b_o I_{om} - I_{0o} - b_{11} I_o \tag{18}$$

Combination of (16), (17), (18) and (15) yeilds:

$$\begin{aligned} I_{\alpha 6} = {} & 0.087 b_o b_1 b_c I_o I_{in} \\ & + 0.087 b_o b_1 (I_{0c} + 0.263) I_{in} \\ & + [0.087 b_o b_c (I_{01} + 33) - b_{11}] I_0 \\ & + 0.087 b_o (I_{01} + 33)(I_{0c} + 0.263) - I_{0o} \end{aligned} \tag{19}$$

Equation (19) should be made equivalent to (13), which gives the appropriate values for b_c, b_0, b_{11} and I_{0o}. This is achieved by making the coefficients of $I_o I_{in}$ and I_{in} in (19) equal to the coefficients of $I_o I_{in}$ and I_{in} in (13), respectively and making the third and fourth terms of (19) equal to zero, because there is no constant term and a term proportional to I_o in (13). The $CMOS$ realisation of the block diagram of Fig.8 is shown in Fig.9. The size of squaring characteristic transistors, M_1 and M_2 are equal and it is $\frac{W}{L} = \frac{100\mu m}{10\mu m}$ and $\frac{W}{L}$ of transistors in $i \longrightarrow v$ convertors are $\frac{3\mu m}{10\mu m}$. The other part of the circuit, including S & S, are composed

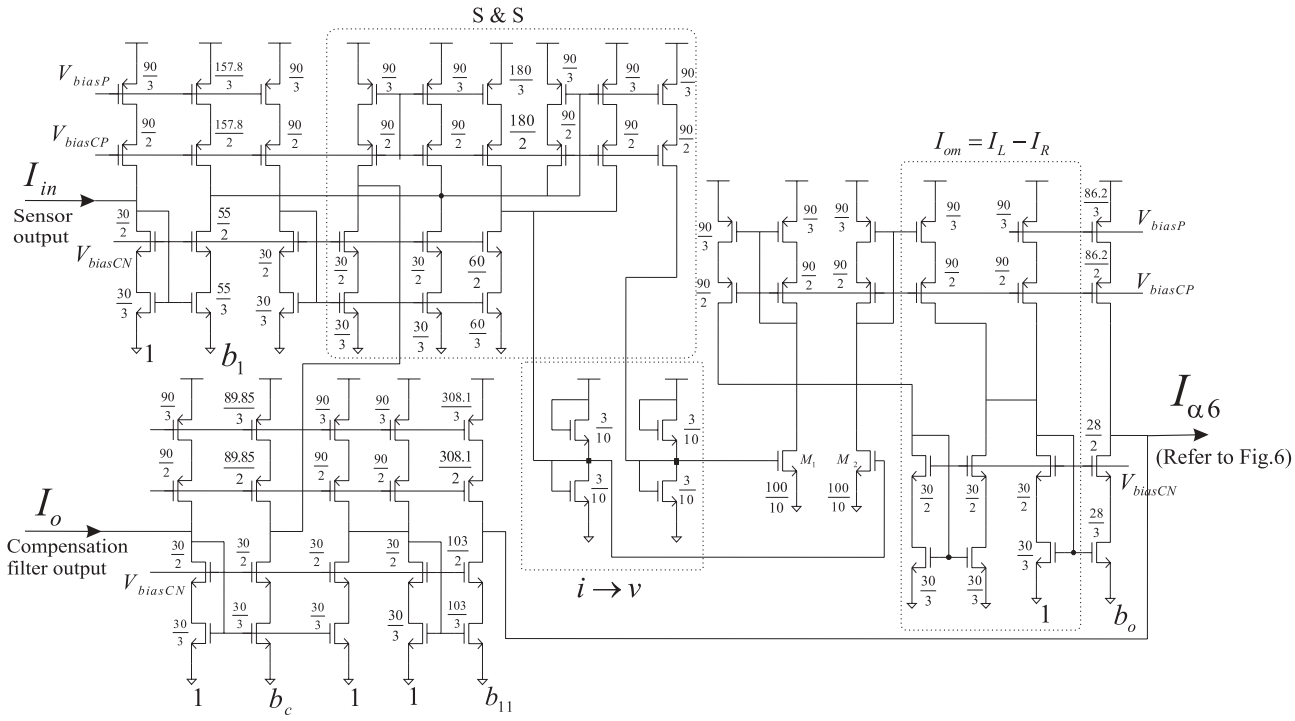

Figure 9: Transistor-level realisation of the multiplier block of Fig.8

of current mirrors. The structure of the current mirrors and the size of their transistors are designed such that to be compatible with the the compensation filter, which is explained in the next section. With this circuit, it is possible to realise equation 13 for $0 < I_{in} < 20\mu A$ and $0 < I_o < 10\mu A$.

4.2 CMOS Adaptive Compensation Filter

The biquadratic filter of Fig.5 contains bias current sources and switch symbols, which need to be replaced by transistor designs to allow $CMOS$ implementation of the circuit. Furthermore, the biquad has memory cells and current mirrors as outlined in section 3. Current mirrors and memory cells affect the performance of switched-current circuits and numerous designs have been proposed to have improved cells [14]. In this work, to improve transmission errors, due to the finite input conductance and nonzero output conductance of transistors, high compliance cascode memory cell and current mirror have been used. The bias currents for the memory cells and NMOS mirrors are chosen to be $J = 100\mu A$, which are provided by PMOS mirrors of the same type and bias voltages (V_{biasP}, V_{biasCP} and V_{biasCN}) can be

produced by a separate bias generation circuit once and distributed to all the current mirrors in the design [16]. Different bias currents in all the current mirrors can be altered easily by scaling all transistor widths. In addition, the circuit needs to be preceded by a sample-and-hold with multiple scaled output currents, which provide the parameters α_1, α_5 and the input of the current multiplier. All the filter switches are implemented by $NMOS$ transistors. The complete adaptive compensation filter is shown in Fig.10, in which the box marked " X " denotes the proposed multiplier circuit of Fig.9 needed to achieve adaptive operation. As it can been seen, the adaptive compensation filter consists of entirely of transistors without using capacitors and resistors, which retains the important advantage of being compatible with digital $CMOS$ process.

The combination of relatively large size memory transistor and minimum geometry switch transistor is chosen primarily to keep the effect of charge injection errors at a reasonable level. However, the use of a reasonably large memory transistor also has other performance benefits, such as lower output conductance, better matching and improved current mirror resolution, which need to be balance against the speed advantage of small devices. Hence, the aspect ratio of the memory transistors is considered to be $\frac{W}{L} = \frac{30\mu m}{3\mu m}$ and for the $NMOS$ switch $\frac{W}{L} = \frac{2\mu m}{0.35\mu m}$.

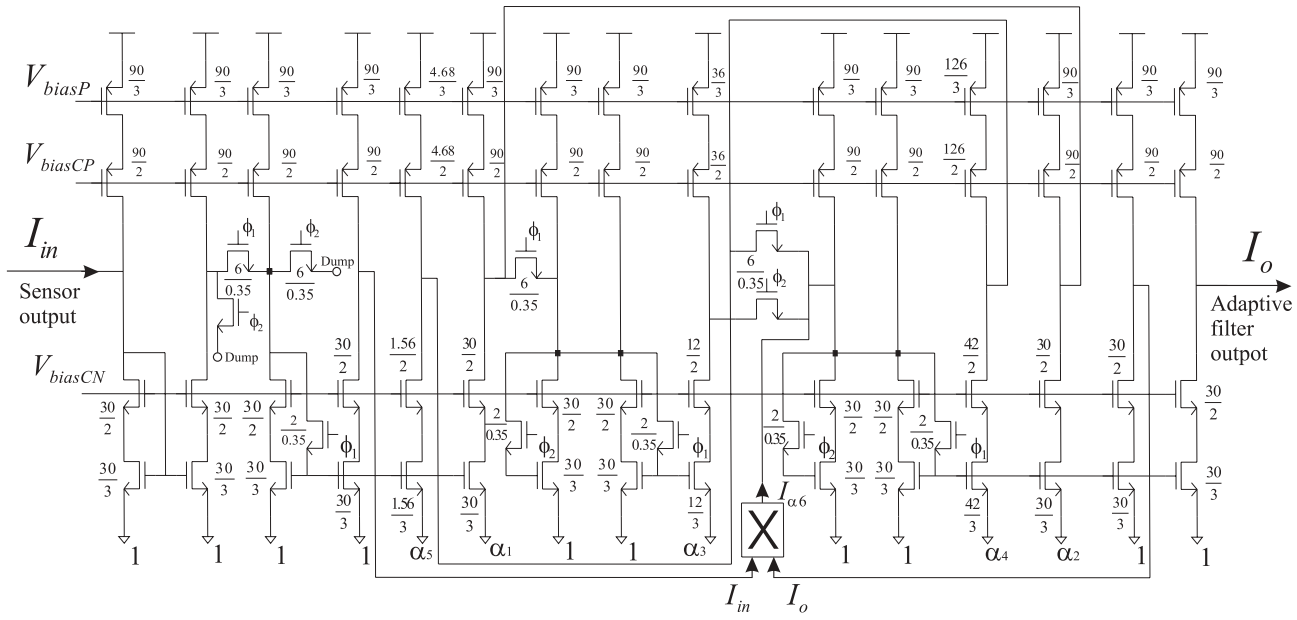

Figure 10: Adaptive compensation filter containing only CMOS transistors

5 Test and Results

To test the compensation filter, the output signal of the load cell is needed. In [4], we developed computer models for the load cell and the adaptive compensation filter and they have been implemented in PSpice, and also validated by practical discrete circuit[5]. However, for CMOS transistor level simulation with Cadence, a VerilogA behavioral modelling facility has been used, which can produce load cell oscillatory current. A step excitation current is applied to the load cell model (Fig.11) whose output has been applied to the compensation filter and according to the amplitude of excitation current, the value of the $(m + m_0)$ has been changed in the VerilogA model.

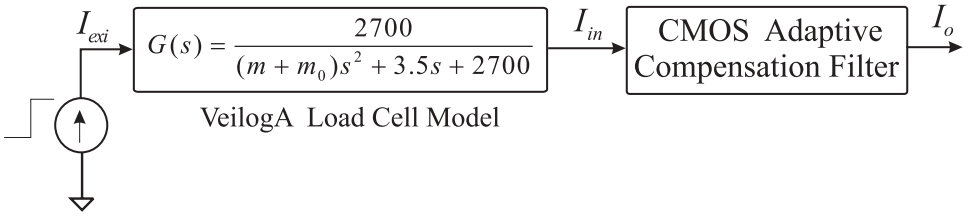

Figure 11: Block diagram of the test setup

The circuit in Fig.10, including the multiplier circuit of Fig.9, was simulated using Cadence with $0.35\mu m$ 3.3V BSim3v3 CMOS foundry models. Fig.12 shows the load cell output and the compensation filter output for $m = 0.1kg$, which corresponds to $1\mu A$ excitation current. To illustrate the capability of the filter in tracking changes in m, Fig.13 shows one of the sample results for $m = 0.5kg$ corresponding to $5\mu A$ excitation current. Clearly these results show that fully $CMOS$ adaptive compensation filter can be used to correct the oscillatory output of the load cell. To indicate the effectiveness of using an adaptive filter, a fixed filter was also used for compensation. When the excitation current is $5\mu A$, a fixed filter suitable for $m = 0.1kg$ have been used and the input and output of the filter are depicted in Fig.14, which shows that the fixed filter is unable to perform the sensor response correction.

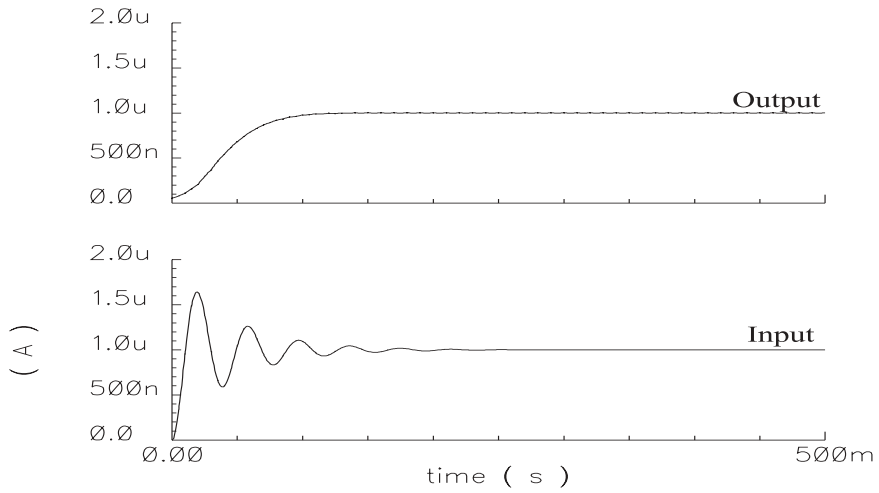

Figure 12: Input and output of the adaptive compensation filter for m=0.1kg

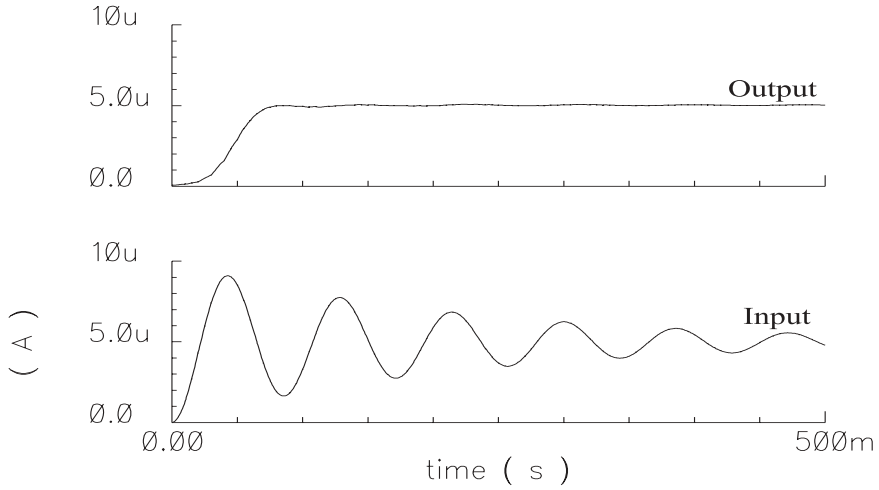

Figure 13: Input and output of the adaptive compensation filter for m=0.5kg

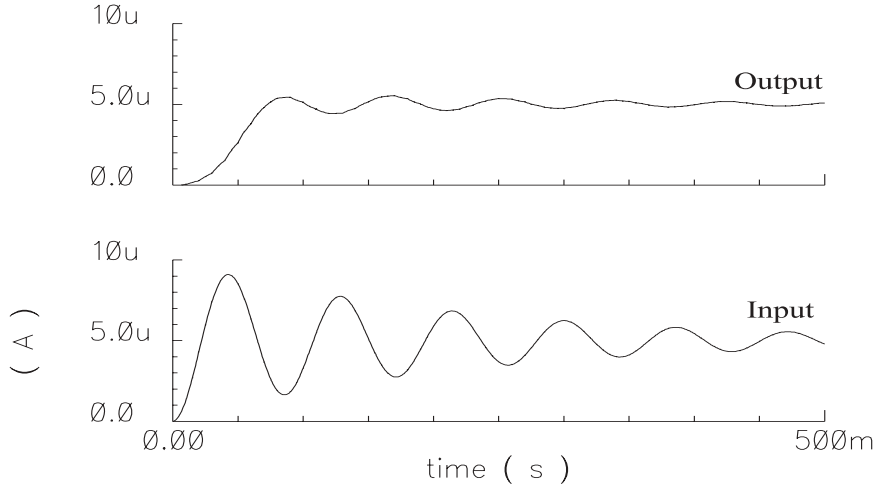

Figure 14: Input and output of the non-adaptive filter with m = 0.5kg

6 Concluding Remarks

This paper has shown that it is possible to perform effective response compensation of dynamic sensors using switched-current techniques. The proposed analogue adaptive filter employs only transistors without using passive elements and therefore compatible with digital $CMOS$ process, which makes it suitable for system-on-chip applications. This has been demonstrated with a reference to a load cell sensor. It has been shown that the integrator-based biquadratic filter provides an accurate and flexible compensation filter model, since it needs only one filter parameter to track variations in the load cell measurand. Adaptive response correction is achieved by developing a new $CMOS$ current multiplier circuit. Transistor-level simulations of the adaptive compensation filter, with realistic Spice transistor models, confirm the effectiveness of the proposed technique.

References

[1] W J Shi N M White and J E Brignell. 'Adaptive filters in load cell response correction'. *Sensors and Actuators A*, A 37-38:280–5, 1993.

[2] A A Yasin and N M White. 'The application of artificial neural network to intelligent weighing systems'. *IEE proceedings- Science, Measurement and Technology*, 146:265–9, Nov. 1999.

[3] W-Q. Shu. 'Dynamic weighing under nonzero initial condition'. *IEEE Transaction on Instrumentation and measurement*, 42(4):806–11, Aug. 1993.

[4] M. Jafaripanah B. M. Al-Hashimi and N. M. White. 'Load cell response correction using analog adaptive techniques'. pages IV752–5, IEEE International Symposium on Circuits and Systems, Thailand, May 2003.

[5] M. Jafaripanah B. M. Al-Hashimi and N. M. White. Application of analog adaptive filters for dynamic sensor compensation. *IEEE Transaction on Instrumentation and Measurements*, 54(1):245–251, Feb. 2005.

[6] A. Graupner J. Schreiter S. Getzlaff and R. Schuffny. 'CMOS image sensor with mixed signal processor array'. *IEEE Journal of Solid-State Circuits*, 38(6):948–957, June 2003.

[7] M. Sergio N. Manaresi F. Campi R. Canegallo M. Tartagni R. Guerrieri. 'A dynamically reconfigurable monolithic CMOS pressure sensor for smart fabric'. *IEEE Journal of Solid-State Circuits*, 38(6):966–975, June 2003.

[8] S. Chatzandroulis D. Goustouridis P. Normand D. Tsoukalas. 'A solid-state pressure-sensing microsystem for biomedical applications'. *Sensors and Actuators A*, 62:551–5, July 1997.

[9] S. Kawahito. 'Recent developments in sensor interfaces'. pages 37–40, EUROSENSORS XVI, Czech Republic, Sep. 2002.

[10] C. Rubio S. Bota J. G. Macias J. Samitier. 'Modelling, design and test of a monolothic integrated magnetic sensor in a digital CMOS technology using a switched current interface system'. *Analog Integrated Circuits and Signal Processing*, 29:115–126, 2001.

[11] J. B. Hughes A. Worapishet and C. Toumazou. 'Switched-capacitors versus switched-currents'. pages 409–412. IEEE International Symposium on Circuits and Systems, Switzerland, May 2000.

[12] C. Rubio O. Ruiz S. Bota J. Samitier. 'Switched current interface circuit for micromachined accelerometer'. pages 458–63. IEEE Instrumentation and Measurement Technology Conference, Italy, May 1999.

[13] J.B. Hughes N.C. Bird and I. C. Macbeth. 'Switched-current, a new technique for analogue sampled-data signal processing'. pages 1584–7. IEEE International Symposium on Circuits and Systems, May 1989.

[14] C. Toumazou J. B. Hughes and N. C. Battersby, editors. *'Switched-Current: An Analogue Technique for Digital Technology'*. IEE Peter Peregrinus Ltd., London,UK, 1993.

[15] Z. Wang. 'Two CMOS large current-gain cells with linearly variable gain and constant bandwidth'. *IEEE Transaction on circuits and systems I: Fundamental theories and Applications*, 39(12):1021–4, Dec. 1992.

[16] R. Wilcock and B. M. Al-Hashimi. 'Power-aware design method for class A switched-current wave filter'. *IEE proceedings- Circuits, Devices and Systems*, 151(1):1–9, Feb. 2004.