Differential Acquisition of m-Sequences Using Recursive Soft Sequential Estimation

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***Abstract*—In this paper, a novel sequential estimation method is proposed for the acquisition of m-sequences. This sequential estimation method exploits the principle of iterative soft-in–soft-out (SISO) decoding for enhancing the acquisition performance, and that of differential preprocessing for the sake of achieving an enhanced acquisition performance, when communicating over various communication environments. Hence, the advocated acquisition arrangement is referred to as the differential recursive soft sequential estimation (DRSSE) acquisition scheme. The DRSSE acquisition scheme exhibits a low complexity, which is similar to that of an m-sequence generator, while achieving an acquisition time that is linearly dependent on the number of stages in the m-sequence generator. A low acquisition time is achieved with the advent of the property that the proposed DRSSE scheme is capable of determining the real-time reliabilities associated with the decision concerning a set of, say, S consecutive chips. This set of consecutive chips constitutes the sufficient initial condition for enabling the local m-sequence generator to produce a synchronized local despreading m-sequence replica. Owing to these attractive characteristics, the DRSSE acquisition scheme constitutes a promising initial synchronization scheme for acquisition of long m-sequences, when communicating over various propagation environments.**

***Index Terms*—Acquisition, differential detection, initial synchronization, m-sequence, pseudonoise (PN) signals, recursive decoding, sequential estimation, soft-in–soft-out (SISO) decoding, spread-spectrum signals.**

I. Introduction

PSEUDONOISE (PN) code acquisition—which is also often referred to as initial synchronization—is inevitably the first step in the receiver of spread-spectrum communications schemes, since data demodulation becomes possible only after code acquisition has been accomplished. Various m-sequences have been employed in both IS-95 and in the cdma2000 standards [1], [2] either for direct-sequence spreading or for scrambling. In the context of the acquisition of m-sequences, the sequential estimation acquisition arrangement proposed by Ward [3] constitutes one of the simplest acquisition schemes. The philosophy behind the sequential estimation acquisition scheme is as follows. The acquisition of an m-sequence of length $(2^S - 1)$ is deemed successful, provided that S consecutive chips are correctly received by the acquisition device and are loaded into the local m-sequence generator, where successive shifts of the chips in the generator will generate chips that exactly match the forthcoming received chips of the transmitted m-sequence. However, in the presence of noise, one or more of the S consecutive chips might be in error, potentially resulting in erroneous loading of the m-sequence generator. In this case, a new set of S chips can be processed similarly.

Clearly, the most critical requirement for attaining the successful acquisition of PN sequences based on sequential estimation [3] is that S consecutive chips of the received and noise-contaminated PN sequence have to be correctly estimated. Ward [3] has shown that, for moderate SNR per-chip values, this acquisition scheme is capable of providing a shorter expected acquisition time than the conventional sliding correlator-based acquisition scheme [4]. However, in spread-spectrum communications, the transmitted signal energy is spread over dozens or even hundreds of chips and hence the SNR per chip value is typically low. Therefore, the estimation of S consecutive chips using chip-by-chip-based hard decisions is typically unreliable. In order to improve the reliabilities associated with deciding upon the value of S consecutive initial chips, Kilgus [5] proposed a majority logic decoding-aided scheme for estimating the required S number of consecutive chips. By contrast, in [6], Ward and Yiu have proposed a recursive sequential estimation-assisted acquisition scheme. It was shown that both of the above schemes are capable of significantly improving the acquisition performance by exploiting the inherent properties of the m-sequences for aiding the estimation of the S consecutive chips. However, all existing sequential estimation-based acquisition schemes operate on the basis of hard-decision chips. In [7] and [8], a soft sequential estimation scheme has been proposed for the acquisition of m-sequences. The soft sequential estimation scheme is designed based on the principles of iterative soft-in–soft-out (SISO) decoding. However, in the existing sequential estimation-based acquisition schemes, coherent detection was assumed, which is often unrealistic to achieve, since prior to despreading the SNR is usually insufficiently high for attaining a satisfactory carrier-phase tracking.

In this paper, we invoke the iterative SISO decoding principle—which has originally been developed for turbo channel decoding [9]–[11]—for improving the reliabilities associated with deciding upon the S consecutive chips to be loaded into the local m-sequence generator. Upon exploiting the inherent properties of m-sequences, a differential recursive soft sequential estimation (DRSSE) acquisition scheme is proposed. In the DRSSE acquisition scheme, the transmitted m-sequence is first mapped to another m-sequence, where the time-varying carrier phase is removed with the aid of differential preprocessing. Then, S consecutive chips of the resultant m-sequence

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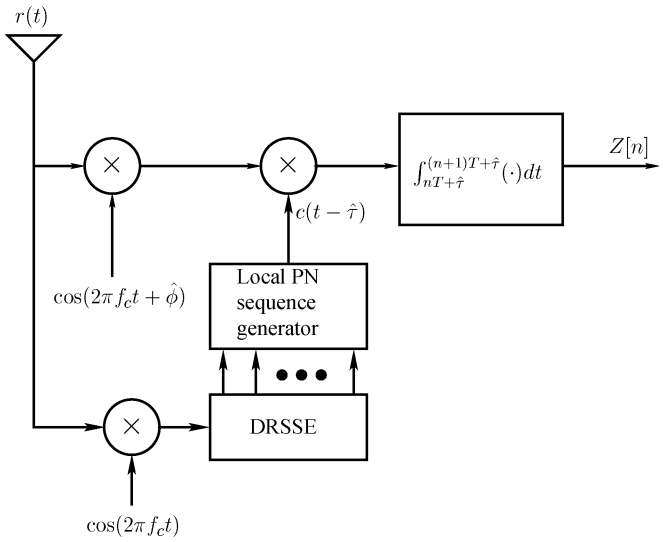

Fig. 1. Coherent correlation receiver using the proposed DRSSE acquisition scheme.

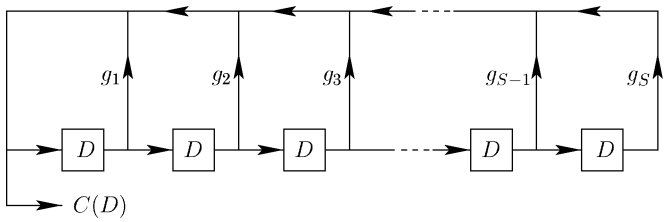

Fig. 2. Maximal-length sequence (m-sequences) generator that outputs binary sequences.

are estimated using a recursive SISO decoder. The recursive SISO decoder receives soft information from the differential processor's output (*intrinsic* information) and soft *extrinsic* information [9]–[11] from the soft channel outputs associated with the previous chips. The soft output of the recursive SISO decoder is then shifted into a so-called soft-chip register, which provides *extrinsic* information for the forthcoming decoding steps. An important feature of the proposed DRSSE acquisition scheme is that it exploits the real-time knowledge of the reliabilities associated with the S consecutive chips. By exploiting this real-time knowledge of the chip reliabilities, the acquisition device becomes capable of astutely managing the loading of S consecutive chips into the local m-sequence generator. The proposed DRSSE acquisition scheme has an algorithmic complexity which is similar to that of an m-sequence generator. Our simulation results will show that the acquisition time of the DRSSE acquisition scheme is a linear function of the number of stages in the m-sequence generator. Furthermore, the DRSSE acquisition scheme is suitable for m-sequence acquisition, when communicating over various environments including additive white Gaussian noise (AWGN), slow fading, and fast fading channels. This is because the differential processing is at the chip level of the m-sequences and, during a chip interval, the fading-induced phase changes are low, even when the Doppler frequency shift is relatively high.

The remainder of this paper is organized as follows. Section II describes the principle of the sequential estimation acquisition. In Section III, the proposed DRSSE acquisition scheme is described and investigated. In Section IV, we provide simulation results, and, finally, in Section V, we present our conclusions.

II. Principle of Sequential Estimation Acquisition

The correlation detector of a typical coherent direct-sequence spread-spectrum (DS-SS) invoking the proposed DRSSE initial PN acquisition scheme is shown in Fig. 1, where $\hat{\tau}$ and $\hat{\phi}$ represent the local estimates of the transmission delay and the carrier phase angle of the received signal, respectively. In Fig. 1, the local PN sequence generator constituted by the m-sequence generator in this contribution, generates a despreading waveform $c(t)$, which is correlated with the received signal, in order to despread the received spread-spectrum signal and to generate the decision variable $Z[n]$ related to the nth transmitted symbol. Furthermore, in Fig. 1, the DRSSE block implements the initial PN sequence acquisition scheme. Let us now focus our attention on the detailed operation of the DRSSE acquisition scheme.

The well-established maximum-length sequences, which are also known as m-sequences, are generated using feedback shift registers of the form shown in Fig. 2. In Fig. 2, D represents a unity time-delay operation while each of the coefficients $g_1, g_2, \ldots, g_S$ represents the presence of a connection if it is a 1 or the absence of a connection if it is a 0. Since spread-spectrum communication systems usually employ binary spreading sequences having chip values of $\{+1, -1\}$, in this contribution we assume that the m-sequence generator outputs duo-binary $\{+1, -1\}$ symbols, representing a logical zero with $+1$. Consequently, the conventional modulo-2 addition defined over the field of {1,0} is now replaced by the modulo-2 multiplication operation defined in the field of $\{+1, -1\}$, as shown in Fig. 2. More specifically, let the output binary sequence be $\ldots, c_{-2}, c_{-1}, c_0, c_1, c_2, \ldots$, where $c_i \in \{+1, -1\}$. Furthermore, we assume, without loss of any generality in Fig. 2, the coefficients $g_{s_1} = g_{s_2} = \ldots = g_{s_l} = \ldots = g_{s_M=S} = 1$, where s_i is an integer in the range of $[1, S]$, while the remaining coefficients are 0s. The above configuration corresponds to the generator polynomial of

$$g(D) = 1 + D^{s_1} + D^{s_2} + \ldots + D^{s_l} + \ldots + D^{s_M=S} \quad (1)$$

where $g(D)$ must be a primitive polynomial [12], i.e., a polynomial that cannot be factorized, in order to generate an m-sequence. Based on the above assumptions, it can be shown that the output symbols of Fig. 2 obey the recursive relationship of

$$\begin{aligned} c_i &= c_{i-s_1} c_{i-s_2} \cdots c_{i-s_l} \cdots c_{i-(s_M=S)} \\ &= \prod_{m=1}^{M} c_{i-s_m} \text{ for } i = \ldots, -1, 0, 1, \ldots \end{aligned} \quad (2)$$

where $\prod$ represents the product of the coefficients.

In spread-spectrum communications using m-sequences as spreading sequences, (2) implies that, if the receiver has the knowledge of the chip values $c_{i-1}, c_{i-2}, \cdots, c_{i-S}$ before the transmitter generates the ith chip c_i and if the receiver uses the same m-sequence generator as the transmitter, then the chip values $c_{i-1}, c_{i-2}, \cdots, c_{i-S}$ can be loaded into the corresponding registers of the m-sequence generator at the receiver for generating the forthcoming chips. Consequently, the corresponding replicas of the ith as well as the forthcoming chips,

namely $c_i, c_{i+1}, \ldots$, can be obtained at the receiver, which exactly match the received chips as a result of the transmitted m-sequence. Hence, the despreading of the spread transmitted signal can be successfully carried out by correlating it with the m-sequence replica generated at the receiver. What we have described above constitutes the principle behind the sequential estimation acquisition scheme proposed by Ward [3].

Below we propose and investigate the philosophy of a recursive soft sequential estimation acquisition scheme, namely the DRSSE acquisition scheme.

III. Differential Recursive Soft Sequential Estimation Acquisition

The motivation of employing a chip-based differential preprocessing operation is two-fold. Firstly, prior to despreading the signal-to-noise ratio (SNR) is usually insufficiently high for attaining a satisfactory performance with the aid of coherent carrier phase estimators based on carrier-phase tracking loops. By contrast, the chip-based differential operation is capable of reducing the effects of the time-varying phase fluctuations imposed by fading and frequency offset. Consequently, chip-based differential preprocessing is capable of significantly enhancing the performance of the following sequential estimation process. Second, from the shift-and-add property of m-sequences [13], the product of the spreading waveform and its chip-time delayed phase yields another phase. This indicates that the differential processing of an m-sequence preserves the characteristics of the m-sequences. Specifically, this property can be demonstrated as follows.

The recursive equation of the m-sequence generator using the generator polynomial of (1) is given by (2). We multiply both sides of (2) by c_{i-1} and, upon substituting c_{i-1} at the right-hand ,side by $c_{i-1} = \prod_{n=1}^{M} c_{i-1-s_n}$, we obtain

$$\begin{aligned} c_i \cdot c_{i-1} &= \prod_{m=1}^{M} c_{i-s_m} \cdot \prod_{n=1}^{M} c_{i-1-s_n} \\ &= \prod_{m=1}^{M} \left(c_{i-s_m} \cdot c_{i-1-s_m} \right), \qquad \text{for } i = \ldots, -1, 0, 1, \ldots. \end{aligned} \tag{3}$$

Let $b_j = c_j \cdot c_{j-1}$ in (3), where j is an integer. Then (3) can be expressed as

$$b_i = \prod_{m=1}^{M} b_{i-s_m}, \qquad i = \ldots, -1, 0, 1, \ldots. \tag{4}$$

Explicitely, both recursive equations, namely (2) and (4), describe the same m-sequence generator. The m-sequence generated by (4) represents a specifically delayed or phase-shifted version of the m-sequence generated by (2). Consequently, once the m-sequence of (4) has been acquired, the acquisition of the m-sequence generated by (2) can also be achieved. The objective of the DRSSE is to achieve the acquisition of the m-sequence generated by (4) using the proposed soft recursive sequential estimation scheme.

A. Description of the DRSSE Scheme

The schematic diagram of the proposed DRSSE acquisition arrangement is shown in Fig. 3, which includes five fundamental building blocks, namely a chip-based differential processor, an m-sequence generator, a soft-chip register, a SISO decoder, and a code phase-tracking loop. The chip-based differential processor excutes differential processings at the chip level, which requires that the carrier phases between two adjacent chips remain similar. Hence, the DRSSE acquisition scheme is suitable for communicating over fading channels exhibiting a high fading rate. The soft-chip register of Fig. 3 has the same S number of delay units—which we refer to as soft-chip delay units (SCDUs)—as the m-sequence generator. The SCDUs store the instantaneous log-likelihood ratio (LLR) values of S consecutive chips of the m-sequence in the form of (4). With the aid of these S number of LLR values, S number of consecutive chips can be determined, which are loaded into the corresponding delay units of the m-sequence generator of Fig. 3. The SISO decoder estimates the corresponding LLR soft output after receiving a soft output sample from the differential processor associated with a given chip of the m-sequence of (4). In addition to the so-called *intrinsic* information of this chip, which characterizes its reliability at the output of the channel, we also exploit the so-called *a priori* (*extrinsic*) information related to the chip considered. This *extrinsic* information is provided by the previously decoded LLR values stored in the SCDUs of Fig. 3. The soft output of the SISO decoder is then shifted to the left-most position of the SCDUs in the soft-chip register, while the soft value in the right-most position of the SCDUs is shifted out and discarded. Note that both the m-sequence generator and the soft-chip register use the same feedback branches. However, in the m-sequence generator, the feedback elements are duo-binary values and the product of these feedback elements is used for generating a binary feedback quantity. By contrast, the feedback elements of the soft-chip register feeding information back to the input of the SISO decoder consists of the LLR values. Hence, the specific operations must be carried out in the soft-value domain for the sake of providing *extrinsic* information for the SISO decoding.

B. DRSSE Acquisition Algorithm

As shown in Fig. 3, the SISO decoder requires both *intrinsic* information conveyed to the input of the SISO decoder by the differential processor and *extrinsic* information provided by the previous estimates of the SISO decoder, in order to generate the soft output required for updating the contents of the soft-chip-register. Let us now consider these sources of information. Let $Z_i = \alpha_i e^{j\phi_i} c_i + n_i$ represent the received channel output sample corresponding to chip c_i, where $i = 0, 1, 2, \ldots$. The parameter α_i denotes the fading amplitude, while ϕ_i represents the phase shift due to carrier modulation and channel fading. Note that when communicating over AWGN channels, the term α_i is set to one. Furthermore, n_i denotes the complex AWGN having zero mean and a normalized variance of N_0/E_c, where N_0 represents the single-sided power spectral density of the AWGN, E_c represents the transmitted chip energy, and E_c/N_0 represents the SNR per chip. Assuming that the channel-induced

fading and phase rotation remain constant over two adjacent chip time durations, i.e., that we have $\alpha_i = \alpha_{i-1}$ and $\phi_i = \phi_{i-1}$, the differential processor's output can be expressed as

$$\begin{aligned} U_i &= \mathrm{Re}\left(Z_i \cdot Z_{i-1}^*\right) \\ &= \alpha_i^2 c_i \cdot c_{i-1} \\ &\quad + \mathrm{Re}\left(\alpha_i e^{j\phi_i} c_i n_{i-1}^* + \alpha_i e^{-j\phi_i} c_{i-1} n_i + n_i n_{i-1}^*\right) \end{aligned} \quad (5)$$

where * represents the complex conjugate operation. Using $b_i = c_i \cdot c_{i-1}$ and without changing their statistical properties, absorbing the terms of $e^{j\phi_i} c_i$ and $e^{-j\phi_i} c_{i-1}$ into the Gaussian noise components n_{i-1}^* and n_i, the above equation can be written as

$$U_i = \alpha_i^2 b_i + \alpha_i \cdot \mathrm{Re}\left(n_{i-1}^* + n_i\right) + \mathrm{Re}\left(n_i n_{i-1}^*\right). \quad (6)$$

It was shown in [14] that, at the SNRs of practical interest, the term $n_i n_{i-1}^*$ is small relative to the dominant noise term of $\alpha_i(n_{i-1}^* + n_i)$. Consequently, if we neglect the term $n_i n_{i-1}^*$, then U_i can be described as a Gaussian variable having mean given by $\alpha_i^2 b_i$ and variance given by $\Omega N_0/E_c$, where $\Omega = \overline{\alpha_i^2}$ represents the ensemble average of α_i^2. Hence, the probability density function (pdf) of U_i can be approximated as

$$p_{U_i}(y|b_i) \approx \frac{1}{\sqrt{\frac{2\pi\Omega N_0}{E_c}}} \exp\left(-\frac{E_c}{2\Omega N_0}\left(y - \alpha_i^2 b_i\right)^2\right). \quad (7)$$

The *intrinsic* information is derived from the LLR of b_i conditioned on the channel-related variable U_i, which can be expressed as

$$\begin{aligned} L(b_i|U_i) &= \log\left[\frac{p_{U_i}(b_i = +1|y = U_i)}{p_{U_i}(b_i = -1|y = U_i)}\right] \\ &= \log\left[\frac{p_{U_i}(y = U_i|b_i = +1)}{p_{U_i}(y = U_i|b_i = -1)} \cdot \frac{P(b_i = +1)}{P(b_i = -1)}\right]. \end{aligned} \quad (8)$$

Upon substituting $p_{U_i}(y = U_i|b_i)$ of (7) associated with $b_i = +1$ and $b_i = -1$ into (8), we obtain

$$\begin{aligned} L(b_i|U_i) &= \log\left[\frac{\exp\left(-\frac{E_c}{2\Omega N_0}\left(U_i - \alpha_i^2\right)^2\right)}{\exp\left(-\frac{E_c}{2\Omega N_0}\left(U_i + \alpha_i^2\right)^2\right)}\right] \\ &\quad + \log\left[\frac{P(b_i = +1)}{P(b_i = -1)}\right] \\ &= L_c \cdot U_i + L(b_i), \quad i = 0, 1, 2, \ldots \end{aligned} \quad (9)$$

where we have $L_c = 2\alpha_i^2 E_c/\Omega N_0$, which is referred to as the reliability value of the channel, while $L(b_i)$ is the LLR of a random variable b_i, which is defined as [11] $L(b_i) = \log(P(b_i = +1)/P(b_i = -1))$. Furthermore, we set $L(b_i) = 0$, if we have no *a priori* information related to b_i, which corresponds to assuming a chip value of $+1$ or -1 with equal probability, i.e., if we have $P(b_i = +1) = P(b_i = -1)$.

Note that at the initial synchronization stage the estimation of the channel parameters might be unreliable. If we have no prior knowledge concerning the channel parameters, we can simply set $L_c = 2E_c/N_0$. However, our simulation results in Section IV will show that the acquisition performance degrades in the absence of perfect knowledge of the channel. Furthermore, for transmission over AWGN channels, the reliability value of the channel is set to $L_c = 2E_c/N_0$.

In the context of the *extrinsic* information, as in Section II, we assume that in Fig. 3 the generator coefficients are given by $g_{s_1} = g_{s_2} = \ldots = g_{s_l} = \ldots = g_{s_{M=S}} = 1$, while the other coefficients are 0's, i.e., the m-sequence generator obeys the recursive equation (2) or (4). Consequently, the previous soft outputs of the SISO decoder of Fig. 3 obtained at the time instants of $(i-s_1), (i-s_2), \ldots, (i-(s_M = S))$ are fed back to the input of the SISO decoder, in order to provide *extrinsic* information for enhancing the correct decoding probability of chip b_i. Let the previous S number of soft outputs of the SISO decoder be $L(y_{i-1}), L(y_{i-2}), \ldots, L(y_{i-S})$. According to (2), the *extrinsic* information used for enhancing the correct decoding probability of b_i can be approximately expressed as [11, eq. (12)]

$$\begin{aligned} L_e(b_i) \approx &\left[\prod_{m=1}^{M} \mathrm{sign}\left(L\left(y_{i-s_m}\right)\right)\right] \cdot \min\left\{\left|L\left(y_{i-s_1}\right)\right|, \right. \\ &\left.\left|L\left(y_{i-s_2}\right)\right|, \ldots, \left|L\left(y_{i-(s_M=S)}\right)\right|\right\}, \quad i = 0, 1, 2, \ldots, \end{aligned} \quad (10)$$

where we assumed that we have $L_e(y_{-\infty}) = \ldots = L_e(y_{-2}) = L_e(y_{-1}) = 0$. Note that, although the *extrinsic* information of (10) or that of [11, eq. (12)] has been derived based on the assumption that $y_{i-s_1}, y_{i-s_2}, \ldots, y_{i-(s_M=S)}$ are independent random variables, nonetheless, this approximate formula can be used regardless of whether the variables $y_{i-s_1}, y_{i-s_2}, \ldots, y_{i-(s_M=S)}$ are independent or correlated. More specifically, concerning the derivations carried out in [11], without exploiting the independence of the variables, we are unable to arrive at [11, eqs. (10) and (11)]. By contrast, the approximate formula of [11, eq. (12)] can be used for both independent and correlated variables. The above argument becomes more explicit with the aid of the following observations. First, the square-bracketed first part of (10), which constitutes the polarity of $L_e(b_i)$, is determined by the recursive equation (or parity-checking equation) of (4). Second, once we have obtained the reliabilities of the variables $y_{i-s_1}, y_{i-s_2}, \ldots, y_{i-(s_M=S)}$, regardless of whether they are independent or not, the reliability of b_i based on the parity-checking equation (4) should not be lower than the minimum reliability associated with the set of variables $y_{i-s_1}, y_{i-s_2}, \ldots, y_{i-(s_M=S)}$.

Finally, with the aid of the *intrinsic* information $L_c \cdot U_i + L(b_i)$ of (9) and the *extrinsic* information $L_e(b_i)$ of (10), the soft output of the SISO decoder associated with chip b_i can be expressed as

$$\begin{aligned} L(y_i) &= L(b_i|U_i) + L_e(b_i) \\ &\approx L_c \cdot U_i + L(b_i) + \left[\prod_{m=1}^{M} \mathrm{sign}\left(L\left(y_{i-s_m}\right)\right)\right] \\ &\quad \cdot \min\left\{\left|L\left(y_{i-s_1}\right)\right|, \left|L\left(y_{i-s_2}\right)\right|, \ldots, \right. \\ &\qquad \left.\left|L\left(y_{i-(s_M=S)}\right)\right|\right\}, \quad i = 0, 1, 2, \ldots \end{aligned} \quad (11)$$

where, again, we assumed that we have $L_e(y_{-\infty}) = \ldots = L_e(y_{-2}) = L_e(y_{-1}) = 0$. Equation (11) represents a recursive equation that can be used for estimating the S number of

consecutive chips required by the receiver's m-sequence generator for producing the full m-sequence of (4). Provided that the channel's output SNR per-chip value of E_c/N_0 is sufficiently high, the LLR values of the S consecutive chips will increase upon increasing the depth of this recursion. In other words, the reliabilities associated with the S consecutive chips increase, while the erroneous loading probability of the m-sequence generator—which is defined as the probability of the event that the m-sequence generator is loaded with one or more erroneous chips—decreases upon increasing the number of recursions or iterations. Therefore, the acquisition device is capable of observing the reliabilities of the S consecutive chips through observing the amplitudes of the LLR values stored in the SCDUs. If the amplitudes of the LLR values in the SCDUs become sufficiently high after a number of update operations using (11) and they result in a sufficiently low erroneous loading probability, then, as shown in Fig. 3, a "loading command" can be activated for loading the corresponding hard-decision-based binary $+1$ or -1 chip values into the delay-units of the m-sequence generator according to the signs of the corresponding LLR values stored in the SCDUs.

We have noted in the context of (10) that the *extrinsic* information of $L_e(b_i)$ can be derived from (10) without taking into account the correlations among the variables $y_{i-s_1}, y_{i-s_2}, \ldots, y_{i-(s_M=S)}$. Here, we note furthermore that, when we increase the depth of the recursion, the adjacent variables, such as $y_i, y_{i+1}, y_{i+2}, \ldots$, will become more and more correlated, and hence they exhibit a similar reliability. However, as a consequence of the correlation among the adjacent variables, the statistical analysis of the proposed acquisition scheme, which would provide a formula for the erroneous loading probability, for example, is impractical. Therefore, in this contribution, all of the results obtained in Section IV are based on simulations.

The operation of the DRSSE acquisition scheme can be summarized in the following steps.

1) All of the SCDUs are initialized to zero. The delay unit in the differential processor is initialized to one.
2) Whenever the SISO decoder receives a sample U_i corresponding to the chip b_i from the differential processor, the SISO decoder computes the LLR of b_i conditioned on U_i using (9) and computes the *extrinsic* information of $L_e(b_i)$ using (10). Finally, the soft output $L(y_i)$ of the SISO decoder, which is related to chip b_i, is computed according to (11).
3) The soft output $L(y_i)$ is then shifted into the left-most SCDU of Fig. 3 after all of the other soft outputs $L(y_{i-1})$, $L(y_{i-2})$, and $L(y_{i-S+1})$ have been shifted to the right by one position, while $L(y_{i-S})$ is removed from the soft-chip register. In other words, the soft-chip register always stores the most recent S number of soft outputs of the SISO decoder, which correspond to S consecutive chips of the m-sequence at the output of the differential processor.
4) Following a number of recursions according to (11), when the amplitudes of the most recent S number of soft outputs of the SISO decoder become sufficiently high for guaranteeing a sufficiently low erroneous loading probability, a "loading command" is activated by the SISO decoder. Then, S consecutive chips are determined using hard decisions based on the most recent S LLR values stored in the soft-chip register of Fig. 3. Next, the S consecutive binary chips are loaded into the corresponding delay units of the local m-sequence generator.
5) Once the m-sequence generator is loaded with the initial binary chip values, the received differentially processed spread-spectrum signal can be despread using the locally generated m-sequence replica, provided that the initial chip values of the m-sequence generator have been correctly loaded. The despread signal is then low-pass-filtered and forwarded to the code tracking loop. If the code tracking loop is capable of tracking the phase, the code acquisition process is completed. However, if the tracking loop is incapable of tracking the phase, the code tracking loop activates a "reloading command," in order to load another group of S consecutive chips into the delay units of the m-sequence generator. The above process can be repeated until successful code tracking is accomplished.

Finally, for the family of spread-spectrum communication systems using coherent demodulation, we have to derive the S number of consecutive chips of the originally transmitted m-sequence, in order to generate a local m-sequence replica for directly despreading the transmitted m-sequence, instead of despreading the differentially processed m-sequence. These S number of consecutive chips of the originally transmitted m-sequence, namely $\{c_i\}$, can be determined using the relationship between the m-sequences $\{c_i\}$ and $\{b_i\}$. Below we specify three methods for achieving this objective.

1) Since each specific delay in the m-sequence of $\{c_i\}$ corresponds to a specific delay of the m-sequence $\{b_i\}$, we can design a look-up table of size $(2^S-1)\times 2S$, where each row contains S consecutive chips of $\{b_i\}$ and the corresponding S consecutive chips of $\{c_i\}$. Once the S consecutive chips of $\{b_i\}$ have been obtained, the S number of consecutive chips of $\{c_i\}$ can be obtained by referring to this table. However, since this table has a dimension of $(2^S-1)\times 2S$, it may becomes impractical to use this method, if S is large.
2) The second method is based on the recursive equation (4) and the differential processing operation of $b_j = c_j \cdot c_{j-1}$. Let $b_G, b_{G+1}, \ldots, b_{G+S-1}$ be the S number of consecutive chips of $\{b_i\}$. From (4) we obtain

$$b_j = b_{j+S} \cdot \prod_{m=1}^{M-1} b_{j+S-s_m}, \quad j = G-1, G-2, \ldots, 0. \quad (12)$$

With the aid of (12), we can generate all of the chip values of $b_0, b_1, \ldots, b_{G+S-1}$. Then, from $b_j = c_j \cdot c_{j-1}$, we arrive at $c_j = b_j \cdot c_{j-1}$. Furthermore, we assumed that the delay unit in the differential processor was initialized to one, i.e., we have $c_0 = 1$. Explicitly, based on these quantities, S number of consecutive chips $c_G, c_{G+1}, \ldots, c_{G+S-1}$ associated with the originally transmitted m-sequence can be obtained by solving the recursive equation $c_j = b_j \cdot c_{j-1}$ for

$j = 1, 2, \ldots, G + S - 1$. Note that the complexity of this scheme is linearly dependent on the SISO recursive decoding depth. Hence, this procedure is efficient, provided that the SISO recursive decoding depth is sufficiently low.

3) The third proposed scheme is independent of both the length $(2^S - 1)$ of the m-sequence and of the SISO recursive decoding depth. It has a complexity, which is linearly dependent on the number of stages, S, in the soft-chip register. However, in order to determine the S number of consecutive chips, say $c_G, c_{G+1}, \ldots, c_{G+S-1}$, this scheme requires a further stage of decision. More explicitly, let $b_G = c_G c_{G-1}, b_{G+1} = c_{G+1} c_G, \ldots, b_{G+S-1} = c_{G+S-1} c_{G+S-2}$ be the S number of consecutive chips of $\{b_i\}$, which have been reliably determined. By setting $c_{G-1} = +1$ or $c_{G-1} = -1$, we obtain two different S-chip sequences, which are expressed as $\{c_G, c_{G+1}, \ldots, c_{G+S-1}\}_{c_{G-1}=+1}$ and $\{c_G, c_{G+1}, \ldots, c_{G+S-1}\}_{c_{G-1}=-1}$. It can be readily shown that these two S-chip sequences have a Hamming distance of S. However, only one of them is the desirable one, which can be further determined using the following approach. By loading them into two local m-sequence generators, two despread PN sequences having different phases can be generated, although only one of them has the same phase as the originally transmitted m-sequence. Consequently, by correlating the received m-sequence with both of the above-mentioned locally generated PN sequence replicas, we can select the specific S number of consecutive chips corresponding to the higher correlation output as the desirable initial chips. This is because the correlator using the desirable S consecutive chips has higher correlation outputs associated with a significantly higher probability than that using the undesirable S consecutive chips.

C. Acquisition Time and Complexity

According to our analysis in Section III-B, the DRSSE acquisition scheme is capable of observing the reliabilities of the most recent S consecutive chips through observing the amplitudes of the corresponding soft outputs stored in the soft-chip-register of Fig. 3. The DRSSE acquisition scheme then decides as to when it should activate the "loading command" for loading the initial chips into the m-sequence generator. When the erroneous loading probability is deemed sufficiently low, i.e., it is in the region of for example 10^{-4}, successful PN-sequence acquisition can typically be declared with a high probability right after the first loading of the initial chips. Therefore, the total acquisition time of the DRSSE acquisition scheme can be approximated by the time duration required by the DRSSE for carrying out the recursive SISO decoding, in order to reach a sufficiently low erroneous loading probability. According to the iterative decoding principle [10], [11] and to our results to be presented in Section IV, it can be shown that, for a reasonable SNR per-chip value, the time duration required by the DRSSE for carrying out recursive SISO decoding is linearly dependent on the number of stages, S, in the related m-sequence generator.

As shown in Fig. 3, the implementation of the proposed DRSSE acquisition scheme requires a soft-chip register having the same length S, as the m-sequence generator, plus a simple differential processor and a low-complexity SISO decoder. The complexity of the DRSSE acquisition scheme is dominated by that of the soft-chip register, which is linearly dependent on the number of stages, S, in the soft-chip register. Therefore, due to the fact that both the complexity and the acquisition time are linearly dependent on the number of stages S in the m-sequence generator, the proposed DRSSE acquisition scheme is particularly attractive for the acquisition of long m-sequences.

IV. Performance Results

In this section, we provide a range of simulation results for characterizing the proposed DRSSE acquisition scheme. Our simulation results were mainly based on the acquisition of two different-length m-sequences having $S = 5$ and $S = 13$ stages, which correspond to having PN-sequence periods of $N = 2^5 - 1 = 31$ and $N = 2^{13} - 1 = 8191$, respectively. The generator polynomial associated with $S = 5$ and $N = 31$ was $g(D) = 1 + D^2 + D^5$, while that associated with $S = 13$ and $N = 8191$ was $g(D) = 1 + D + D^3 + D^4 + D^{13}$. Note that the curves were drawn either versus the SNR per chip, namely E_c/N_0, or versus the normalized number of chips received, which also represents the normalized number of chips that the SISO decoder processed. The normalized number of chips L/S was defined as the total number of received chips L divided by the number of generator stages S of the corresponding m-sequence generator.

When considering fading channels, in our simulations, flat Rayleigh fading channels were assumed where the channel magnitude remained constant over a set of S consecutive chips associated with a generator's shift-register-based stage length, while the fading of the different sets of S chips was assumed to be independent. For the proposed DRSSE acquisition scheme, the above assumptions are indeed practical for a wide range of flat Rayleigh fading channels having various fading rates, since chip-level differential operation was used. In contrast to the bit rate or the frame rate, the chip rate of the spreading sequences is on the order of Mega-chips per second, which is typically higher than the fading rate, even when fast-fading channels having a Doppler frequency of hundreds of Hertz are considered. Hence, the fading amplitudes and phases associated with two adjacent chips invoked in a differential operation can be assumed to be identical.

In Fig. 4, we show the erroneous loading probability P_e versus the SNR per-chip E_c/N_0 performance for an m-sequence generated using the generator polynomial of $g(D) = 1 + D^2 + D^5$ and transmitted over AWGN channels. Note that in Fig. 4 the curve corresponding to the parameter of $L = 1 \times S$ represents the erroneous loading probability of the DRSSE acquisition scheme using no recursive SISO decoding. From the results, we can see that, when more channel output chips are involved in the recursive SISO decoding process, a higher correct detection reliability and hence a lower erroneous loading probability can be achieved. For the sake of illustration, let us assume that the transmitted m-sequence can be reliably acquired, once the erroneous loading probability is lower than 10^{-4}. Then, from the results of Fig. 4 we can

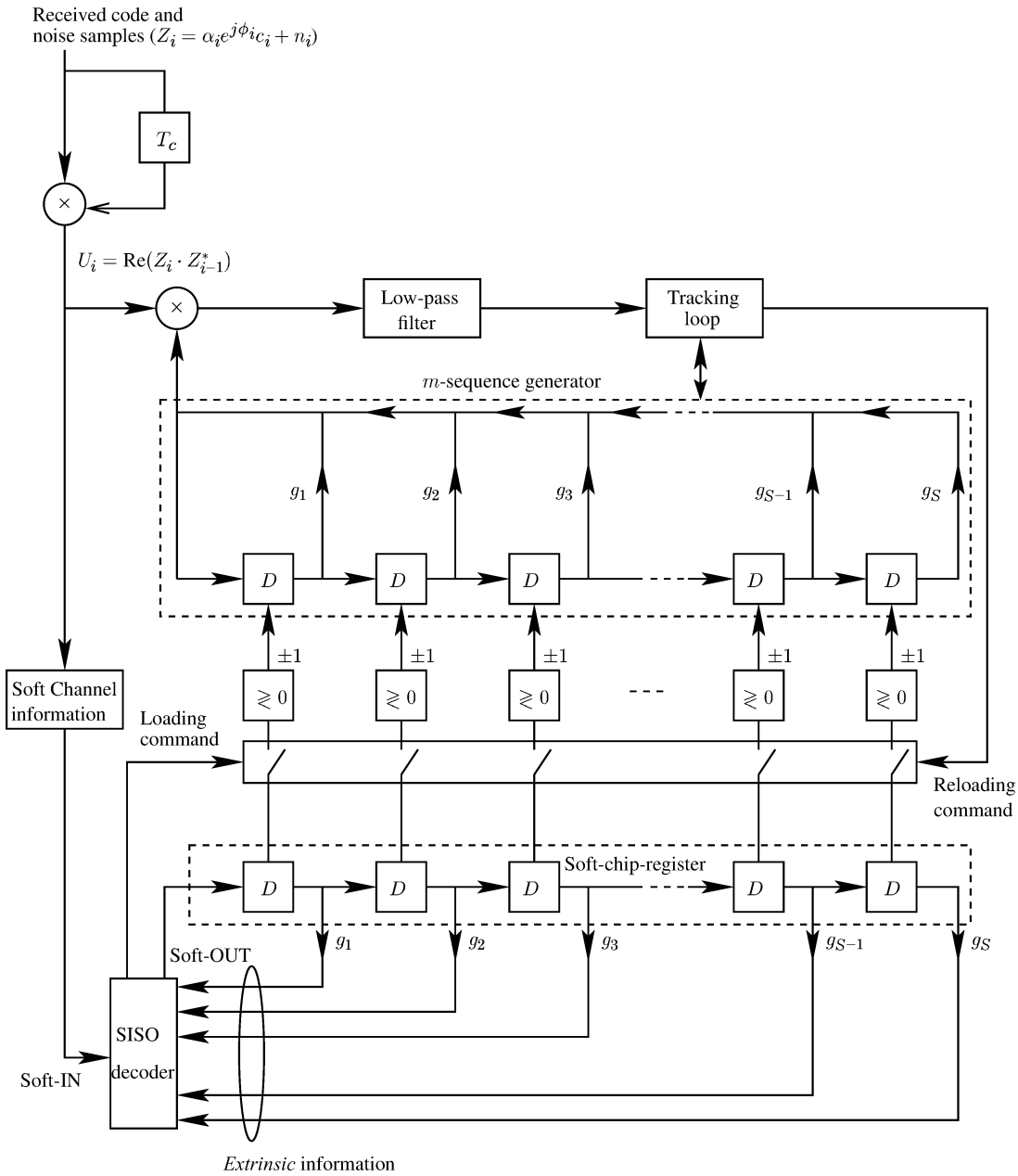

Fig. 3. Schematic diagram of the proposed DRSSE.

observe that the m-sequence can be reliably acquired at an SNR per-chip value of $E_c/N_0 = 0$ dB by invoking about $L = 40 \times S = 40 \times 5 = 200$ chips into the recursive SISO decoding scheme. By contrast, without exploiting the power of recursive SISO decoding, the DRSSE acquisition scheme has to operate at an SNR per-chip value of $E_c/N_0 = 9.5$ dB, in order to achieve the same erroneous loading probability of 10^{-4}. Explicitly, at the erroneous loading probability of 10^{-4}, the SNR per chip gain is about 9.5 dB, when $L = 200$ chips are invoked by the recursive SISO decoding scheme. In general, it is expected that, when more chips can be used during the recursive SISO decoding process, an increasing gain can be achieved by the proposed DRSSE acquisition scheme. For example, when invoking $L = 200 \times S$ instead of $L = 40 \times S$ chips into the recursive SISO decoder, another 1.7-dB SNR per-chip gain can be achieved at the erroneous loading probability of 10^{-4}.

Fig. 5 shows the acquisition performance for an m-sequence having a period of $N = 8191$ chips, which was generated by a thirteen-stage $(S = 13)$ generator using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$. As shown in Fig. 5, the m-sequence can be reliably acquired at an SNR per-chip value of $E_c/N_0 = 1.7$ dB by invoking about $L = 40 \times S = 40 \times 13 = 520$ chips by the recursive SISO decoder. This m-sequence can also be reliably acquired at a reduced SNR per-chip value of $E_c/N_0 = 1$ dB by invoking about $L = 200 \times S = 200 \times 13 = 2600$ chips in the recursive SISO decoder. By contrast, without the recursive SISO decoding, the PN code acquisition scheme has to operate at the SNR per chip value of $E_c/N_0 = 10$ dB, in order to achieve the erroneous loading probability of 10^{-4}. Hence, the SNR per-chip gain at the erroneous loading probability of 10^{-4} is about 8.3 or 9 dB, respectively, when $L = 520$ or $L = 2600$ chips are invoked by the re-

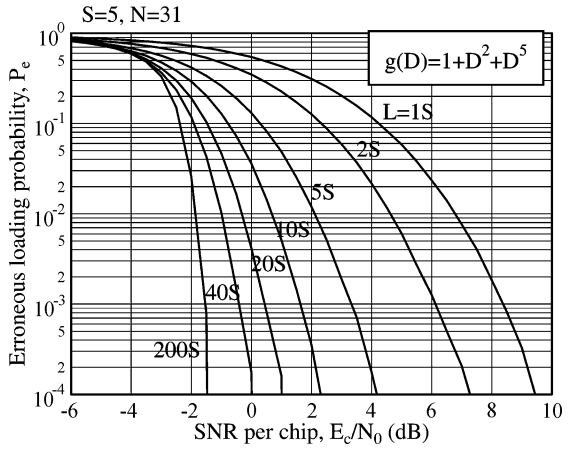

Fig. 4. Erroneous loading probability P_e versus the SNR/chip E_c/N_0 performance for various numbers of chips invoked by the proposed recursive SISO decoder, when transmitting the m-sequence generated using the generator polynomial of $g(D) = 1 + D^2 + D^5$ over AWGN channels.

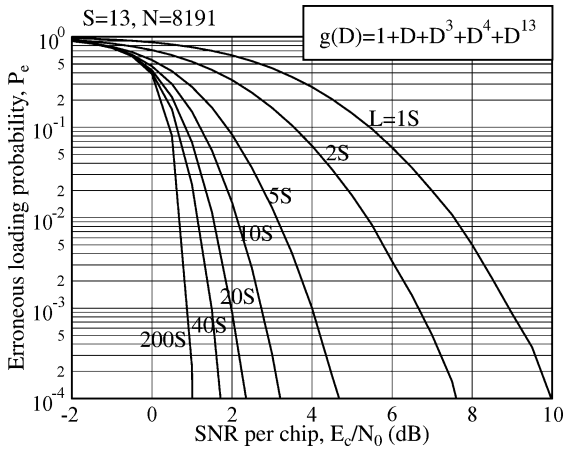

Fig. 5. Erroneous loading probability P_e versus the SNR/chip E_c/N_0 performance for various numbers of chips invoked by the proposed recursive SISO decoder when transmitting the m-sequence generated using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$ over AWGN channels.

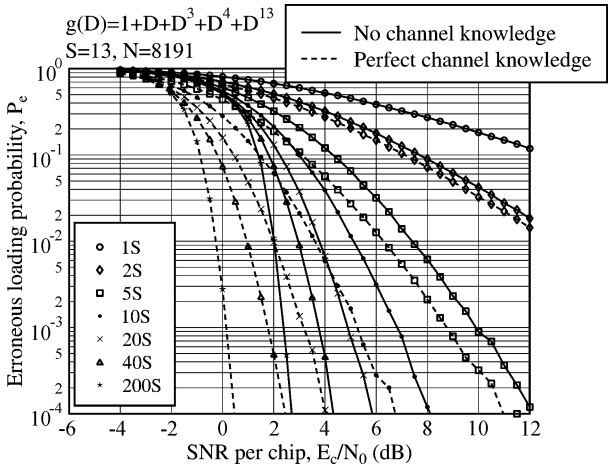

Fig. 6. Erroneous loading probability P_e versus the SNR/chip E_c/N_0 performance for various numbers of chips invoked by the proposed recursive SISO decoder when transmitting the m-sequence generated using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$ over Rayleigh fading channels.

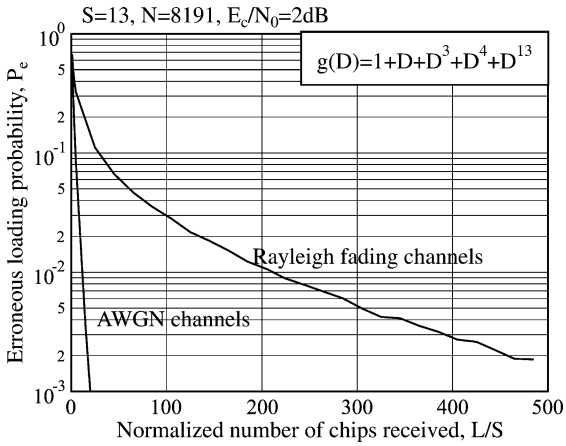

Fig. 7. Erroneous loading probability P_e versus the normalized number of received chips invoked by the proposed recursive SISO decoder for an m-sequence having a period of 8191 when communicating over AWGN or Rayleigh fading channels and using an SNR per chip value of $E_c/N_0 = 2$ dB for $S = 13$.

cursive SISO decoder. Note that, even though $L = 2600$ chips are invoked by the recursive SISO decoder for achieving reliable acquisition at the SNR per chip value of $E_c/N_0 = 1$ dB, the acquisition time of $L = 2600$ chips durations is still significantly lower than that of any conventional serial search acquisition schemes [4], [15], which demand a mean acquisition time on the order of the period of the m-sequences considered, i.e., 8191 chips in this example.

The results portrayed in the above figures were evaluated when communicating over AWGN channels. In Fig. 6, we investigated the acquisition performance of the DRSSE acquisition scheme for transmission over Rayleigh fading channels. As we analyzed in Section III, when communicating over fading channels, depending on whether the recursive SISO decoder employs perfect knowledge or no knowledge of the fading channel, the term L_c in the *intrinsic* information of (9) can be set to $L_c = 2\alpha_i^2 E_c/\Omega N_0$ or to $L_c = 2E_c/N_0$. In Fig. 6, we also compared the acquisition performance recorded in the context of these two cases. In Fig. 6, the m-sequence was generated by a thirteen-stage m-sequence generator using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$. From the results of Fig. 6, we observe that the acquisition performance improves in both cases when increasing the number of received chips invoked by the recursive SISO decoder. However, compared to the acquisition performance using no recursive SISO decoding (the curve marked with circles), for a given number of received chips, the recursive SISO decoder using perfect channel knowledge provides a higher SNR per chip gain than that attained without using any channel knowledge. This observation can be explained with the aid of (11). When perfect knowledge of the channel is employed, (11), in fact, is processed based on the "maximal-ratio combining" (MRC) principle. By contrast, without the knowledge of the channel, (11) is processed based on the "equal-gain combining" (EGC) principle. It is well known that the MRC scheme outperforms the EGC scheme in multipath fading channels.

Finally, in Fig. 7, we show the erroneous loading probability performance versus the normalized number of received chips used by the recursive SISO decoder for an m-sequence generated by an $S = 13$-stage m-sequence generator and hence

having a period of 8191 chips. The results were generated for transmissions over both AWGN and Rayleigh fading channels at the SNR per chip value of $E_c/N_0 = 2$ dB. According to the results of Fig. 7, it can be shown that for AWGN channels the DRSSE acquisition scheme is capable of achieving an erroneous loading probability of 10^{-3} after receiving approximately $20 \times 13 = 260$ chips. By contrast, when communicating over Rayleigh fading channels, the DRSSE acquisition scheme is capable of reaching the erroneous loading probability of 10^{-3} after receiving approximately $500 \times 13 = 6500$ chips. These results imply that with the aid of the proposed recursive SISO decoder the required target performance can be achieved, regardless of the specific communication environment encountered by invoking a sufficiently high number of chips in the SISO decoder. The results of Fig. 7 indicate that successful acquisition can be achieved by the proposed DRSSE acquisition scheme, when communicating over Rayleigh fading channels at $E_c/N_0 = 2$ dB within about 6500 chip durations, which is lower than the 8191-chip period of the transmitted m-sequence.

V. Conclusion

In summary, in this paper, the acquisition of m-sequences using the proposed differential soft-decision based sequential estimation scheme has been investigated. We have highlighted the principle of differential acquisition of m-sequences. Using the principles of iterative SISO decoding, we have proposed a differential recursive soft sequential estimation acquisition scheme. The acquisition performance of the DRSSE acquisition scheme has been investigated. It has been demonstrated that the DRSSE acquisition scheme has both an implementational complexity and an initial synchronization time, which are linearly dependent on the number of stages in the m-sequence generator. Furthermore, the DRSSE acquisition scheme is suitable for m-sequence acquisition, when communicating over various environments including AWGN, slow fading and fast fading channels. This is because that the differential processing employed is carried out at the chip-level of the m-sequence. Owing to these attractive characteristics, the DRSSE acquisition scheme constitutes a promising initial synchronization scheme for acquisition of long m-sequences, when communicating over various propagation environments.

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