Gate capacitance of deep submicron MOSFETs with high-K gate dielectrics

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Abstract - We study gate capacitance of deep sub-micron MOSFETs with high-K gate dielectrics. Schrödinger's equation is solved by applying an open boundary condition at silicon-gate dielectric interface. Self-consistent numerical results reveal that accounting for wave function penetration into the gate dielectric causes the carrier distribution to be shifted closer to the gate dielectric. This effect increases with increasing gate voltage and also increases with the decreasing conduction band offset of the gate dielectric material with silicon. Gate capacitance calculated from conventional modeling is found to be independent of dielectric materials for a given equivalent oxide thickness (EOT). But our study shows that when wave function penetration into the gate dielectric is considered, gate capacitance for a given EOT increases with a decrease in the conduction band offset. Effects of substrate doping density on gate capacitance are found to be negligible when wave function penetration effects are incorporated.

1 Introduction

Due to scaling down of MOSFET gate dielectric equivalent oxide thickness (EOT) to sub-2 nm regime, the direct tunneling (DT) of inversion carriers has become significant. Some penetration of the wave function into the gate-dielectric is expected in such devices. Modeling of gate capacitance of these MOS structures, so far reported in the literature, has neglected wave function penetration into the gate dielectric layer to avoid the computational involvement associated with the common solution techniques of Schrödinger's equation with open boundary conditions [1]-[2]. A comparison between modeled gate-capacitance with and without considering wave function penetration into the gate dielectric has been performed in [3]. But this work does not consider the effect of conduction band offset of the gate dielectric material on gate capacitance. A comprehensive study of the effects of conduction band offset (due to selecting different gate dielectric materials) on gate capacitance is yet to be reported in the literature.

In this paper, we calculate the gate capacitance of deep submicron MOSFETs, where different high-K dielectric materials have been used as gate insulator. Wave function penetratation into the gate dielectric layer has been taken into account in our self-consistent calculation. We also investigate the effects of substrate doping on modeling of gate-capacitance.

2 Theory

We use the logarithmic derivative technique of the retarded Green's function, G^R, to solve one-dimensional (1D) Schrödinger's equation in the direction normal to the silicon-gate-oxide interface (z direction) with open boundary conditions. This method is discussed in details in [4]-[5]. Our boundary conditions are based on the realistic assumption that electrostatic potential is flat at deep inside the gate-electrode as well as deep inside the bulk silicon. In the presence of tunneling, the Hamiltonian for the MOS structure becomes non-Hermitian and the eigenenergies become complex, where the real part gives the energy of the jth quasi-bound state in the ith valley, E_{ij} and the imaginary part is related to the lifetime, t_{ij}. In order to avoid determining complex eigenenergies of the a non-Hermitian matrix, we evaluate the local 1D density-of-states (DOS), N_{1D} at some point within the quantum well from the diagonal element of G^R [4]:

$$N_{1D}(z;E) = -\frac{1}{p}\Im m[G^R(z,z;E)]. \qquad (1)$$

E_{ij}s are calculated by locating the peaks of N_{1D}. Once E_{ij}s are calculated, corresponding wave functions including penetration into the gate dielectric are evaluated in a straight-forward manner [4]. 1D Poisson's equation is solved for the combined metal-oxide-semiconductor regions using the calculated wave functions to describe the inversion charge density. Thus, the effects of wave function penetration on the electrostatic potential within the self-consistent loop are taken into account. After the convergence of the self-consistent loop, the inversion capacitance (C_{inv}) and gate capacitance (C_g) are determined from the fundamental relationships

$$C_{inv} = \frac{q\partial N_{inv}}{\partial f_s} \qquad (2)$$

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$$C_g = \frac{q\partial(N_{inv} + N_{dep})}{\partial V_g} \qquad (3)$$

Here, N_{inv} and N_{dep} are the number of charges per unit area in the inversion region and the depletion region, respectively, f_s is the silicon surface potential and V_g is the gate voltage.

3 Results and Discussions

The results of our numerical calculations for nMOSFETs are presented in this section. Calculations are performed at room temperature and values for different parameters for (100) silicon are taken from [6]. The effective mass of electrons within the gate-oxide region has been assumed to be equal to $0.5rn_0$ with a parabolic dispersion relationship. This study is done for four different gate dielectrics, which are SiO_2, Si_3N_4, Ta_2O_5 and TiO_2. Conduction band offset and dielectric constant of these materials are taken from [7] and are given in Table 1.

Table I: Dielectric constants and conduction band offsets at silicon-dielectric interface for different dielectric materials used in our calculation (from [7]).

Material	Dielectric constant (K)	ΔE_C to silicon (eV)
SiO_2	3.9	3.2
Si_3N_4	7	2
Ta_2O_5	26	1.3
TiO_2	80	1.2

Fig. 1 shows calculated average distance of inversion carriers (Z_{avg}) from silicon/dielectric interface as a function of gate voltage for SiO_2, Si_3N_4, Ta_2O_5 and TiO_2 dielectrics for EOT=1 nm with and without considering wavefunction penetration into the gate dielectric. We see that the Z_{avg} is material independent when penetration is neglected. When penetration effects are included in the calculation, it is found that Z_{avg} depends on the gate dielectric material. It is shifted closer to silicon/dielectric interface with decreasing conduction band offset and increasing dielectric constant.

Fig. 2 shows the dependence of C_{inv} on N_{inv} for different gate dielectrics with three different EOT, as described in the figure both considering and without considering penetration. C_{inv} at a given value of N_{inv} is found to be independent of the oxide thickness and dielectric material if we neglect penetration effect. But when penetration effect is incorporated, C_{inv} is larger and this effect is more prominent for dielectric materials with lower DE_C.

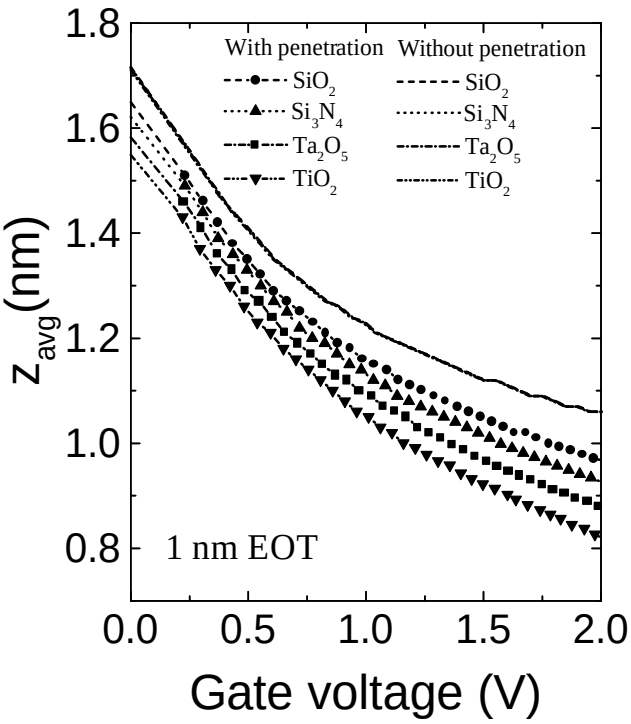

Fig. 1: Z_{avg} variation with gate voltage for different dielectrics of 1 nm EOT both considering and without considering penetration.

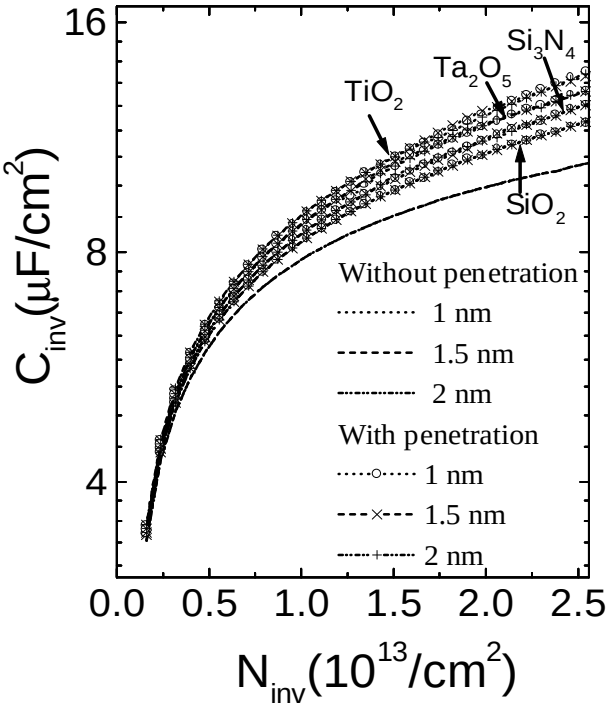

Fig. 2: C_{inv} vs N_{inv} for different gate dielectrics of 1 nm EOT both considering and without considering wave function penetration

Fig. 3 shows gate capacitance as a function of gate voltage for all four gate dielectrics of 1 nm EOT both considering and without considering wave function penetration. When C_g is calculated using conventional closed boundary conditions, for a given EOT, it is independent of gate dielectric material. Fig. 3 shows that due to different DE_C for different dielectrics, wave function penetration effects on C_g are not the same for all the materials. Consequently, the gate capacitance varies from material to material even when the EOT is the same. This is an important observation and it emphasizes the need for incorporating penetration effects in *C-V* calculation, particularly for MOSFETs with high-K dielectric material. We have also calculated C_g vs V_g for different dielectric materials for an EOT of 1.5 nm. The trend is identical with that for 1 nm EOT except for the fact that penetration effects are more pronounced at lower EOT.

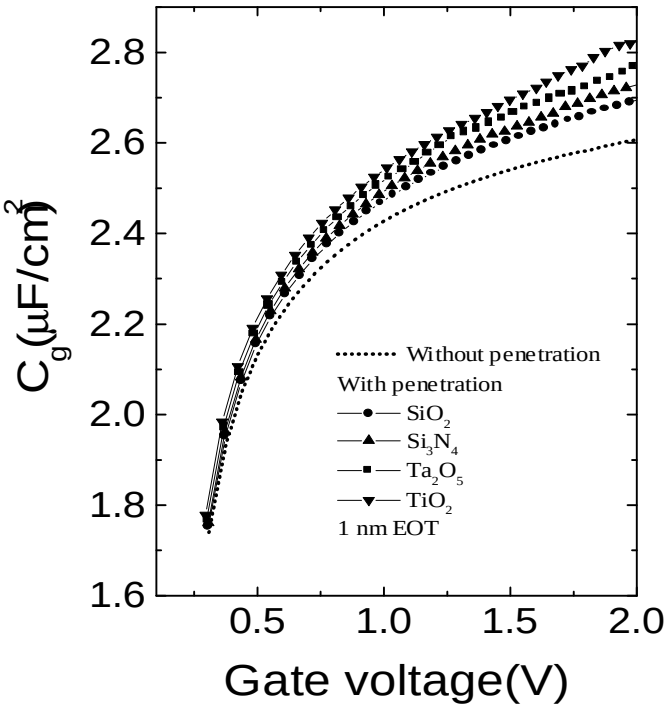

Fig. 3: C_g as a function of gate voltage for different gate dielectrics of 1 nm EOT.

Fig. 4 shows the variation of C_g with voltage for three different substrate doping density N_A for two different gate dielectric materials of 1 nm EOT. In strong inversion region, increase of C_g due to increase in N_A at a given gate voltage is observed when penetration effect is neglected. However, little variation in C_g with N_A is observed beyond threshold when penetration effect is incorporated. This implies that conventional modeling where penetration effect is neglected will predict overestimated increase in C_g due to increase in N_A for a given voltage.

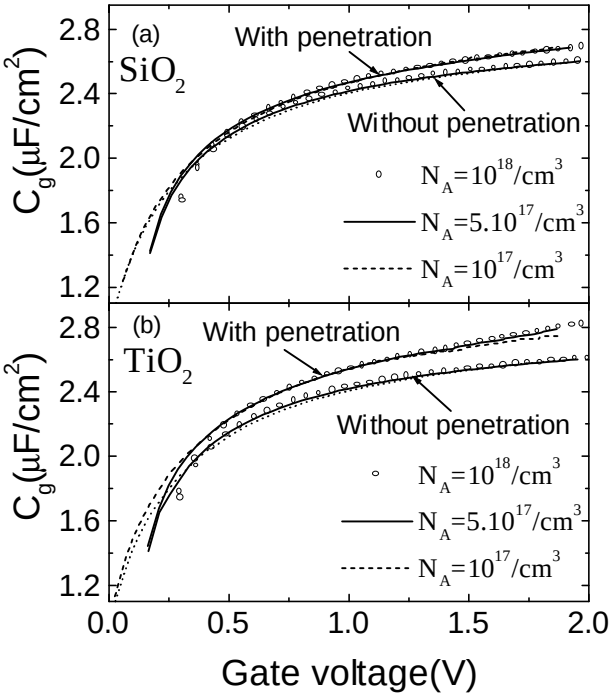

Fig. 4: C_g as a function of gate voltage for different substarte doping density N_A for two different gate dielectric materials of 1 nm EOT.

Relative error in C_g for different gate dielectrics is plotted in Fig. 5 for various substrate doping concentrations for an EOT of 1 nm. We see in this figure that the error is higher at low substrate doping concentration for a given dielectric material and increases with decreasing conduction band offset. In case of Ta_2O_5 and TiO_2, this error is above 5%, which is above the maximum permissible error in gate capacitance simulation as dictated by ITRS roadmap [8]. Therefore, it can be concluded that for accurate modeling of gate capacitance of high-K dielectrics, wave function penetration effect must be considered.

4 Conclusions

Accurate modeling of the gate capacitance of deep sub-micron MOSFETs, with high-K dielectrics used as gate insulator, is presented in this work. It is found that the value of gate capacitance is independent of gate dielectric material for a given EOT from conventional modeling that uses closed boundary conditions for the solution of Schrödinger's equation. However, in the presence of wave function penetration into the gate dielectric, gate capacitance is found to vary from material to material even when the EOT is the same. This emphasizes the need for incorporating penetration effects in gate capacitance modeling, particularly in MOSFETs with high-K gate dielectric materials. Effects of substrate

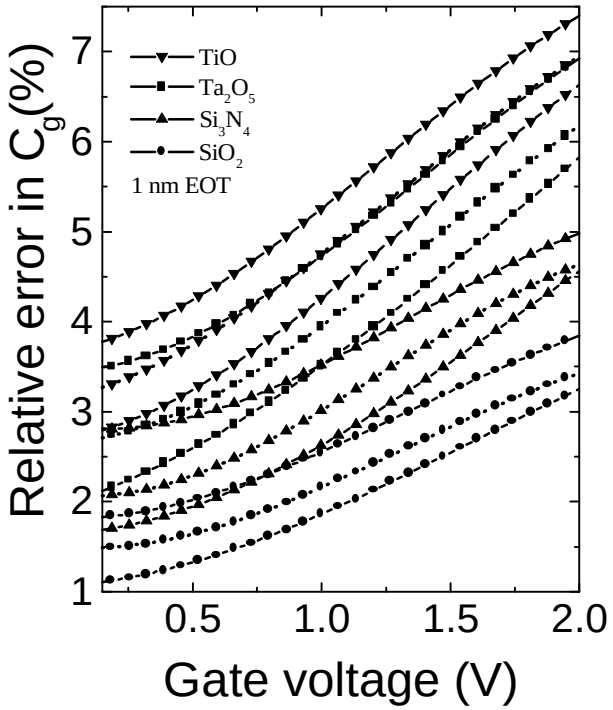

Fig. 5: Relative error in C_g due to neglect of wave penetration effects for different N_A and four different gate dielectrics of 1 nm EOT. For a given material, solid line represents $N_A=10^{17}cm^{-3}$, dotted line represents $N_A=5\times10^{17}cm^{-3}$, and dashed line represents $N_A=10^{18}cm^{-3}$.

doping density on gate capacitance beyond threshold voltage are found to be negligible if penetration effects are incorporated.

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