IC Design and Manufacture for Undergraduates: *Theory, Design and Practice*

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ABSTRACT

In this paper we describe how the practical design and manufacture of modern CMOS integrated circuits (ICs) have been incorporated into the second year of our undergraduate Electronics degree program. While many undergraduate degree programs offer theoretical and design of ICs, none have published a complete design cycle teaching approach including practical manufacture and test of ICs. We demonstrate how the design process has been tightly coupled with theoretical aspects of the degree course and incorporate transferable skills into the design exercise. We will also provide the technical information on how this design exercise can be accomplished sensibly for a large cohort of students (~100) in practical terms.

1. INTRODUCTION

Recent advances in IC CMOS process technology have forced Electronics departments world-wide to adapt their educational programs and the contents thereof in order to equip students with the right skills and knowledge needed by industry [1]. Recent examples of this progress include ASIC design and CAD tools in the mid 80's to programmable devices and hardware languages in the mid 90's and more recently emphasis on system design. In addition, design cycle times (the time it takes to get from product specification to delivery to the market) are being driven ever shorter. The skills that are required to support this level of design are rapidly changing, as are the software and hardware tools required for engineers. The current undergraduate program at the University of Southampton has run successfully for many years and provides a good grounding in hardware design. This paper develops Southampton's most recent adaptation to modern industry requirements, the educational rationale behind the design of this exercise [2],[3], the delivery approach and highlights the relevant portions of its implementation and delivery.

2. LABORATORY TEACHING

A. Learning Outcomes

The student's learning outcomes (LO) [4] for this exercise are listed below:
1. To carry out a complete ASIC design flow
2. To implement a specification
3. To carry out self-study of the design tools
4. To effectively manage a workload as a team
5. To experience industrial conditions and practice
6. To test their fabricated design vs. simulations

B. Laboratory Design Overview

Producing a full custom IC design is extremely expensive and time consuming, and many aspects are beyond the abilities of undergraduate students and if left visible would potentially even harm their learning due to added confusion and complexity. This laboratory uses cell based IC design which usefully limits ASIC design complexities while preserving the essential learning outcomes of this exercise.

This design exercise consists of two distinct parts: the "Design Phase" and the "Testing Phase". In the first of these two the students create their implementation of the specification and prepare functionality and performance simulations. The purpose of this phase is to introduce the students to schematic design, schematic verification, layout and layout verification. The tools used are ORCAD for schematics, PSpice for simulation and L-Edit for layout.

The second phase is after the ASIC fabrication and requires them to test their design for functionality and performance. The goal of this phase is to introduce the concepts of testing ICs and using test vectors to achieve this. This lab also introduces digital simulation (using VHDL in Modelsim) rather than the PSpice analogue simulation used in the "Design Phase".

The practical details of the custom design flow and bespoke hardware is given in section 3, Practical Details.

Both phases use the same strategy to achieve the LOs: Introductory lectures inform the students of the tools, deliverables and schedule. This is followed by periods of independent study in teams supported and reinforced by intensive supervised laboratory sessions.

C. Running the "Design Phase"

In this phase the students are given access to the specification, for example an 8 bit integer ALU. They are briefed on the design environment and given the location of self study resources on the tools and the specific design flow. After being assigned to teams of 6 the students then self study the tools and flow before the first of two full 8 hour supervised laboratory sessions.

Lab session 1 aims to efficiently handle queries arising from the initial period of self study and to ensure all students have a working knowledge of the tools and flow.

This session is then followed by one week in which the student teams self manage to implement a significant portion of their design and simulations.

Lab session 2 is the second of the 8 hour supervised sessions and is intended to guide the students through any challenges that arose from the previous period of unsupervised work and to finalize their design.

The deliverable from the "Design Phase" is the "Design Package". This package mimics the output produced from an industrial ASIC design project and consists of:
1. Design Schematics
2. Design Simulations (Spice)
3. Design Simulation Test Circuits (Spice)
4. Layouts (L-Edit)
5. Layout Simulations (Spice)
6. Layout Simulation Test Circuits (Spice)
7. The "Design Phase" report

There are two deadlines for the deliverable. The first is for the silicon layout and is one week after the second lab session. The second is for the complete "Design Package" and is two weeks after the second lab session.

D. Assessing the "Design Phase"

The first section of the lab is assessed on the contents of the "Design Package" with the majority of the emphasis on the content of the report. This report should contain:

Section 1: The Design – a description of the design approach

Section 2: The schematic designs – simulation results confirming the design's functionality.

Section 3: The layout –simulations demonstrating the design's functionality. This should contain a DRC report showing no errors.

The active involvement of all team members is also assessed.

E. The "Testing Phase"

This session proceeds in a very similar manner to the "Design Phase" (detailed in the previous section, C). The initial briefing introduces the task and the self study resources for the new tools. The student teams then familiarize themselves with the tools.

Lab session 1, as before, attempts to efficiently handle queries about the new tools presented to the students and ensure they are capable of the further period of self study.

The team has a week of self study to complete their test vectors, test circuits and plan their result collection in lab session 2.

In lab session 2 the teams test their schematic design with the complete test vector set. They then test their IC design with the complete test vector set. Finally the power consumption of the IC is measured.

The deliverable from this phase is the final report which extends the "Design Phase" report detailing the test methodology and their design's test results.

F. Assessing the "Testing Phase"

This assessment is based around the design of the test strategy and the performance of the ASIC evaluated in lab session 2 and the final report. The majority of the marks reside with the report that should detail:

Section 1: The test strategy, test circuits and test vectors.

Section 2: The functionality of the schematic design.

Section 3: The functionality and performance of the IC.

Again the active involvement of all team members is also assessed.

3. PRACTICAL DETAILS

This section details the practical resources needed to efficiently support the laboratory described above for a large student cohort.

A. The ASIC Design Flow

The design uses a simplified cell library extracted from the 0.35um (C35B4), 4 metal layer standard digital CMOS process used extensively by industry. The cell data is supplied in compatible forms to support the various tools used throughout this exercise: Cadence ORCAD Capture schematic library, Cadence ORCAD PSpice analogue simulation library, Cells for Tanner L-Edit layout and finally a Modelsim library for the final digital simulation and validation.

B. The Southampton "Superchip"

A crucial aspect of the program is the ability to effectively support a large number of individual IC designs without excessive cost in terms of time or resources. In order to achieve this, the Southampton "Superchip" has

been developed, which allows multiple student designs to be fabricated on a single IC, and encapsulated in a standard package. There are 16 separate design slots ~$100\mu m^2$ within this single chip, each with 24 inputs and 24 outputs, fully buffered. The "Superchip" is currently manufactured by Austria MicroSystems (AMS) and is fabricated using a. A sample "Superchip" is shown in Figure 1.
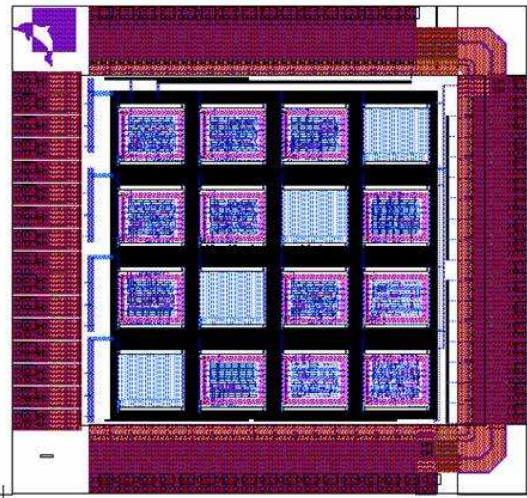

Figure 1, Layout of a "Superchip" showing the 16 design slots inside the pad ring

C. Superchip Automated Testbed

After manufacture, the chips are tested by the students in a simple PCB with an IC socket, connected to a PC via a single USB cable enabling simple, efficient IC testing to take place without the need for expensive and complex test equipment. The test PCB activates one site and breaks out all the inputs and outputs for direct investigation as well as providing automated application of test vectors downloaded from the PC.

4. CONCLUSIONS

This design exercise is unique as far as the authors know, in that the undergraduates will have experienced a complete, high fidelity CMOS IC design process flow by the end of the second year of their degree. Since 2004 over 300 students have produced their own designs on Silicon in that time. The benefits to industry are clear, as the students leave the University with not only the theoretical and design skills, but also a practical knowledge of real design deadlines, team-working and achievement.

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