Three-Dimensional Numerical Analysis of Switching Properties of High-Speed and Nonvolatile Nanoelectromechanical Memory

Tasuku Nagami, Hiroshi Mizuta, *Member, IEEE*, Nobuyuki Momo, Yoshishige Tsuchiya, Shin-ichi Saito, Tadashi Arai, Toshikazu Shimada, and Shunri Oda, *Member, IEEE*

***Abstract*—Static and dynamic mechanical properties of the movable floating gate are investigated for a newly proposed high-speed and nonvolatile nanoelectromechanical memory, which features a buckled floating gate incorporating the nanocrystalline silicon quantum dots integrated onto the gate of a MOSFET. By conducting a 3-D finite element simulation, we analyze the structural parameter dependence of the switching force F_S needed for the buckled floating gate to flip-flop between its bistable states and derive the relationship $F_S \propto L^{-4}\ T\ Z_0^3$, where L, T, and Z_0 represent the length, thickness, and equilibrium displacement of the buckled floating gate, respectively. We demonstrate that the switching frequency can be increased while maintaining the switching force when we downscale all the floating gate dimensions proportionally along with the scaling law. We also show that the switching voltage can be reduced down to less than 15 V while maintaining the ON/OFF operation range of the sense MOSFET by optimizing the cavity structure which sustains the inside buckled floating gate.**

***Index Terms*—Mechanical bistability, movable gate, NEMS, nonvolatile memory, silicon nanodot.**

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T. Nagami is with the Quantum Nanoelectronics Research Center and the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo 152-8552, Japan (e-mail: nagami@neo.pe.titech.ac.jp).

H. Mizuta was with the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo 152-8552, Japan. He is now with the School of Electronics and Computer Science, University of Southampton, SO17 1BJ Southampton, U.K., and also with the Solution Oriented Research for Science and Technology program, Japan Science and Technology Agency, Kawaguchi 332-0012, Japan.

N. Momo was with the Quantum Nanoelectronics Research Center and the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo 152-8552, Japan. He is now with the Center for Semiconductor Research and Development, Semiconductor Company, Toshiba Corporation, Yokohama 235-0032, Japan.

Y. Tsuchiya and S. Oda are with the Quantum Nanoelectronics Research Center and the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo 152-8552, Japan, and also with the Solution Oriented Research for Science and Technology program, Japan Science and Technology Agency, Kawaguchi 332-0012, Japan.

S. Saito and T. Arai are with the Central Research Laboratory, Hitachi Ltd., Tokyo 185-8601, Japan and also with the SORST Japan Science and Technology, Kawaguchi 332-0012, Japan.

T. Shimada is with the Quantum 14, Company Ltd., Koganei 184-8588, Japan, and also with the Solution Oriented Research for Science and Technology Program Japan Science and Technology, Kawaguchi 332-0012, Japan.

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I. Introduction

OVER the past few decades, the performance of very large scale integrated circuits (VLSI circuits) has steadily been improving by scaling down the dimensions of CMOSFETs. The International Technology Roadmap of Semiconductors (ITRS) [1] shows that the "Nano Era" for the CMOS started in 1999 with the gate length being shorter than 100 nm. The ITRS also predicts that this "miniaturization" trend will be pursued further, and the gate length will reach under 10-nm long in the next decade. However, maintaining this top–down miniaturization trend is getting exceedingly hard due to fundamental physical and technological limitations, as well as of the economical limitation.

Along with such an aggressive miniaturization trend of the Si VLSI devices, various Si-based nanoelectromechanical systems (NEMS) have recently been developed by making the characteristic length (such as the resonator length) smaller, and their mechanical and electrical properties have been investigated [2]–[5]. For example, the oscillation frequency of over 1 GHz has already been reported for the 1.1-μm-long SiC-based beam [5]. Since the operation speed of the NEMS increases primarily in inverse proportion to the square of the beam length, the extremely fast NEMS with the switching time close to the electronic devices may be realized by reducing their dimensions even smaller. It may therefore be worthwhile to consider integrating the NEMS components into conventional Si devices for adding new functionality [6], [7].

We have recently proposed a new fast and nonvolatile memory device [8] based on the bistable operation [9], [10] of the submicrometer-long NEMS structure, combined with the nanocrystalline (nc) Si quantum dots [11]. A concept of nonvolatile memory based on the mechanical bistability of a micromachined bridge has been reported in [12]. Our NEMS memory features a suspended SiO_2 beam formed in the cavity, which incorporates the nc-Si dots as a single-electron storage [Fig. 1(a) and (b)]. The beam is bent steady either upward or downward, and its both ends are clamped at the cavity sidewalls. When the gate voltage is applied, the charged beam moves in the cavity via electrostatic interactions between the gate electrode and the charge stored in the beam. A positional displacement of the beam changes the surface potential of the MOSFET sitting underneath and is therefore sensed as a shift of its threshold voltage. Write and erase operations of the NEMS memory are not associated with charge tunnelling

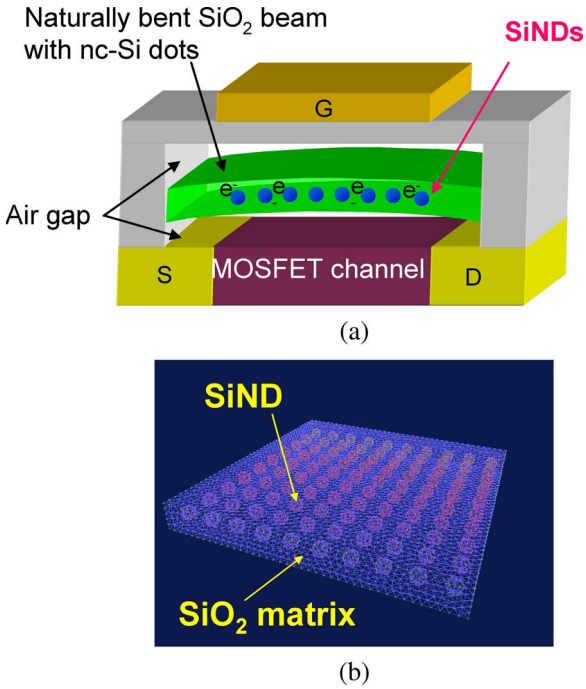

Fig. 1. (a) Schematic illustration of a NEMS memory device featuring a buckled floating gate suspended in the cavity above the sense MOSFET and (b) a multiscale floating gate consisting of a 2-D array of nanometer-scale Si dots embedded in a micrometer-scale SiO_2 thin beam.

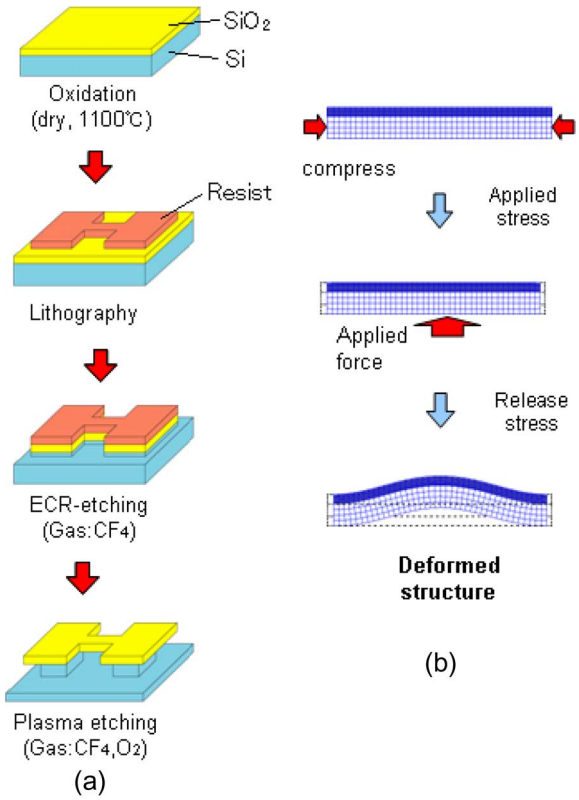

Fig. 2. (a) Fabrication process of the naturally bent SiO_2 floating gate and (b) modeling process of the initial floating gate structure by taking account of the internal stress.

via the gate oxide and, therefore, do not cause any gate oxide deterioration which limits the endurance cycles of the conventional flash memory. Mechanical fatigue of the beam should be studied as it will limit the endurance cycle of our NEMS memory, although amorphous SiO_2 is supposed to be mechanically robust as demonstrated by the recent experimental study of high-frequency mechanical vibration characteristics for a SiO_2 wire [13]. Various emerging memory devices have been proposed and studied intensively, such as ferroelectric RAM (FeRAM) [14], phase change RAM (PCRAM) [15], and magnetic RAM [16]. All these competing devices, however, need to adopt exotic materials which are not compatible with the conventional Si manufacturing technology.

The use of suspended MEMS gate coupled with MOSFETs has been studied for sensor applications [17], [18] over the past decades. Methods of passivating the surface of the suspended gates have been crucial as the device characteristics may vary depending on how the surface bonds are terminated chemically. The SiO_2-based suspended gate employed in our NEMS memory seems to be immune against that sort of falling as it is chemically robust.

In the recent experiment [8], we have fabricated a 3-μm-long free-standing SiO_2 single beam using a Si undercut etching technique. Fabricated samples have shown that the beams bent upward as a result of mechanical stress, stored in the SiO_2 being released. The mechanical bistability of the beam has successfully been demonstrated by using the nanoindentor loading system [19]. The experimental result showed clearly that it is possible to switch the beam from its upward bent state to the downward one by applying the external force. At the same time, however, we found that it is hard to estimate the switching force quantitatively as it is comparable to or even smaller than the load resolution of the nanoindentor system, which is about 10 μN. It will also be increasingly difficult to apply this kind of direct characterization method as the beam dimensions are scaled down to the submicrometer regime. In this paper, therefore, we conduct the 3-D finite element simulation and investigate the static and dynamic mechanical properties of the beam to evaluate the switching power and speed of our NEMS memory.

II. Numerical Analysis of Switching Characteristics for a NEM Floating Gate

A. Mechanical Bistability

In our past experiments [8], the test structure of the naturally bent floating gate was fabricated in the following manner [Fig. 2(a)]. A thin SiO_2 layer of 50–100 nm in thickness was formed on the Si substrate by using a thermal oxidation. Introduction of oxygen atoms causes the volume expansion of SiO_2 compared with Si, and therefore, the stress is generated at the SiO_2/Si interface. A few micrometer-long gate was then patterned by using the electron beam lithography, and the Si region under SiO_2 was etched out by applying anisotropic dry etching, followed by isotropic etching. As a result of release of the stress at the interface, the SiO_2 beam was naturally bent upward. In the present simulation, it is therefore crucial to prepare the initial model structure by taking account of the stress generated in the floating gate. We constructed a flat SiO_2

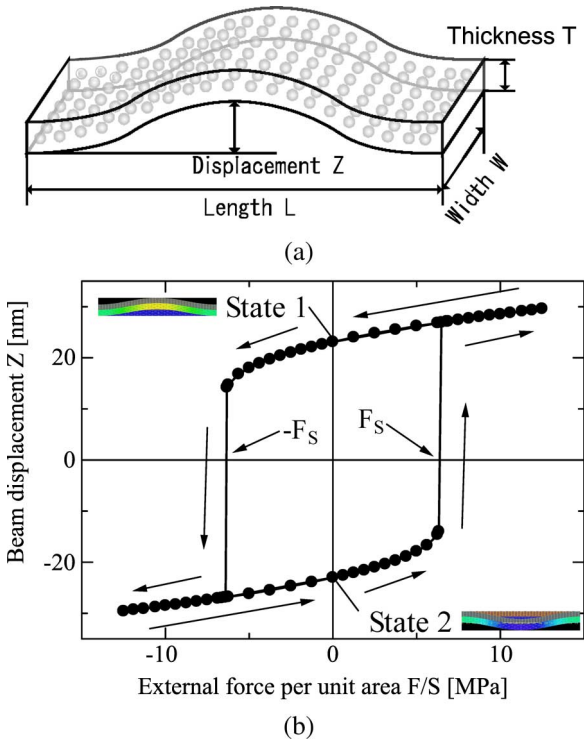

Fig. 3. (a) Structural parameters used for defining the buckled floating gate and (b) the beam displacement Z—external force per unit area F/S characteristics calculated for the floating gate of 400 nm in length, 200 nm in width, and 20 nm in thickness. The embedded nc-Si dots are of 10 nm in diameter, and the spacing between two adjacent dots is 10 nm.

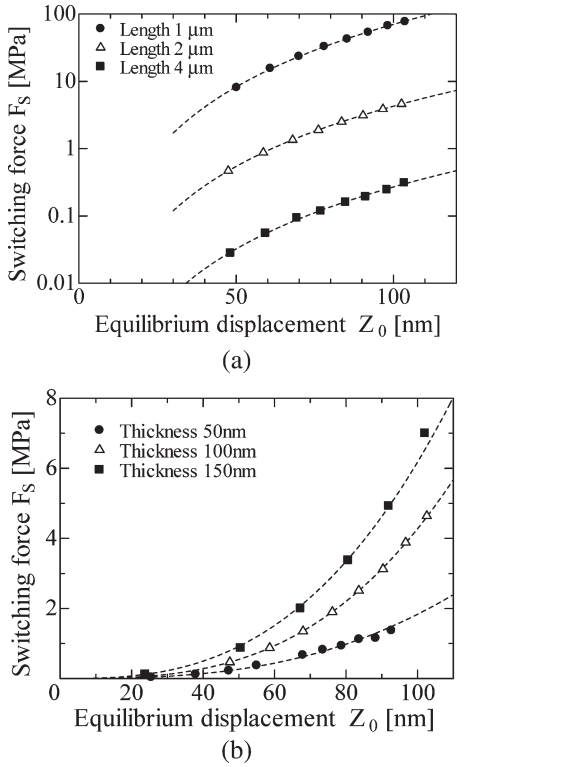

Fig. 4. (a) Switching force F_S calculated as a function of the equilibrium displacement Z_0 for the beam length of 1.0, 2.0, and 4.0 μm. The width W and thickness T are fixed to be 1.0 μm and 100 nm, and (b) F_S-Z_0 curves calculated for various values of beam thickness T of 50, 100, and 150 nm with $L = 2.0$ μm and $W = 1.0$ μm.

beam structure incorporating a 2-D array of spherical nc-Si dots. The flat beam was compressed laterally from both ends, and a small force was then applied onto the back surface in a direction perpendicular to the film. Degree of bending was adjusted via the applied compression force to reproduce the fabricated beam structures.

By using the initial beam structure prepared above, we studied the beam deformation under the external force. The beam dimensions are 400 nm in length L, 200 nm in width W, and 20 nm in thickness T [Fig. 3(a)]. The embedded nc-Si dots are of 10 nm in diameter, and the distance between the adjacent dots is 10 nm. The beam was clamped at its both ends, and the equilibrium upward displacement Z_0 was adjusted to 23 nm. We hereafter define an external force F. A positive value shows that the beam is uniformly pushed upward by using a force applied normal to the bottom surface. A negative value shows that the beam is uniformly pushed downward by using a force applied normal to the top surface. We performed the nonlinear static analysis for the above beam structure by using NEi Nastran [20]. We monitored the vertical shift of the beam center from its equilibrium position Z by sweeping the external force and calculated the displacement Z-force F characteristics. As shown in Fig. 3(b), the $Z-F$ curve shows a hysteresis loop, and the upper and lower branches indicate the upward and downward bent beams, respectively. It shows that the beam switches its state at $F = \pm F_S$, and we define F_S as the switching force. The mechanical bistability at $F = 0$ represents two memory states of our NEMS memory.

B. Switching Force

Next, we analyze how the switching force F_S depends on the beam structural dimensions. F_S was evaluated in the same way as above for various values of the length L, width W, thickness T, and the equilibrium displacement Z_0 of the beam. In the following analysis, we adopted the uniform beam structure composed of SiO_2 for simplicity, and chose $L = 2.0$ μm, $W = 1.0$ μm, and $T = 100$ nm as mean values for the beam dimensions. This simplification does not give any significant underestimation of F_S as the volume ratio of the embedded nc-Si dots to the entire SiO_2 beam is only about 3%. We then calculated F_S as a function of Z_0 for various sets of L, W, and T. Fig. 4(a) and (b) shows the F_S-Z_0 curves obtained for L of 1.0, 2.0, and 4.0 μm and those for T of 50, 100, and 150 nm, respectively. The results show that F_S increases proportional to Z_0 to the third power. It was also found that F_S increases inversely proportional to L to the fourth power and proportional to T. On the other hand, there was virtually no effect with varying W which is 0.5, 1.0, and 2.0 μm. As a result, we obtained the relationship between F_S and the floating gate dimensions expressed as $F_S \propto L^{-4}\ T\ Z_0^3$. This scaling nature indicates that the switching force can be maintained when all the dimensions of the beam are scaled down proportionally, although the scaling law for the entire memory cell is still left for our future study. In Fig. 5, the F_S-Z_0 characteristics are compared for the original beam structure with $L = 2.0$ μm, $W = 1.0$ μm, $T = 100$ nm, and those with all the dimensions

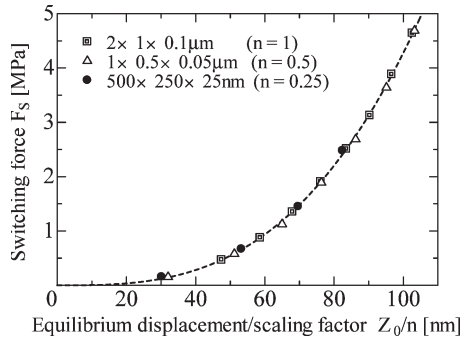

Fig. 5. $F_S - Z_0$ characteristics calculated for the beams with downscaling all the dimensions by 1/2 and 1/4. The horizontal axis indicates the normalized Z_0 with the scaling factor n of 1, 1/2, and 1/4.

are made 1/2 and 1/4. It should be noted that the horizontal axis shows normalized Z_0 with the scaling factor n of 1, 1/2, and 1/4. All three $F_S - Z_0$ curves fit perfectly one another, and this demonstrates that the above relationship between F_S and the floating gate dimensions is valid. Z_0 may be controlled by changing the stress introduced in the SiO_2 layer. One of the methods is to fabricate the SiO_2 bridge by combining the thermal oxidization which results in highly stressed SiO_2 and chemical vapor deposition which gives almost stress-free SiO_2.

C. Switching Speed

We also studied the switching speed of the beam by conducting NEi Nastran nonlinear transient response analysis. We applied an instantaneous force to the top surface of the beam, which was the minimum force to switch the initial beam state to another, and monitored the transient motion of the beam. Three beam structures were studied here: $L = 2.0$ μm, $W = 1.0$ μm, $T = 100$ nm (BM1), $L = 1.0$ μm, $W = 0.5$ μm, $T = 50$ nm (BM2), and $L = 0.5$ μm, $W = 0.25$ μm, $T = 25$ nm (BM3). No internal and external damping mechanisms were taken into consideration in the present simulation. Damping factors should be introduced into our future analysis for discussing the process of stabilization of the beam after switching. In this paper, however, we estimated the beam switching speed from the oscillating period of the beam free from damping. Fig. 6(a) plots the time dependence of the vertical beam displacement Z obtained for BM2 with four different values of the equilibrium displacement Z_0. The transient beam displacement is not simple sinusoidal because the beam oscillates between two mechanical stable states. It also showed that the oscillation period is heavily dependent of Z_0. The switching times are 33, 19, 14, and 12 ns for 15.1, 26.6, 34.7, and 41.3 nm, respectively. Fig. 6(b) plots the switching frequencies obtained for BM1, BM2, and BM3 as a function of Z_0. Note that the horizontal axis indicates the normalized equilibrium displacement with the scaling factor n of 1 (BM1), 1/2 (BM2), and 1/4 (BM3) in the same way as in Fig. 5. The oscillation frequency decreases linearly as Z_0 is reduced with all other beam dimensions being fixed. The oscillation frequency increases in inverse proportional to the dimensions of the beam. The switching speed of

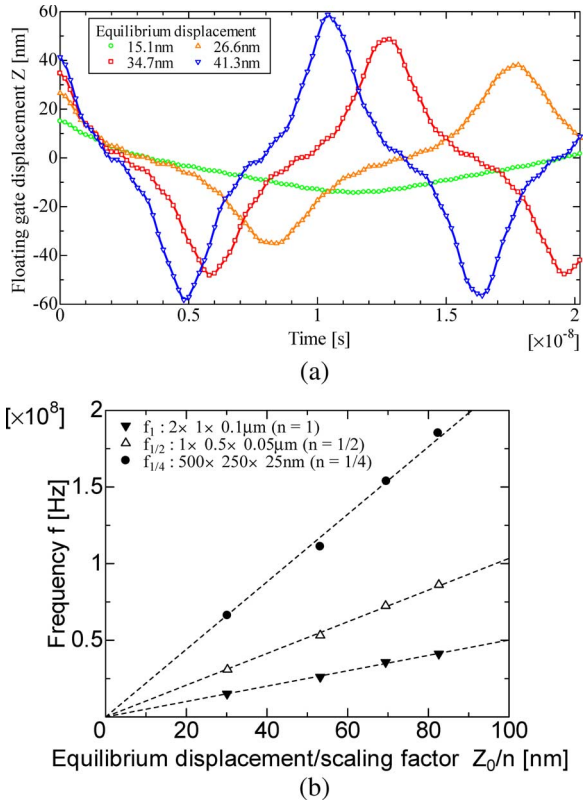

Fig. 6. (a) Transient beam displacement Z calculated for the beam with $L = 2.0$ μm, $W = 1.0$ μm, $T = 100$ nm, and various values of Z_0 when the minimum switching force was applied to the top surface of the beam at $t = 0$. (b) The switching frequency calculated as a function of Z_0 for the original beam structure and downscaled structures by the scaling factor n of 1/2 and 1/4. The horizontal axis indicates Z_0 normalized with n.

the beam, therefore, increases linearly by scaling down all the beam dimensions.

III. Discussion

A. Switching Voltage Reduction and Memory Operational Range

In this section, we discuss the switching voltage of our NEMS memory by using the semianalytical method. For simplicity, we hereafter assume that the floating gate is a flat beam composed of a 20-nm-thick poly-Si layer sandwiched with two 40-nm-thick SiO_2 layers [see Fig. 7(a)]. Length and width of the floating gate are 2.0 and 1.0 μm, and other structural parameters are shown in Fig. 7(a). We also assume that the floating gate is placed in the cavity in parallel to the top electrode and the substrate and simply moves up and down in the cavity rather than being deformed. When the gate voltage is applied, the force applied to the floating gate is expressed by

$$F = \sigma_{\mathrm{FG}} E S = \sigma_{\mathrm{FG}} \frac{V_g}{d} S \tag{1}$$

where E is the electric field between the top electrode and the substrate, $S = L \times W$, σ_{FG} is the sheet charge density stored in the floating gate, and d is the equivalent vacuum distance

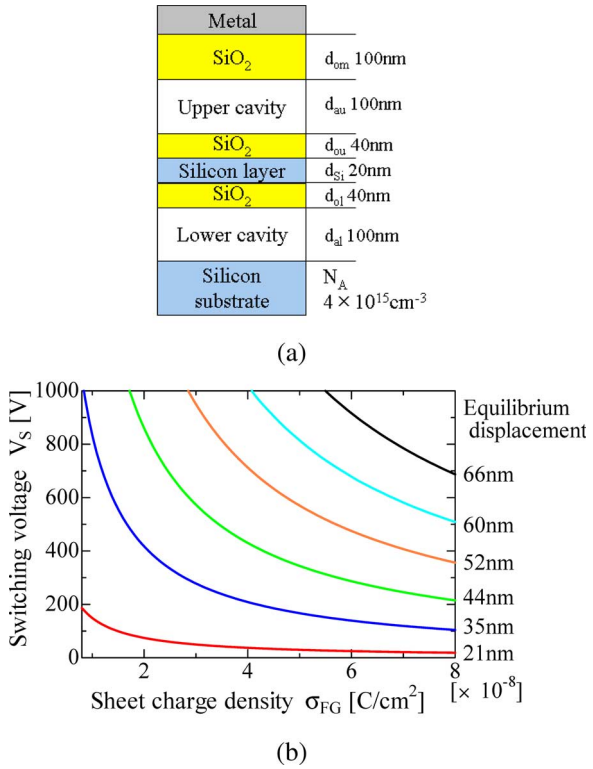

Fig. 7. (a) Schematic cross section of the simplified structure. Length and width of the floating gate are 2.0 and 1.0 μm, respectively. (b) Switching voltage V_S calculated as a function of the sheet charge density $\sigma_{\rm FG}$ calculated with various values of Z_0.

between the top electrode and the substrate [21]. The switching voltage V_S is then given by

$$V_S = \frac{F_S d}{S\sigma_{\rm FG}}. \tag{2}$$

For evaluating V_S by using (2), we used F_S calculated numerically in the same way as in Section II-A. Fig. 7(b) shows V_S as a function of $\sigma_{\rm FG}$ calculated with various values of equilibrium displacement Z_0. We see that the switching voltage can be decreased with reducing Z_0.

Reduction of Z_0, however, means a smaller positional change of the floating gate at ON and OFF states, and it is anticipated that electrical detection of the NEMS memory states, "0" and "1," becomes more difficult. We calculated the relationship between the surface potential and the stored charges by using a simple capacitance circuit shown in Fig. 8. An upper capacitance C_U is associated with the SiO_2 film under the gate electrode, the upper air cavity, and the upper SiO_2 film of the floating gate. A lower capacitance C_L is associated with the lower SiO_2 film of the floating gate and the lower air cavity. We assume that the sense MOSFET is in n-type operation, and therefore, a stored charge $Q_{\rm FG}$ in the floating gate is positive, and the stored charges Q_U and Q_L in the capacitors C_U and C_L are negative, respectively. For the equivalent circuit in Fig. 8, we derive the following equation:

$$\frac{Q_U}{C_U} - \frac{Q_L}{C_L} - \psi_S = 0 \tag{3}$$

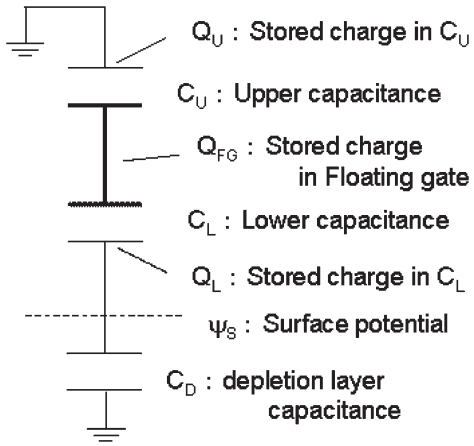

Fig. 8. Simple capacitance circuit used for the NEMS memory. C_U is associated with the oxide film under the electrode, the upper air cavity, and the upper oxide film of the floating gate. C_L is associated with the lower oxide film of the floating gate and the lower air cavity.

by using the Kirchhoff's voltage law. We also have the relationship $Q_U + Q_L = Q_{\rm FG}$, and the charge Q_S induced on the Si substrate surface is equal to Q_L. The relationship between Q_S and ψ_S is expressed as

$$\begin{aligned}\frac{Q_L}{S} &= Q_S \\ &= \mp\sqrt{2\varepsilon_{\rm Si}kTN_A}\cdot\left[\left(e^{-q\psi_S/kT} + \frac{q\psi_S}{kT} - 1\right)\right. \\ &\qquad \left. + \frac{n_i^2}{N_A^2}\cdot\left(e^{q\psi_S/kT} - \frac{q\psi_S}{kT} - 1\right)\right]^{1/2} \\ &\qquad (\psi_S > 0 \rightarrow -, \psi_S < 0 \rightarrow +)\end{aligned} \tag{4}$$

where $\varepsilon_{\rm Si}$ is the dielectric constant of the silicon, k is Boltzmann constant, T is the room temperature (300 K), N_A is the acceptor concentration, and n_i is the intrinsic carrier concentration. From these equations, the relationship between $Q_{\rm FG}$ and ψ_S is obtained, and we finally obtain the following relationship:

$$\sigma_{\rm FG} = \frac{Q_{\rm FG}}{S} = -\left(1 + \frac{C_U}{C_L}\right)\cdot Q_S + \frac{C_U\psi_S}{S}. \tag{5}$$

We assume that the floating gate moves down at the ON state and up at the OFF state by the equilibrium displacement Z_0 of 60 nm. Fig. 9 shows the Si surface potential ψ_S as a function of the floating gate charge density $\sigma_{\rm FG}$ at the ON and OFF states. We may define the operational range of the NEMS memory as a range of $\sigma_{\rm FG}$ where the ON and OFF states are given by the strong surface inversion and the surface depletion of the MOSFET, respectively. The operational range is indicated by a shaded region in Fig. 9. We evaluated the operational range for various values of Z_0 ranging from 66 nm down to 21 nm. As shown in Fig. 10, the operational range becomes narrower as Z_0 is reduced. It should be noted that we do not have any finite operational range for Z_0 of 21 nm.

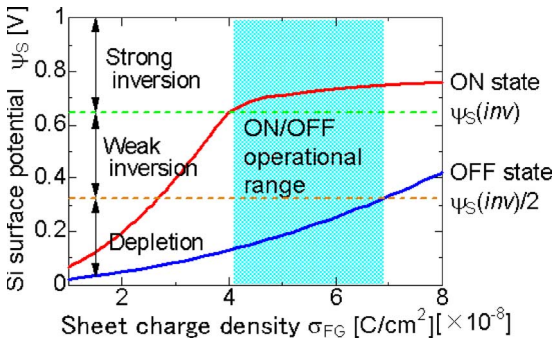

Fig. 9. Two solid curves show Si substrate surface potential ψ_S calculated as function of $\sigma_{\rm FG}$ at the ON and OFF states. Upper and lower horizontal broken lines indicate the minimum ψ_S for strong inversion mode operation and the maximum for the depletion mode operation, respectively. A hatched area indicates the operational range of the NEMS memory.

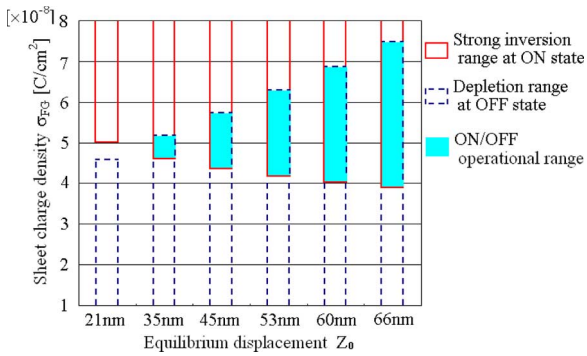

Fig. 10. Operational range spectra evaluated for various values of Z_0 in the same way as in Fig. 9.

B. *Structural Optimization for Improving* ON/OFF *Range*

As shown above, there is a certain tradeoff between decreasing switching voltage and increasing operational range when Z_0 is varied. We therefore examined to optimize other structural parameters without changing Z_0 of 21 nm for improving the operational range. Equation (5) indicates that the upper and lower capacitances, C_U and C_L, are the key parameters determining $\sigma_{\rm FG}$. We evaluated the operational range while varying the upper and lower cavity heights, $d_{\rm au}$ and $d_{\rm al}$, and the oxide film thickness under the gate electrode $d_{\rm om}$ [see Fig. 7(a)]. Fig. 11(a) shows the operational ranges calculated for various values of $d_{\rm au}$. The operational range improves by making the upper cavity smaller, and we have a finite operational range for $d_{\rm au}$ less or equal to 60 nm. Fig. 11(b) shows that further improvements can be achieved by reducing $d_{\rm om}$ with $d_{\rm au}$ being fixed to be 40 nm. Based on these guidelines for widening the operational ranges, we evaluated the switching voltages for four improved structures (Improved 1–4, see Table I) which provide the finite operational ranges. Fig. 12 shows the switching voltages V_S calculated for Improved 1–4 as a function of $\sigma_{\rm FG}$. All the curves are shown using both a broken line and a thick solid line. The finite solid lines indicate the operational range for the individual improved structures. These results show that it is possible to reduce V_S down to 10–15 V while keeping a certain range of operational window. It should be noted that the upper and lower cavity dimensions were optimized carefully so that

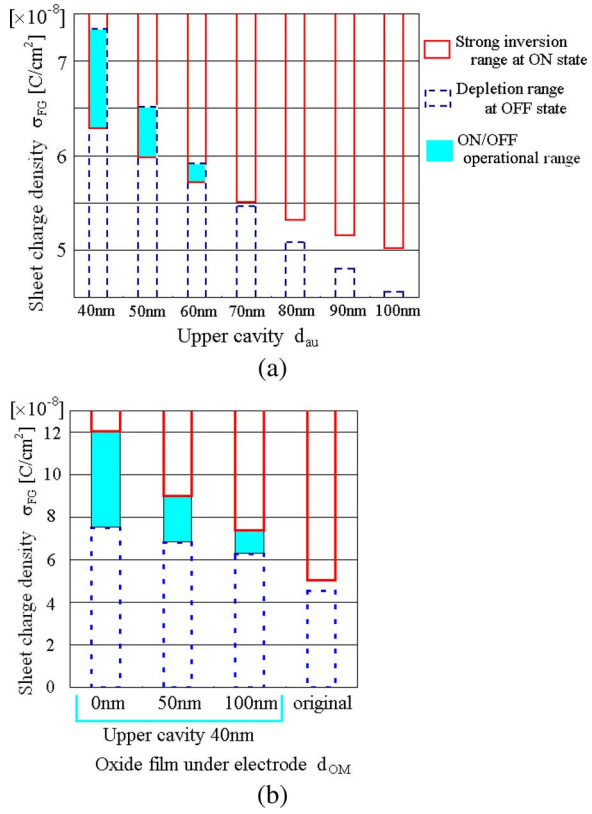

Fig. 11. (a) Operational range spectra calculated for various values of $d_{\rm au}$ with Z_0, $d_{\rm al}$, $d_{\rm om}$ fixed at 21, 100, and 100 nm, respectively, and (b) those for various values of $d_{\rm om}$ with Z_0, $d_{\rm au}$, $d_{\rm al}$ fixed at 21, 40, and 100 nm, respectively.

TABLE I
KEY STRUCTURAL PARAMETERS ADJUSTED FOR WIDENING THE OPERATIONAL RANGE: UPPER AND LOWER CAVITY HEIGHTS AND THE OXIDE FILM UNDER GATE ELECTRODE

	Oxide film	Lower cavity	Upper cavity
Original	100nm	100nm	100nm
Improved1	100nm	100nm	40nm
Improved2	100nm	40nm	40nm
Improved3	0nm	100nm	40nm
Improved4	0nm	40nm	40nm

the floating gate does contact either the gate or the substrate. In our device structure, however, switching of the floating gate is controlled via the electrostatic interaction between the gate electrode and the charge stored in the floating gate, and therefore, the pull-in phenomenon is less likely to occur, which is common for conventional suspended metal gate structures [6], [7]. For further reducing V_S down to those for FeRAMs and PCRAMs (typically 3–5 V), we should also optimize the structural and material parameters of the outer cavity such as the upper and lower cavity dimensions, thickness of the side walls as well as the choice of material for them.

IV. CONCLUSION

Static and dynamic mechanical properties of the floating gate structure have been investigated for the new NEMS memory

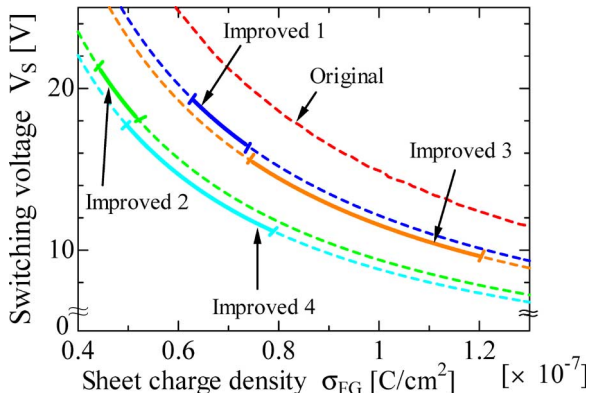

Fig. 12. Switching voltage V_S calculated as a function of $\sigma_{\rm FG}$ for various improved structures with $Z_0 = 21$ nm. The finite thick solid lines on the broken curves indicate the operational range for the individual structures.

by using the 3-D finite element simulation. The structural parameter dependence has been found for the switching force, $F_S \propto L^{-4}\, T\, Z_0^3$, and it has been proven that F_S is maintained when all the floating gate dimensions are scaled down proportionally. On the other hand, it has been found that the switching frequency increases when the floating gate dimensions are downsized along with the scaling law. It has been demonstrated that the switching voltage may be reduced down less than 15 V by optimizing the overall structures.

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Tasuku Nagami received the B.E. degree in electrical and electronic engineering and the M.S. degree in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2005 and 2007, respectively. He is currently working toward the Ph.D. degree in the Department of Physical Electronics, Tokyo Institute of Technology.

His field of interests includes modeling and design of silicon nanoelectromechanical devices.

Hiroshi Mizuta (M'89) received the B.S. and M.S. degrees in physics and the Ph.D. degree in electrical engineering from Osaka University, Osaka, Japan, in 1983, 1985, and 1993, respectively.

In 1985, he joined the Central Research Laboratory, Hitachi Ltd., Tokyo, Japan, and engaged in research on high-speed heterojunction devices and resonant tunneling devices. From 1989 to 1991, he worked on quantum transport simulation, and from 1997 to 2003, he worked on single-electron devices and other quantum devices as the Laboratory Manager and Senior Researcher at the Hitachi Cambridge Laboratory, Cambridge, U.K. From 2003 to 2007, he was an Associate Professor in the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, Japan. Since April 2007, he has been a Professor of nanoelectronics in the School of Electronics and Computer Science, University of Southampton, Southampton, U.K. He is also with the Solution Oriented Research for Science and Technology program, Japan Science and Technology Agency, Kawaguchi, Japan. He has coauthored more than 200 scientific papers and filed more than 50 patents. He has also coauthored books and chapters, including *Physics and Applications of Resonant Tunnelling Diodes* (Cambridge University Press, 1995). His current research interests include silicon-based nanoelectronics, silicon nanostructures such as silicon nanodots and nanowires, silicon nanoelectromechanical devices for information processing, and *ab-initio* calculations of nanomaterial properties and quantum transport in silicon nanostructures.

Dr. Mizuta is a Member of the Physical Society of Japan, Japan Society of Applied Physics, Institute of Physics, and the IEEE Electron Device Society.

Nobuyuki Momo was born in Aichi, Japan, in 1980. He received the B.S. and M.S. degrees in physical electronics from Tokyo Institute of Technology, Tokyo, Japan, in 2004 and 2006, respectively.

In 2006, he joined the Center for Semiconductor Research and Development, Semiconductor Company, Toshiba Corporation, Yokohama, Japan, where he has been engaged in the research and development of advanced analog devices.

Yoshishige Tsuchiya received the B.S., M.S., and Ph.D. degrees from the University of Tokyo, Tokyo, Japan, in 1996, 1998, and 2001, respectively.

In 2001, he joined the Quantum Nanoelectronics Research Center and the Department of Physical Electronics, Tokyo Institute of Technology, Tokyo, as an Assistant Professor. He is also with the Solution Oriented Research for Science and Technology program, Japan Science and Technology Agency, Kawaguchi, Japan. His current research interests include fabrication of ordered structure of silicon nanodots, silicon nanoelectromechanical device, high-k dielectric thin-film fabrication by MOCVD, and silicon quantum information device.

Dr. Tsuchiya is a Member of the Materials Research Society, Japan Society of Applied Physics, and Physical Society of Japan.

Shin-ichi Saito was born in Tokyo, in 1972. He received the B.S., M.S., and Ph.D. degrees from the Department of Physics, Waseda University, Shinjuku-ku, Japan, in 1995, 1997, and 2000, respectively.

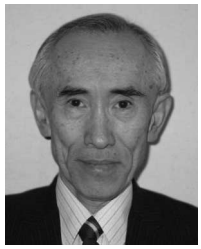
From 1998 to 2000, he was a Research Associate with the Waseda University, where he studied theoretical condensed matter physics of high-temperature superconductivity and strongly correlated electrons systems. In 2000, he joined the Central Research Laboratory, Hitachi Ltd., Tokyo, Japan, where he has been engaged in the device physics and process technology of silicon-based nanoelectronic devices. He is currently working on quantum effects in CMOS devices, carrier transport modeling, high-k gate stacks, mobility enhancement, self-organized nanoparticles, and silicon photonics.

Dr. Saito is a member of the Japan Society of Applied Physics and the Physical Society of Japan. He won the SSDM Paper Award for his analysis on the mobility reduction mechanism in high-k gate transistors in 2003.

Tadashi Arai was born in Gunma, Japan, in 1967. He received the B.S., M.S., and Ph.D. degrees in engineering from Gunma University, Gunma, Japan, in 1990, 1992, and 1995, respectively.

In 1995, he joined the Central Research Laboratory, Hitachi, Ltd., Tokyo, Japan, where he has been engaged in the research and development on chemical materials for devices.

Dr. Arai is a member of the Japan Society of Applied Physics and the Chemical Society of Japan.



Toshikazu Shimada received the B.S. degree in electrical communication engineering from Ritsumeikan University, Kyoto, Japan, in 1963, and the M.S. and Ph.D. degrees in physics from Osaka University, Osaka, Japan, in 1965 and 1968, respectively.

In 1969, he joined the Central Research Laboratory, Hitachi Ltd., Tokyo, Japan, and has been engaged in research on ion implantation into semiconductors, amorphous semiconductors, solar cells, and nano- and quantum devices. From 1995 to 1999, he worked as the Head of Liaison and Coordination Office in the Central Research Laboratory. Since 1999, he has been a member of a research project headed by Prof. S. Oda, supported by Japan Science and Technology Agency. Since 2003, he has been the CEO of Quantum14 Corporation and a Director of ProTech Company. He has coauthored more than 100 scientific papers in journals and conference proceedings and filed over 70 patents. He has also coauthored books and chapters, including *Amorphous Silicon* (John Wiley and Sons) and *Properties and Applications of Amorphous Materials, Encyclopedia of Applied Physics* (VCH Publishers, Inc.).

Dr. Shimada is a member of the Physical Society of Japan, the Japan Society of Applied Physics, and the Institute of Electrical Engineers of Japan.

Shunri Oda (M'89) received the B.Sc. degree in physics, and the M.S. and Ph.D. degrees from Tokyo Institute of Technology, Tokyo, Japan, in 1974, 1976, and 1979, respectively.

He is currently a Professor in the Department of Physical Electronics and the Quantum Nanoelectronics Research Center, Tokyo Institute of Technology. He is also with the Solution Oriented Research for Science and Technology program, Japan Science and Technology Agency, Kawaguchi, Japan. He has authored more than 200 papers published in journals and conference proceedings. His current research interests include fabrication of silicon quantum dots by pulsed plasma processes, single electron tunneling devices based on nanocrystalline silicon, ballistic transport in silicon nanodevices, silicon-based photonic devices, and high-k gate oxide ultrathin films prepared by atomic layer MOCVD.

Dr. Oda is a Member of the Electrochemical Society, Materials Research Society, and Japan Society for Applied Physics. He is a Distinguished Lecturer of the IEEE Electron Devices Society.