

# Yield Improvement Using Configurable Analogue Transistors (CATs)

P.R Wilson and R. Wilcock

*Abstract:* Continued process scaling has led to significant yield and reliability challenges for today's designers. Analogue circuits are particularly susceptible to poor variation, driving the need for new yield resilient techniques in this area. This paper describes a new configurable analogue transistor structure and supporting methodology that facilitates variation compensation at the post-manufacture stage. The approach has demonstrated significant yield improvements and can be applied to any analogue circuit.

*Introduction:* Yield and reliability have been identified as one of the greatest present and future challenges associated with nanometer process technologies [1]. The reduction in CMOS parameter precision as a result of aggressive technology scaling has led to variability becoming a first order limitation and one of the most urgent problems facing designers today [2]. Variability can be broadly categorized into spatial and temporal effects. Spatial variability can include die to die parameter mean shifts, on-chip layout induced variations and device to device mismatch caused by atomistic dopant variations, line edge roughness and parameter standard deviation [1],[3]. Temporal effects refer to time dependant changes in performance and reliability such as dielectric breakdown (DB), hot carrier injection (HCI) and negative bias temperature instability (NBTI), and these are now causing

significant changes in a circuit's performance over its lifetime [3]. In the case of analogue circuits the impact of variability can be complex due to a large number of performance specifications. Traditional approaches to increase robustness and resilience can introduce unacceptable power and area penalties when applied to modern process nodes [4]. In this paper a configurable analogue transistor (CAT) structure and supporting methodology is proposed, that facilitates post manufacture compensation variation. Both random and systematic variations can be compensated to address spatial variability and furthermore, compensation can be performed regularly during the circuit's lifetime, addressing temporal variability issues.

*The Configurable Analogue Transistor (CAT):* An NMOS example of a CAT device is shown in Figure 1 and consists of a main device,  $M_0$ , and  $n$  additional, adjustment devices,  $M_1$  to  $M_n$ . The adjustment device drains, sources and bulks are connected in parallel to the main device, and their gates are connected to the main device gate through the switches,  $S_1$  to  $S_n$ . The configuration of these switches, achieved through the digital signals  $B_1$  to  $B_n$ , provides a mechanism to adjust the overall device size, giving  $2^n$  possible width variations. The number of additional adjustment devices and their sizes depends on the context in which a specific CAT device is used. Typically, however, the lengths of  $M_1$  to  $M_n$  are all identical and equal to  $M_0$ , and the widths of  $M_1$  to  $M_n$  decrease incrementally by factors of two. In the context of a high performance analogue circuit, the physical layout of a CAT device must follow good layout practice, and have minimal impact on any matching scheme. Figure 2 shows the suggested approach for an  $n=3$  example where

the CAT device is embedded in a matched stack of transistors. It should be noted that digital selection signals would be static during normal operation so switching interference is not an issue.

*CAT methodology:* The proposed CAT design methodology is shown in Figure 3 and contains three main stages: critical device selection; optimal CAT sizing; and post fabrication optimization.

*1 Critical device identification:* The first stage of the CAT design flow is to identify devices in the target schematic which are most sensitive with respect to yield degradation. This is achieved during the schematic design phase using Monte Carlo analysis with statistical process variation models. The result from this stage is an ordered list of all circuit devices, starting with those which most affect the circuit's yield, to those which affect yield the least. At this point, a tradeoff exists between CAT overheads and potential yield improvement. If more devices are swapped with CAT devices, the potential yield improvement is greater, but the area and complexity overheads also rise. In reality, it has been found that only a small number of yield-critical devices need to be swapped for CATs to give a significant improvement.

*2 Optimal CAT sizing:* After the yield-critical devices have been identified it is crucial that the replacement CAT devices are sized to give the greatest potential for yield improvement. It will be appreciated that the adjustment device sizes must be calculated to take into account the expected process spread. If the adjustment is too fine, then variations may not be sufficiently

compensated to meet the target value. Conversely, if the adjustment is too coarse then there may be insufficient resolution for effective variation compensation. The expected process spread is a function of the device's purpose in the circuit. For example, matched devices will suffer from a smaller expected spread than unmatched devices due to their ability to reject common mode effects. The CAT sizing algorithm is therefore a function of the expected variation for a given device. The optimal adjustment range can be calculated theoretically, through iterative simulation or numerically. All three approaches have been investigated and give similar results. Figure 4 shows the adjustment range for an example device against the potential improvement in yield, and the optimum point can be clearly seen.

*3 Post-manufacture optimization:* After manufacture, each die's performance must be maximized through adjustment of the CAT devices. The simplest way to achieve this is to test the circuit with all possible CAT configurations to find the best solution, but this rapidly becomes intractable for anything more than a simple design. In some structures, which have a large quantity of unmatched devices, it is possible to use a single calibration device to obtain the correct configuration and then apply this to all unmatched CAT devices within the circuit in question, drastically reducing the post-manufacture overhead. Differential CAT structures suffer mainly from mismatch variation which is mostly random in nature and so the way in which process variations affect performance is more complex. However, with circuit knowledge it is possible to derive faster optimization procedures based on standard techniques. Although for smaller designs the use of external test equipment

is most suitable for the post-manufacture stage, it is envisaged that built-in test structures may increasingly be used with the CAT technique. Additional advantages of this approach are that it provides the potential for regular test and calibration cycles, which would tackle the increasing challenge of age related variability effects [3].

*Results:* The key benefit of the CAT technique is that transistors on fabricated dies can be individually adjusted to improve performance and therefore yield. To demonstrate the potential benefits, the drain current variation of a single device on a 120nm process was plotted using 1000 Monte Carlo simulations based on foundry statistical models. A suitable CAT device with three adjustment transistors was optimally sized and a further 1000 Monte Carlo simulations were run (with the same seed) for each of the eight CAT configurations. For each of the 1000 simulations the process of post-manufacture optimization was simulated using a program that inspects the eight drain current readings then chooses the drain current closest to the mean. The resulting distribution is plotted against the single transistor example in Figure 5. The reduction in standard deviation from  $3.32 \times 10^{-5}$  to  $6.75 \times 10^{-6}$  demonstrates the potential improvement provided by this technique.

*Conclusions:* One of the biggest challenges of shrinking process geometries is the associated increase in intrinsic device variability and analogue circuit design has become a major bottleneck as a result. The configurable analogue transistor (CAT) approach and supporting methodology described in this paper facilitates adjustment of critical devices after manufacture, allowing

poor circuit performance due to process variations to be compensated. This gives the potential for significant yield improvement, and even age effect compensation. In the example provided, the standard deviation is shown to reduce from  $3.32 \times 10^{-5}$  to  $6.75 \times 10^{-6}$  when a CAT device is used. The CAT technique offers a new practical approach for analogue designers using modern deep sub micron digital processes.

## References

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**Figure captions:**

Fig. 1 Configurable analogue transistor (CAT) schematic

Fig. 2 Configurable analogue transistor (CAT) layout

Fig. 3 CAT supporting methodology

Fig. 4 Optimal transistor sizing curve

Fig. 5 Design improvement on a 120nm process

Figure 1

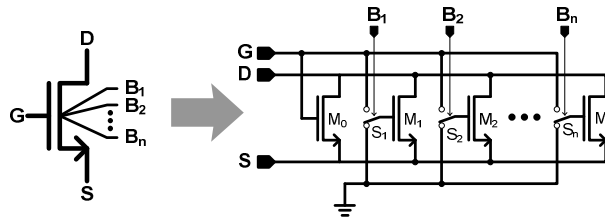


Figure 2

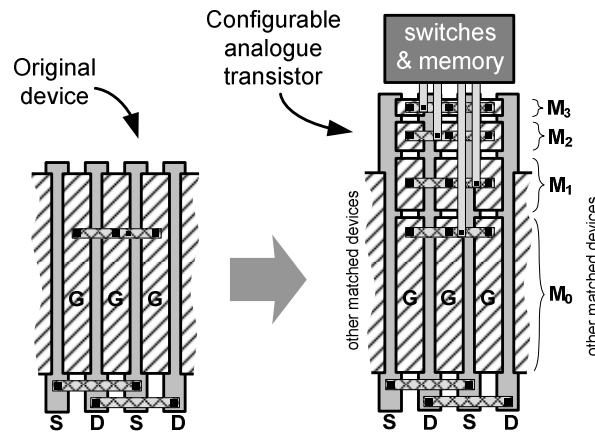


Figure 3

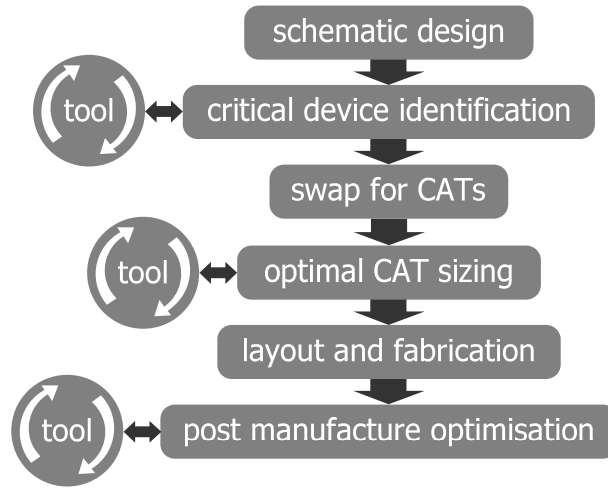


Figure 4

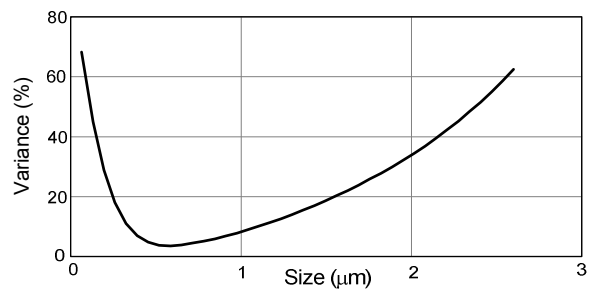


Figure 5

