Variation Resilient Adaptive Controller for Subthreshold Circuits

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***Abstract*—Subthreshold logic is showing good promise as a viable ultra-low-power circuit design technique for power-limited applications. For this design technique to gain widespread adoption, one of the most pressing concerns is how to improve the robustness of subthreshold logic to process and temperature variations. We propose a variation resilient adaptive controller for subthreshold circuits with the following novel features: new sensor based on time-to-digital converter for capturing the variations accurately as digital signatures, and an all-digital DC-DC converter incorporating the sensor capable of generating an operating operating V_{dd} from 0V to 1.2V with a resolution of 18.75mV, suitable for subthreshold circuit operation. The benefits of the proposed controller is reflected with energy improvement of upto 55% compared to when no controller is employed. The detailed implementation and validation of the proposed controller is discussed.**

I. Introduction and Related Work

Sub-threshold logic is attracting considerable attention from the low power research community for applications such as scavenging ambient energy. Over the last couple of years there has been considerable progress in designing subthreshold circuits and architectures that operate with supply voltages (V_{dd}) well below the transistor threshold voltage (V_{th}) and with minimum computation energy. Recent examples include a $3.5\frac{pJ}{inst}$ processor [1], a $27.3\frac{pJ}{inst}$ microcontroller [2], 180mV FFT processor [3] and $1.33\frac{pJ}{sample}$ FIR filter [4]. Most of the recent research efforts in the area of subthreshold logic has been focusing on addressing variability [5] [6]. This is because subthreshold circuits have exponential sensitivities to V_{dd}, V_{th} and temperature. To address the process variations in subthreshold circuits, a number of approaches have been proposed. In both [5] and [6] the authors have reported that V_{th} fluctuation is more a critical design issue in subthreshold voltages. Small variations in V_{th} ($\sim \pm 10\%$) results upto 96% degradation in the circuit performance at subthreshold voltages ($< V_{th}$), yet these are hardly noticeable at higher voltages ($> V_{th}$). A change in temperature also influences the circuit performance significantly. This can be mitigated through the applications of transistor sizing [7] and body biasing [8].

In [7] the authors have demonstrated that the optimal supply voltage V_{opt} exist below the threshold voltage V_{th} for maximum energy efficiency in subthreshold circuits. This occurs when the dynamic energy and leakage energy is comparable and is often referred to as the 'minimum energy point *(MEP)*'. Scaling the supply voltage further below V_{opt} may result in correct circuit operation but doesn't necessarily improve energy efficiency because the leakage energy starts to dominate. In [1], the importance of both process variations and the *MEP* operation for subthreshold circuits is reported. *MEP* in subthreshold circuits varies with the computation carried out [9]. Normally the V_{dd} at which the *MEP* occurs for a given computation is known. To provide greater flexibility, it is desirable to carry out different computation at different V_{dd}, requiring a DC-DC conversion. In [9] the regulation and generation of supply voltage is discussed for *MEP* operation and uses mixed mode design for measuring the actual energy consumption of the circuit. The usefulness of voltage scaling is discussed at superthreshold voltages in [10] [11] and ultra dynamic voltage scaling for subthreshold voltages in [12]. In [10], it has been shown that in case of systems with buffering capability, the workload variations can be accommodated with variable power supply at differing clock rates. This is achieved by varying the power supply and reducing the operating clock frequency during reduced workload periods instead of operating at fixed frequency and then shutting down.

This paper addresses two related problems in subthreshold design: supply voltage regulation for operation at *MEP* and mitigating variability due to process and temperature variations. We provide the architecture of a new DC-DC converter which allows ultra dynamic voltage scaling into the subthreshold region. The DC-DC converter provides different operating V_{dd} from 0V to 1.2V with a resolution of 18.75mV. This is necessary in subthreshold circuits since the *MEP* of a particular computation occurs at a specific V_{dd} [13]. To achieve different computations with *MEP*s will require different V_{dd}, therefore adaptive V_{dd} controller is necessary. Operating the circuits at very low voltage subthreshold region are susceptible to process variation [1]. In this paper we show that the proposed architecture with the DC-DC converter can be made more variation resilient to process and temperature variations. This is achieved by incorporating a Time to Digital converter within the DC-DC converter that can quantify the variations as a digital code.

II. Effect of Process and Temperature Variations in Subthreshold Logic

We focus on the effect of process and temperature variations on the minimum energy point for subthreshold circuits at different process corners and show why it is necessary to address such variations. Performing the corner analysis one guarantees correct operations considering both local and global variations. To study the effect of variations on the *MEP* that is dependent on V_{dd}, switching activities, process and temperature, we have performed spice simulations on the circuit discussed in [14]. The circuit is a ring oscillator with NAND gates. It offers fine control of the switching activity and thus is an ideal platform to study the subthreshold energy and delay characteristic.

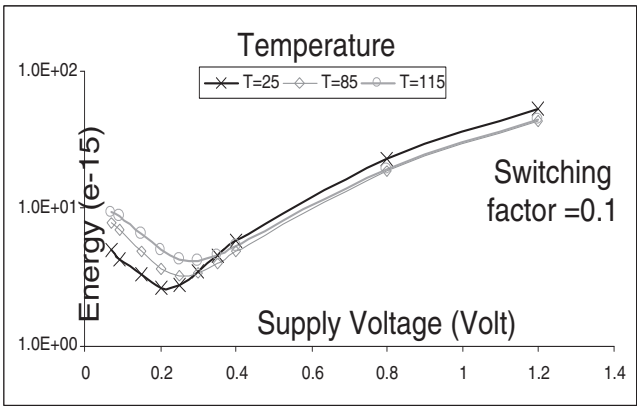

Fig. 2. *MEP* with temperature variation

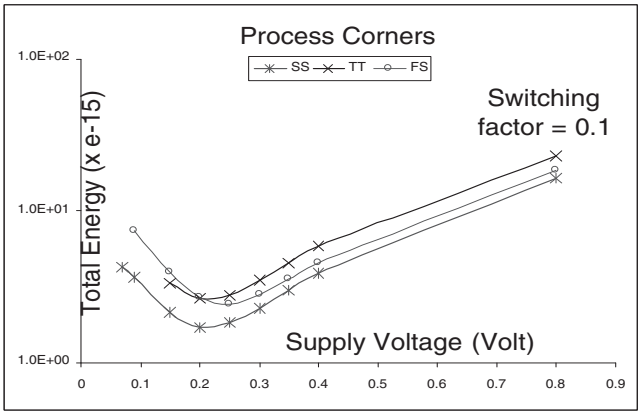

Fig. 1. *MEP* with process variation

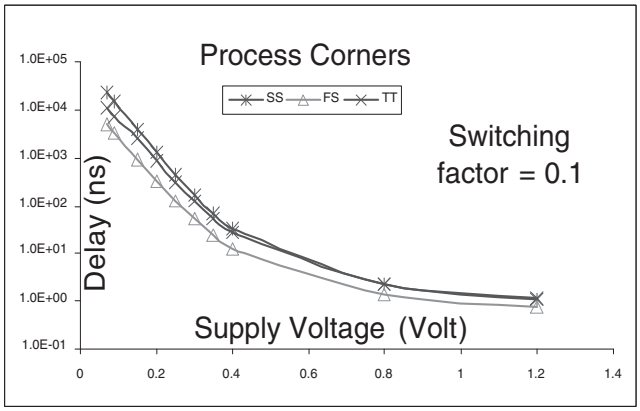

Fig. 3. Delay with process variation

Simulation results of the *MEP* for the ring oscillator are shown in Fig.1. Simulations were run for slow (SS), typical (TT), fast (FF) and fast-slow (FS) process corners on a 0.13μm CMOS process. The nmos V_{th} is 302mV for slow, 287mV for typical and 272mV for a fast process corner and can vary up to 10%. All simulations were run at the same power supply, switching activity ($\alpha = 0.1$) and temperature to explicitly demonstrate the effect of process shifts on the minimum energy point. As can be seen in Fig.1, process shifts can cause variations of up to 60% of the *MEP*. For example, in Fig.1, the V_{opt} is 200mV at typical corner, 220mV at slow and 250mV for FS corner. The minimum energy is 2.65*fJ* for typical, 1.7*fJ* for slow and 2.42*fJ* for fast-slow. This shows a variation in the V_{opt} of 25% and the energy variation of 55%. It also shows that it is desirable to implement the circuit at SS corner to obtain an energy efficient design. The exact variation will depend on the process parameters of the particular fabrication run as well as the circuit techniques used to calculate the *MEP*.

Temperature variations impact minimum energy point in the same manner as process variations. Shifts in temperature cause the actual delay to deviate from the expected delay. This has a direct influence on the *MEP*. Simulation results of the *MEP* for our case study circuit for different temperatures are shown in Fig.2. As can be seen the temperature variation influence the *MEP*. For example, in Fig.2, the V_{opt} at T$=$ 25°C is 200mV and at T$=$ 85°C is 250mV. The energy at *MEP* for T$=$ 25°C is 2.6*fJ* and at T$=$ 85°C is 3.2*fJ*. This represents a variation of energy of 25%. The delay is strongly dependent on the power supply voltage. Running at a lower supply voltage results in higher delays. These values can be inconsistent with the desired values. Simulation results of the delays for slow (SS), typical (TT) and fast-slow (FS) process corners are shown in Fig.3 for different V_{dd} values. As expected, the high V_{dd} results in lower delays while the low V_{dd} results in higher delays. For example, in Fig.3, a $10\%V_{dd}$ variation will cause the delay to vary up to 30% from the expected value in the subthreshold region. The magnitude of the impact of V_{dd} variation depends on the the delay differences between the actual and desired values. An adaptive method which can track and correct these variations (in Fig.1, Fig.2, Fig.3) is necessary for subthreshold logic which is one of the main aims of the paper.

A. Novel Variation Sensor based on TDC

A key component of the proposed adaptive controller is a novel time to digital converter. In this section, we quantify the shift of *MEP* due to the variations. The TDC generates a pulse width proportional to a desired voltage that is realizable using digital CMOS circuits. The novel variation sensor captures the variation in operating conditions based on time to digital conversion. Therefore, it can be used as a signature for a change in process and temperature variations. Based on this sensor, we propose a variation resilient adaptive control for subthreshold circuits.

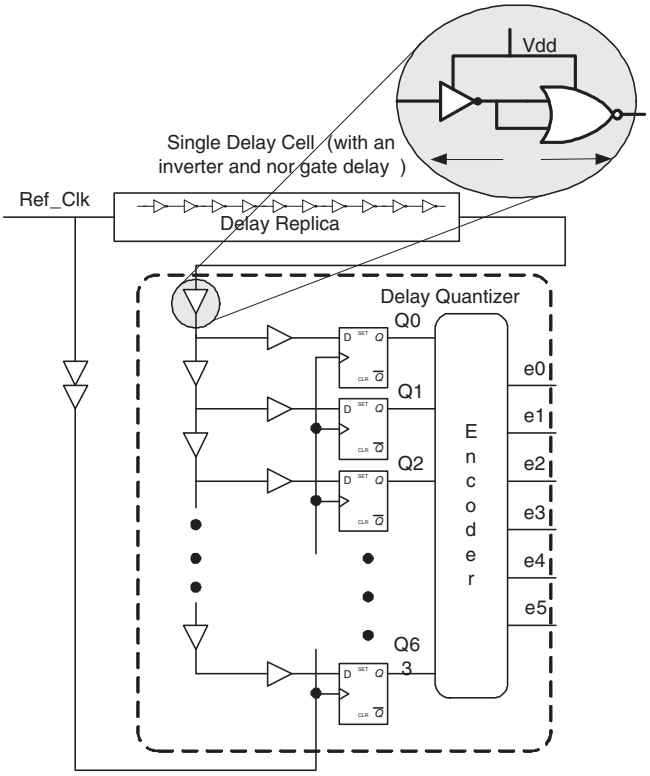

Fig. 4. Time to Digital Converter

The TDC block consists of a delay replica (critical path or the longest path replica of the load circuit), quantizer and an encoder as shown in Fig.4. The delay replica comprises of several INV-NOR stages. It is to be noted that only the circuit elements in delay and the flip flops are working in the subthreshold voltage region. Rest of the circuit is implemented with standard CMOS cells that operates above the transistor threshold voltage. And therefore it is assumed in this work that the controller is not affected by variations. The input reference signal '*Ref_clk*' could be generated by off-chip or on-chip methods. This clock propagates through the delay replica and the quantizer. It is then captured and digitized by the D-flip flops. The buffer inserted between the delay elements and the DFFs guarantees the timing requirement. The quantizer provides the quantized delay and is encoded to a 6-bit value that captures the actual variations in the chip. The number of bits has been selected as '6', since it provides the best resolution ($\frac{1.2V}{2^6} = 18.75mV$) and best tradeoffs in terms of performance. This 6-bit value is compared with the desired output voltage supplied by the rate controller. If the quantized output is the same as the desired value then it is concluded that the process variations are minimal and the comparator output is on a hold state. In practice the comparator output is used to increase(up), decrease(down) or hold(hold) the current supply voltage.

The pulse width in TDC needs to be linearly proportional to the measured voltage. This is implemented as a chain of delay elements placed back to back and is governed by the nonlinear behavior of the delay (Fig.3) in the subthreshold region explained in detail in [7]. Due to this, the reference signal is chosen carefully so that the range of the conversion is quantified by an initial calibration process. This calibration can be explained as follows. For example, the delay of inverter at full V_{dd} is 102 ps and at 0.6V is 442 ps and at 200mV is 79430 ps. In practice, the '*Ref_clk*' is delayed by multiple of these delays at respective voltages. For a '*Ref_clk*' of 14 ns input, the quantizer in the TDC outputs a digital code as shown in TableI. This digital code quantifies the number of shift due to the differential voltage (200mV). For example, the quantizer output at 1.2V is "FE0000..." and at 1.0V it is "FFFFFE00..". This signifies a total of 16 shifts due to the 200mV differential voltage from 1.2V to 1.0V, where each shift can be quantified as 12.5mV. In SecIV we have taken an adjusted '*Ref_clk*' to match the resolution τ of the TDC with the shift value, where each shift equals 18.75mV. At 0.6V, the output from the quantizer is not reliable. This is due to the exponential characteristics of delay that results in data being latched twice by a faster '*Ref_clk*'. The metastability associated with the flip flops due to the variations are considered and incorporated in the design. The full range of the TDC can be accommodated with a single conversion employing a larger TDC converter having more number of delay elements. Alternate method employs feedback loop where the range of the conversion can be controlled by keeping track of a single counter with resolution higher than the direct method or varying the '*Ref_clk*' to a much lower frequency. In Sec IV we will show how this is used to correct the '*MEP*' by compensating for the differential voltage affected by variations.

TABLE I
SUPPLY VOLTAGE AND QUANTIZER OUTPUT

Supply Voltage	Quantizer Output (HEX)
1.2V	"FE00 0000 0000 0000"
1.0V	"FFFF FE00 0000 0000"
0.8V	"01FF FFFF FF00 0000"
0.6V	"000F FFE0 001F FFC0 "

During measurement, the reference signal '*Ref_clk*'

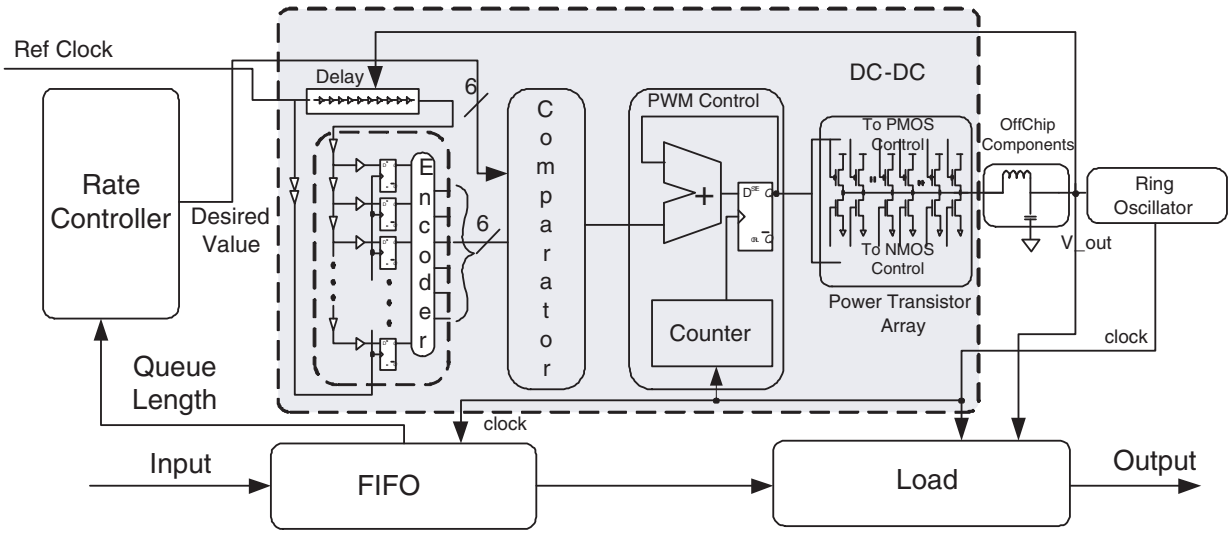

Fig. 5. Proposed Variation Resilient Adaptive Controller

circulates by a delay resulting from INV-NOR circuit and is shrunk by a specific pulse-width/cycle until it diminishes completely. It is difficult to keep the pulsewidth shrinking to zero which happens because of the H-L and L-H transition that are dependent upon the transconductance parameters. However, for practical purpose as employed in this design, the width shrinking is minimized by sizing the transistors and the insertion of buffer stages[15]. It is observed that the error of the offset offered by pulse width shrinking doesn't bring so much variations to the actual DC-DC conversion. The pulse shrinking from stage $(n-1)$ to $(n+1)$ is given by [16]:

$$\Delta W = (\beta - \frac{1}{\beta}) C_{L\ n-1} (\frac{1}{k_{p\ n-1}} - \frac{1}{k_{n\ n-1}}) \delta_i \qquad (1)$$

Where C_L is the effective capacitance, k_p, k_n are the transconductance parameters and δ_i is a proportional factor. Therefore the delay elements can have same dimension except for the n^{th} one whose width can be β times those of the others. Hence the width shrinking is controlled ($\beta > 1 \rightarrow$ shrink, $\beta < 1 \rightarrow$ expand) by keeping a tighter control on the aspect ratio of the transistors, within the range of variations upto 50% observed at *MEP*. In this section we have shown how the process variations are captured and encoded as digital signatures within our proposed TDC.

III. Proposed Variation Resilient Adaptive Controller

The adaptive supply voltage for obtaining minimum energy point is discussed in this section. The block diagram of the proposed adaptive controller consist of a FIFO, rate controller, DC-DC converter, Ring Oscillator and a load. We have implemented the rate controller as follows. The input data is buffered at the FIFO and the data rate is used to estimate the processing rate through the rate control. As the data fills up the FIFO, the queue length in the FIFO is updated. The queue length is the difference between the write pointer and the read pointer of the FIFO. If the processing rate is faster than the arrival of data, the queue length diminishes rapidly, idling the load most of the time. Thus, operating at the minimum energy point proves advantageous. If the data approaches faster than it can process, it results in loss of data. To avoid this, the circuit has to be operated at a higher rate. Therefore there is a direct relationship between the queue length and the processing rate. For example, a 6-bit value "001111" will mean the desired output from DC-DC will be $15 \times 18.75 \sim 282$mV. It is implemented as a 6-bit look up table (LUT). This is due to the resolution defined earlier SecII-A, the LUT data width is fixed at 6. The look up table is updated at regular intervals as the variations are sensed and needs to be corrected. The rate controller consists of only an adder and a LUT, hence area consumed by the rate controller is not significant.

The other main blocks of the adaptive controller is the DC-DC converter which consists of the TDC (Sec II-A), the comparator, PWM control and a power transistor array [15]. The TDC generates a digital code for the output voltage (V_{out}) and compared with the desired voltage value (6-bit) from the rate controller in the comparator. The comparator output is a two bit value based on whether the output voltage V_{out} is less than ("01") or equal to ("10") or greater than ("11") the desired voltage. This two bit value is fed to the PWM controller that provides a "1" or a "0" for a controlled period of time. A 6-bit register is used to store the value generated from the rate controller used for pulse width modulation. A new value at the up-down counter register is updated in each duty cycle where a toggle flip-flop generates the PWM output. This is done to increase, decrease or hold

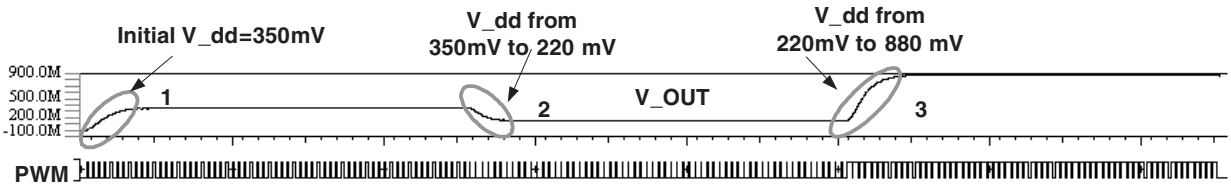

Fig. 6. Simulation of Adaptive Controller to generate different V_{dd}

the current output from the transistor array. At terminal count it triggers the toggle flip-flop to drive the PWM signal high, driving the PWM signal from low to high. The duty cycle of the PWM signal is controlled by the data value (N) loaded to the up/down counter and can be varied by specifying various data values. The higher the data value, higher is the duty cycle.

PWM controller generates the modulated signal with a duty ratio of $\frac{N}{2^6=64}$ which is also proportional to the resolution of the circuit. The input to the power transistor array is the modulated signal from the PWM. This controls the PMOS or NMOS switching time in the array. The power transistor array has several back to back transistors connected together. By doing so we could select a group of PMOS and NMOS transistors based on the workload. For the highest workload, all the transistors in the array is selected. Thus, the resolution of this array is fine grained with PWM control alongwith the selection of group of transistors and is about $\frac{1}{64}V_{dd} = 18.75$mV. With this configuration, however care is to be taken for spurious transitions occurring when the transitions in counter occurs from $N = 64$ to 0. To avoid this a simple upper bound and lower bound of the desired voltage is set to avoid the unwanted switching of all transistors occurring at once. The average voltage is dependent on the low pass filter consisting of external components L and C. The adaption mechanism of our proposed controller to capture the process variations is based on [10].

IV. Experimental Results

We have validated the proposed adaptive controller (Fig.6) using a mixed mode simulation environment from Mentor Graphics, using combination of spice and *VHDL-AMS*. The digital blocks (FIFO, rate controller and encoder, comparator, PWM of the DC-DC converter) were modelled in VHDL. The delay, TDC, power transistor array, ring oscillator and a capacitive load (ring oscillator [14]) have been modeled using spice with 0.13μm CMOS foundry transistor models based on ST process (Fig.5). Several A-D and D-A *VHDL-AMS* models were inserted for communication between the digital and analog blocks of the controller. To verify the adaptive performance of the controller, we performed simulations as shown in Fig.6. Through the simulations, we will show how the rate controller inputs are translated to voltage levels. Secondly, we will also show how the TDC within the adaptive controller captures the variations. Finally we will show how these are corrected in the controller.

As shown in Fig.5, the data to be processed is the input to the FIFO. Depending on the data rate, input data will fill up the FIFO that determines the queue length. Therefore, the queue length will change based on the data rate. Based on the range of the queue length, the location of the look up table is selected from which a 6-bit word is fetched. This is the desired voltage value encoded as bits. These values were obtained prior to the circuit operation through simulations. For example, a digital word '19' from the rate controller will get translated to $19 \times 18.75 \sim 356$mV from the DC-DC converter. This is shown as marked '1' in the Fig.6. The *Ref_clk* that is delayed and processed at the TDC as a digital signature is compared with the desired value. If the comparator output shows no changes in these two values then it shows that the variations did not occur. However, any deviation due to variation will reflect in the comparator output. We will explain this with the following example. During the initial design phase, we constrain the circuit when it is fabricated. It is assumed that the circuit be operational at the slow corner. Due to process and temperature variations the circuit will be operated at a different process corner. During all this time, the rate controller is first set to issue voltages to operate at typical corner. However, the desirable points were for the slow corner.

Based on the stored values in the LUT, the rate controller issues a 6-bit word (19 in this case). At this voltage the delay values found form typical and slow process (discussed in Sec II) corners are at 69ns and 54ns respectively. Due to the induced process variation response, the encoder will show the variation in the form of a digital signature. In our case, the encoder shows a one bit variability when compared to the desired value. The shift in this one bit needs to be reflected in the LUT, so that the values coming out from the rate controller in the operation is compensated. This takes place in the first 2 system cycles as shown in Fig.6 marked '1'. The operational frequency of the clock is 64 MHz and the system cycle is 1 MHz (64 MHz$/2^6$, due to terminal count of the 6-bit counter). The 1-bit value is the resolution of the DC-DC converter and is equal to 18.75mV. This ensured that the variation is recorded and corrected. As shown in Fig.6, the simulation marked '2' shows the compensation. Initially, the LUT was loaded with the typical process voltage levels.

At this point, the circuit is expected to work at the *MEP* for typical, the voltage from the DC-DC converter will be 200mV. It should be noted that the ring oscillator circuit has been used as a load for this purpose. As was shown in Fig.3 in SecII the *MEP* operating voltage is 200mV at typical and 220mV at slow corner. But because of the 1-bit shift the corrected value will be $\sim 200 + 18.75 = 218.75$ which is the optimal voltage for *MEP* for the slow process. Operating at this voltage ensures a net energy savings of up to 55%.

This demonstrates the capability of the proposed TDC capturing and correcting efficiently the process and temperature variations. This is reflected by achieving the *MEP* of the ring oscillator circuit which is 1.7*fJ* with V_{dd} =220mV (see SecII for details). To show that the adaptive controller works for other voltages in the simulations marked '3' in Fig.6, we show an additional step change of voltage to 880mV due to a new word issued from the rate controller. These three values are a subset of the values between 0 to 1.2V with a resolution of 18.75mV that the DC-DC converter can produce. We have used a ring oscillator as the load of the adaptive controller (Fig.5). We have also examined the capability when the load is a 9-tap FIR filter [4]. It is observed that the proposed controller behaving as expected. With variation due to process and temperature, energy gains up to 55% can be achieved by our proposed adaptive controller. We have experimented with different digital loads and found that our proposed adaptive controller can capture the variations in a wide range of load scenarios. It is assumed that the circuit with voltage scaling capability would have an embedded DC-DC converter which will be reused for the proposed controller reducing its area overhead. As future work, we will investigate the energy consumption of the proposed adaptive controller through simulations and the chip which will be implemented and tested.

V. Conclusion

In this paper we have proposed a new all digital, variation resilient adaptive controller for subthreshold circuits. The controller features a new DC-DC controller, a novel TDC converter. The novel TDC captures the variation as digital signatures, that translates and adjusts the variations and supplies a specific supply voltage generated by DC-DC converter. The controller is variation resilient as it captures the process and temperature variations by which it is able to correct itself and this enables minimum energy points for subthreshold circuits. We have shown through the simulations, that the new DC-DC converter provides different operating V_{dd} from 0 to 1.2V with a resolution of 18.75mV that is necessary to achieve the *MEP* in subthreshold circuits. It is hoped that the proposed variation resilient adaptive controller makes a sound contribution to the continuing research efforts in improving the robustness of threshold circuits to process and temperature variations.

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