Fabrication of Magnetooptical Atom Traps on a Chip

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Abstract—**Ultracold atoms can be manipulated using micro-fabricated devices known as atom chips. These have significant potential for applications in sensing, metrology, and quantum information processing. To date, the chips are loaded by transfer of atoms from an external macroscopic magnetooptical trap (MOT) into microscopic traps on the chip. This transfer involves a series of steps, which complicate the experimental procedure and lead to atom losses. In this paper, we present a design for integrating a MOT into a silicon wafer by combining a concave pyramidal mirror with a square wire loop. We describe how an array of such traps has been fabricated, and we present magnetic, thermal, and optical properties of the chip.** [2008-0124]

Index Terms—**Atom chips, cavity patterning, electrophoretic resist, magnetooptical traps (MOTs).**

I. INTRODUCTION

ATOM CHIPS are microfabricated devices that control electric, magnetic, and optical fields in order to trap and manipulate cold atom clouds [1], [2], [4], [5] and to form Bose–Einstein condensates [6]–[8]. Potential applications include atomic clocks [9], atom interferometers [10], [11], and quantum information processors [12], [13]. Silicon is one of several materials used as a substrate for atom chips. It is attractive for this purpose because its properties are well known and fabrication techniques are highly developed. The small scale of microfabricated current-carrying wires makes it easy to generate strong magnetic-field gradients near the surface of the chip, forming tight traps for paramagnetic atoms. The loading of such magnetostatic traps usually starts with a magnetooptical trap (MOT), typically some 3–4 mm from the surface. This collects atoms from a tenuous room-temperature vapor and cools them, typically to 100 μK, using circularly polarized light beams in conjunction with a spherical quadrupole magnetic field. The atoms are sometimes further cooled to a few tens of microkelvins using optical molasses, before being captured in a weak magnetic trap to form a large atom cloud, typically 1 mm in size. At this point, the atoms still have to be handed over to the microscopic magnetic traps on the chip, a process that involves further compression of the cloud and very accurate positioning of the atoms. This sequence of loading and transfer is complicated and could be largely eliminated if the MOT were integrated into the chip. A first step in this direction was made in [3] by gluing a matrix of insulated wires together; however, fully integrated fabrication would open up the possibility of building large arrays of MOTs to prepare many independent cold atom clouds.

This paper describes the fabrication and initial testing of an integrated array of MOTs on an atom chip, as proposed by Trupke *et al.* [14]. Each of these MOTs automatically prepares all the required light beams from a single circularly polarized input beam by reflecting the light in a concave square pyramid of mirrors [15]. This greatly reduces both the number of expensive optical components needed to prepare the light beams and the amount of laser power needed. Integrated wires encircling the opening at the base of the pyramid produce the required magnetic-field distributions with modest electrical power consumption and accurate positioning. The fabrication of an integrated MOT array on a chip represents an important step toward a truly integrated atom chip for portable applications.

The atom chip we have fabricated has six rows of pyramids, ranging in size from 200 to 1200 μm, serviced by 12 separate wires to produce the magnetic fields. For pyramids up to 600 μm, the encircling wires have a width of 25 μm. The larger pyramids are serviced by wires of 50-μm width. In total, there are 48 pyramid MOTs. The whole chip is packaged into a ceramic pin-grid array (CPGA) with multiple wire bonds of diameter 50 μm to bring high currents in and out of the chip. The silicon sidewalls of the pyramids are coated with gold to create micromirrors for reflecting the laser light. The pyramids formed by etching silicon have a 70.5° apex angle, rather than the ideal 90°. The optical properties of such a pyramid have already been investigated in [14]. In those experiments, it was observed that light reflected near the diagonal edges can prevent the MOT from working. Here, we have developed the necessary fabrication steps to eliminate these reflections by removing the gold near the corners of the pyramids.

This paper is organized as follows. Section II outlines the principles of atom trapping in these pyramidal micromirrors, Section III describes the microfabrication, Section IV presents initial tests of the device, and Section V discusses some prospects for using the chip in applications.

II. PRINCIPLE OF THE MOT ON A CHIP

Circularly polarized light, incident along the axis of a square pyramid, is reflected by the four metal mirrors that form
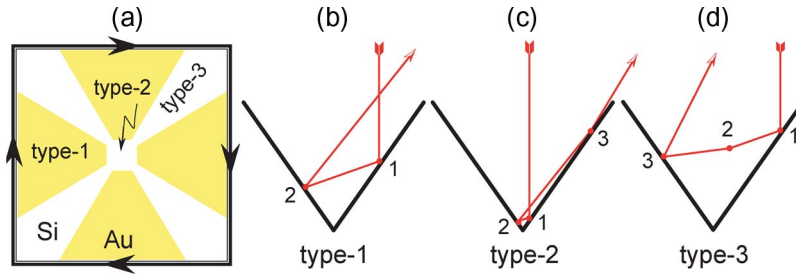
Fig. 1. (a) Plan view of pyramid showing the three regions of reflection and the encircling current. The following three figures illustrate the sequence of reflections. (b) Cross section through pyramid showing a type-1 reflection. (c) Type-2 reflection. (d) Type-3 reflection, where the ray is intercepted by the adjacent mirror at the point marked "2."
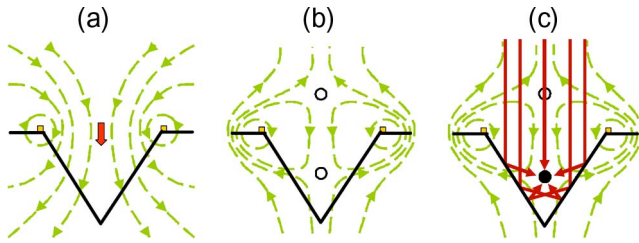

Fig. 2. (a) (Dashed lines) Magnetic field created solely by the wires around pyramid opening. (Block arrow) Maximum field strength is at the center of the loop. (b) With the addition of a uniform bias, the net field acquires two minima, indicated by solid circles. (c) Circularly polarized light creates a MOT at the field minimum, indicated by a filled circle. The beams that contribute are shown as solid arrows.

the pyramid. At each reflection, the helicity of the light is reversed. If the pyramid has a 90° angle between opposite faces, these reflections produce three counterpropagating pairs of light beams that are mutually orthogonal. Together with a magnetic quadrupole field, this configuration creates a MOT, whose radiation pressure forces cool and trap atoms from a room-temperature vapor [15], [16].

We form the pyramids by etching a silicon wafer, cut on the {100} plane. Potassium hydroxide (KOH) etches anisotropically through square openings to reveal the {111} planes, which form hollow pyramids with an apex angle of 70.5°. This departure from a right angle causes the beams to be reflected into a variety of directions. We classify these beams as Type 1, 2, or 3, based on the region of the pyramid where the first reflection occurs, as shown in Fig. 1(a). Type-1 rays are reflected on two opposite sides of the pyramid before leaving, as shown in Fig. 1(b). Type-2 rays also reflect on opposite faces but strike the original face again before leaving, as shown in Fig. 1(c), making a total of three reflections. The area contributing to this is only the central 1.1%. After the first reflection in Fig. 1(d), type-3 rays head toward the opposite face; however, considering that they are incident close to the diagonal edge of the pyramid, they are intercepted on the way by the adjacent face. Here, they undergo a grazing reflection, marked (2) in Fig. 1(d), where the helicity of the light is reversed. Finally, the opposite face is reached for a third reflection.

The wires electroplated on our chip form a square loop of side L around the pyramid base. A current I in this loop makes a magnetic field, as shown in Fig. 2(a). At the center of the loop, in the plane of the wire, the field strength is $(2\sqrt{2}/\pi)\mu_0 I/L$ downward. We superpose a uniform vertical bias field in order

to create the quadrupole field configuration required by the MOT, as shown in Fig. 2(b). The strength B_T of this bias is chosen to center the quadrupole halfway between the base and the apex, at a distance $(1/2\sqrt{2})L$ from the surface of the chip. This requires $B_T = (8\sqrt{2}/3\pi\sqrt{5})\mu_0 I/L = 0.54\mu_0 I/L$. The light beams needed to create the MOT inside the pyramid are formed from the incoming circularly polarized beam by the first and second reflections of the type-1 rays, as shown in Fig. 2(c). The type-2 rays produce a slight imbalance in the MOT force but are largely unimportant. The type-3 rays tend to destabilize the MOT because they have the wrong helicity and produce a strong force that pushes the atoms out of the pyramid instead of trapping them.

We have conducted preliminary experiments using a large glass pyramid coated with gold. Initially, this failed to produce a MOT because of the presence of the type-3 rays. Atoms were successfully trapped once the gold was removed from the areas where the type-2 and type-3 rays are produced. We were also able to make the MOT operate [14] by using a lower reflectivity (78%) coating of aluminum, which was not cut away at the edges and center. In such a pyramid, the intensity of the harmful type-3 light is decreased relative to the type-1 beams, considering the additional reflection by the lossy surfaces.

The current in the wire determines the vertical gradient in the MOT, which is related to the corresponding bias field according to $(26\sqrt{2}/15)B_T/L = 2.45B_T/L$. Under typical operating conditions used in most MOT experiments, the gradient is approximately 0.15 T/m. This is readily achieved on the chip because of the small scale; for example, in the 1-mm loop, it requires 0.1 A. The same wires can also be used to create a purely magnetic trap, with a depth of μB_T, where μ is the magnetic moment of the atom. Such a trap can hold atoms for a few seconds, provided its depth exceeds the temperature of the atoms by a factor of five or so. Ideally, we would like to be able to hold a 100-μK cloud, which requires a 0.7-mT bias field, corresponding to a current in a 1-mm loop of 1 A. The feasibility of using such currents is discussed more fully in Section IV-B. Further details about magnetic trapping of neutral atoms can be found in [1].

In summary, the aims of the fabrication were to create pyramidal micromirrors which would not reflect the damaging type-3 beams and to surround these mirrors with wires able to create the required magnetic-field strengths and gradients. In the following sections, we describe how these aims have been achieved.
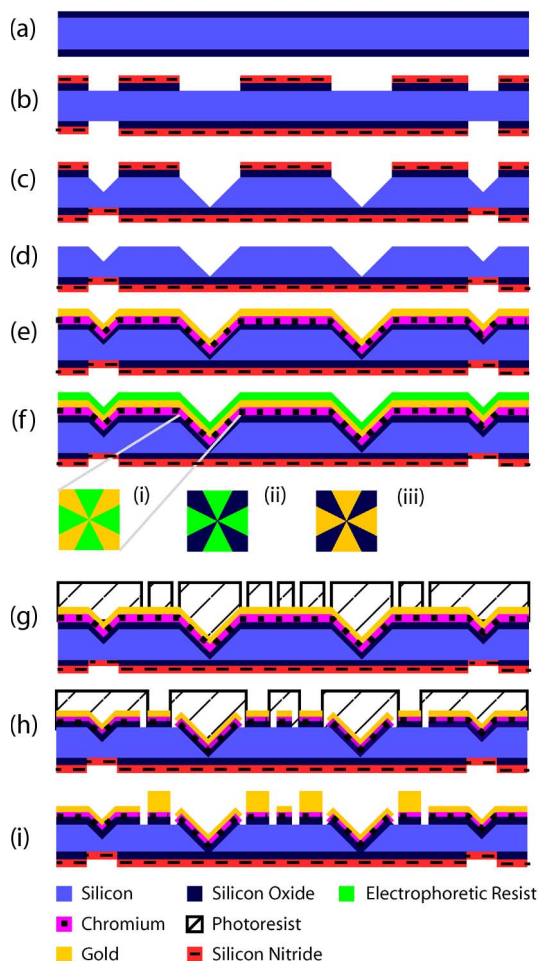
Fig. 3. Process flow for fabricating the pyramid MOT chip. (a) ⟨100⟩ Silicon wafer with 170 nm of oxide deposited. (b) Fifty nanometers of nitride deposited; alignment marks etched into the back, and pyramids opened on the front. (c) Back alignments protected with PECVD nitride layer and pyramids etched in KOH. (d) Front nitride and oxide stripped. (e) One-hundred-seventy-nanometer TEOS oxide deposited along with 50 nm of chromium and 100 nm of gold. (f) Electrophoretic resists deposited on the gold [(f-i) electrophoretic resist extends into pyramids, where it is patterned; (f-ii) gold and chromium are wet-etched; and (f-iii) resist removed from the whole wafer, leaving flower-patterned pyramids]. (g) AZ6612 spun onto the gold and patterned to create wire tracks. (h) Wire tracks are etched, and a layer of AZ9260 is spun and patterned to form a mold for electroplating. (i) Gold wires electropolated, resist removed, and chips completed.

III. FABRICATION

The fabrication processing sequence is shown in Fig. 3. We start by preparing the wafer and etching the pyramids. The whole surface is then coated with gold and patterned to remove the gold from the type-3 regions and to form the wire tracks. In these steps, the main fabrication challenge was to cover the wafer with a uniform resist layer, considering that the pyramid openings in the surface impeded the flow of the resist during spinning. Finally, the wires are electroplated to make them thick enough to carry the required current. These processes are described in more detail in the next three sections.

A. Wafer Preparation and Pyramid Etch

The process begins with a 4-in 1-mm-thick silicon wafer cut on the {100} plane. This is given a standard Radio Corporation

of America (RCA)[1] and fuming-nitric-acid clean. A 170-nm-thick layer of silicon dioxide is grown by wet oxidation in a furnace at 1000 °C [Fig. 3(a)]. Subsequently, a 50-nm layer of low-stress silicon nitride is deposited on both sides by low-pressure chemical vapor deposition. A reactive ion plasma etch is then used to make alignment marks on the backside of the wafer for accurate positioning of all the masks used in the fabrication process.

In order to make the pyramids, a 1-μm layer of photoresist AZ6612 is spun onto the wafers. An array of square openings is patterned into the resist using a photomask on a Karl Suss MA8 contact mask aligner. The silicon nitride and dioxide layers are removed through these openings using a dry plasma etch, and the resist is then stripped in a plasma asher [Fig. 3(b)]. Before etching the silicon, the backside alignment marks are protected by depositing a layer of plasma-enhanced chemical vapor deposition (PECVD) silicon nitride 1 μm thick, and the wafer edges are protected by polytetrafluoroethylene tape. The wafer is then etched for 19 h in KOH at a concentration of 33% by volume and at a temperature of 80 °C. This produces pyramidal pits bounded by the four most slowly etched surfaces $\{1, 1, 1\}$, $\{\bar{1}, 1, 1\}$, $\{1, \bar{1}, 1\}$, and $\{\bar{1}, \bar{1}, 1\}$ [Fig. 3(c)]. The faces of the pyramids are very smooth because of the layer-by-layer etching mechanisms involved [17] and have been shown to have rms surface roughness as low as 0.5 nm [14]. The wafers are once again cleaned in a fuming-nitric-acid bath before the remaining silicon nitride is stripped from the front by a dry plasma etch and the remaining silicon dioxide is removed in a HF dip [Fig. 3(d)]. Finally, the whole front surface is covered with a plasma-enhanced tetraethyl orthosilicate (TEOS) oxide layer, 170 nm thick. This is to provide electrical insulation between the silicon and the metallic coating that comes next.

B. Metallic Coating and Flower Patterning

The metal coating consists of 50 nm of chromium and 100 nm of gold, evaporated onto the front of the wafer [Fig. 3(e)]. In order to make the flower pattern on the faces of the pyramids, we require them to be covered by a uniform layer of resist. Spinning the resist at this stage does not produce a uniform layer because of the large depth of the pyramidal pits. In order to avoid this problem, we use the electrophoretic deposition of Eagle 2100 negative photoresist. The wafer is placed in the resist bath and heated to 33 °C, where it acts as a cathode at −125 V. It remains in the bath until the current drops to zero, and then, it is rinsed in deionized water and dried in a vacuum oven at 65 °C. At this point, the resist remains tacky; hence, the wafer is dipped into Eagle 2002 topcoat for 30 s and again dried in the vacuum oven. This method leaves a highly uniform layer of resist over the complex topography [Fig. 3(f)].

Next, the wafer is exposed to ultraviolet light for 77 s at 6.5 mW/cm^2, using a mask designed to remove the gold from the type-3 regions. This pattern is developed using Eagle 2005 developer heated to 40 °C, which is sprayed onto the surface for 4 min. The wafer is then dipped for 1 min in water at 80 °C

[1]A standard set of wafer cleaning steps developed by Werner Kern at the RCA laboratories in the 1960s.
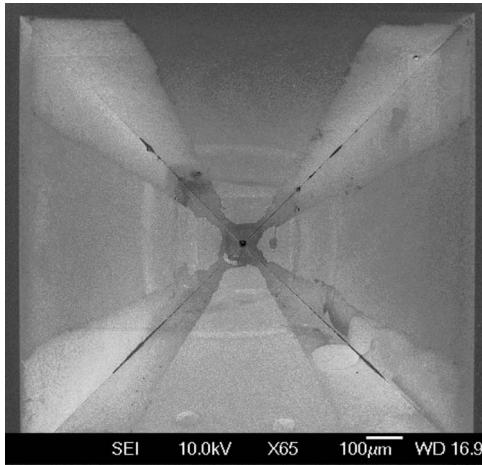
Fig. 4.   SEM image showing the flower pattern created on the sidewalls of all the pyramids.
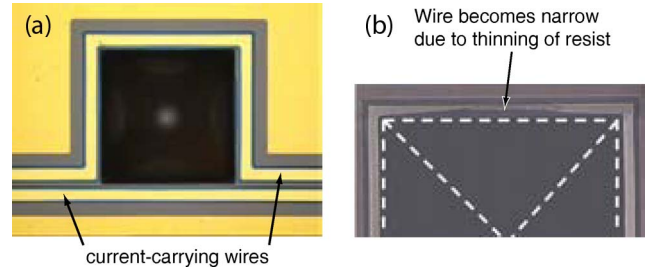

Fig. 5.   Optical microscope image of the wire tracks. (a) Wires are well formed around a 200-μm pyramid. (b) On the side furthest from the axis of spinning, the wire of a 1.2-mm pyramid is malformed because the resist was too thin.

to remove the resist residues and to smooth the surface of the resist. It is dried in a vacuum oven and descummed for 3 min in oxygen plasma at 110 °C [Fig. 3(f-i)].

The exposed gold and chromium are removed by a 35-s potassium iodide etch, followed by a 5-s chrome etch [Fig. 3(f-ii)]. The wafers are then sprayed for 15 min, to strip the resist, with Eagle 2007 remover at 50 °C, and placed in an asher for 1 h at 600 W and 110 °C [Fig. 3(f-iii)]. This process leaves a flower pattern on the gold inside each pyramid, as shown in Fig. 4. This scanning electron microscope (SEM) image shows that the gold has been removed in the diagonal and central regions corresponding to the type-2 and type-3 areas shown in Fig. 1(a). We found that it was difficult to achieve a uniform exposure of the resist inside the pyramid. When the lower part of the pyramid (near the apex) is correctly exposed, the upper part tends to be overexposed. The dark lines on the diagonals and the dark spot at the apex are due to residual resist. The color of the silicon surface appears darker at increasing depth in the pyramid. We attribute this to charging of the silicon dioxide surface by electron bombardment from the SEM.

C. Wire Fabrication

The final stage of fabrication is to form the wires around the base of each pyramid, as described in [18]. First, the tracks are patterned by optical lithography on the gold coating, and then, the wires are electroplated to provide the 3-μm thickness required for carrying the electrical current.

Once again, spinning a uniform layer of resist is very challenging since the radial flow is interrupted by the pyramid openings. To solve this problem, we use the viscous photoresist AZ4533, as follows. A primer is spun onto the wafer to help adhesion. Then, the wafer needs to be completely flooded with the resist before the spinning begins to ensure coverage inside pyramids and in the areas of the spin shadow just outside the pyramids. Spinning is carried out at 500 r/min for 10 s, followed by 30 s at 2000 r/min. We create a 5-μm layer of resist, which varies in thickness by approximately ± 3 μm where the pyramids interfere with the flow [Fig. 3(g)]. The uniformity of the resist improves substantially around pyramids that are

smaller than 1 mm, and impeccable wires are formed around the smallest pyramids, as shown in Fig. 5(a). However, the thinning of the photoresist in the spin shadow of the larger pyramids leads to overexposure and results in a thinning of the wire tracks there, as shown in Fig. 5(b).

A 6-μm-thick electroplating mold is then created by optical lithography of AZ9260, which is spun at 500 r/min for 8 s, followed by 30 s at 4000 r/min. This layer is exposed at 200 mW/cm^2 for 30 s to create the plating mold with a minimum thickness of 3 μm [Fig. 3(h)]. The electrochemical deposition is controlled by an Autolab PGSTAT30. We use a commercial cyanide-free gold-plating solution (Metalor Technologies UK Ltd., with 1 g of gold per liter of solution). A standard three-electrode setup is used with a platinum counter electrode. The deposition bath is placed in a water bath kept at 50 °C, and the solution is agitated throughout the deposition process using a magnetic stirrer. The current is fixed at 6 mA, corresponding to a current density of 5 mA/cm^2, and the plating is run for 15 min to achieve a 3-μm-thick gold deposit [Fig. 3(i)]. Finally, the resist is stripped to leave the free-standing gold wires.

Electrophoresis could potentially provide a solution to the problem of the thinning of the wires. However, it can only be used when pattering the wire tracks and not when creating the electroplating mold, since the Eagle 2100 resist can only cover areas previously covered with gold. For this reason, the fabrication of the wires was entirely designed and performed with the use of spin-on positive photoresists.

D. Packaging

Fig. 6 shows, on the right, an array of patterned pyramidal micromirrors with integrated current-carrying wires. The chip is fixed to a CPGA package (CPG18023, Spectrum Semiconductor Materials Inc.) using an epoxy compatible with ultrahigh vacuum (Bylapox 7285). Gold bond wires connect the package pins to the microfabricated chip wires, with nine bond wires serving each end of a chip wire. The view on the left of Fig. 6 shows the bond wires connecting the chip to the CPGA. The ceramic package is then plugged into a PGA of sockets, which, in turn, is soldered into an FR4 printed circuit board. This design permits a large number of connections to be made in the limited space available in the high-vacuum chamber.

We place the chip assembly in a stainless steel vacuum chamber where a 20-L/s ion pump yields a pressure below the
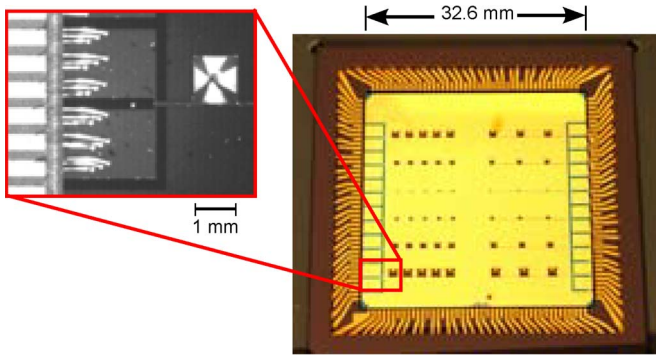
Fig. 6.   Photographs of the pyramid–MOT chip mounted in its CPGA package. (Right) Chip in its package. (Left) Detailed view of bond wires connecting the package to the chip wire pads and of a pyramid with the flower-patterned gold coating.

10^{-9} mbar limit of our gauge after modest baking at 100 °C for two days. At this low pressure, a trapped atom will remain undisturbed by the background gas for, typically, 10 s.

A stray magnetic field moves the zeros of magnetic field, which form the center of each MOT. To ensure that every pyramid encloses a field zero, we require the stray field to be less than 10 μT over the chip. Much stronger fields were initially found in the recess of the CPGA where the wafer is mounted, due to permanent magnetization of the nickel/gold coating. We therefore removed the coating by sandblasting. Immediately above the Kovar pins, there remained a stray field that reached a maximum of 10 μT; however, this was of short range and did not affect the 3 cm × 3 cm active area of the chip. There, the field was below 500 nT, the gradients were similarly negligible, and remagnetizing the assembly produced no perceptible change at that level.

IV. DEVICE CHARACTERIZATION

In this section we characterize the magnetic properties of our device, demonstrating that the microfabricated wires can carry sufficient current for magnetooptical and purely magnetic trapping. Measurements of the heating of our chip wires allow us to infer the maximum depth and gradient achievable in our trap. Finally, it is shown that the flower patterning of the pyramid coating leads to the desired suppression of the type-3 beams.

A. Magnetic-Field Measurements

We used a Hall probe (Lakeshore 421 Gaussmeter) to measure the field produced by a current of 480 mA around the 800-μm pyramid. Fig. 7(a) shows the result of a vertical scan along the axis of the pyramid, while Fig. 7(b) shows a horizontal scan through the center, at a height of 0.7 mm. The wires around the base of the pyramid almost form a square loop of wire 50 μm wide, centered on a 895-μm square, as shown in Fig. 5(a). In order to calculate the expected magnetic field, we approximated this by a fully closed square loop and integrated the field over the 750-μm square active area of the Hall probe, with the results shown as solid lines in Fig. 7(a) and (b). The measurement shows that the field is entirely as expected.
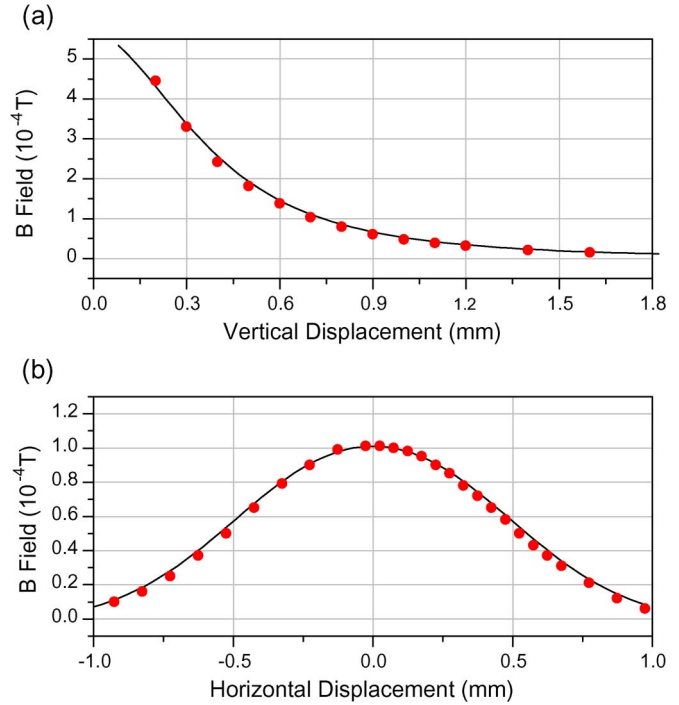

Fig. 7.   Vertical component of magnetic field above an 800-μm pyramid with 480 mA in the wire. (Dots) Hall probe measurement. (Lines) Theory. (a) Vertical variation along the pyramid axis. (b) Transverse variation parallel to the pyramid row, through the pyramid axis at a height of 0.7 mm.

B. Heating Tests

Although the gold wires are very good conductors, they, of course, dissipate electrical energy, and at sufficiently high currents, they blow like a fuse. Considerably below that limit, the wafer heats up to 120 °C. At this temperature, the epoxy used to bond the silicon to the CPGA begins to decompose, losing strength and outgassing strongly, thereby compromising both the mechanical stability of the chip and the high vacuum. This limiting temperature determines the largest current that we run through the wires and thereby limits the field and field gradient that are available.

With the chip mounted and placed under moderate vacuum (10^{-5} mbar), we first tested how much current could be passed through individual bond wires 50 μm in diameter and 2–3 mm in length. We found that these blow at approximately 1.8 A but can survive indefinitely at 1.5 A. Since each chip pad is normally connected by nine 50-μm-diameter wires in parallel, failure of the bond wires is not a limiting factor. In order to determine the operating currents for the chip wires, we monitored the temperature of the assembly at several points using thermocouples, and we monitored the temperature of the wire itself by measuring the increase of its resistance. Passing a current through the 50-μm-wide chip wires, we measured the time it takes for the wire to reach 120 °C, with the results being shown by the filled circles in Fig. 8. In all cases, the chip itself was much colder than the wire. Below 1 A, the temperature limit was never reached; however, at 1.3 A, the wire approached 120 °C in 10 s. For the 25-μm-wide wires, the operation was continuous below 0.5 A and was limited to 10 s at 0.75 A, as shown by the open squares in Fig. 8.
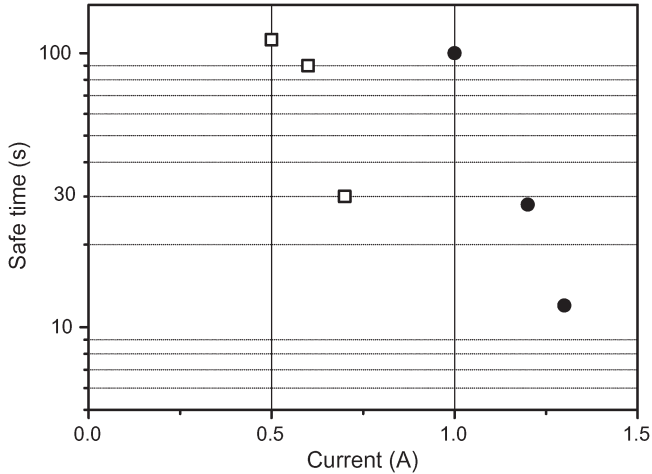
Fig. 8. Time taken for the chip wire temperature to reach 120 °C for various currents. (Filled circles) Fifty-micrometer-wide wires. (Open squares) Twenty-five-micrometer-wide wires.
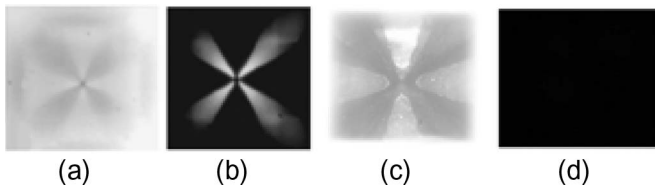

Fig. 9. Images of the pyramidal mirrors under a microscope, focused on the apex. (a) and (b) Unpatterned pyramids. (c) and (d) Patterned pyramids. (a) and (c) No polarizers. (b) and (d) Crossed polarizer and analyzer.

Since a suitable field gradient for the MOT is 0.15 T/m, the normal operating current is 5 mA for a 200-μm pyramid and 100 mA for a 1-mm pyramid. At these low currents, there is negligible heating of the chip. By contrast, the 1-mm loop needs to operate at 1 A if it is to make a purely magnetic trap for a 100-μK cloud of atoms. This cannot be sustained indefinitely, as shown in Fig. 8; however, substantially less than 1 s should suffice for most practical applications. Since the field scales as I/L, the situation is even better for purely magnetic trapping in the smaller loops.

In the course of these measurements, we found that the resistivity of the gold wire on the chip is 3.9×10^{-8} $\Omega \cdot$ m, approximately 1.6 times higher than that of bulk gold. This is typical of electrodeposited gold. The main consequence for us is a slightly higher power dissipation than we had anticipated in our design using the book value for the resistivity.

C. Optical Properties

Observation of the pyramids under a microscope allowed us to check that the type-2 and type-3 reflections were indeed eliminated by removal of the gold coating to create the flower pattern. Fig. 9(a) shows the image using unpolarized light, with the microscope focused on the apex of an unpatterned pyramid. In Fig. 9(a), most of the area is bright since the mirrors are reflecting light over the whole area of the pyramid. By contrast, Fig. 9(b) shows the same pyramid illuminated with linearly polarized light and viewed through a crossed polarizer, which suppresses all but the type-3 contribution, making the corner regions bright. Fig. 9(c) and (d) shows the corresponding
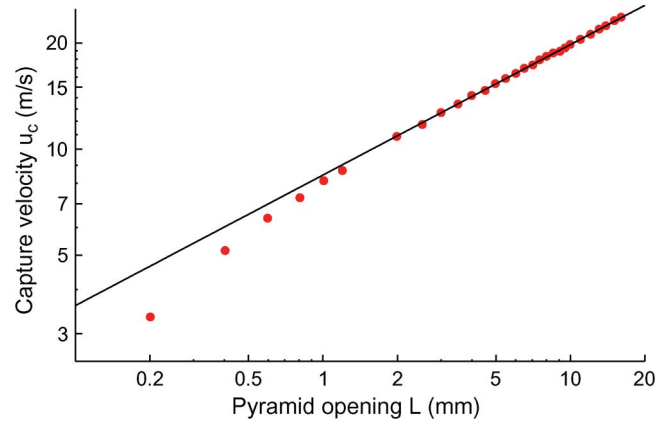

Fig. 10. Capture velocity versus the size of the pyramid opening. This is calculated by numerical integration using the model of [16].

images for a patterned pyramid. In Fig. 9(c), we see that there are no longer reflections near the apex of the pyramid, in the region of the type-2 rays. In Fig. 9(d), we see that the removal of the gold at the edges has completely suppressed the type-3 reflections.

V. OUTLOOK

It is useful to estimate the number of cold atoms that may be captured in one of these micropyramids. This will depend on the usual operating variables, such as the laser detuning from the atomic transition, the positioning of the magnetic-field zero, the balance of the light beams inside the pyramid, and the pressure of the atomic vapor. In addition, these pyramids are at the extreme limit of small laser beam size. Normally the laser beams of a MOT are 1 or 2 cm in diameter, whereas these pyramids are less than a millimeter across. Based on the well-established model first described by Lindquist *et al.* [16], the number of atoms N captured in a MOT is expected to scale as $N \propto L^2 u_c^4$. Here, the L^2 factor derives from the area of the laser beam, which, in our case, is set by the area of the pyramid opening. The quantity u_c is the capture velocity, i.e., the speed of the fastest atoms captured by the MOT from the thermal background vapor. Using the model of [16], we have computed u_c numerically, setting the maximum allowed stopping distance equal to the vertical height of the pyramid. The circles in Fig. 10 show the results on a log–log plot for a variety of pyramid sizes, with the laser detuning optimized separately to maximize u_c for each size. For pyramids larger than 1 mm, we find the empirical scaling law $u_c \propto L^{0.37}$, leading to the result $N \propto L^{3.48}$. When the pyramids are smaller than that, the atom number drops a little more rapidly. We have established in a previous experiment [14] that a 16-mm pyramid made from glass blocks can capture 10^8 atoms. With the help of this model, we extrapolate our 16-mm result to predict that a 1-mm pyramid will capture some 6×10^3 atoms. The smallest pyramids on this chip, having $L = 0.2$ mm, are expected by the same argument to collect approximately 25 atoms.

Although this model is a reasonable estimate, it neglects some aspects of the full 3-D geometry. For example, it assumes that the atoms of the vapor have the normal thermal distribution close to the walls of the pyramid, and it neglects the polarization

gradients in the laser field, which lead to additional Sisyphus cooling [19]. Experiment will have to determine how many atoms are actually captured. The number of atoms needed depends, of course, on the application. At one extreme, with an array of small clouds, each containing perhaps 10^4 atoms, the relative displacement of the clouds could provide a map of local magnetic-field variations or be used to sense inertial forces. At the other extreme, the pyramids could serve as single-atom sources for loading integrated optical cavities, which have recently been demonstrated [20]. This would permit the production of single photons on demand for applications in quantum information processing.

VI. SUMMARY

We have fabricated a silicon chip designed to trap cold atoms in an array of integrated MOTs. The device contains 48 micro-fabricated hollow micropyramids surrounded by electroplated gold wires. This was packaged into a CPGA, and the chip's optical and magnetic properties were tested. We found that the chip wires can easily sustain the currents needed to operate the MOTs and can even operate for many seconds at the much higher currents needed to trap atoms magnetically. The use of electrochemical deposition of photoresist allowed us to pattern a flower design on the reflective coating, a feature necessary for achieving the proper optical conditions in the MOTs. Numerical estimates show that we should be able to collect small but useful numbers of atoms in these traps, providing a simple way to feed arrays of devices on future chips. This represents an important integration step because atom chips currently have to be loaded from a single large cloud by a series of somewhat involved maneuvers.

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