Self-Aligned Silicidation of Surround Gate Vertical MOSFETs for Low Cost RF Applications

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***Abstract*—We report for the first time a CMOS-compatible silicidation technology for surround-gate vertical MOSFETs. The technology uses a double spacer comprising a polysilicon spacer for the surround gate and a nitride spacer for silicidation and is successfully integrated with a Fillet Local OXidation (FILOX) process, which thereby delivers low overlap capacitance and high-drive-current vertical devices. Silicided 80-nm vertical n-channel devices fabricated using 0.5-μm lithography are compared with nonsilicided devices. A source–drain (S/D) activation anneal of 30 s at 1100 °C is shown to deliver a channel length of 80 nm, and the silicidation gives a 60% improvement in drive current in comparison with nonsilicided devices. The silicided devices exhibit a subthreshold slope (S) of 87 mV/dec and a drain-induced barrier lowering (DIBL) of 80 mV/V, compared with 86 mV/dec and 60 mV/V for nonsilicided devices. S-parameter measurements on the 80-nm vertical nMOS devices give an f_T of 20 GHz, which is approximately two times higher than expected for comparable lateral MOSFETs fabricated using the same 0.5-μm lithography. Issues associated with silicidation down the pillar sidewall are investigated by reducing the activation anneal time to bring the silicided region closer to the p-n junction at the top of the pillar. In this situation, nonlinear transistor turn-on is observed in drain-on-top operation and dramatically degraded drive current in source-on-top operation. This behavior is interpreted using mixed-mode simulations, which show that a Schottky contact is formed around the perimeter of the pillar when the silicided contact penetrates too close to the top S/D junction down the side of the pillar.**

***Index Terms*—Fillet Local OXidation (FILOX), interface states, silicidation, vertical MOSFETs (v-MOSFETs).**

I. Introduction

THIN-PILLAR fully depleted surround-gate vertical MOSFETs (v-MOSFETs) are being researched as candidates for end-of-roadmap CMOS technology [1]–[4]. The advantages of these devices stem from their excellent electrostatic control, the resulting short-channel effect (SCE) immunity, and high drive current. Better SCE immunity also allows the use of low-doped/undoped channels, which improves carrier transport properties (mobility) and reduces dopant fluctuation problems. Scaling the pillar thickness in the fully depleted regime has been shown to deliver excellent subthreshold and drain-induced barrier lowering (DIBL) characteristics, although the expected improvement in drive current has only been demonstrated for pillar diameters of less than 20 nm, where a very strong volume inversion exists in the channel [1], [2]. However, these devices usually require aggressive electron beam lithography and/or complex processing [1]–[4], and so far, no silicidation technology has been reported for these devices.

Thick-pillar surround-gate v-MOSFETs are also of interest [5]–[17] because they can easily be integrated into a mature CMOS technology to provide a low-cost route to radio-frequency (RF) transistors. Thick-pillar surround-gate v-MOSFETs have several obvious advantages over planar MOSFETs. First, surround-gate structures allow more channel width and drive current per unit silicon area. Second, the channel length is controlled by nonlithographic methods, allowing the devices with sub-100-nm channel length to be realized without any advanced lithography. Hence, the advantages of short-channel transistors can be enjoyed without costly processing. Third, co-integration of surround-gate v-MOSFETs and conventional planar MOSFETs can easily be achieved due to the bulk silicon starting material. However, v-MOSFETs have several important disadvantages, i.e., high overlap capacitance, dry etch damage on the pillar sidewall, and lack of an appropriate silicidation technology. The problem of overlap capacitance has been addressed using Fillet Local OXidation (FILOX) [15], [16]. In this process, a thicker oxide is grown at the bottom and top of the active pillar using nitride spacer to suppress oxidation on the pillar sidewall. The thick FILOX oxide reduces the overlap capacitance between the gate and the source/drain (S/D) electrodes. Dry etch damage occurs during pillar dry etch and polysilicon gate etch, and degrades the subthreshold slope. Damage occurring during pillar dry etch can be eliminated by sacrificial oxidation, and we have recently shown how the device architecture and the FILOX process [15] can be optimized to eliminate dry etch damage during silicon gate etch and deliver excellent values of subthreshold slope [18], [19]. However, to date, there have been no reports in the literature on silicidation technologies for surround-gate v-MOSFETs. Self-aligned silicidation is one of the key features

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of advanced MOSFETs, which reduces S/D series resistances and increases the drive current, and hence is essential for RF applications.

We recently reported preliminary results on silicided v-MOSFETs [20] and showed that a subthreshold slope degradation and drive current asymmetry in silicided devices could be eliminated by using a frame-gate architecture [18]. In this approach, a frame of polysilicon is incorporated around the perimeter of the pillar, which unfortunately has the disadvantage of increasing the overlap capacitance. In this paper, we show that excellent values of subthreshold slope can be achieved in silicided devices without resorting to a frame gate. A double spacer is implemented, comprising a polysilicon spacer for the surround gate and a nitride spacer for the silicidation, and excellent values of subthreshold slope are achieved by optimizing the FILOX process and S/D anneal. The silicided 80-nm n-channel devices deliver a 60% improvement in drive current in comparison to nonsilicided devices, an excellent subthreshold slope of 87 mV/dec, and a DIBL of 80 mV/V. The RF performance of the v-MOSFETs is characterized, and issues with the silicidation down the pillar sidewall are investigated.

II. Experimental Procedure

A mature 0.5-μm CMOS technology was used to fabricate v-MOSFETs. Boron-doped (0.75–1.25 $\Omega \cdot$ cm) (100) wafers were taken as the starting material, and a p-type body was formed by boron implantation ($2 \times 10^{14}/\text{cm}^2$, 100 keV, 7° tilt) and high-temperature drive-in. Transistors with different channel lengths were then produced by varying the Si pillar dry etch, with pillar heights varying from 300 to 450 nm. A sacrificial oxidation was performed to eliminate dry etch damage and reduce the surface roughness on the pillar sidewall. After stripping of this oxide, a 10-nm stress relief oxide was thermally grown at 900 °C. For the FILOX process [15], a 90-nm silicon nitride was deposited at 720 °C and anisotropically etched to create a nitride spacer; subsequently, a 60-nm FILOX oxide layer was thermally grown at 1100 °C [Fig. 1(a)].

The source and drain were then implanted using a single 3×10^{15} cm^{-2} 110-keV As implant at 7° tilt, and the nitride fillet and pad oxide were subsequently removed by wet etch. A 2.8-nm gate oxide was then grown at 700 °C, and a 230-nm *in situ* phosphorous-doped $(1 \times 10^{20}/\text{cm}^3)$ polysilicon gate was deposited and patterned by dry etch to create a surround gate. A rapid thermal annealing (RTA) at 1100 °C for 10 or 30 s was then performed for dopant activation, which resulted in different junction depths and, hence, different channel lengths for the same pillar height. In the silicided wafers, the underlying FILOX oxide was also removed by dry etch just after the gate etch. A 20-nm oxide layer and an 80-nm nitride layer were then deposited, and subsequently, the nitride layer was dry etched to leave nitride spacers over the polysilicon fillet around the pillar sidewall [Fig. 1(b)].

After a brief hydrofluoric acid (HF) dip etch, a 20-nm Ni layer was deposited by e-beam evaporation. A silicide layer was formed by annealing for 30 s at 450 °C, and unreacted Ni was removed using a piranha solution. In this way, the S/D regions and the horizontal portions of the polysilicon gate were silicided [Fig. 1(c)]. A 300-nm LTO layer was used as a passivation layer, and contacts and metal were defined.

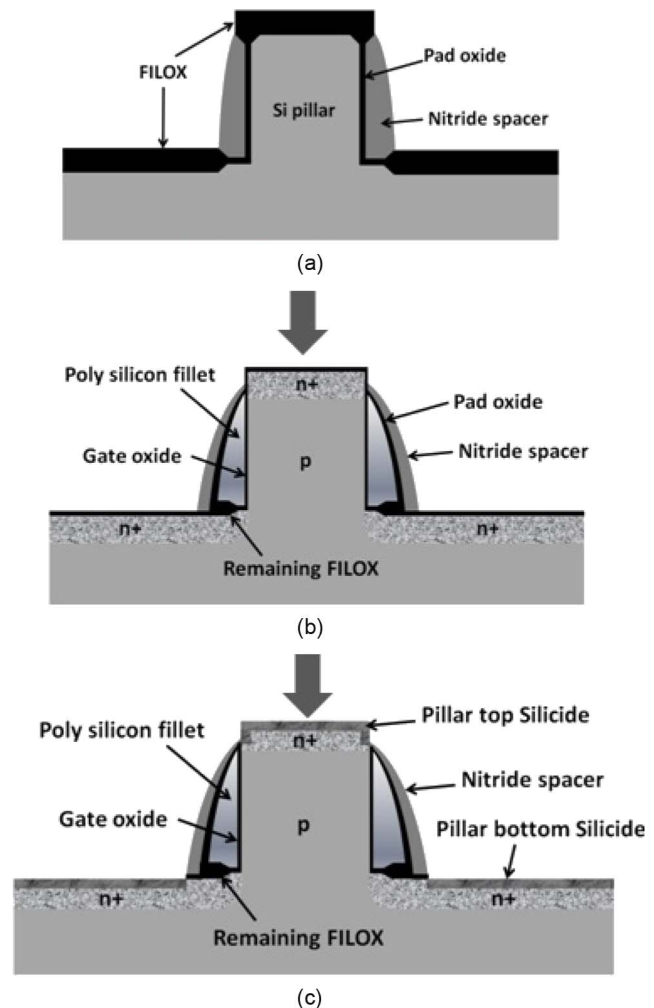

Fig. 1. Schematic process flow for silicidation of surround-gate v-MOSFETs. (a) FILOX process [15], [16]. (b) Nitride spacer process for silicidation. (c) Silicided v-MOSFETs.

The gate oxide thickness was measured from the second derivative of the high-frequency capacitance/voltage characteristic [21], and a value of 2.8 nm was obtained. The body doping was also extracted from this measurement, and a value of $1 \times 10^{18}/\text{cm}^3$ was obtained. A similar method was used to measure the FILOX oxide thickness at the end of the process, and a value in the range of 35–40 nm was obtained. S/D sheet resistances were measured from Van der Pauw structures; values of 32 and 42 Ω/sq were obtained for 30- and 10-s anneals in nonsilicided wafers, and 7 Ω/sq were obtained in silicided wafers. The channel length L was obtained from measurements of the pillar heights using cross-sectional scanning electron microscope (SEM) and measurements of the junction depths by stain etching in a HF : HNO_3 : CH_3COOH, 1:3:8 for 5–10 s [22]. For a 10-s RTA at 1100 °C, channel lengths of 120, 170, and 220 nm were obtained for pillar heights of 350, 400, and 450 nm, respectively. For a 30-s RTA at 1100 °C, a channel length of 80 nm was obtained. We also extracted the channel length by gate-channel capacitance C_{GC} measurements [23] and the drain conductance method [24]. The

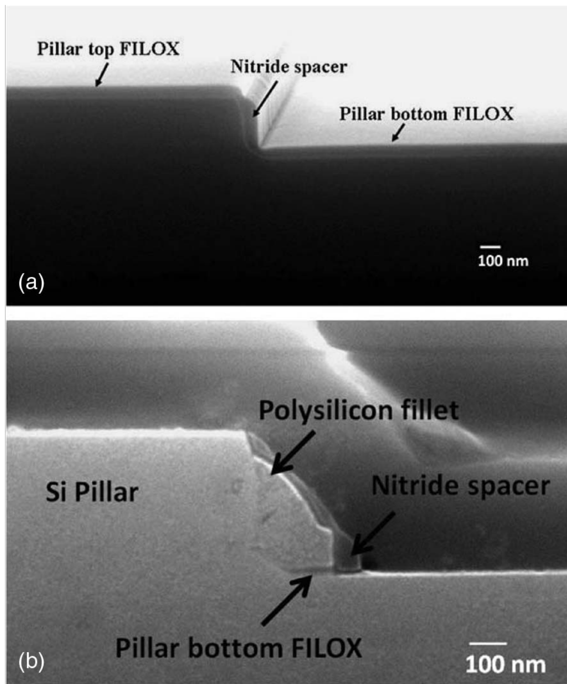

Fig. 2. SEM cross section of the v-MOSFET process (a) directly after the FILOX [15], [16] oxidation and (b) after the nitride spacer process prior to silicidation.

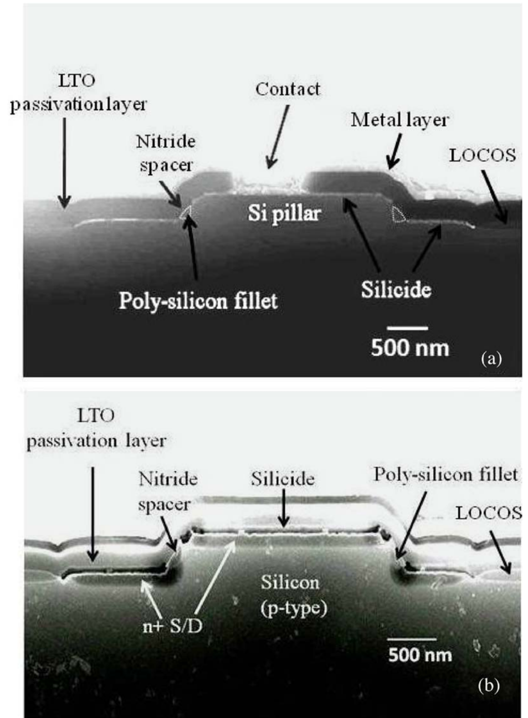

Fig. 3. SEM cross section of a 120-nm v-MOSFET after silicide formation (a) without any etch and (b) after stain etching [22]. The outline of the sidewall polysilicon fillet has been highlighted in (a) for clarity.

extracted channel lengths by these measurements were in good agreement with the preceding results. Both dc and ac transistor characterizations were performed from on-wafer measurements using a Cascade semiautomatic Summit 12000B-AP probe station. DC measurements were performed using an Agilent B1500A semiconductor device analyzer, and ac electrical data was acquired from S-parameter measurements using an Agilent 8361A microwave vector network analyzer. The parasitics were de-embedded from the S-parameter measurements using open, short, load, and through structures.

III. Results

A. Process Characterization

A SEM cross section of the transistor immediately after the FILOX process is shown in Fig. 2(a). The figure clearly shows the 70-nm nitride spacer and the presence of the FILOX oxide at the top and bottom of the pillar. The thickness of the FILOX oxide is 60 nm, in agreement with expectations. Oxide encroachment of 75 nm can be seen at the pillar top, but there is no such encroachment at the pillar bottom. Fig. 2(b) shows a SEM micrograph after the formation of the nitride spacer on the polysilicon surround gate ready for silicidation. The successful processing of the nitride spacer on the polysilicon gate can be clearly seen. The nitride spacer and polysilicon gate have thicknesses of 70 and 200 nm, respectively, at the pillar bottom.

Fig. 3(a) shows a SEM cross section of a 120-nm v-MOSFET after silicide formation. A 45-nm-thick continuous silicide layer can be easily seen at the pillar top and bottom. The silicided surface is rather rough due to the polycrystalline grains formed during the silicidation process. Furthermore, silicidation down the pillar sidewall can be observed, which is found to be around 190 nm down from the pillar top. Fig. 3(b) shows the SEM cross section at the same stage of the process but after a delineation etch [22] that has been used to stain the p-n junction. The silicided regions and the S/D junctions can be easily seen from this image, although the nickel silicide has been etched by the HF in the stain etch. The junction depth is around 200 nm, and from the 190-nm extension of the silicide layer down the pillar sidewall, which was measured from Fig. 3(a), the silicided region extends to within 5–15 nm of the top p-n junction. At the pillar bottom, the silicide layer is 250–270 nm away from the bottom p-n junction in the horizontal direction. Similar experiments on 80-nm v-MOSFETS gave a top p-n junction depth of 240 nm and extension of the silicide layer to within 45–55 nm of the top p-n junction.

B. DC Electrical Characteristics

Fig. 4 shows typical output characteristics of 80-nm v-MOSFETs for drain-on-top (DOT) and source-on-top (SOT) modes of operation. Results are shown for (dashed line) silicided and (solid line) nonsilicided v-MOSFETs. For the DOT mode of operation, Fig. 4(a) shows a drive current of 400 $\mu A/\mu m$ for silicided devices at a gate voltage overdrive of 1 V and a V_{DS} of 1.5 V, which compares with a value of 250 $\mu A/\mu m$ for nonsilicided devices. The silicidation has therefore delivered a 60% improvement in drive current for the DOT mode of operation. Fig. 4(b) shows the equivalent results for the SOT mode of operation, and drive currents of 385 and 255 $\mu A/\mu m$ are obtained for silicided and nonsilicided devices, respectively. For SOT operation, silicidation has delivered a 51% improvement in drive current. Measurements were made

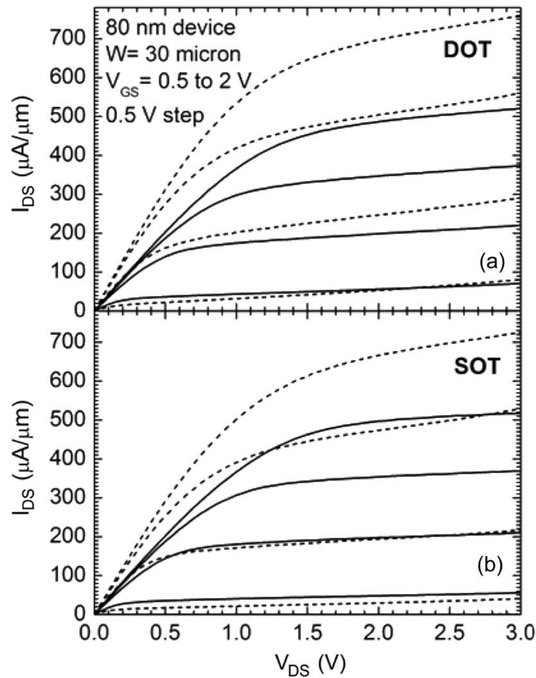

Fig. 4. Output characteristics of 80-nm v-MOSFETs annealed for 30 s at 1100 °C for (a) DOT and (b) SOT modes of operation. Results are shown for (dashed line) silicided and (solid line) nonsilicided v-MOSFETs.

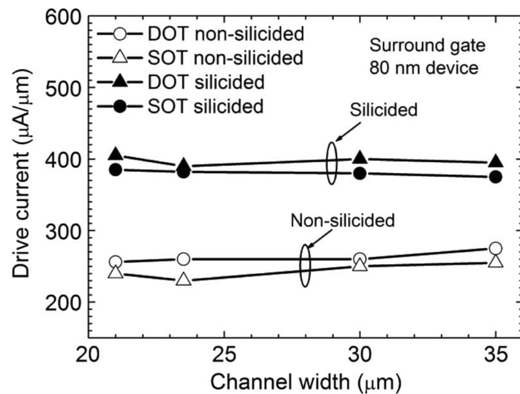

Fig. 5. Drive current (i.e., for a gate voltage overdrive of 1 V and a V_{DS} of 1.5 V) of 80-nm surround-gate v-MOSFETs for different drawn channel widths. Results are shown for silicided and nonsilicided v-MOSFETs and for DOT and SOT modes of operation.

on v-MOSFETs with a variety of different channel widths, and a similar behavior was observed (Fig. 5). For example, for v-MOSFETs with a channel width of 21 μm, silicidation gave 65% and 51% improvements in the drive current for DOT and SOT modes of operation, respectively. This result indicates that the characteristics of these v-MOSFETs are rather symmetrical.

Fig. 6 shows the effects of silicidation on the subthreshold characteristics of 80-nm v-MOSFETs. The silicided and non-silicided devices exhibit almost identical values of subthreshold slope, with values of 87 and 86 mV/dec, respectively. However, there are small differences in the values of DIBL (80 and 60 mV/V) and threshold voltage (0.34 and 0.23 V) for silicided and nonsilicided devices, respectively. Measurements on 120-nm v-MOSFETs (not shown) gave a smaller degradation of the subthreshold slope after silicidation from 78 to 85 mV/dec. The 120-nm v-MOSFETS also showed a 0.17-V increase in the threshold voltage after silicidation. The OFF-state leakage for both silicided and nonsilicided devices increases gradually with increasing negative gate bias in Fig. 6 due to gate-induced drain leakage and gate leakage. Measurements have shown that the gate leakage originates from the bottom of the pillar and is presumably due to the thinning of the gate oxide at the bottom corner. We have seen much lower values of OFF-state leakage in some of our FILOX v-MOSFETs [18], [19], indicating that the leakage current can be significantly reduced by optimizing the FILOX process. For example, a thinner nitride spacer will allow the FILOX oxide to encroach further around the bottom of the pillar, thereby thickening the oxide at the bottom corner.

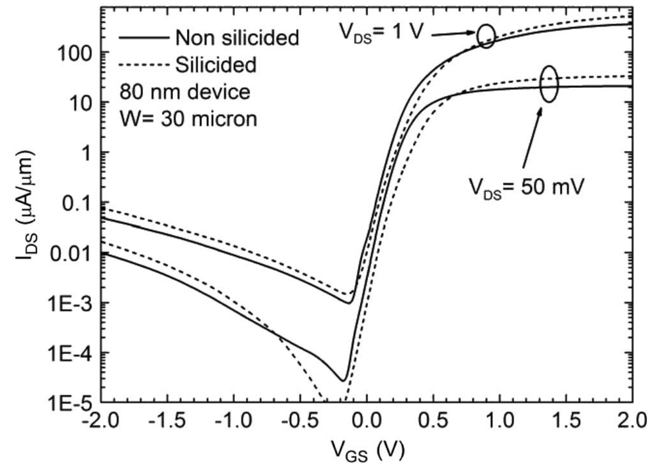

Fig. 6. Subthreshold characteristics of 80-nm v-MOSFETs annealed for 30 s at 1100 °C. Results are shown for silicided and nonsilicided v-MOSFETs.

To investigate the effects of silicidation down the pillar sidewall, Fig. 7 shows the output characteristics of transistors (120-nm channel length), which have been given a shorter anneal of 10 s at 1100 °C. For DOT operation, Fig. 7(a) shows drive currents for a gate voltage overdrive of 1 V and a V_{DS} of 1.5 V of 240 and 180 μA/μm for silicided and nonsilicided transistors, respectively, indicating a 30% improvement. However, below $V_{DS} = 1$ V, a nonlinear transistor turn-on can be seen in the characteristic of the silicided device. For SOT operation, Fig. 7(b) shows that the silicided transistors surprisingly have a much lower drive current than the nonsilicided transistors, with values of 55 and 170 μA/μm, respectively.

C. AC Electrical Characteristics

Fig. 8 shows the gate–S/D capacitances $C_{\mathrm{GS/D}}$ at the pillar top and pillar bottom as a function of gate voltage. Measurements were made on test structures with an array of 500 transistors connected in parallel, and the parasitic interconnect capacitances were decoupled by measurements on dummy metal line structures. The measured capacitances in accumulation represent overlap capacitances, whereas measured capacitances in inversion represent the sum of overlap and gate-channel capacitances. It is observed that FILOX vertical transistors exhibit pillar top and pillar bottom overlap capacitances $C_{\mathrm{GS/D}}$ of 1.1 and 2.25 fF/μm, respectively. For a 0.5-μm technology node, planar MOSFETs have an overlap capacitance around 1 fF/μm when estimated for a gate oxide thickness of

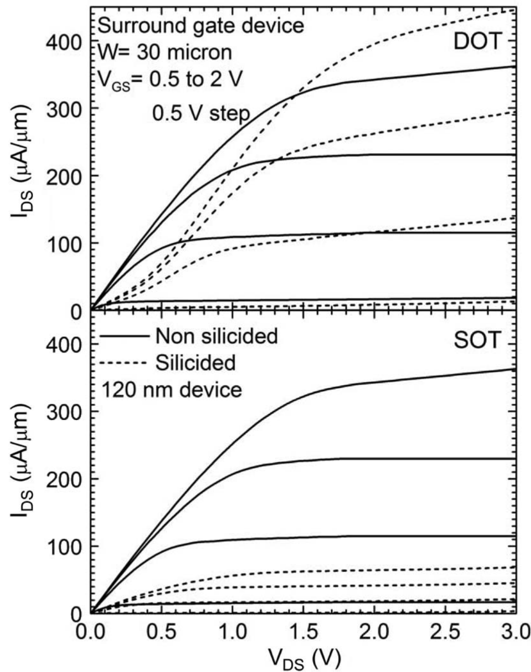

Fig. 7. Output characteristics of 120-nm surround-gate v-MOSFETs annealed for 10 s at 1100 °C for DOT and SOT modes of operation. Results are shown for silicided and nonsilicided v-MOSFETs.

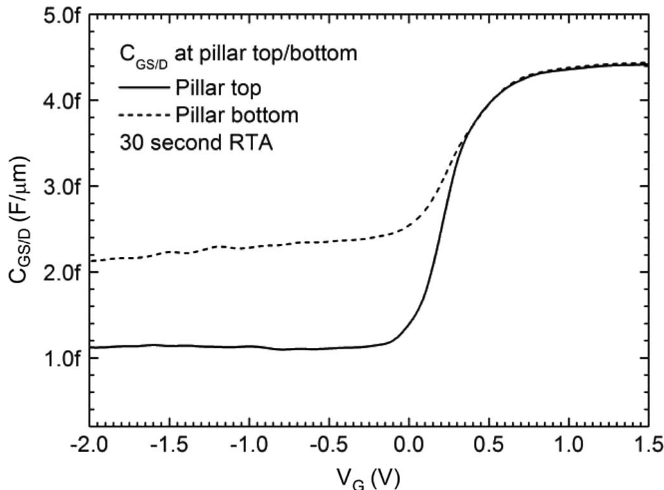

Fig. 8. Gate–S/D capacitances $C_{\mathrm{GS/D}}$ at the pillar top and bottom as a function of gate voltage for surround-gate FILOX v-MOSFETs. These devices have a channel length of 80 nm and were annealed for 30 s at 1100 °C.

2.8 nm [25]. This indicates that FILOX v-MOSFETs exhibit a similar value of overlap capacitance at the top of the pillar to comparable planar MOSFETs. This is achieved by using a thick FILOX oxide and a significant polysilicon fillet overetch (∼170 nm from the pillar top as calculated from Fig. 3), thereby reducing the overlap between the polysilicon gate and the top p-n junction. However, the pillar bottom overlap capacitance is twice that of a comparable 0.5-μm planar MOSFET. This is due to the use of a thick polysilicon surround gate (∼200 nm) that creates a large overlap at the pillar bottom. The pillar bottom overlap capacitance can be easily optimized by reducing the polysilicon gate thickness, increasing the FILOX thickness, or reducing the FILOX nitride spacer thickness.

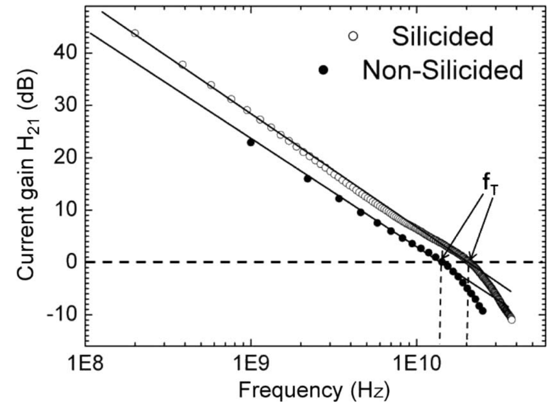

Fig. 9. Current gain as a function of frequency for surround-gate FILOX v-MOSFETs with and without silicidation. The silicided v-MOSFETs have a channel length of 80 nm, and the nonsilicided v-MOSFETs have a channel length of 70 nm. The 20-dB/dec lines are shown for illustration. The devices had a channel width of 30 μm, and the measurements were made at biases of $V_{GS} = 0.75$ V and $V_{DS} = 1$ V.

Fig. 9 shows the current gain as a function of frequency for silicided and nonsilicided v-MOSFETs. For the silicided v-MOSFET, a cutoff frequency f_T of around 20 GHz has been achieved, which compares with a value of 14.6 GHz for the nonsilicided v-MOSFET. This 6-GHz improvement in f_T has been achieved by reducing the S/D series resistances using the aforementioned silicidation process. It should be noted that this improvement in f_T has been achieved, even though the silicided v-MOSFET has a slightly longer measured channel length (80 nm) than the nonsilicided v-MOSFET (70 nm).

IV. Discussion

The preceding results have shown that a silicidation technology has been successfully developed for 80-nm v-MOSFETs. The silicidation gives a 60% improvement in drive current, and the output characteristics are symmetrical in SOT and DOT modes of operation. A drive current of 400 μA/μm has been achieved, which is significantly higher than previous results reported in the literature, as shown in Table I [5]. Furthermore, the AC results in Fig. 9 show that an f_T of 20 GHz has been achieved in the silicided 80-nm v-MOSFETs, which represents an excellent outcome for a technology that only used 0.5-μm lithography. To investigate how this performance compares with that achieved for conventional lateral MOSFETs at the same 0.5-μm lithography node, Fig. 10 plots f_T as a function of technology node for a variety of conventional planar RF technologies taken from [26]. It can be seen that our 80-nm silicided v-MOSFET delivers a significantly higher f_T than comparable planar MOSFET technologies implemented using the same 0.5-μm lithography. We have also estimated the peak transconductances G_M of silicided devices from Fig. 6, and these were found to be 1.4×10^{-3} and 1.2×10^{-2} A/V for $V_{DS} = 0.05$ and 1 V, respectively. These G_M values are noticeably better than those reported for planar MOSFETs with comparable 0.5/0.7-μm channel lengths [27], [28] and better than the 0.18-μm planar MOSFET reported in [29]. It can therefore be concluded that v-MOSFETs offer a viable route for improving the RF performance of mature lateral CMOS

TABLE I

COMPARISON OF SILICIDED SURROUND-GATE v-MOSFETs FABRICATED IN THIS WORK WITH DEVICES REPORTED IN THE LITERATURE. THESE DATA WERE TAKEN FROM [5] AND UPDATED WITH MORE RECENT RESULTS. THE VALUES OF I_{on} WERE CALCULATED FOR $V_{DS} = V_{DD}$ AND FOR A 1-V GATE OVERDRIVE. TO ENSURE A MEANINGFUL COMPARISON, FULLY DEPLETED THIN-PILLAR v-MOSFETs HAVE BEEN EXCLUDED FROM THE TABLE, BECAUSE IMPROVED DRIVE WOULD BE EXPECTED FROM THESE DEVICES DUE TO THE VOLUME INVERSION FROM THE ACTION OF THE DUAL OR SURROUND GATES

Parameter	L (nm)	t_{ox} (nm)	N_A (10^{17}/cc)	V_{DD} (V)	Ion (μA/μm)	S (mV/dec)	DIBL (mV/V)
Schulz et al [5]	100	3	20	1.5	240	102	70
Schulz et al [5]	50	3	70	1.5	80	166	300
VRG [13]	100	2.8	35	1.5	140	90	30
VRG [13]	50	2.8	35	1.5	100	105	90
Mori et al [11]	100	7	20	1.5	160	100	73
Gili et al [16]	125	3	40	1.5	127	107	80
Previous report [18]	100	2.6	10	1.5	160	70-80	30-35
Surround gate (non-silicided)	120	2.8	10	1.5	180	78	20
Surround gate (Silicided)	**120**	**2.8**	**10**	**1.5**	**240**	**85**	**40**
Surround gate (non-silicided)	80	2.8	10	1.5	250	86	60
Surround gate (Silicided)	**80**	**2.8**	**10**	**1.5**	**400**	**87**	**80**

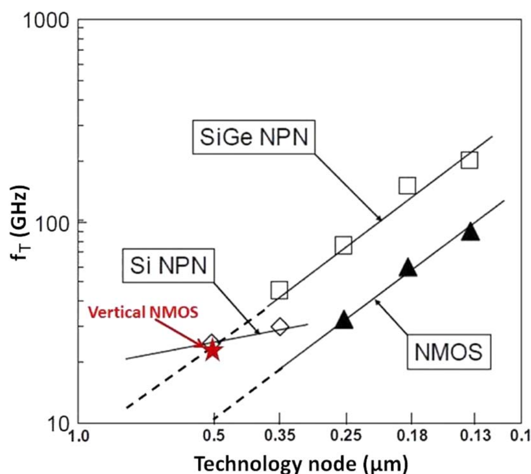

Fig. 10. Cut-off frequency f_T as a function of technology node for the silicided 80-nm surround-gate FILOX v-MOSFET and a variety of comparator technologies taken from [26].

technologies at the cost of only one additional mask for pillar dry etch.

The results in Fig. 7 show a dramatic degradation in the dc performance of the silicided v-MOSFETs when the anneal time is reduced to bring the silicided region closer to the top S/D junction. As previously discussed, the 30-s anneal used for the 80-nm v-MOSFETs locates the silicide layer 45–55 nm from the top S/D junction, whereas the 10-s anneal used for the 120-nm v-MOSFETs reduces this distance to 5–15 nm. SIMS analysis on the v-MOSFET with a 10-s anneal gave a doping concentration of $4 \times 10^{20}/\text{cm}^3$ near the pillar top, which dropped to around $1 \times 10^{18}/\text{cm}^3$ at the edge of the silicide. NiSi work functions (WFs) are known to vary with doping, and in heavily doped silicon, silicidation-induced submonolayer segregation of dopants causes a change in the apparent WF [27]. In low-doped Si, NiSi has a WF of around 0.56–0.67 eV [30], [31], whereas, in high-doped silicon, this reduces to a value of around 0.31 eV [30]. This reasoning suggests that silicidation could lead to the formation of a Schottky barrier on the pillar sidewall close to the top S/D junction, which could explain the nonlinear turn on and asymmetry observed in the output characteristic of the silicided v-MOSFET in Fig. 7(a).

To confirm this hypothesis, ATLAS mixed-mode simulations were performed, incorporating numerical models for a Schottky diode and the v-MOSFET. In these simulations, the drain–source current entering the top S/D from the channel sees two conduction paths in parallel [inset in Fig. 11(a)]. One is through the bulk junction and into the NiSi ohmic contact on top of the pillar. The other is along the sidewall surface and into the Schottky NiSi contact on the sidewall of the pillar. The total drain–source current collected at the drain is therefore the sum of these two currents. In simulations, the quantum mechanical tunneling and the thermionic emission models were both turned on. In order to reproduce the measured current drive, arbitrary series resistors (not shown) were introduced into the Schottky and the ohmic conduction paths, and the barrier height was set to a value that reproduced the onset of turn-on in the measured I_{DS}–V_{DS} characteristics.

The simulated output characteristics for both DOT and SOT operations are shown in Fig. 11 for 2-V gate bias. In DOT operation, at low values of V_{DS}, the current along the pillar sidewall is limited by the Schottky contact, and hence, the total current is dominated by the path through the bulk junction to the ohmic contact on top of the pillar. However, once the Schottky diode turns on, the current along the pillar sidewall

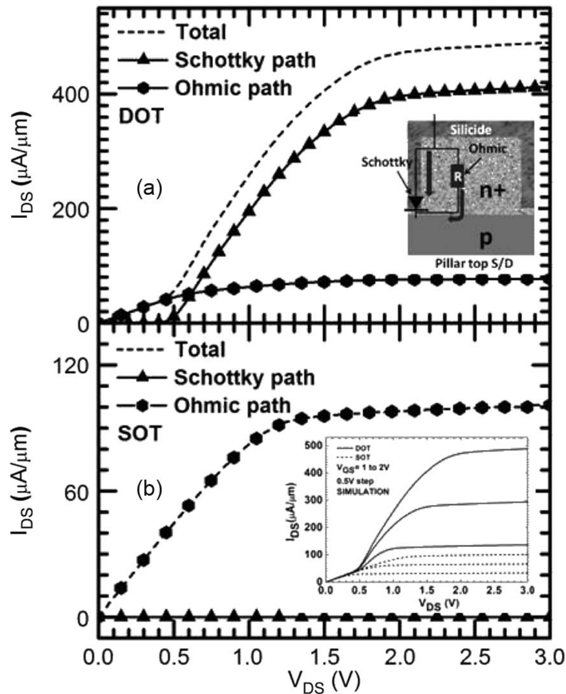

Fig. 11. Simulated output characteristics of the 120-nm silicided surround-gate v-MOSFETs annealed for 10 s at 1100 °C. (a) DOT operation and (b) SOT operation under a gate bias of 2 V. Results are shown for two current paths through the device, a surface current through a peripheral Schottky contact, and a bulk current to the top ohmic contact. The inset of (b) shows the total current in DOT and SOT operation.

is significantly larger than that through the bulk junction and therefore dominates the total current. In SOT operation, the Schottky diode is reverse biased, so conduction along the pillar surface is completely blocked and the total current is dominated by conduction through the bulk junction. Hence, no nonlinear turn-on is seen at low V_{DS}, and the drive current is very low due to a relatively larger resistance expected in the bulk junction conduction path. The total drain–source current in DOT and SOT operation is shown in the inset of Fig. 11(b), and it can be seen that this characteristic successfully reproduces the main features of the measured results in Fig. 7. This analysis confirms that the observed nonlinear turn-on and asymmetrical drive current seen in Fig. 7 are due to the close proximity of the silicidation to the top S/D junction. To characterize the effect of different anneal conditions on this behavior, we have simulated different RTA times using the ATHENA process simulator using measured SIMS profiles to calibrate the simulations. These simulations show that the optimum RTA is around 22 s at 1100 °C, which places the NiSi interface 35 nm from the channel and gives a silicidation tip doping density of around $10^{19}/\mathrm{cm}^3$, which is sufficient for an ohmic contact.

Finally, we discuss the degradation of the subthreshold slope from 78 to 85 mV/dec in the silicided 120-nm v-MOSFETs and the general trends of threshold voltage shift and DIBL degradation after silicidation. The small degradation in subthreshold slope suggests the presence of interface states, presumably due to the proximity of the silicided region to the top S/D junction. To further investigate this possibility, we have estimated the increase in the interface state density ΔN_{it} and oxide charge ΔN_{ot} after silicidation for 80- and 120-nm v-MOSFETs using the change in subthreshold slope and shift of midgap voltage, respectively, [32]. For 80- and 120-nm v-MOSFETs, the values of ΔN_{it} are found to be $6 \times 10^{11}/\mathrm{cm}^2$ and $1.3 \times 10^{12}/\mathrm{cm}^2$, and the values of ΔN_{ot} are found to be $2 \times 10^{11}/\mathrm{cm}^2$ and $1.9 \times 10^{11}/\mathrm{cm}^2$, respectively. The twice higher ΔN_{it} in the 120-nm v-MOSFET, compared with the 80-nm v-MOSFET, clearly shows that the closer proximity of the silicidation region to the top S/D junction favors the creation of interface states in the channel. Furthermore, the positive shift of the subthreshold plots in silicided devices indicates that these interface states are acceptorlike, which also agrees with a study of Ni irradiation-induced modifications of nMOSFETs done by Shinde *et al.* [33]. A similar reasoning can be used to explain the DIBL degradation after silicidation, as we have discussed in previous work [19].

V. Conclusion

We have reported a CMOS-compatible silicidation technology for surround-gate v-MOSFETs, which is integrated with a FILOX process, delivering low-overlap-capacitance and high-drive-current vertical devices. Silicided 80-nm vertical n-MOSFETs show an excellent drive current improvement in comparison to nonsilicided devices, with improvements of 60% and 51% for DOT and SOT operations, respectively. The silicided devices also exhibit an excellent subthreshold slope of 87 mV/dec and a DIBL of 80 mV/V, compared with 86 mV/dec and 60 mV/V for nonsilicided devices. The silicided 80-nm v-MOSFETs have an f_T of 20 GHz, which is approximately twice the value expected for comparable planar MOSFETs fabricated using the same 0.5-μm lithography. This result demonstrates the promise of v-MOSFETs as a route for improving the RF performance of mature CMOS technologies. We have also investigated issues associated with silicidation down the pillar sidewall by reducing the activation anneal time to bring the silicided region closer to the p-n junction at the top of the pillar. In this situation, nonlinear transistor turn-on is observed in DOT operation and dramatically degraded drive current in SOT operation. These results have been explained by the formation a Schottky contact around the pillar perimeter when the silicided region comes too close to the top S/D junction.

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References

[1] M. Masahara, Y. Liu, S. Hosokawa, T. Matsukawa, K. Ishii, H. Tanoue, K. Sakamoto, T. Sekigawa, H. Yamauchi, S. Kanemaru, and E. Suzuki, "Ultrathin channel vertical DG MOSFET fabricated by using ion-bombardment-retarded etching," *IEEE Trans. Electron Devices*, vol. 51, no. 12, pp. 2078–2085, Dec. 2004.

[2] H. Cho, P. Kapur, P. Kalavade, and K. C. Saraswat, "A low-power, highly scalable, vertical double-gate MOSFET using novel processes," *IEEE Trans. Electron Devices*, vol. 55, no. 2, pp. 632–639, Feb. 2008.

[3] B. Yang, K. D. Buddharaju, S. H. G. Teo, J. Fu, N. Sing, G. Q. Lo, and D. L. Kwong, "CMOS compatible gate-all-around vertical silicon-nanowire MOSFETs," in *Proc. 38th ESSDERC*, 2008, pp. 318–321.

[4] H. Liu, Z. Xiong, and J. K. O. Sin, "An ultrathin vertical channel MOSFET for sub 100 nm applications," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1322–1327, May 2003.
[5] T. Schulz, W. Rösner, L. Risch, A. Korbel, and U. Langmann, "Short-channel vertical sidewall MOSFETs," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1783–1788, Aug. 2001.
[6] L. Risch, W. H. Krautschneider, F. Hofmann, H. Schäfer, T. Aeugle, and W. Rösner, "Vertical MOS transistor with 70 nm channel length," *IEEE Trans. Electron Devices*, vol. 43, no. 3, pp. 1495–1498, Sep. 1996.
[7] H. Gossner, F. Wittmann, I. Eisele, T. Grabolla, and D. Behammer, "Vertical MOS technology with sub-0.1 μm channel lengths," *Electron. Lett.*, vol. 31, no. 16, pp. 1394–1396, Aug. 1995.
[8] F. Kaesen, C. Fink, K. G. Anil, W. Hansch, T. Doll, T. Grabolla, H. Schreiber, and I. Eisele, "Optimization of the channel doping profile of vertical sub-100 nm MOSFETs," *Thin Solid Films*, vol. 336, no. 1/2, pp. 309–312, Dec. 1998.
[9] J. Moers, D. Klaes, A. Tönnesmann, L. Vescan, S. Wickenhäuser, T. Grabolla, M. Marso, P. Kordoš, and H. Lüth, "Vertical p-MOSFETs with gate oxide deposition before selective epitaxial growth," *Solid State Electron.*, vol. 43, no. 3, pp. 529–535, Mar. 1999.
[10] D. Klaes, J. Moers, A. Tönnesmann, S. Wickenhäuser, L. Vescan, M. Marso, T. Grabolla, M. Grimm, and H. Lüth, "Selectively grown vertical Si MOS transistor with reduced overlap capacitances," *Thin Solid Films*, vol. 336, no. 1/2, pp. 306–308, Dec. 1998.
[11] K. Mori, A. Duong, and W. F. Richardson, "Sub-100 nm vertical MOSFET with threshold voltage adjustment," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 61–66, Jan. 2002.
[12] E. Gili, T. Uchino, M. M. A. Hakim, C. H. de Groot, O. Buiu, S. Hall, and P. Ashburn, "Shallow junctions on pillar sidewalls for sub-100 nm vertical MOSFETs," *IEEE Electron Device Lett.*, vol. 27, no. 8, pp. 692–695, Aug. 2006.
[13] J. M. Hergenrother, D. Monroe, F. P. Klemens, A. Kornblit, G. R. Weber, W. M. Mansfield, M. R. Baker, F. H. Baumann, K. J. Bolan, J. E. Bower, N. A. Ciampa, R. A. Cirelli, J. I. Colonell, D. J. Eaglesham, J. Frackoviak, H. J. Gossmann, M. L. Green, S. J. Hillenius, C. A. King, R. N. Kleiman, W. Y.-C. Lai, J. T.-C. Lee, R. C. Liu, H. L. Maynard, M. D. Morris, S.-H. Oh, C.-S. Pai, C. S. Rafferty, J. M. Rosamilia, T. W. Sorsch, and H.-H. Vuong, "The vertical replacement (VRG) MOSFET: A 50 nm vertical MOSFET with lithography-independent gate length," in *IEDM Tech. Dig.*, 1999, pp. 75–78.
[14] S. K. Jayanarayanan, S. Dey, J. P. Donnelly, and S. K. Banerjee, "A novel 50 nm vertical MOSFET with a dielectric pocket," *Solid State Electron.*, vol. 50, no. 5, pp. 897–900, May 2006.
[15] V. D. Kunz, T. Uchino, C. H. de Groot, P. Ashburn, D. C. Donaghy, S. Hall, Y. Wang, and P. L. F. Hemment, "Reduction of parasitic capacitance in vertical MOSFETs by spacer local oxidation," *IEEE Trans. Electron Devices*, vol. 50, no. 6, pp. 1487–1493, Jun. 2003.
[16] E. Gili, V. D. Kunz, C. H. de Groot, T. Uchino, P. Ashburn, D. C. Donaghy, S. Hall, Y. Wang, and P. L. F. Hemment, "Single, double and surround gate vertical MOSFETs with reduced parasitic capacitance," *Solid State Electron.*, vol. 48, no. 4, pp. 511–519, Apr. 2004.
[17] J. Moers, S. Trellenkamp, A. van der Hart, M. Goryll, S. Mantl, P. Kordoš, and H. Lüth, "Vertical p-channel double gate MOSFETs," in *Proc. 33rd ESSDERC*, 2003, pp. 143–146.
[18] M. M. A. Hakim, L. Tan, T. Uchino, O. Buiu, W. Redman-White, S. Hall, and P. Ashburn, "Improved sub-threshold slope in RF vertical MOSFETS using a frame gate architecture," in *Proc. 38th ESSDERC*, 2008, pp. 95–98.
[19] M. M. A. Hakim, L. Tan, O. Buiu, W. Redman-White, S. Hall, and P. Ashburn, "Improved sub-threshold slope in short channel vertical MOSFETS using a FILOX oxidation," *Solid State Electron.*, vol. 53, no. 7, pp. 753–759, Jul. 2009.
[20] M. M. A. Hakim, K. Mallik, C. H. de Groot, W. Redman-White, L. Tan, S. Hall, and P. Ashburn, "A self-aligned silicidation technology for surround-gate vertical MOSFETS," in *Proc. 39th ESSDERC*, 2009, pp. 363–366.
[21] B. Ricco, P. Olivo, T. N. Nguyen, T.-S. Kuan, and G. Ferriani, "Oxide thickness determination in thin-insulator MOS structures," *IEEE Trans. Electron Devices*, vol. 35, no. 4, pp. 432–438, Apr. 1988.
[22] C. Spinella, V. Raineri, and S. U. Campisano, "Selective etching of B-doped silicon: Mechanisms and two-dimensional delineation of concentration profiles," *J. Electrochem. Soc.*, vol. 142, no. 5, pp. 1601–1607, May 1995.
[23] N. Arora, *MOSFET Models for VLSI Circuit Simulation*. New York: Springer-Verlag, 1993.
[24] F. H. De La Moneda, H. N. Kotecha, and M. Shatzkes, "Measurement of MOSFET constants," *IEEE Electron Device Lett.*, vol. EDL-3, no. 1, pp. 10–12, Jan. 1982.
[25] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*., 2nd ed. New York: Cambridge Univ. Press, 2004.
[26] M. Racanelli and P. Kempf, "SiGe BiCMOS Technology for RF circuit applications," *IEEE Trans. Electron Devices*, vol. 52, no. 7, pp. 1259–1270, Jul. 2005.
[27] J.-C. Gou, M.-C. Chang, C.-Y. Lu, C. C.-H. Hsu, and S. S.-S. Chung, "Transconductance improvement due to back bias for submicron NMOSFET," *IEEE Trans. Electron Devices*, vol. 42, no. 2, pp. 288–294, Feb. 1995.
[28] G. A. Sai-Halasz, M. R. Wordeman, D. P. Kern, S. Rishton, and E. Ganin, "High transconductance and velocity overshoot in NMOS devices at the 0.1- μm gate-length level," *IEEE Electron Device Lett.*, vol. 9, no. 9, pp. 464–466, Sep. 1988.
[29] A. Cester, S. Gerardin, A. Tazzoli, and G. Meneghesso, "Electrostatic discharge effects in ultrathin gate oxide MOSFETs," *IEEE Trans. Device Mater. Rel.*, vol. 6, no. 1, pp. 87–94, Mar. 2006.
[30] J. Kedzierski, D. Boyd, P. Ronsheim, S. Zafar, J. Newbury, J. Ott, C. Cabral, Jr, M. Ieong, and W. Haensch, "Threshold voltage control in NiSi-gated MOSFETs through silicidation induced impurity segregation," in *IEDM Tech. Dig.*, 2003, pp. 315–318.
[31] H. Iwai, T. Ohguro, and S.-I. Ohmi, "NiSi technology for scaled CMOS," *Microelectron. Eng.*, vol. 60, no. 1/2, pp. 157–169, Jan. 2002.
[32] P. J. McWhorter and P. S. Winokur, "Simple technique for separating the effects of interface traps and trapped-oxide charge in metal–oxide–semiconductor transistors," *Appl. Phys. Lett.*, vol. 48, no. 2, pp. 133–135, Jan. 1986.
[33] N. Shinde, V. N. Bhoraskar, and S. D. Dhole, "Swift heavy-ion induced trap generation and mixing at Si/SiO_2 interface in depletion n-MOS," *Nucl. Instrum. Methods Phys. Res. B, Beam Interact. Mater. At.*, vol. 242, no. 1/2, pp. 659–662, Jan. 2006.

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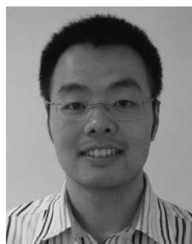

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