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Novel Chalcogenide Optoelectronic and Nanophotonic Information Storage and Processing Devices

by

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A thesis submitted in partial fulfillment for the
degree of Doctor of Philosophy

in the
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<u>ABSTRACT</u>

FACULTY OF PHYSICAL AND APPLIED SCIENCES
OPTOELECTRONICS RESEARCH CENTRE

<u>Doctor of Philosophy</u>

by Behrad Gholipour

This project is focused on the application of new electronic and optical materials. In particular it involves examining the use of chalcogenide thin films as phase change and ion conducting glasses for emerging optoelectronic applications. The ability of this group of materials to easily change their state from glass to crystal has meant that they have been widely used in CD's and DVDs. However, their ability to also conduct electrons and ions, promises novel solutions for next generation logic and memory devices which will take us in the short term beyond the limits of the silicon chip and, into the world of neuromorphic cognitive computing (computers that think and adapt). Additionally, this reversible change in the structure of these thin films allows their utilisation in ultra-high speed optical and optoelectronic switches to power the internet and future computers.

Three main goals are pursued within this research. First, next generation phase change (PCRAM) and nano-ionic resistive (ReRAM) memory is pursued for faster, non-volatile high density data storage. Secondly, the design of novel processing elements like next generation logic gates enabling neuromorphic cognitive processing and data storage in one structure based on material properties. Finally, the integration of phase change thin films with metamaterial arrays to produce electro-optic and all optical switches for future photonic computers and communication networks.

Statement of Authorship

Declaration of Authorship I, Behrad Gholipour, declare that the thesis entitled 'Novel chalcogenide optoelectronic and nanophotonic information storage and processing devices' and the work presented in it are my own. I confirm that:

- this work was done wholly while in candidature for a research degree at this University;

- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;

- where I have consulted the published work of others, this is always clearly attributed;

- where I have quoted from the work of others, the source is always given; With the exception of such quotation, this thesis is entirely my own work;

- I have acknowledged all main sources of help;

- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;

- parts of this work have been published as shown in the List of Publications;

Signed: .... Date: ....

List of Publications

1. Characterization of supercooled liquid $Ge_2Sb_2Te_5$ and its crystallization by ultra-fast-heating calorimetry, J. Orava, A. L. Greer, B. Gholipour, D. W. Hewak and C. E. Smith, Nature Materials, 11, 279283, 2012.

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3. Laser-induced forward transfer of thermoelectric materials on polymer and glass substrates, M. Feinaeugle, C. Sones, E. Koukharenko, B. Gholipour, D. W. Hewak and R. Eason, E-prints conference, Basle, Switzerland, 2012.

4. Laser Induced Forward Transfer-printing of pre-machined crystalline magneto-optic garnet discs, C. L. Sones, M. Feinaugle, B. Gholipour and R. Eason, Cleo 2012, San Jose, CA, United States, 6–11, May 2012.

5. Non-volatile bi-directional all-optical switching in chalcogenide glass metamaterials, B. Gholipour, J. Zhang, K. F. MacDonald, D. W. Hewak and N. I. Zheludev, Cleo 2012, San Jose, CA, United States, 6–11, May 2012.

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8. Laser assisted fabrication of chalcogenide glass microspheres on a planar waveguide device, V. Leonard, B. Gholipour, K. Khan and D. W. Hewak, ISNOG 2012, San melo, France, 1–5, July 2012.

9. Fabrication and aero dynamic levitation of chalcogenide glass spheres, K. Khan, T. Farmer, B. Gholipour, V. Leonard, D. Hewak, and A. C. Barnes, ISNOG 2012, San melo, France, 1–5, July 2012.

10. Non-volatile bi-directional all-optical switching in chalcogenide glass metamaterials (Poster), B. Gholipour, J. Zhang, K. F. MacDonald, D. W. Hewak, and N. I. Zheludev, SPIE Photonics Europe, Brussels, Belgium, 16 - 19, April 2012.

11. Metamaterial All-Optical Switch of Nanoscale Thickness, B. Gholipour, J. Zhang, K. F. Macdonald, D. W. Hewak and N. I. Zheludev (In preparation).

12. Sulphide nanowires for ultra low power thermally stable phase change memory applications, B. Gholipour, C. C. Huang and D. W. Hewak (In preparation).

13. High throughput nanowires: The search for the perfect memory material, B. Gholipour, F. Al Saab, A. Anastasopoulos, B. Hayden and D. W. Hewak (In preparation).

14. Deposition and characterization of CVD grown Ge-Sb thin film device for phase change memory application, C. C. Huang, B. Gholipour, K. Knight, J. Y. Ou, and D. W. Hewak, (Accepted, Advances in optoelectronics).

15. Electrical phase change of CVD Ge-Sb-Te thinfilm device, C. C. Huang, B. Gholipour, J. Y. Ou, K. Knight and D. W. Hewak, Electronics Letters, 47, 288–289, 2011.

16. Thermally Stable, Low Current Consuming Gallium and Germanium Chalcogenides for Consumer and Automotive Memory Applications (Invited talk), D. W. Hewak, C. C. Huang, B. Gholipour and K. Knight, S. Guerin and B. Hayden, E/PCOS 2011, Zurich, Switzerland, September 2011.

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21. Metamaterial electro-optic switch of nanoscale thickness, Z. L. Samson, K. F. MacDonald, F. De Angelis, B. Gholipour, K. Knight, C. C. Huang, E. Di Fabrizio, D. W. Hewak and N. I. Zheludev, Applied Physics Letters, 96, 143–105, 2010.

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Nomenclature

C Celsius

V Voltage

A Current

GLS Gallium Lanthanum Sulphide

GST Germanium Antimony Telluride

$GLSO$ Oxygen rich Gallium Lanthanum Sulphide

$GeSbTe$ Germanium Antimony Telluride

$GeSb$ Germanium Antimony

OUM Ovonic Unified Memory

CVD Chemical Vapour Deposition

$PCRAM$ Phase change Random Access Memory

$RRAM$ Resistive Random Acccess Memory

$OxRRAM$ Oxide Resistive Random Access Memory

$CBRAM$ Cross bridge Random access Memory

$Memristor$ Memory resistor

AC Alternating Current

DC	Direct Current
UV	Ultra Violet
CD	Compact Disk
DVD	Digital Video Disk
PCB	Phase change bridge
$DRAM$	Dynamic random access memory
$SRAM$	Static random access memory
ORC	Optoelectronics Research Centre
CaF	Calcium Flouride
MFC	Mass flow controller
$MOSFET$	Metal oxide field effect transistor
$CMOS$	Complimentary metal oxide semiconductor
VAP	Valence Alternation Pairs
$PRAM$	Phase change Random access memory
Vt	Threshold Voltage
PMC	Programmable Metallisation cell
TiN	Titanium Nitride
PDP	Personal Development Plan
NIR	Near infra red
NW	Nanowire
IR	Infra red

SEM Scanning electron microscopy

EDX Energy dispersive X-ray spectroscopy

XRD X-ray diffraction

FIB Focused Ion beam

RIE Reactive ion etching

PVD Physical vapour deposition

DSC Differential scanning calirometry

Tx Crystallisation temperature

Tc Crystallisation temperature

Tm Melting temperature

Tg Glass transition temperature

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To My Dear Wife,

Rudabeh

Chapter 1

Introduction

High speed fibre optic broadband, high definition television, smart phones, and the advent of tablet computing and many other similar devices make up the ever expanding list of novel technologies that are becoming the quintessential part of life in the 21st century. All of these however create a common need, the need for a non-volatile, high speed, highly scalable, high endurance and versatile memory architecture for both dynamic operation and to allow the possibility to store new forms of memory hungry media, in the most power efficient way possible.

The scaling and performance limit of conventional memory devices like Flash and DRAM is close and to push the memory market past these technologies a series of novel architectures are being pursued using magnetic and phase change material, as well as electromechanical mechanisms to store data. In this chapter an overview of the candidates being touted as replacements for current market leaders is presented and discussed, with a view of the work being presented in this thesis on PCRAM. Subsequently, the trend of recent research in both phase change is presented followed by an introduction into the novel and rapidly expanding field of metamaterials which are a cornerstone of the work being presented in Chapter 6, where the concept of phase change and metamaterials have been ammalgamated into new devices for future applications.

The success of these architectures will most likely not depend on the physical advantages of the architecture, but on a series of specific commercial parameters that include both performance characteristics as well as a series of industrial specific financial aspects that determine the road the product takes to mass market integration. As such it is argued that each of the architectures in development should exhibit both a operational superiority to existing memory devices but also be superior in scalability, endurance, access time, CMOS integration as well as being cost effective for the performance it offers.

When reviewing the possible successors to current technologies, one must first understand the advantages and limitations that current technologies have and the benefits
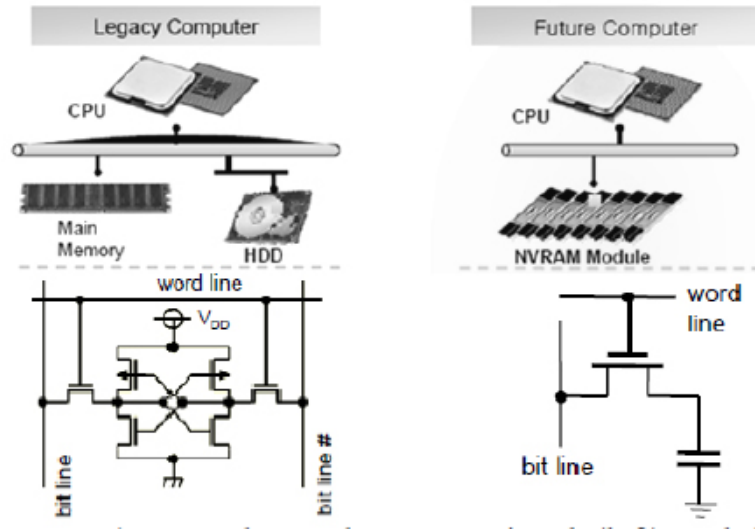
FIGURE 1.1: Top: shows the conventional (left) and future computer architectures (right) which can be achieved through non volatile fast reliable memory [Adapted from (1)]. Bottom: the schematic representation of SRAM (left) and DRAM (right).

that future technologies can bring to the field of data storage and processing. Static RAM (SRAM) alongside the faster Dynamic RAM (DRAM) has traditionally been used for the purpose of fast retrieval of data within computer architectures. SRAM provides relatively high speed operation while consuming low power. However, due to its six transistor structure, scaling is a major issue. As such, the limitation in terms of higher storage capacity, given the same wafer size, shows the need for DRAM. The fact that structurally, DRAM (a capacitor and a transistor) provides much better scaling capability is offset by the fact that it provides no improvement upon the volatility exhibited with SRAM, this means that both static and dynamic RAM do not retain data without power thus making instant on PCs, not possible using these technologies.

Whilst DRAM has been the market driver for a considerable time, its shortfall in terms of data retention has given way to the exploration and development of superior NAND and NOR Flash technology (Figure 1.1) that have extremely good scaling capability given present fabrication processes. This is coupled with the fact that due to its non-volatility, Flash is capable of replacing both hard disks and RAM segments within conventional computer architectures.

Flash uses charge trapping within the floating gate structure, resulting in a change in the threshold voltage of the MOSFET, which is then detected. This means that there will be a scaling limit as the smaller the device, the fewer the number of electrons that are trapped. As it stands today approximately 100 electrons are trapped per level (2), therefore the scaling limit is close to being reached (Figure 1.2).

It should be clear that the future will demand alternative structures that allow more data to be stored given the same chip size. As such there have been a number of proposed
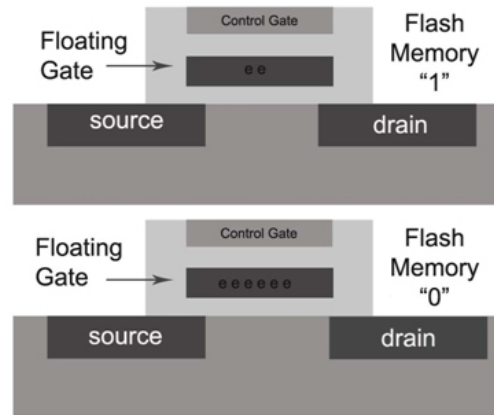
FIGURE 1.2: The simplified structure of the floating gate Flash architecture showing the 1 and 0 bit representation [Redrawn from (2)].
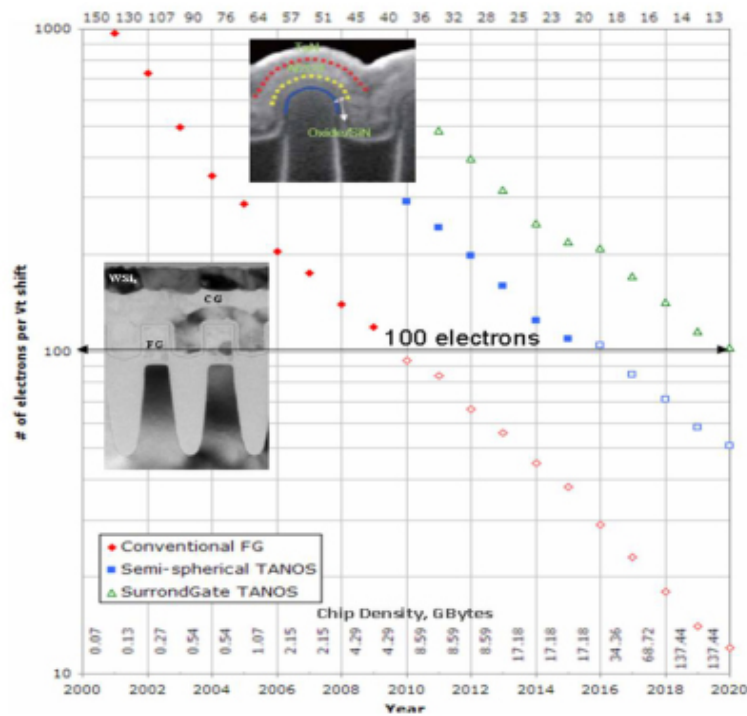
FIGURE 1.3: Scaling limitation of Flash memory [Reprinted from (2)].

novel RAM structures that aim to go beyond the limitations of conventional RAM and Flash architectures, most notably phase change RAM (PRAM or PCRAM), ferroelectric RAM (FRAM), Magnetoresistive RAM (MRAM) and nano-electro-mechanical RAM (NEMRAM) (39; 40).

When evaluating the structure and conceptual design of novel memory architectures, the most important parameter to consider is their non-volatility which is a direct manifestation of the material property being manipulated by the architecture. From the novel architectures being developed, FRAM and MRAM are very similar, in that they take advantage of the ferroelectric properties of material to store data. FRAM uses a
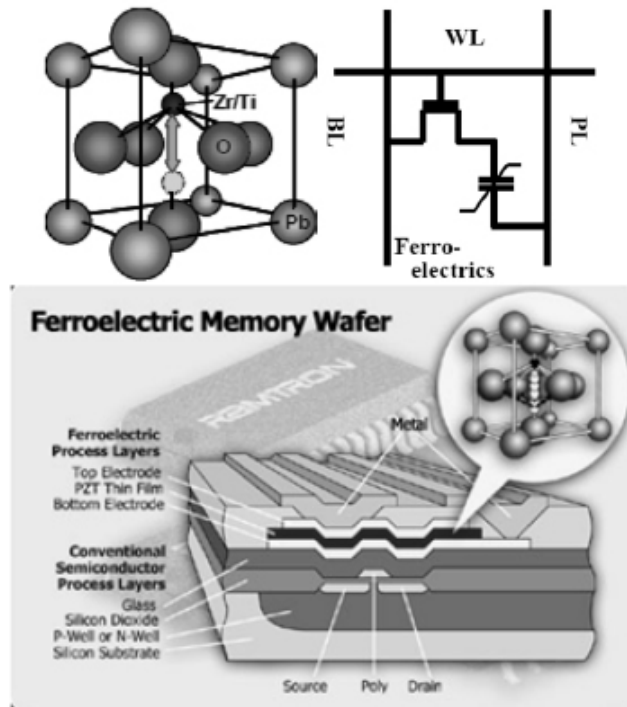
FIGURE 1.4: Top: Representation of crystal structure of FRAM ferroelectric atom showing the movement of the central atom for data representation (right) along with the schematic model of the 1T1C FRAM cell (left) adapted from [Reprinted from (3)]. Bottom: Representation of the fabricated FRAM structure produced by Ramtron Inc. Showing the two electrodes on either side of the ferroelectric layer that controls the electric field responsible for adjusting the position of the central atom. [Reprinted from (4)].

ferroelectric layer in the design, which contains ferroelectric crystals that have a central atom, which moves when an electric field is applied to the crystal (41) (See Figure 1.4).

The direction of the movement of the central atom depends on the direction of the electric field applied (42). When the central atom moves inside the crystal, a peak is detected by the architecture circuitry, as it moves through an energy barrier (43). The position of the central atom is fixed until another electric field with an opposite direction moves the atom. Thus, this architecture is non-volatile and preserves information without the constant need for refreshing, as is the case for the presently used D-RAM. Similarly Magnetic RAM (MRAM) takes advantage of the direction of the north and south poles of magnetic atoms to store data. When a magnetic field is applied the direction of these magnetic poles, align with that of the field. MRAM implements this concept through a magnetic tunnel junction (MTJ) to allow for non-volatility (44). The MTJ consists of a fixed ferroelectric layer in parallel with a dynamic free moving ferroelectric layer. The spins in the moving layer can either be in parallel or anti-parallel to the direction of the fixed layer [Figure 1.5].

Data is obtained through reading the resistance of the cell. If the two layers are parallel in terms of magnetic polarity, a lower resistance is observed as electrons move with more
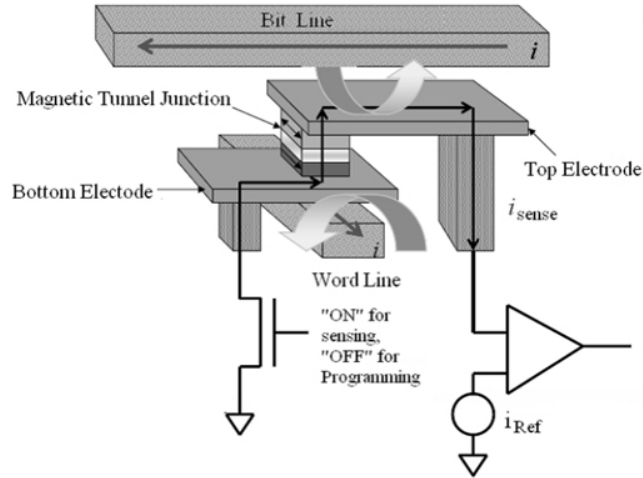
FIGURE 1.5: The structure of the MTJ MRAM cell showing the fixed and dynamic layers as well as the flow of the electrons and data path through the memory architecture and operational circuitry. [Reprinted from (5)]
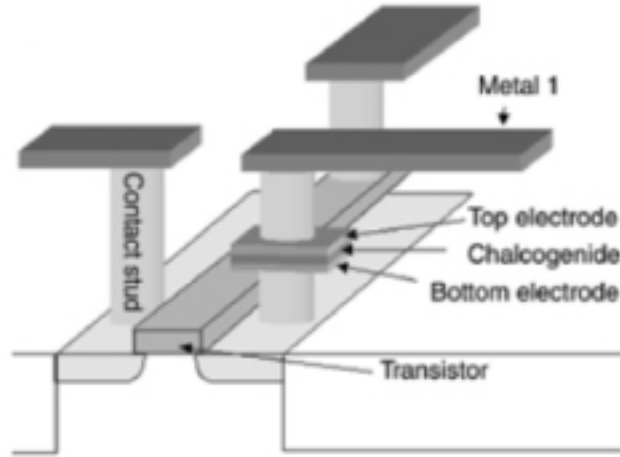
FIGURE 1.6: The conventional chalcogenide based phase change memory architecture with the electrodes that supply the energy needed for phase change and ultimately data storage. As the phase of the material changes the change in resistivity shifts the threshold voltage of the transistor that is connected to the electrodes, thus data is stored [Reprinted from (6)].

freedom through the layers compared to the anti-parallel state. To eliminate the effect of external fields, a reference layer is also incorporated into the design. The resistance obtained from the ferroelectric layers is compared to the reference cell (8). This is in contrast to the proposed PRAM which relies on the property of Chalcogenide alloys, and takes advantage of the reversible change between the amorphous and crystalline state of these alloys (45). This transition is achieved through heating and cooling of the material, done within PRAM by applying high and low currents (46). The crystalline state has a much lower resistivity than the amorphous states due to charge scattering. This difference in conductance as a result of the change in resistivity is how data is stored using this architecture [Figure 1.6].

Memory type	DRAM	SRAM	Flash NOR	Flash NAND	FRAM	MRAM	NEMRAM	PRAM
Cells size factor F^2	6–12	90–150	8–10	4	18	10–20	6	5–8
Volatile/non-volatile	Volatile	Volatile	Non Volatile	Non Volatile	Non Volatile	Non Volatile	Non Volatile	Non Volatile
SER susceptibility	Yes	Yes	No	No	Yes	No	Yes	No

TABLE 1.1: Non-volatility as well as soft error susceptibility are extremely important commercial parameters as they firstly ensure reliability in data retention over time without corruption of data and more specifically non volatility allows the production of instant-on personal computers, as there is no need to load data on the RAM.
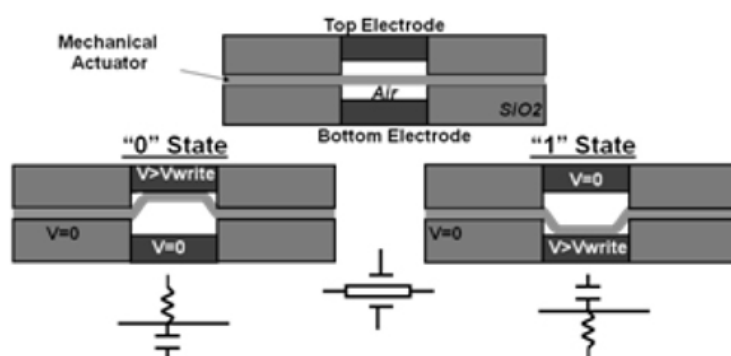
FIGURE 1.7: The NEMRAM structure showing the actuation of the floating actuator based on the field applied by the electrodes. Depending on the position of the actuator the threshold voltage of the transistor will be different as a different level of electrostatic control is observed over the channel [Reprinted from (7)].

The approaches outlined, use new materials to achieve better architectures [Table 1.1]. Nanoelectromechanical memory however is an alternative to these in that it uses existing methods and materials to achieve faster devices (7). NEMRAM uses the movement of a mechanical actuator as the gate and achieves a two state transistor operation based on the position of this floating actuated gate [Figure 1.7].

The memory read/write/erase time directly effects how fast the resulting computer system will be. Also, for a commercially viable architecture there should also be a high degree of endurance if not infinite endurance, to read and write cycles. Theoretically, FRAM should have one of the fastest access speeds. However, its use of a destructive read process severely limits its speed. This means that the data is destroyed during read cycles. As such the data needs to be rewritten every time it is read, thus slowing the process down severely (47). Both MRAM and PRAM boast a much better read and write speed compared to FRAM as they have a non-destructive read and write process. While PRAM claims to have the overall fastest access time [Table 1.2]. This is offset by the comparatively longer erase time which PRAM exhibits compared to MRAM. This is due to the fact that to erase the data the chalcogenide needs to be heated and cooled

Memory type	DRAM	SRAM	Flash NOR	Flash NAND	FRAM	MRAM	NEMRAM	PRAM
Endurance write/read	∞/∞	∞/∞	$10^6/\infty$	$10^6/\infty$	$10^{12}/10^{12}$	$10^{14}/\infty$	$10^9/10^9$	$10^{12}\infty$
Read	Destructive	Partially destructive	Non-destructive	Non-destructive	Destructive	Non-destructive	Non-destructive	Non-destructive
Read Program voltage (V)	1	1	2/ 10	2/ 10	1.8/1.8	3.5/3.5	<10/<10	0.4/1
P/E/R speed (ns)	50/50/8	8/8/8	1us/1-100ms (block)/60ns	1ms/ 1-100ms/60ns	62/62/62	30/30/30	<50/<20/ <50	10/50/20
Direct over-write	Yes	Yes	No	No	Yes	Yes	Yes	Yes
Bit/byte	Yes	Yes	Yes	Block erase	Yes	Yes	Yes	Yes

TABLE 1.2: Access times and erase mechanisms as well as endurance will directly influence the speed of system that uses the particular memory. MRAM shows extremely good program/erase/read times. This is also true of NEMRAM, however PRAM demonstrates the best all around access time superiority as its infinite read endurance as well as good P/E/R times makes it a very good candidate for low power high speed devices.
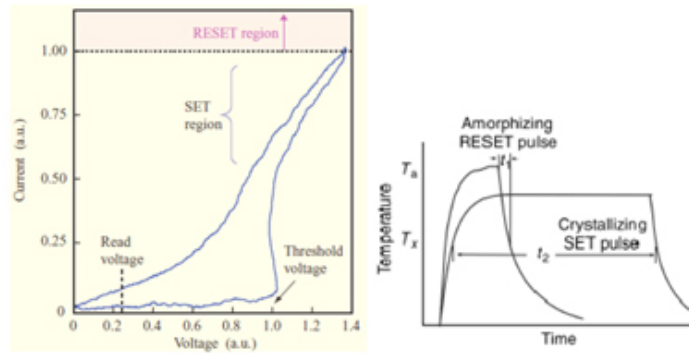
FIGURE 1.8: The I-V characteristic of a typical PRAM showing the relatively high current needed for resetting the bits (left) [Reprinted from (20)] as well as, The relatively long current pulse needed for erasing the PRAM device is shown (right), both show the need for reducing the power consumption of the devices at lower scales.[Reprinted from (8)]

using a long current pulse, thus the process is more time consuming than the MRAM process of resetting magnetic polarisation [Figure 1.8].

Both PCRAM and MRAM have an infinite read cycle endurance compared to an endurance of 10^{12} for FRAM (48). However it should be noted that as a replacement for the likes of DRAM and Flash memory, all three of these novel technologies are an improvement in both access speed and endurance. It should also be noted that NEMRAM exhibits extremely fast read and write speeds with demonstrations of read speeds of less than 20ns as well as programming/erase speeds of less than 50ns makes it a very promising product (simulations confirm the possibility of even faster access times [Figure 1.9]). Also has a very large R_{off}/R_{on} ratio, which makes it very reliable at high speed switching This makes it an extremely marketable product for the short term if the cell size can be reduced (7). The limits of scalability for each of the architectures discussed will determine to a large extent the future development of these technologies. As a smaller cell size, results in less space used on the chip allowing lower costs per unit and higher density final devices. Current technologies like Flash have been claimed to
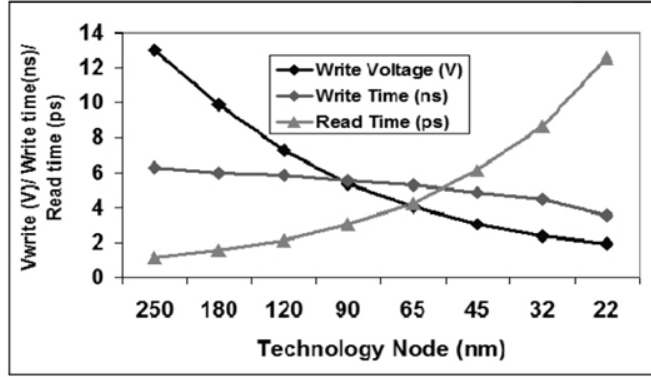
FIGURE 1.9: Showing the progression of the NEMRAM as nodes are scaled down to much smaller scales. Showing the trade off between speed and read times as the technology is scaled further. Although the lower energy needed for smaller scales is a promising feature for the future development. Data is based on simulations [Reprinted from (7)].

Memory type	DRAM	SRAM	Flash NOR	Flash NAND	FRAM	MRAM	NEMRAM	PRAM
Scalability limit	Capacitor	6T(4T possible)	Tunnel oxide/HV	Tunnel oxide/HV	Polarized capacitor	Current density	Lithography limit	Lithography Thermal
Multi-bit storage	No	No	Yes	Yes	No	No	No	No
3D potential	No	No	Possible	Possible	N/A	N/A	Yes	Yes

TABLE 1.3: The limits of scalability depend on different physical parameters or processes. The NEMRAM and PRAM have the benefit of having a very high scalability potential in line with lithography limits, however both have operational issues at lower dimensions. However the 3D integration potential of NEMRAM makes it a very good candidate for short to medium term future commercialization (7).

have a node limit of approximately 22nm (2), and as such future technologies have to show the capability to surpass these limitations to be successful.

While MRAM exhibits good potential in terms of read/write and erase speed, the large cell size [Table 1.3] of this architecture restricts the final density of the device. As such MRAM needs to be scaled further down to be commercially viable for future development (49). Also it is understood that at higher densities and smaller scales the current needed for writing to MRAM needs to be lowered to achieve low power operation [Table 1.3]. Spin torque transfer MRAM which uses polarized electrons. If the electrons entering a particular layer have to change their spin, the torque developed as a result is transferred to nearby layers within the device thus lowering the energy in the form of current needed for writing to the memory at higher density, although the cell sizes are large even for this variant of the technology (50).

Similarly, FRAM is also being fabricated at larger cell sizes [Table 1.3], although it presents the capability to fabricate the device as a single chip, which integrates both the analogue and digital functions all in one chip is highly desirable for future development and scaling.
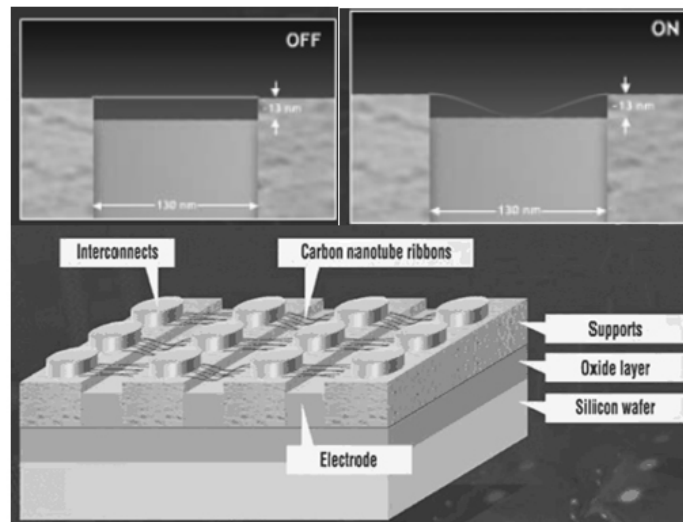
FIGURE 1.10: Top: The data representation of the carbon nanotube based NEMRAM produced by Nantero, taking advantage of the same actuating concept of NEMRAM but the nanotubes are bent through applying a current to them. Bottom: The array of the implemented architecture showing the electrodes used for actuation as well the nanotube ribbons connected to the device using the interconnects shown [Reprinted from (9)].

In comparison PRAM is highly scalable, exhibiting the smallest feature size even at present (51). Although thermal proximity corrupting data with decreasing feature size is an operational issue as we get to lower device dimensions. This would directly impact the read performance and the retention of the data being stored on the device. Also, the melting point of commonly used chalcogenide glass (GeSbTe) is around 600^oC. This attribute along with a low on-state resistance means that large programming currents are needed to achieve these temperatures in order to write to the PRAM device (for more detail see Chapter 3 and 4). As such, these current consumption levels need to be lowered for future scaling in order to get reliable high density low power devices (45) [Table 1.2 and 1.3].

Although NEMRAM has a large cell size at present, it theoretically exhibits very good power reduction capability with high level scaling as demonstrated through simulations [Figure 1.9]. Although Nantero is producing a CNT based Non-volatile memory that takes advantage of the same actuating concept of NEMRAM, with window sizes of around 130nm being demonstrated [Figure 1.10]. This is a promising device in the medium term for specialized applications, as this is an early attempt at highly scaled electromechanical memory. Nevertheless PCRAM at the present shows the best long term future potential in terms of scaling capability as it essentially relies on thin film technology for ultimate scaling [Table 1.3]. FRAM is mainly developed by Fujitsu and Ramtron, as well as Texas Instruments. Through these companies FRAM is mainly being distributed to automotive, industrial, metering and computing mainly for the purpose of data collection as its relatively fast write speed compared to DRAM as well
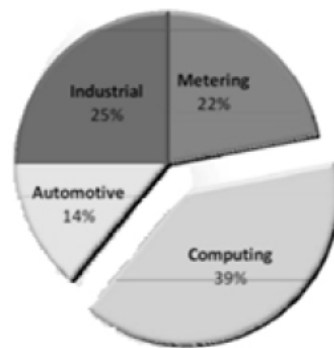
FIGURE 1.11: The demonstrated industrial distribution of FRAM by Ramtron showing
limited distribution to a number of specific industries, where high costs are acceptable
[Reprinted from (4)].
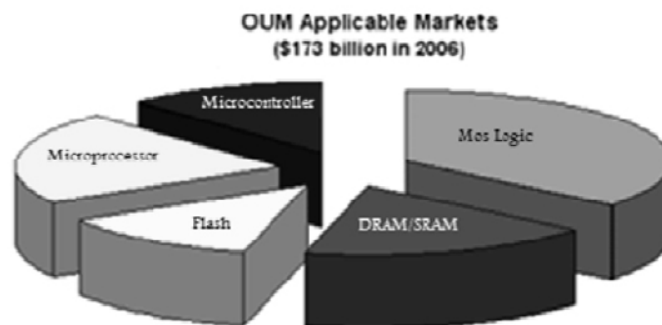
FIGURE 1.12: Intel predicted market for their PRAM variant OUM which effectively
shows the great potential for the successful non-volatile memory not just for PRAM but
for the successfully commercialized future non volatile memory [Adapted from (10)].

as its high endurance along with its low power consumption is ideal for these applications
at the moment [Figure 1.11]. Comparatively, MRAM (mainly produced by Freescale) is
not in the same stage of distribution as they have not achieved the density needed at the
comparatively commercially acceptable price. It should be noted that although the cost
of production is high and as yet, not fully commercially viable for large volume mass
production, MRAM in particular has been used in the satellite and industrial automation
market specifically by Siemans AG as in these applications higher costs can be tolerated.
This is also true of Freescale who has licensed its MRAM to Honeywell for military
and aerospace applications. Companies developing the architectures tend to predict
market viability for their products. Intel with Ovonyx are the main developers of phase
change memory competing with STMicroelectronics and most notably Samsung who has
already developed a memory chip for mobile phone applications based on PCRAM (6).
The market share predicted by Intel for their device [Figure 1.12], is contestable as they
have indicated the different devices that phase change memory can replace, but have not
taken into account and nor can it be certain how widespread the implementation of the
device will be in different markets. In particular, PRAM is presented as a replacement
for NOR flash memory while being able to replace both types of conventional RAM as

Memory type	DRAM	SRAM	Flash NOR	Flash NAND	FRAM	MRAM	NEMRAM	PRAM
Largest array buily (mb)	4 Gb	291 Mb	256 Mb	2 Gb	128 Mb	32 Mb	-	512 Mb
CMOS logic compatibility	Bad	Good	High voltage needed	High voltage needed	Ok	Ok	Very good	Good
New materials	Yes	No	No	No	Yes	Yes	No	Yes
Expected Relative cost per bit	Low	High	Medium	Medium	High	Medium to High	Low to Medium	Low

TABLE 1.4: Due to the present financial climate, there will be a restructuring of research on developing new technologies, as companies will mostly work on producing technologies that have high potential for commercialization in the short to medium term. Thus, advancement of promising architectures that are still underdeveloped may slow down. As such the array density already achieved along with CMOS integration both in terms of design and fabrication process will determine whether reasonable prices can be achieved for mainstream market commercialization.

well. With its high scalability potential it is also being considered as an ideal device for embedded and system on chip applications.

In order to be commercialized, these architectures have to show CMOS integration, as well as major company support (52) [Table 1.4]. However, FRAM has been shown to have issues with CMOS integration as the hydrogen involved in fabrication process steps degrades the ferroelectric capacitor used in this technology (53), although it should be noted that Ramtron claims to have solved this problem through encapsulation of the capacitor, but nevertheless the extra process steps involved is not desirable. While MRAM has its own issues with high temperature CMOS process steps (in particular the 400°C anneal used for curing the plasma induced damage) as the magnetic material used within the architecture is sensitive to high temperatures, which means modifications have to be made to the likes of dielectric deposition and other high temperature process steps within the fabrication process (3).

In contrast, PRAM is easily integrated into existing processes with adding extra photolithography steps and due to its structure is much more cost effective and well suited to highly scaled, embedded and portable applications. This makes it much more ideal financially in the long run. As such in this work in the first instance the technology pursued is phase change RAM (PRAM or PCRAM). Subsequently the phase change phenomenon behind PCRAM is also used as the central switching mechanism in the novel information processing and nanophotonic devices presented.

1.1 Project aim

There is currently worldwide interest in the development of the next generation of computer memory, fuelling research in new materials which can be used to potentially store vast amounts of information. While there are several promising candidates, the ideal memory material has yet to be demonstrated, particularly for electronic phase change
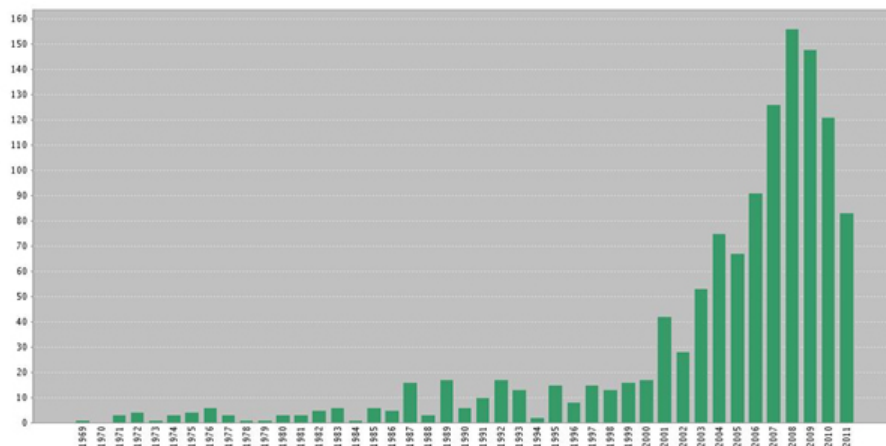
FIGURE 1.13: "Chalcogenides" +"phase change" -Published items per year (as presented in Web of Sciences)
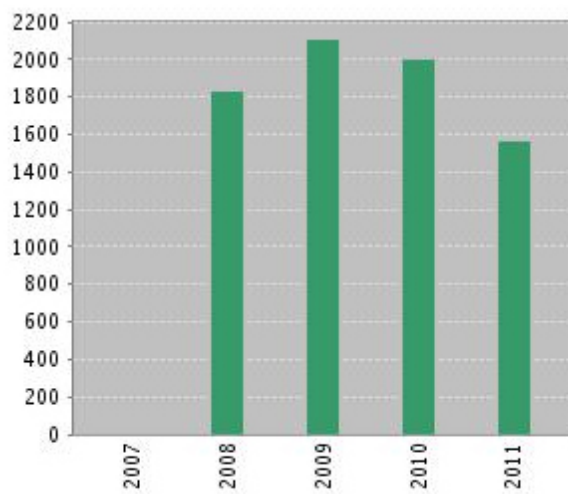
FIGURE 1.14: published items per year - "Metamaterials", (as presented in Web of Sciences).

memory. Today, chalcogenide based memory, is the subject of intense and far reaching research as can be seen by the high number of publications in recent years [Figure 1.13]. With the above as the central focus of the project we will focus on the development of nanoscale elements made from these new chalcogenide phase-change materials whilst also examining the use of these materials for other novel applications such as RRAM as well as other optoelectronic and logic devices such as AND gates and OR gates.

Finally, the integration of phase change thin films with metamaterial arrays to produce electro-optic and all optical switches for future photonic computers and communication networks is pursued in the latter part of this report. The field of photonic metamaterials is a relatively new and rapidly growing field of nanotechnology as the possibilities that these nanoscale photonic structures bring is seen by many as the path to the much touted photonic revolution. This is seen by the publications in this field in recent years [Figure 1.14].

In particular the marriage of reversible non-volatile phase change with metamaterials can enable the realisation of an actively switchable metamaterial resulting in either a nanophotonic electro-optic or all optical switch, i.e the building block for a nanophotonic processors. Through pursuing these different paths, the aim has been to use the reversible phase change of chalcogenide alloys in order to realise novel nanoelectronic and nanophotnic devices which can allow advances in the fields of data storage and processing, as well as nanophotonic switches for next generation transformation optics.

As such the objectives of the project can be summarised to:

- Tellurium based materials have dominated the phase change memory market because of their good glass forming ability (54) and these glasses tend to have a lower glass transition temperature than Se and S (55). However, with the increase in data storage densities, and reduced size of electrically addressed phase change memory cell dimensions, novel materials which operate at higher temperatures are becoming increasingly desirable. As such the examination of sulphide alloys and comparison with the standard tellurium based materials for highly scaled memory applications is pursued through the design, fabrication and characterisation of lateral nanowire memory cells.

- Phase change material are perfectly suited to information processing devices where one can achieve "true sleep" computing through non-volatile logic components, in addition their intrinsic ability to allow multi-level cognitive switching lends itself very well to logic applications. Chalcogenides also provide a unique platform for hybrid optoelectronic devices which provides a bridge between the world of photonics and electronics. In this pursuit, a series of electronic and optoelectronic logic gates are proposed, as well as other novel information processing devices.

- The integration of chalcogenide thin films with novel nanostructured metamaterials can provide a perfect platform for realising nanophotonic switches, as such the aim of this part of the project is producing next generation ultrathin non-volatile optical switches that can be tuned to any part of the transparent region of the dielectric spectrum, i.e the building block for a photonic processing unit or communication networks.

1.2   Thesis synopsis

As well as presenting a review of the current technologies on the market, the aims of this project have also been described in this chapter. This thesis details original research aimed at fulfilling the objectives outlined in the previous section. This is initiated with a brief introduction to the phase change phenomenon in Chapter 2, followed by

a background into the tools and techniques used during the course of this project in Chapter 3.

These two chapters aim to review the area of chalcogenide phase change and discuss methodologies of deposition and characterisation. All of these methodologies have been employed at some point throughout the course of this project. The concept of high throughput and combinatorial methodology is also introduced and particular emphasis is given to the approach used to achieve the composition spread samples, analysed in Chapters 4 and 6.

Chapter 4, 5 and 6 describe the bulk of the experimental work carried out and the results which were observed. These chapters start by giving a general background to the work done in the field thus far and the noteworthy work carried out by others. This is followed by the motivation for the work specifically set out in the respective chapter. Subsequently this provides a background for the devices and results reported here, which make up the remainder of each chapter.

Chapter 4 sets out the work done in examining the use of novel high thermal stability chalcogenide alloys in the field of electronic phase change memory for data storage purposes. After providing a review of electrically induced phase change of chalcogenides, the fabrication steps used in the production of the different types of memory cells is set out, with corresponding experimental setups created to characterise the devices. Subsequently the results observed are shown with a view to the objectives of the project.

Chapter 5 describes the work carried out in examining the use of chalcogenides in the formation of next generation non-volatile information processing logic components. After an overview of the field of next generation information processing, the fabrication steps and experimental setups are set out. This is followed by the results observed and the fascinating applications they exhibit.

Chapter 6 is the account of the work carried out in realising hybrid chalcogenide metamaterial devices for all optical switching in nanophotonic applications. The overview of the field of metamaterials is given following a review of optical switching in phase change chalcogenides. The efforts in designing all optical and electro-optic high throughput dielectric optimisation chips are also set out. The fabrication processes used and the results observed have been presented.

The final chapter contextualises the results of this work and suggests areas of possible advancement and work generated as a result of this research.

The principle highlights of this thesis which contributed to fulfilling the outlined objectives are:

- Design and development of GeSbTe, GeSb and GaLaS nanowires, the latter showing ultralow current consumption (among the lowest ever reported).

- A highly scaled nanowire memory cell combinatorial study of GaLaS phase change alloy over the widest ever reported compositional range.

- The demonstration of a series of non-volatile electronic and optoelectronic logic gates using GaLaS and GeSbTe. Whilst also observing multi-level optical switching of the GeSbTe phase change thin films.

- Observation of bidirectional memristive switching in Oxide rich GaLaS phase change alloy based devices.

- Demonstrated of a family of reversible nanophotonic non-volatile all optical switches in the near and mid infrared using hybrid chalcogenide metamaterial devices.

Chapter 2

Chalcogenide Phase Change

2.1 Materials

The novel devices demonstrated in this report rely on the use of chalcogenide thin films which are amorphous semiconductors as the active switchable layer to store or process information. As stated previously, chalcogenides are alloys of sulphur, selenium or tellurium. The devices proposed here make use of the reversible phase change which has been demonstrated and studied previously by a vast array of researchers. As such an overview of the properties of chaclcogenide materials focusing on their phase change capability is set out here.

2.1.1 Glassy amorphous semiconductor thin films

Conventional glasses, like silica, are poor electrical conductors. The conduction band is not close to the valence band. In fact, for silica the energy gap between these two levels is approximately 10eV . At room temperature the energy given to the electrons is k_BT = 0.025eV . Thus the proportion of electrons thermally excited to the conduction band is very low. The overall electrical conductivity is small resulting in a high value for its resistivity (38).

Materials which have a band-gap of a few eV are classed as semiconductors. Since the energy gap is small, an appreciable number of electrons can be thermally excited from the valance band into the conduction band. There are many empty states in the conduction band, thus a small applied electric field can promote the electrons resulting in a moderate current. At higher temperatures more electrons are thermally excited and the conductivity rises rapidly. The chalcogenide glasses investigated for this report can be classed as amorphous semiconductors as their band-gap is in the range between 1 and 3eV.

2.1.2   Chalcogenides

Their unique optical properties have brought about their use in lenses and prisms, special optical fibres and even as windows in submarines. Most importantly today, the ability of this group of materials to easily change their properties, i.e their structure from glass to crystal has meant that they have been widely used to store information as shown in Table 2.1. Although chalcogenides can exist over a wide range of compositions, not all

Phase change alloys	Onset of crystalization (°C)	Melt (°C)
GaLaS	640	830
GaSb	195	589
$Ge_2Sb_2Te_5$	160	620
AgInSbTe	200	537
InSb	168	490
InSbTe	200	500 - 600
InSe	200 & 650	890
Sb_2Te_3	121	570
$Te_{81}Ge_{15}Sb_2S_2$	-	380
GeTe	182	725

TABLE 2.1: Common phase change alloys and their properties

of them exist in a glassy form. It is often possible to find materials with which these non-glass forming compositions can be alloyed in order to form a glass. The model of a binary glass-forming chalcogenide is considered to be analogous to silica; there are two chalcogen (group 6) elements bonded to a single group 4 element. Another common class of chalcogenides have glass forming regions where three chalcogens are bonded to two group 5 elements. Most stable binary chalcogenide glasses are compounds of a chalcogen and a group 4 or 5 element. This allows a wide range of atomic ratios. Ternary glasses allow a larger variety of atoms to be incorporated into the glass structure; thus giving even greater engineering capacity (38).

Amorphous chalcogenide materials can be broadly classed by the type of atoms to which they bond to form amorphous systems. Table 2.2 lists the chalcogenide classification and gives some common examples of the type of chalcogenide which falls into the category.

Class	Examples
Pure chalcogenide	S, Se, Te, S_xSe_{1-x}
Pnictogen-chalcogen(V-VI)	As_2S_3, P_2Se
Tetragen-chalcogen (IV-VI)	$SiSe_2$, GeS_2, $Ge_2Sb_2Te_5$,GaLaS
III-VI	$B4_2S_3$, In_xSe_{1-x}
Metal chalcogenide	MoS_3, WS_3, Ag_2S-GeS_2
Chalco-halides	As-Se-I, Ge-S-Br, Te-CI

TABLE 2.2: Amorphous chalcogenide systems grouped by class (38)

2.2 Phase change

In order to achieve reversible phase change between the amorphous and crystalline states of chalcogenide alloys an energy barrier has to be overcome before the switch (phase transition) in the structure can be achieved. When the energy applied to the material exceeds this threshold energy, the material is excited to a high mobility state, where it is possible to rearrange bond lengths and angles through the slight movement of the individual atoms within the lattice structure.

The energy provided to the material can be applied through a number of different mechanisms. A reversible transition between the two stable states of the material can be achieved by optical heating, through exposing the material to intense laser beams, thus achieving optical switching. This can also be replicated by the application of a current or voltage pulse or sweep to the material, achieving electrical switching of the material through Joule heating. It should be noted that in essence, both the mechanisms above, excite the material by using thermal switching (25; 56; 57; 58). Both the optical and electrical power is converted to thermal energy within the material which allows the structural change to be achieved. Having said this, each type of switching mechanism has its own characteristics and intricacies which need to be optimised and are specific to optical and electronic properties of the material being reversibly switched from the glassy to crystalline state.

2.2.1 Glass formation

Normally, upon cooling a melt continuously, the crystallization occurs at the freezing temperature, if the cooling rate is low. This melt-crystal transformation is accompanied by discontinuous changes in first order thermodynamic parameters such as volume, entropy, etc. However, upon cooling the melt fast enough, the system passes through a meta-stable super-cooled liquid state into the glassy state. Unlike the crystallization, the transformation of the melt into the glassy state does not involve any latent heat or volume discontinuity as in the case of formation of crystals (59); however, a discontinuity is seen in the second order thermodynamic parameters such as specific heat (Cp) during this transition. It can also be noted that a divergence is seen in the specific heat at the freezing point (T_f) because of the latent heat associated with the crystal to melt transition. However, no such latent-heat singularity accompanies the glass to super-cooled liquid transition. There are several models developed for explaining the glass transition phenomenon. These include the configurational entropy model (60; 61), the free volume model (62; 63; 64), the bond lattice model (65), the potential barrier model, etc (66).

The temperature at which the system enters the glassy state from the super-cooled liquid state or vice versa is known as the glass transition temperature (Tg), see Figure 2.1. For many glass forming systems, the viscosity of the melt (η) attains a value closer to 10^{13}
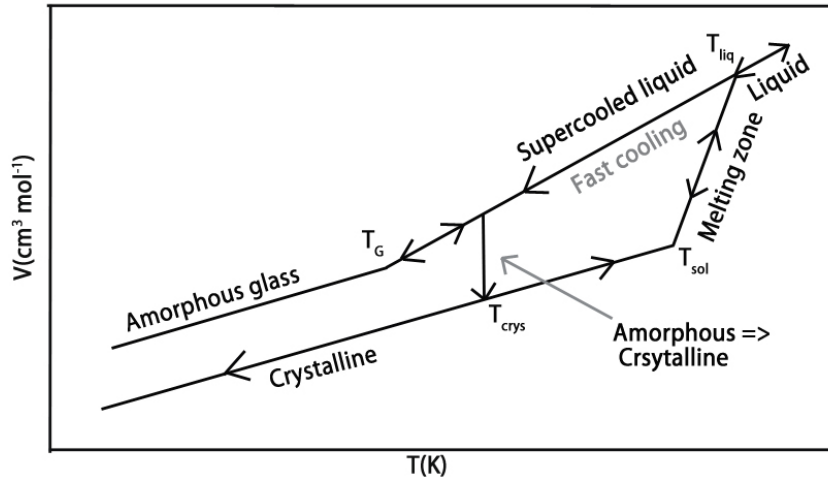
FIGURE 2.1: Dynamics of crystalline to super-cooled liquid transition.

poise at Tg; at this value of η, used sometimes to define the glassy state, the structural relaxation time far exceeds the experimental time-scale ($\approx 10^2$ sec) and consequently the system behaves as mechanically rigid though structurally disordered. In other words, the glassy state thus reached, has an elastic modulus but lacks long range order (67).

2.2.2   Crystallisation

The groups of materials in Table 2.1 can also be distinguished based on their crystallization mechanism. The first one (GeTe-Sb$_2$Te$_3$ tieline alloys) shows a nucleation driven (or nucleation-dominant) crystallization process and the second family of materials (doped SbTe) show a growth-driven (or growth-dominant) crystallization process. In the nucleation-driven crystallization, the nucleation rate is higher than the growth rate, whereas in the growth-driven crystallization the growth rate is higher than the nucleation rate. These processes can be explained in order to have a better understanding of the following: Consider a process of writing an amorphous mark in a crystalline background and subsequently recrystallizing the mark using a (pulsed) laser. If the crystallization starts by (homogeneous) nucleation in the centre or all over the amorphous mark and proceeds towards the circular rim of the amorphous mark (i.e. the interface between the amorphous mark and crystalline surrounding), it is a nucleation driven process. Whereas, if the crystallization starts at the rim and proceeds towards the centre of the mark, it is a growth-driven process. The two types of crystallization mechanisms are schematically depicted in Figure 2.2. Materials from the family of doped Sb exhibits a very fast (explosive type) growth-driven crystallization.
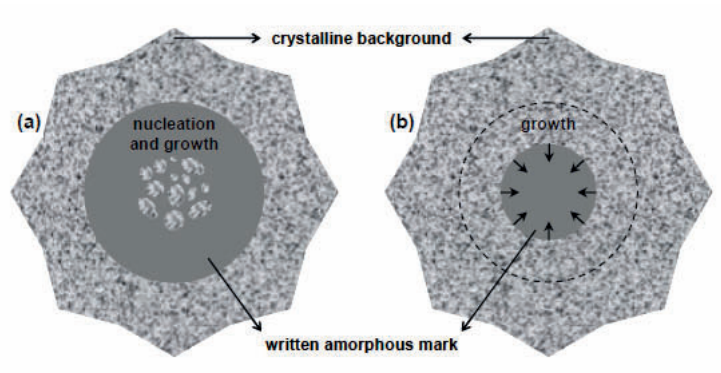
FIGURE 2.2: Nucleation driven crystalliation versus growth driven crystallisation [Reprinted from (11)].

2.2.3 Phase change alloys

A number of chalcogenide alloys have been proposed as good candidates for phase change memory (68; 69; 70; 71; 72). The most widely used being the germanium antimony telluride (GeSbTe) system which is used within the Ovonic Unified Memory (OUM) devices.

However, there are some major problems associated with GeSbTe. It is well known that Te has a low melting temperature and high vapour pressure, which can lead to phase separation and reduction of reliability of the material (73), reducing the endurance cycling.

It has also been found that Te motion in GeSbTe cannot be prevented even using the introduction of a capping a layer, this will result in inhomogeneity and voids in the material upon switching (74). The effect of the contamination of Te elements to the CMOS semiconductor manufacturing equipment and processes is still unclear and of concern. This limits the research and development of PCRAM. For the crystallisation temperature of common phase change materials refer to Table 2.3.

In this project the three systems, Gallium Lanthanum Sulphide (GaLaS), Germanium Antimony (GeSb) and Germanium Antimony Telluride (GeSbTe) are examined for memory application.

2.2.3.1 Germanium antimony telluride (GeSbTe)

The first studies of phase change data storage materials were conducted in the early 1970s (75). At the time the element tellurium (Te) was known to have good glass forming capabilities and it was most frequently reported compounded with various other elements. The most interesting and frequently studied compositions were based around the binary system Ge-Te. The fastest switching composition occurred at equal atomic proportions of Ge and Te (12). At this specific composition the material can melt without

Phase change composition	T_c (as deposited)($°C$)	T_c (dots) ($°C$)	E_{act} (kJ/mol)	Archival life @ $50°C$
Sb_2Te	103	-	-	-
$Ge_8Sb_{72}Te_{20}$	222	192	-	-
$Ag_8Sb_{72}Te_{20}$	175	120	196	100 days
$In_8Sb_{72}Te_{20}$	200	93	121	1 hour
$Ga_8Sb_{72}Te_{20}$	223	88	184	2 hours
$Ga_8Sb_{72}Te_{15}$	230	84	155	0.5 hours
$Sn_8Sb_{72}Te_{20}$	153	-	-	< few days at RT
$Ge_6In_2Sb_{72}Te_{20}$	208	176	465	4×10^{13} years
$Ge_2In_7Sb_{72}Te_{20}$	196	133	290	4×10^2 years

TABLE 2.3: Crystallisation temperature of common phase change materials [Adapted from (17)].

phase separation; this is evident in its phase diagram (76), see Figure 2.4. When the molten state has been quenched into an amorphous film, it is possible to crystallise areas of this film in less than 100ns. This is possible since there is no migration of atoms and it is only the bond angles between atoms which need to change. A small deviation in composition leads to a sharp increase in crystallisation time; this is also seen in Figure 2.3.

Referring back to the Ge-Te phase diagram, one notices that the Ge-Te phase has very little compositional tolerance Figure 2.4. Synthesising compositions GeTe generates a phase separated compound. Crystallising such a compound requires atomic migration from the quenched molten state into phase separated crystallites. This is a time consuming process and a deviation of just 10 at.% increases the crystallisation time by 2 orders of magnitude Figure 2.3.

Sensitivity to composition leads to difficulties in preparation of samples with the same characteristics; thus compositions with looser tolerances are sought. Doping Ge-Te with Sb, reduces atomic mixing and encourages the formation of two mixed phases (77). Much of the phase change data storage material research involves the GeSbTe ternary system. Before analyzing this system, it is interesting to analyse the Sb:Te and Ge:Te binary phase diagrams.

The Sb-Te system is characterised by two congruent melting points, the first at Sb_2Te_3 and the second with a wide composition range centred at 29 at.% Te Figure 2.5. In the Te rich zone there is a eutectic at 89 at.% Te Figure 2.5. Materials which melt without a change in composition are of interest since they are likely to switch without the time consuming atomic migration into phase separated components. Thus the fastest switching GeSbTe compositions lie along a tie-line between the two invariant, congruent melting compositions GeTe and Sb_2Te_3 (38).

This pseudo-binary phase system has three intermediate compounds with similar structures: $Ge_2Sb_2Te_5$, $GeSb_2Te_4$ and $GeSb_4Te_7$, each crystallises into a rocksalt lattice
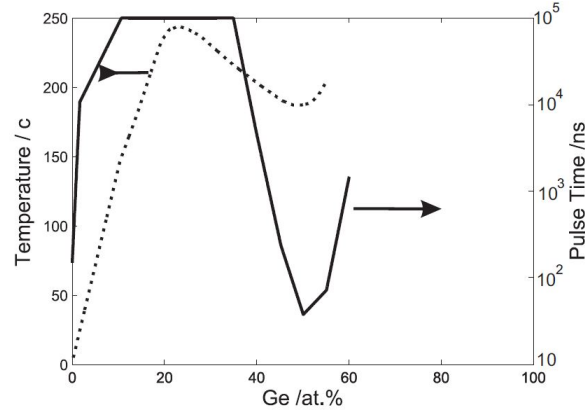
FIGURE 2.3: Ge-Te crystallisation time as a function of composition [Reprinted from (12)].
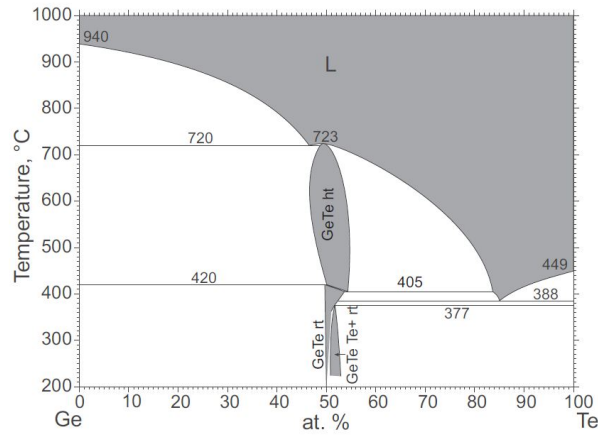
FIGURE 2.4: Phase diagrams for Ge-Te [Reprinted from (13)].

(Figure 2.6). Deviation from one of these stoichiometric compositions, results in a polycrystalline film which is a mix of the other stoichiometric crystals and individual elements (78). Clearly, materials which solidify into a single compound are of interest because phase separation upon repeated heating and cooling cycles is minimised. It is this pseudo-binary system which is often exploited for re-writable optical storage media since it leads to compositions with favorable characteristics (79) such as short crystallisation times.

2.2.3.2 Germanium antonomy (GeSb)

The crystallisation mechanism of Sb has been described as explosive (80). That is, upon crystallisation an exothermic heat release causes a self sustained crystal fast growth, estimated to be 200ns (81), into its amorphous surroundings (82). The main problem with pure Sb films is the amorphous phase stability; it is crystalline at room temperature. Alloying Sb with Ga or Ge has successfully increased the alloy's stability whilst retaining some of the fast growth crystallisation properties. The crystallisation temperature of

Sb_2Te is around 103°C and in the Ge-Sb system, increasing the Sb concentration to $Ge_{15}Sb_{85}$ raises the crystallisation temperature to 250°C. It should be noted that for these types of materials the phase stability and energy required for phase change are competing requirements and increasing the crystallisation temperature clearly means that more heat energy needs to be put into the system. The crystallisation temperature is increased by adding elements that increase the average co-ordination number of the system thus giving an explanation for the stability of $Ge_{15}Sb_{85}$ (83; 84).

GeSb is a promising material for phase change memory as it provides an environmentally friendly Te-free material which has a crystallization temperature of around $230°C$ (72) depending on composition. The special eutectic composition has a distorted tetragonal NaCl-B1 type structure (73). The GeSb used in this project is synthesised through chemical vapour deposition as set out in Chapter 3.
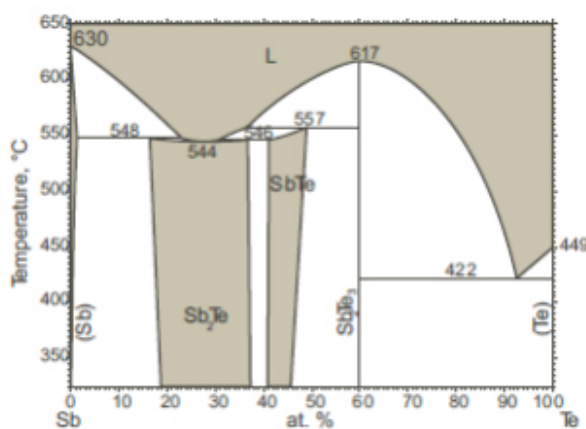
FIGURE 2.5: Phase diagrams for Sb-Te [Reprinted from (13)].
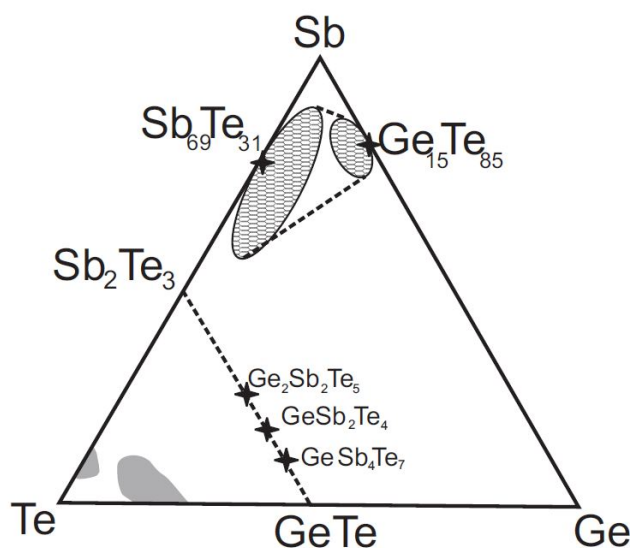
FIGURE 2.6: Ternary of GeSbTe. The pseudo binary line, the amorphous bulk and the fast growth compositional areas are indicated [Reprinted from (13)].

2.2.3.3   Gallium lanthanum sulphide (GaLaS)

GaLaS materials are known to be stable in both their crystalline and amorphous phases (85; 86). The covalent bond strength of chalcogen atoms is greatest for sulphur and is reduced through selenium and is lowest for tellurium (84); this allows a corresponding reduction in the materials' glass transition temperature. Generally for phase change data storage, tellurium based materials are chosen (87) since they are good glass formers and have a lower glass transition temperature than sulphides and selenides (84). However, as one moves down the periodic table from sulphur to tellurium, the atomic bonds become more metallic and isotropic, the energy gap decreases and electronegativity decreases, resulting in a material with higher electrical conductivity (or low resistivity).

However, phase change materials, with a high electrical resistivity in the crystalline phase, are desirable since the electrical current required to Joule heat them can be low. This becomes increasingly important as the device dimensions are reduced, for instance, since the size of the transistor used to address the memory cell is also reduced, as the maximum current that can be supplied to the cell is limited by the transistors current passing capacity.

Gallium lanthanum sulphide (GaLaS) is a chalcogenide material which was first reported by Lozach et al. in 1976 (88). In a glassy phase it is a semiconductor with a band-gap of 2.6eV, corresponding to a wavelength of 475nm (89), consequently GaLaS glass takes a deep orange colour. GaLaS has many useful properties. Initially the low phonon energy of these glasses attracted significant interest as a host for near- and mid-infrared emitters with applications in telecommunications and sensing. In addition, their large nonlinear refractive index has also led to investigation of active waveguides, switches and routers (89; 34). Most notably the other important property of this material is its ability to exist in both glassy and crystalline forms (87; 90).

The structure of the glass consists of Ga-S bonds, with a length of 2.26 $\overset{\circ}{A}$, and La-S bonds of length 2.93 $\overset{\circ}{A}$. It has been reported that the Ga-S distances in the glassy state are identical to those in the crystalline state (86). Therefore it is only necessary to change the bond angles and, thus, it is hypothesised that GaLaS has the potential to be a fast switching phase change material (38).

It can exist in both a crystalline and amorphous phase with a bulk glass transition temperature of $520°C$ and crystallisation temperature of $730°C$ and melting point of $830°C$.

2.3   Applications

Chalcogenide glasses have many interesting properties; optically they are often transparent from the visible spectrum up into the infrared, they can readily be deposited in the form of thin and thick films, they can exist as glasses over a wide composition range with other varying physical properties and they can be applied to many different applications, from optical transmission to electronic taste sensors (91). Some tellurium based glasses can be transparent out to 20μm (92). They also have a high nonlinear refractive index and hence could be useful as the active element in an All Optical Switch (AOS)(93). This has been demonstrated in an As_2S_3 material (56).

More importantly the use of their phase change capability has spun off the CD and DVD industry. It has also given rise to the continued interest in their electronic and cognitive properties which is an exciting area of intense research at the moment for ultra low power data storage and reconfigurable logic applications.

Chapter 3

Tools and Techniques

In this chapter, details of sample fabrication techniques and the general experimental instruments used to characterize the samples are presented. Sputtering and chemical vapour deposition as well as evaporation techniques have been used to deposit thin films of various materials including the phase change materials.

Use of different plasma and ion beam etching tools in order to realise nanoscale features have been utilised extensively throughout the work presented in this thesis, an overview of such techniques along with the complimentary electron microscopy and x-ray spectroscopy techniques have also been employed within the work and set out in this chapter.

Specific tools have been used in order to investigate the crystallisation of fabricated phase change thin films, these include thermal stage microscopy and differential scanning calirometry which allow the observation of crystallisation and melting characteristics of the chalcogenide thin films as well as allowing elevated temperature measurements on different devices.

3.1 Device fabrication

In this work five main deposition techniques were used:

- Sputtering

- Chemical Vapour Deposition (CVD)

- Physical vapour deposition

- E-beam evaporation

Depending on the measurement regime and device application different substrates have been used and detailed in appropriate sections in this report. The deposition techniques used are discussed below.

3.1.1 Sputtering

Sputtering is the process which involves the removal of fractions of a material from the sputtering target and depositing them on a substrate. This is achieved by bombarding the surface of the target material with ions under a high voltage. The ions are formed by what is known as a glow discharge process, this is the ionisation of inert gas atoms through electric discharge, resulting in the creation of plasma. Plasma can be defined as a gas with charged and neutral particles, for example, electrons, positive ions, atoms and molecules. Overall the plasma is charge neutral. Plasma is usually created with argon gas which is fed into the sputtering chamber. Due to the natural cosmic radiation, there are always some ionized Ar+ ions present in the chamber to ignite the plasma.

The ion bombardment using the created plasma results in atoms being ejected from the surface of the target (Figure 3.1). The process is carried out under very high vacuum (10^4 to 10^6 mbar). There are two different sputtering techniques namely DC and magnetron sputtering.

Within either sputtering technique, the sputtering target is negatively biased up to a few hundred volts. This attracts the argon ions within the plasma and provides the means for the bombardment of the surface of the target. These ions are also responsible for the production of secondary electrons that help to sustain stable plasma within the chamber and as a result further ionisation of the gas is also achieved. The deposition rate can be controlled through the optimisation of the ion current to the target .

However it should be noted that this is offset by the fact that at high pressures, the ejected target atoms are scattered before they reach the substrate, thus a reduction in the deposition rate is observed. As such, the two parameters need to be optimised to find a peak performance depending on the gas, target material and vacuum conditions within the chamber.
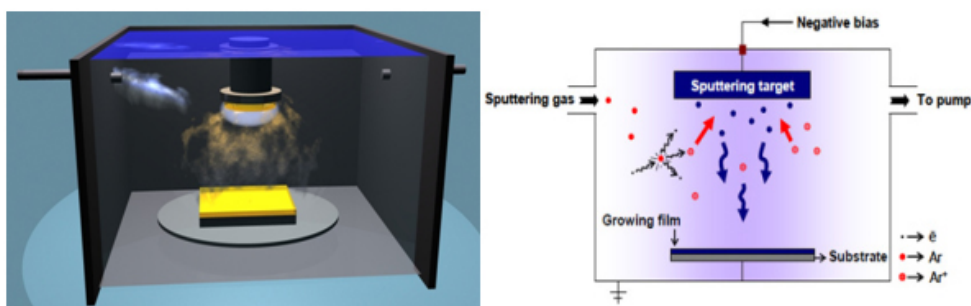
FIGURE 3.1: A typical sputtering system [Reprinted from (11)].

This technique can be used for the deposition of basic thin films. Alternatively by using a mask on top of the substrate, specific patterns can be deposited. Within this work sputtering has been used to deposit phase change chalcogenide layers (e.g gallium lanthanum sulphide and germanium antimony telluride), electrodes (e.g molybdenum) as well as capping layers (e.g zinc sulphide/silicon dioxide).

Sputtering has become one of the powerful techniques in modern manufacturing. In fact, today's technologists use sputtering to coat more surfaces in more industries than ever before. From semiconductors to credit cards; from compact discs to auto parts; magnetron and DC sputtering are adding new value to a growing list of products every day. Specifically in optical data storage applications, sputtering virtually deposits the whole variety of layers (made up of alloys, metals and compounds) used in the optical disk formats and provides a unique combination of advantages. Some specific advantages of sputtering are given below:

1. The high kinetic energy of sputtered atoms gives better film adhesion.

2. Since coverage is independent of line of sight, sputtering inherently produces uniform film coatings over a large area.

3. Unlike evaporation techniques, which require horizontal placement of the crucible containing molten material and vertical placement below the substrate, sputtering works in any orientation, providing it faces the substrate.

4. It offers much greater versatility than other approaches because, as a cold momentum transfer process, it can be used to apply either conductive or insulating materials to any type of substrate including heat sensitive plastics, e.g. polycarbonate typically used in optical disks.

5. Sputter cleaning of the substrate in vacuum prior to film deposition can be done.

6. It enables simultaneous deposition from multiple sources to develop new alloys . For example, GST alloys of various compositions can be deposited using Ge, Sb and Te sources.

7. For industrial applications (for the mass-production of devices in fabrication lines), sputtering can be made a continuous, inline process. Deposition of multiple layer stacks is possible (for e.g. to deposit various layers of an optical disk) by having multiple chambers, in a row, with sputter cathodes of different materials.

8. Tuning of specific film properties (for e.g. composition, microstructure, step coverage) can be more easily achieved, than any other techniques, by varying the sputtering parameters (single or multiple parameters) such as target to substrate spacing, sputtering gas pressure, sputtering gas/ion type, biasing the substrate.

9. Compound thin films can be deposited using reactive sputtering i.e. sputtering in the presence of a reactive gas. Typically oxides or nitrides of phase-change materials are deposited by this method.

3.1.2 Chemical vapour deposition (CVD)

Most of the phase change thin films studied in the past decades were deposited by physical vapor deposition (PVD), such as sputtering, evaporation, or laser ablation; however, conformality of PVD films is poor. Chemical vapour deposition of phase change materials is of interest mainly for its conformal deposition profile and the potential application in phase change memory. Chemical vapor deposition (CVD) may be defined as the deposition of a solid on a heated surface from a chemical reaction in the vapor phase. Generally, the precursors and co-reactant vapors are introduced into a deposition chamber under vacuum, where the substrate can be heated to elevated temperatures. The chemical reaction takes place on the heated surface or in vapor phase above the substrate surface. The advantage of CVD over PVD is its conformal deposition profile, i.e. the film thickness in the field is the same or close to the thickness on the side wall in a trench or via structure. CVD can be used to fill deep recesses, holes, and other difficult three dimensional configurations. The major disadvantage of CVD is the need for a relatively high deposition temperature. In addition, extensive engineering controls can be required due to the high toxicity and volatility of CVD precursors. Most thermal CVD processes are achieved at temperatures of $600°C$ and above, and many substrate materials are not thermally stable at these temperatures. The deposition temperature can be reduced to below $400°C$, by introducing plasma in the chamber to enhance the reaction (PECVD) or by using metal-organic precursors (MOCVD), which have lower reaction temperatures than their inorganic counterparts. Currently, CVD has been implemented in a lot of deposition processes for integrated circuit (IC) manufacturing. For instance, the deposition of poly-silicon, silicon dioxide, silicon nitride, metal nitrides, and tungsten are accomplished by CVD processes. The tradeoff is that CVD is generally a much more complex process than PVD, with more opportunities for introduction of contaminates both beneficial and detrimental.

The composition of GST films can be altered by the process parameters. For instance, the germanium incorporation into GST films by MOCVD is controlled by the precursor bubbling temperature, carrier gas flow rate, deposition temperature and pressure. Generally, when deposition is dominated by surface reactions, film composition is sensitive to the deposition temperature and pressure. When deposition is dominated by mass transport, film composition is sensitive to the ratio of precursor vapor partial pressures. Different carrier gas flow rates or different precursors bubbling temperatures can be used to adjust the ratio of precursor partial pressures, and therefore adjust the GST film composition.
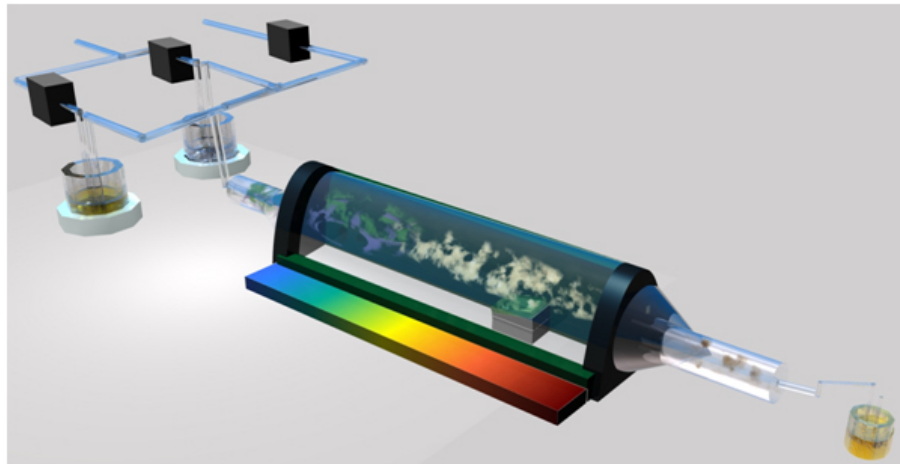
FIGURE 3.2: Schematic diagram of the CVD system used for the deposition of GeSb
as designed and built by Kevin Huang.

For the past few years, within the Novel Glass Group at the ORC, Huang et al, have been developing a novel CVD technique specially targeted at the deposition of chalcogenide materials. Using this technique through the in house built system, glassy and crystalline thin films and high purity bulk materials can be deposited.

The CVD apparatus that has been constructed for GeSb amorphous thin film deposition can be seen in Figure 3.2. In this process, GeSb amorphous thin films are deposited on silica on silicon or glass substrates placed in a quartz tube reactor (25mm $\times$ 500mm long) and heated by an electrical resistance furnace to a temperature of $300°C$. As can be observed, in this system the reactive hydrogen along with the carrier argon gas for $GeCl_4$ and $SbCl_5$ are delivered through the mass flow controllers (MFC). The GeSb discussed in this work are deposited using this setup.

3.1.3 Focused ion beam milling and deposition

Focused ion beam milling as well as scanning electron microscopy has been used extensively for the fabrication and characterisation of the nanowire memory cells described in sections of this report.

Unlike conventional scanning electron microscopy, FIB is destructive to the sample being characterised. When the high-energy gallium ions strike the sample, they will sputter atoms from the surface. Gallium atoms will also be implanted into the top few nanometers of the surface.

Because of this capability, the FIB is used as a micro and nano machining tool, to modify structures at the micro and nanoscale. The common smallest beam size is 2.5–6 nm. FIB systems are designed to etch or machine surfaces (Figure 3.3), an ideal FIB might machine away one atom layer without any disruption of the atoms in the next layer, or any residual disruptions above the surface.
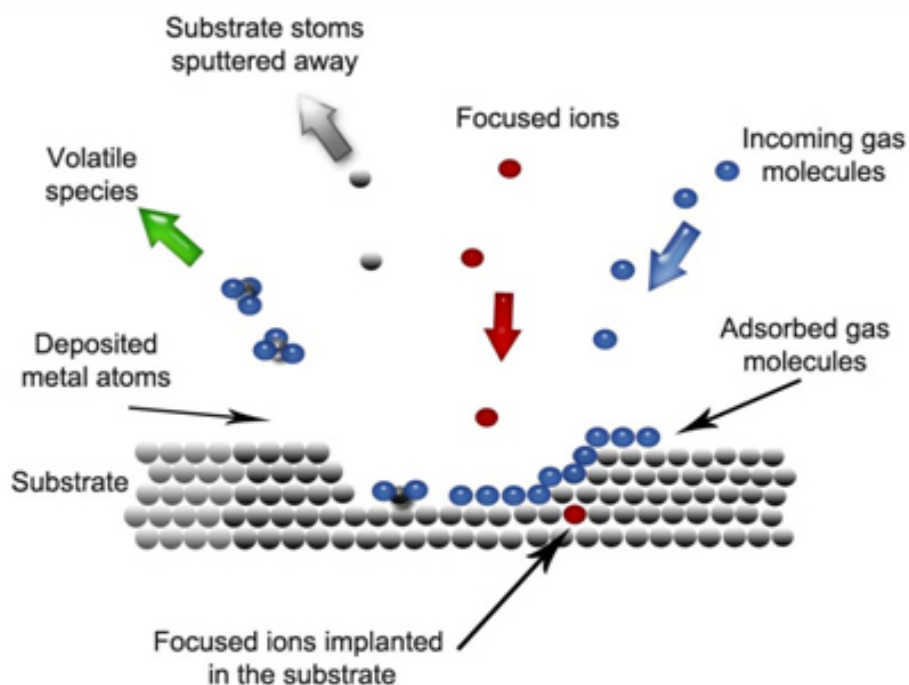
FIGURE 3.3: Schematic diagram of the ion beam milling process [Redrawn from (14)]

An FIB can also be used to deposit material via ion beam induced deposition. FIB-assisted chemical vapor deposition occurs when a gas, such as tungsten hexacarbonyl ($W(CO)_6$) is introduced to the vacuum chamber and allowed to chemisorb onto the sample. By scanning an area with the beam, the precursor gas will be decomposed into volatile and non-volatile components; the non-volatile component, such as tungsten, remains on the surface as a deposition. This is useful, as the deposited metal can be used as a sacrificial layer, to protect the underlying sample from the destructive sputtering of the beam. From nanometers to hundred of micrometers in length, tungsten metal
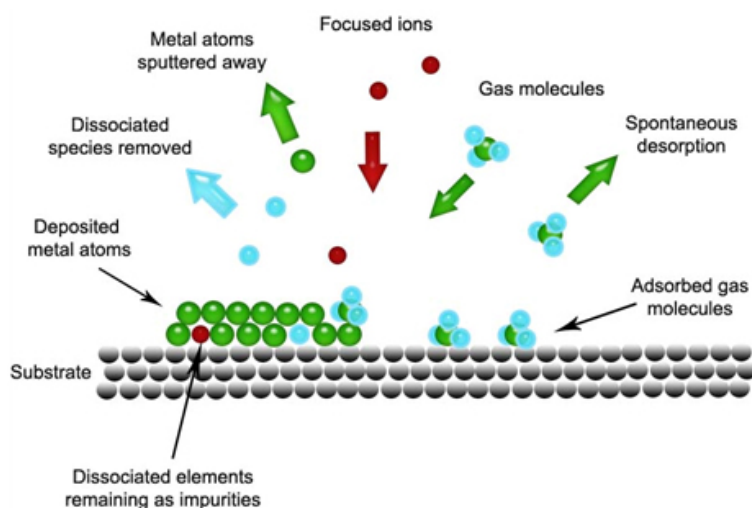
FIGURE 3.4: Schematic diagram of the electron/ion beam deposition process [Redrawn from (14)]

deposition allows to put metal lines right where needed (Figure 3.4). Other materials such as platinum, cobalt, carbon, gold, etc., can also be locally deposited.

3.1.4   Physical vapour deposition (PVD)

3.1.4.1   High throughput synthesis

Historically, material experimentation and characterisation has been on a sample by sample basis. This is a very expensive and time consuming process. However, in recent times, component miniaturisation has allowed a high-tech solution to this process thus, combinatorial experimentation is becoming an increasingly popular and powerful tool for efficient material synthesis and characterisation (94). The concept of high throughput is simple: systematically vary the material composition of a large number of samples and measure the change in properties as a function of composition. Ideally, the whole material system is covered by the compositions synthesised. Spatially varying thin film synthesis is sometimes performed such that the films composition is spread over the substrates area (95).

In Chapters 4 and 6 measurements are made on samples fabricated using a compositional spread Physical Vapour Deposition (PVD) technique (95). The method consists of evaporation of the elemental samples in a Ultra High Vacuum (UHV) by either Knudsen cell or e-beam heating. Simultaneous evaporation was possible from six different elemental sources but for this work only three sources were used; allowing fabrication of ternary systems. Each source was positioned off-axis from the substrate and separated by an angle of $\pm 60^o$. The silicon and quartz square substrates were 32mm by 32mm. Shutters in the vapour beam allow masking, thus the vapour beam casts a shadow onto the substrate allowing a deposition rate change as a function of position on the substrate and growth of a wedge. Therefore deposition from multiple sources at different angles allows the atoms to have an opposing component to their velocity. This is clearly maximised
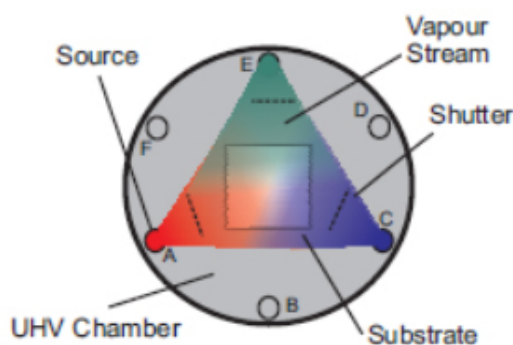
FIGURE 3.5: A schematic showing how composition varying thin films have been synthesised
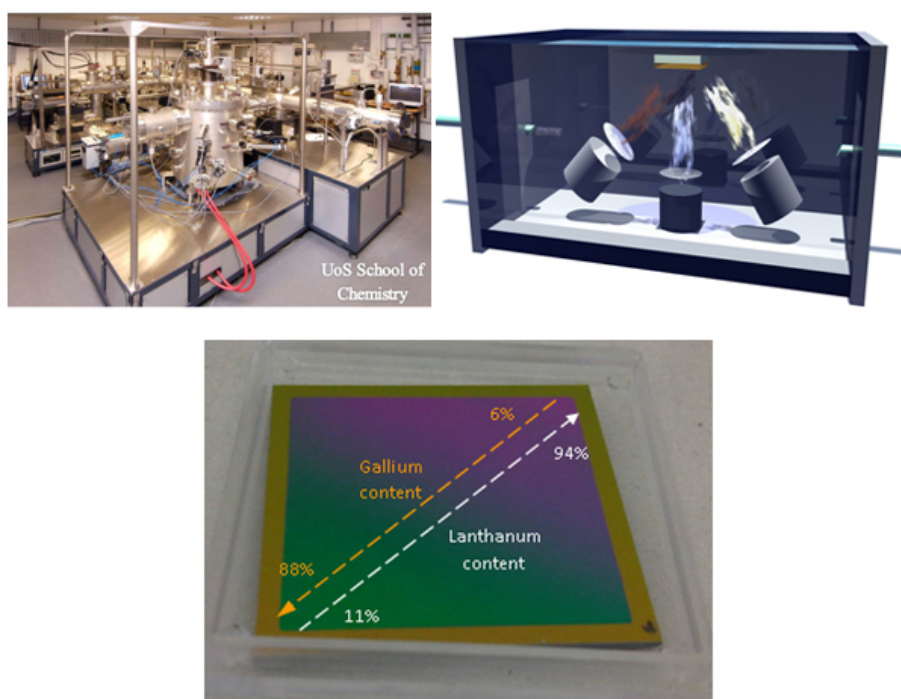
FIGURE 3.6: Compositional gradient GLS sample prepared by high throughput physical vapour deposition

when the sources are separated by 180°. Since each source produces a wedge, the composition of the film changes as a function of position, this can be seen in Figure 3.5 and Figure 3.6.

Characterisation of the synthesised materials is also performed in a high throughput manner; ideally the characterisation of the whole system is performed in parallel. Thus the individual compositions are treated exactly the same and the characterisation of all samples is performed at the same time. This increases reliability by ensuring elimination of measurement differences due to a variable sample history.

In order to map the data from a Cartesian co-ordinate system on the substrate to a ternary plot, it is necessary to measure the composition at the points where measurements are made. Energy Dispersive X-Ray (EDX) analysis is used to measure the composition as a function of position. Further measurements and characterisations are also made as a function of position on the substrate thus they can then be linked and mapped with the EDX data and plotted in compositional space.

3.1.5   E-beam evaporation

In evaporation, the substrate is placed inside a vacuum chamber, in which a block (source) of the material to be deposited is also located (Figure 3.7). The source material
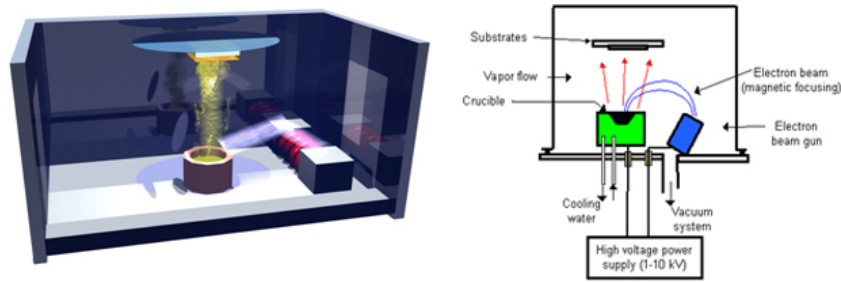
FIGURE 3.7: Schematic view of the electron beam evaporation system used predominantly for the deposition of thin films of gold.

is then heated to the point where it starts to boil and evaporate. The vacuum is required to allow the molecules to evaporate freely in the chamber, and they subsequently condense on all surfaces. This principle is the same for all evaporation technologies, only the method used to heat (evaporate) the source material differs.

There are two popular evaporation technologies, which are e-beam evaporation and resistive evaporation each referring to the heating method. In e-beam evaporation, an electron beam is aimed at the source material causing local heating and evaporation. In resistive evaporation, a tungsten boat, containing the source material, is heated electrically with a high current to make the material evaporate.

3.1.6 Photolithography

All the structures described within this report which are on the micron scale were fabricated using conventional UV photolithography. Using a dark field mask designed by the author and fabricated by Compugraphics Ltd.

The conventional photolithography process consists of three sets of processes that need to be carried out:

- Resist spinning

- Exposure

- Development

These will be discussed in the following subsections.

3.1.6.1 Resist spinning

A resist is applied to the surface using a spin-coating machine. This device holds the sample, using a vacuum, and spins it at high-speed (3000 - 6000 rpm) for a period of
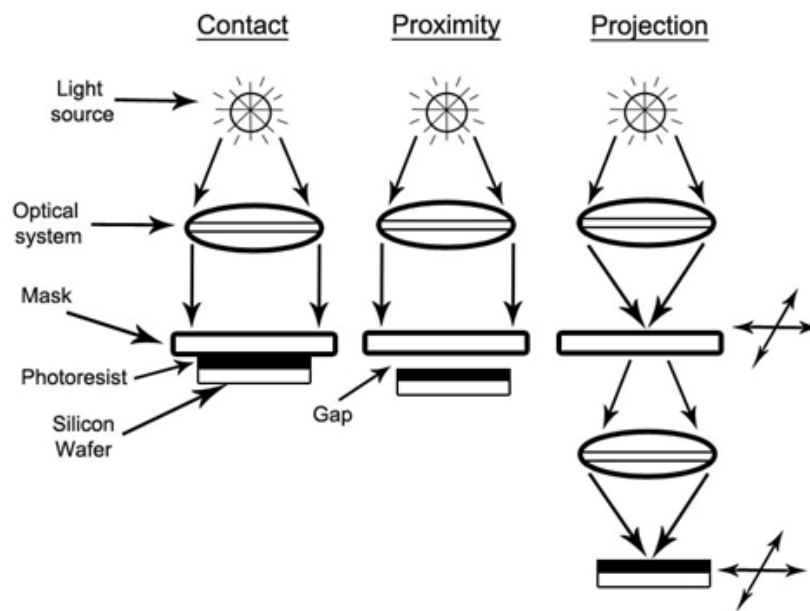
FIGURE 3.8: Different modes of projection in UV photolithography [Reprinted from (14)]

15-30 seconds. A small quantity of resist is dispensed in the centre of the spinning wafer. The rotation causes the resist to be spread across the surface of the wafer with excess being thrown spun off. Preparation of the resist is concluded by a pre-bake, where the wafer is a gently heated in a convection oven (as is the case for positive S181 photoresist used extensively in this work) or on a hotplate (for negative SU8 resist).

3.1.6.2   Exposure

Depending on the design of the photolithography machine, the mask may be in contact with the surface, very close to the surface or used to project the mask onto the surface of the substrate. These methods are called, not surprisingly, contact, proximity and projection respectively. Figure 3.8 shows a schematic diagram of these methods. The projection system is the most complex method, but does mean the projection of the mask can be scaled. The limit of the feature size is limited by the diffraction limit and depends on the size of the wavelength of light used to illuminate the mask.

3.1.6.3   Development

During the exposure process, the resist undergoes a chemical reaction. Depending on the chemical composition of the resist, it can react in two ways when the light strikes the surface. The action of light on a positive resist causes it to become polymerised where it has been exposed to the light. A negative resist has the reverse property. Exposure to
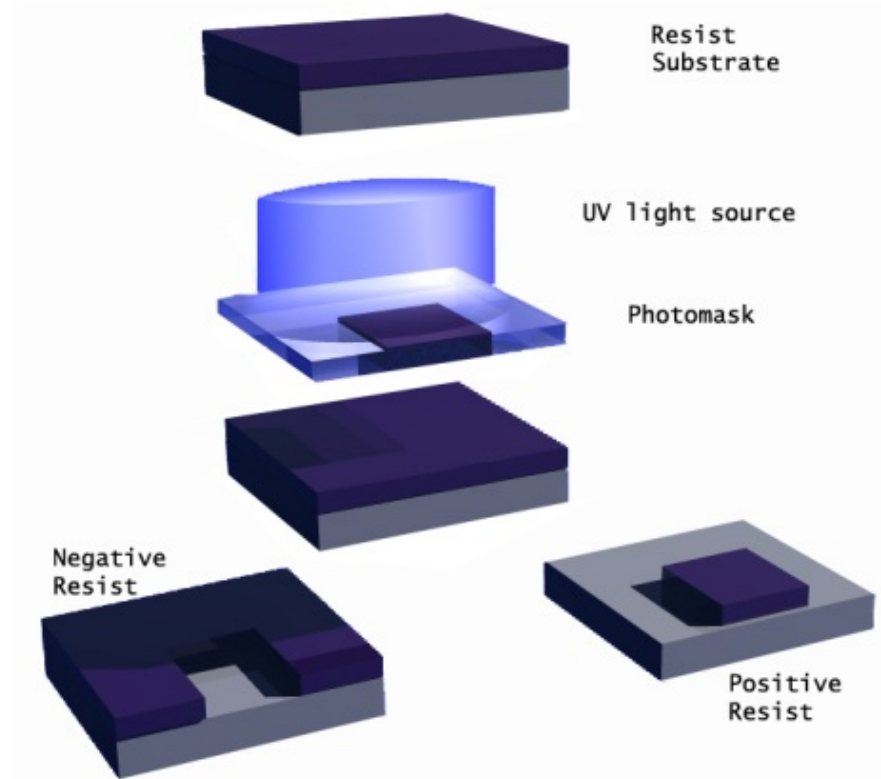
FIGURE 3.9: Simplified process diagram for the photolithography tehcnique.

UV light causes the resist to decompose. During the developing process depending on the resist used either the pattern or the negative of the pattern on the mask will remain on the sample. This may be followed by post exposure bake. This process is represented in Figure 3.9.

3.1.7 Etching

Etching is used in microfabrication to chemically remove layers from the surface of a wafer during manufacturing. Etching is a critically important process module, and every device undergoes many etching steps before it is complete, either for cleaning or structure formation purposes. The two fundamental types of etchants are liquid-phase ("wet") and plasma-phase ("dry"). Each of these exists in several varieties. In this report, dry etching was chosen as the choice of etching. This is due to the disadvantage of wet etching in the undercutting caused by the isotropy of the etch. The purpose of dry etching is to create an anisotropic etch - meaning that the etch is uni-directional. An anisotropic etch is critical for high-fidelity pattern transfer.

3.1.7.1 Reactive ion etching

Plasma is initiated in the system by applying a strong RF (radio frequency) electromagnetic field to the wafer platter. The field is typically set to a frequency of 13.56 megahertz, applied at a few hundred watts. The oscillating electric field ionizes the gas molecules by stripping them of electrons, creating a plasma. In each cycle of the field, the electrons are electrically accelerated up and down in the chamber, sometimes striking both the upper wall of the chamber and the wafer platter. At the same time, the much more massive ions move relatively little in response to the RF electric field. When electrons are absorbed into the chamber walls they are simply fed out to ground and do not alter the electronic state of the system. However, electrons stripped from the wafer platter cause the platter to build up charge due to its DC isolation. This charge build up develops a large positive voltage on the platter, typically around a few hundred volts. The plasma itself develops a slightly negative charge due to the higher concentration of negative ions compared to free electrons. Because of the large voltage difference, negative ions tend to drift toward the wafer platter, where they collide with the samples to be etched. The ions react chemically with the materials on the surface of the samples, but can also knock off (sputter) some material by transferring some of their kinetic energy. Due to the mostly vertical delivery of reactive ions, reactive-ion etching can produce very anisotropic etch profiles, which contrast with the typically isotropic profiles of wet chemical etching. Etch conditions in an RIE system depend strongly on the many process parameters, such as pressure, gas flows, and RF power.

The advantage of reactive ion etching is its speed and selectivity as well as its anisotropy
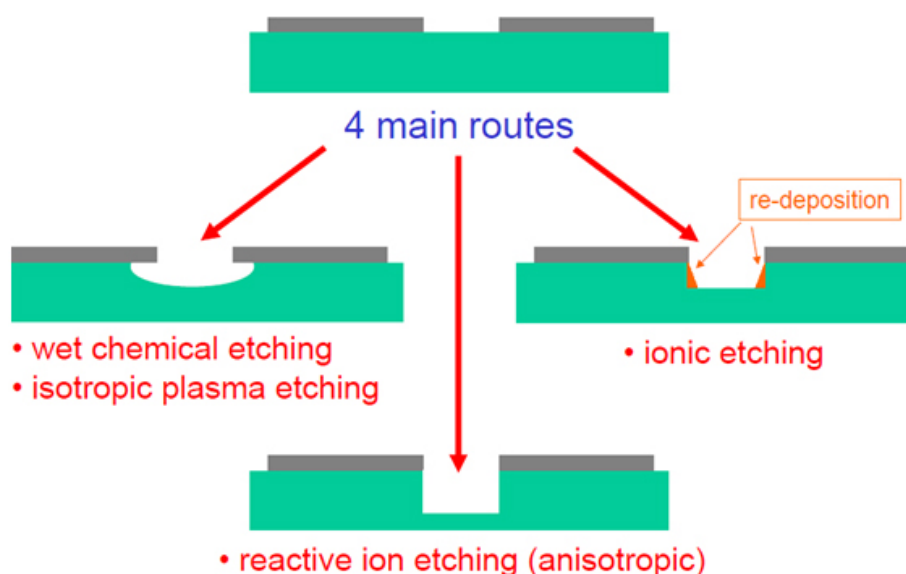
FIGURE 3.10: Different types of wet and dry etching each exhibiting different etch profiles, as a result each type of etching process has its own specific applications and one must choose the type of etch very carefully [Reprinted from (15)].
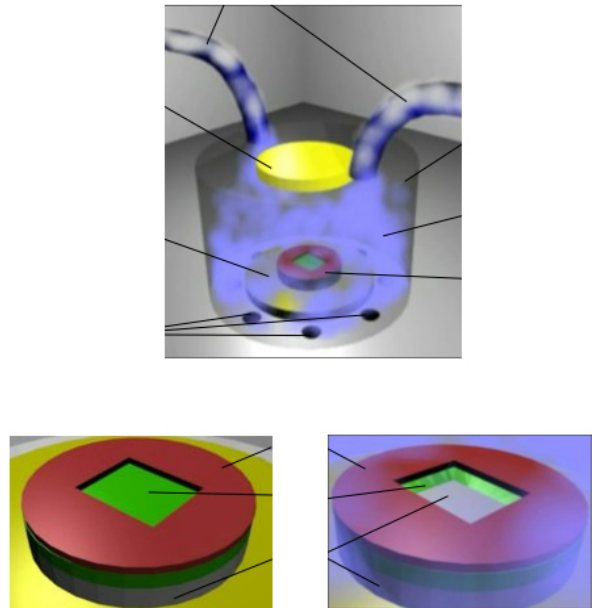
FIGURE 3.11: Simple model of reactive ion etching [Reprinted from (15)].
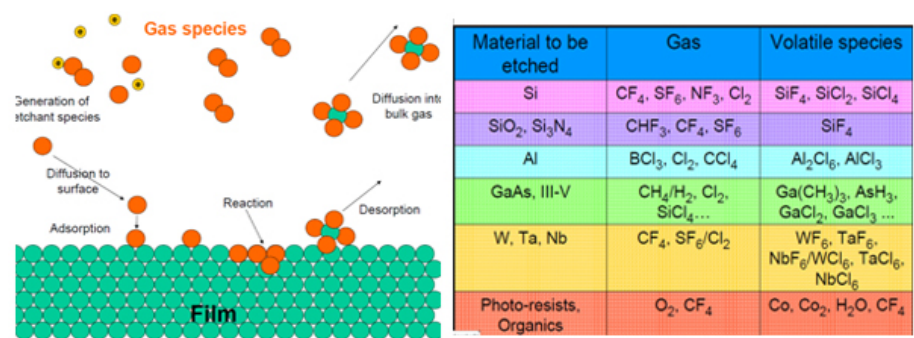
FIGURE 3.12: (left) Reactive ion etching, showing the interaction of species with sample surface. (right) Common materials with the respective plasma gas capable of etching these materials, along with the volatile species which are created in the chamber in order to etch the surface of the material [Reprinted from (15)].

which lends itself very well to strutural formation using passivation layers such as photoresists (Figure 3.10–3.12). It should also be noted that as opposed to other dry ion beam etching techniques, reactive ion etching does not bring about re-deposition during the etching process, making it a relatively low contamination process, this coupled with its wide reaching material capability makes it a great tool for device fabrication (Figure 3.12).

3.2   Characterisation

3.2.1   Scanning electron microscopy

Scanning electron microscopy (SEM) is one of the potential methods widely used for materials and surface analysis. It makes use of an energetically well-defined and highly focused beam of electrons that scans across the sample. The electrons interact with the atoms of the surface layers producing signals that contain information about the surface topography, elemental composition and other properties such as electrical conductivity.

Most of the energy of an incident electron beam will eventually end up heating the sample (phonon excitation of the atomic lattice); however, before the electrons come to rest, they undergo two types of scattering: elastic and inelastic. Back scattered electrons are produced from the elastic scattering events. Inelastic interactions produce diverse effect including:

- phonon excitation (heating).

- cathodoluminescence (visible light fluorescence).

- characteristic X-ray radiation.

- plasmon production (secondary electrons).

- Auger electron production (ejection of outer shell electrons).

Figure 3.13 (though it is given for a thin foil) can also be referred for the various signals from the interaction volume due to the electron bombardment. However, the interaction volumes in TEM and SEM are principally different;. In SEM, the interaction volume is a teardrop shaped volume of the specimen, where the primary electron beam interacts with the sample. This volume extends from less than 100 nm to around 5 μm into the surface (Figure 3.13). The size of the interaction volume depends on the energy of the impinging primary electrons, the atomic number of the specimen and the specimen's density. Figure 3.13 schematically illustrates the interaction volume for various portions of electron-specimen interactions.

By detecting the signals coming out of the sample with suitable detectors, several types of information can be extracted. A schematic diagram of a typical SEM setup is given in Figure 3.14. The electron beam (with an energy range up to 40 keV) is generated typically from a thermionic electron source or a FEG. The electromagnetic lens system (condenser and objective) focuses the beam into a very fine spot with sizes of 1 to 10 nm. A set of scan coils (or deflector plates) placed closer to the objective lens is used to deflect the beam in two orthogonal lateral directions so that it scans a rectangular area of the sample surface. Electronic devices are used to detect, amplify and display the

signals from the sample as an image (or 2D plot) on a display screen (cathode ray tube) in which the raster scanning is synchronized with that of the microscope. The image displayed is therefore a distribution map of the intensity of the signal being emitted from the scanned area of the specimen. The image may be captured on a photographic plate from a high resolution cathode ray tube, but in modern machines it is digitally captured and displayed on a computer monitor.

The most common imaging mode collects the low energy (< 50 eV) secondary electrons. Due to their low energy, these electrons originate from the top few nanometers below the sample surface. These electrons are typically detected by an Everhart-Thornley detector which is a type of scintillator photomultiplier device. The brightness of the signal depends on the number of secondary electrons reaching the detector. If the beam enters the sample perpendicular to the surface, then the activated region is uniform about the axis of the beam and a certain number of electrons escape from the sample. As the angle of incidence increases, the escape distance of one side of the beam will decrease, and more secondary electrons will be emitted. Thus steep surfaces and edges tend to be brighter than flat surfaces, which results in images with a well defined three dimensional appearance.

3.2.2 Energy dispersive x-ray spectroscopy

Elemental composition analysis is the second most commonly used feature of SEM, called EDX (energy dispersive X-ray spectrometry). X-rays are emitted when the electron beam removes an inner shell electron from the sample, causing a higher energy electron
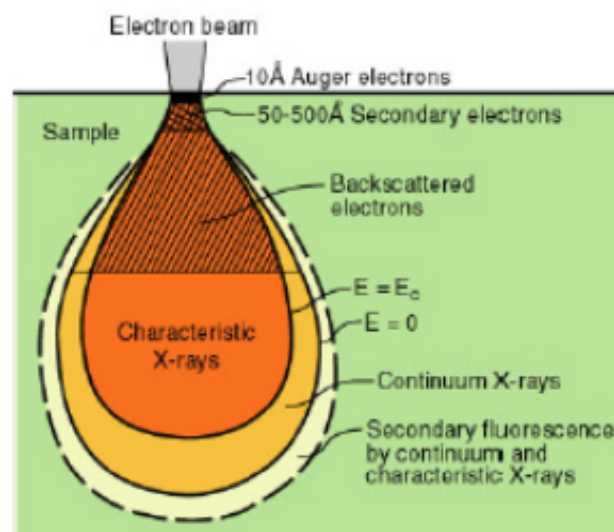
FIGURE 3.13: Interaction volume showing the regions of various electron-specimen interactions [Reprinted from (16)].
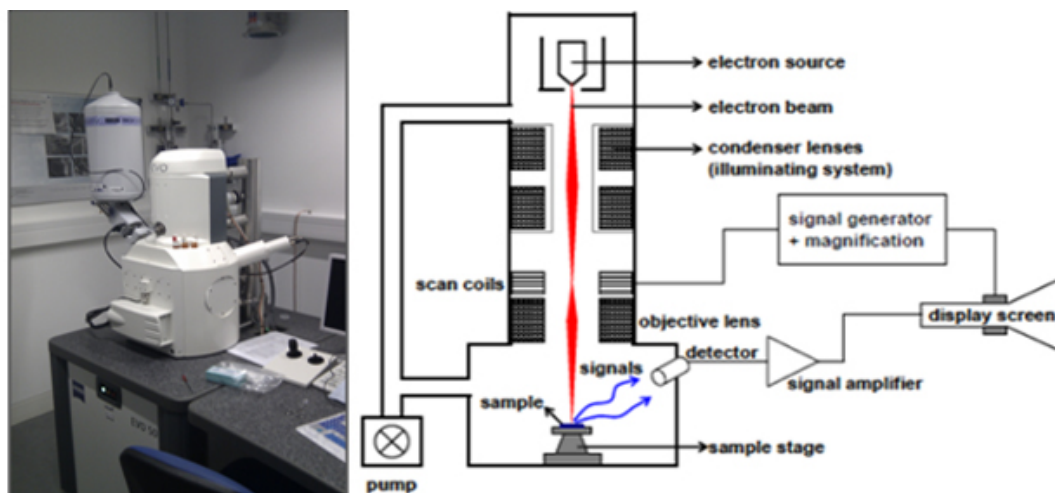
FIGURE 3.14: (left) The ORC Scanning electron microscope facility. (right) Schematic diagram of a typical scanning electron microscope [Reprinted from (16)].

to fill the shell, whereby energy is released. These characteristic X-rays, detected by an X-ray analyzer, are used to identify the elemental composition of the sample.

3.2.3   Infrared spectrophotometry

The UV-visible-NIR microspectrophotometer is an instrument used to measure spectra of microscopic samples or microscopic areas on samples. There are two major classes of devices: single beam and double beam. A double beam spectrophotometer compares the light intensity between two light paths, one path containing a reference sample and the other the test sample. A single beam spectrophotometer measures the relative light intensity of the beam before and after a test sample is inserted. Although comparison measurements from double beam instruments are easier and more stable, single beam instruments can have a larger dynamic range and are optically simpler and more compact. Additionally, some specialized instruments, such as spectrophotometer built onto microscopes or telescopes, are single beam instruments due to practicality. Historically, spectrophotometers use a monochromator containing a diffraction grating to produce the analytical spectrum. The grating can either be movable or fixed. If a single detector, such as a photomultiplier tube or photodiode is used, the grating can be scanned stepwise so that the detector can measure the light intensity at each wavelength (which will correspond to each "step"). Arrays of detectors, such as charge coupled devices (CCD) or photodiode arrays (PDA) can also be used (see Figure 3.15) . In such systems, the grating is fixed and the intensity of each wavelength of light is measured by a different detector in the array. Additionally, most modern mid-infrared spectrophotometers use a Fourier transform technique to acquire the spectral information. The technique is called Fourier Transform Infrared.

When making transmission measurements, the spectrophotometer quantitatively compares the fraction of light that passes through a reference solution and a test solution. For reflectance measurements, the spectrophotometer quantitatively compares the fraction of light that reflects from the reference and test samples. Light from the source lamp is passed through a monochromator, which diffracts the light into a "rainbow" of wavelengths and outputs narrow bandwidths of this diffracted spectrum. Discrete frequencies are transmitted through the test sample. Then the photon flux density (watts per metre squared usually) of the transmitted or reflected light is measured with a photodiode, charge coupled device or other light sensor. The transmittance or reflectance value for each wavelength of the test sample is then compared with the transmission (or reflectance) values from the reference sample. In short, the sequence of events in a modern spectrophotometer is as follows:

1. The light source is imaged upon the sample.

2. A fraction of the light is transmitted or reflected from the sample.

3. The light from the sample is imaged upon the entrance slit of the monochromator.

4. The monochromator separates the wavelengths of light and focuses each of them onto the photodetector sequentially.

In this work two infrared spectrophotometers have been predominantly utilised the CRAIC UV-VIS-NIR microspectrophotometer for NIR part of the spectrum while JASCO FTIR microspectrophotometer has been used for the Mid infrared [See Figure 3.16].

3.3 Elevated temperature measurements

The properties of phase change materials drastically change upon crystallisation. This transition is initiated at a defined temperature. Since the properties of the material change, they can be observed as electrical resistivity, optical transmission and reflectivity changes. Also the exothermic crystallisation reaction and the endothermic melting
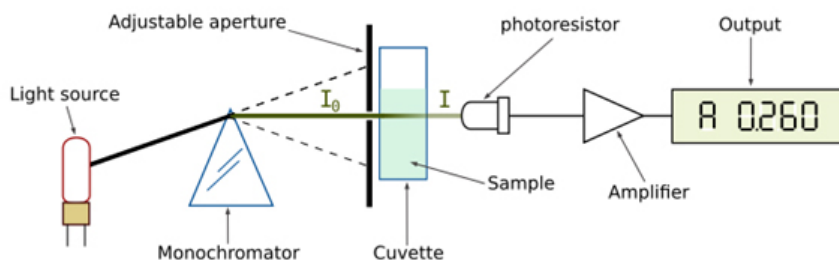
FIGURE 3.15: schematic diagram of an infrared spectrophotometer.

FIGURE 3.16: (left) CRAIC microspectrophotometer for NIR measurements. (right) Jasco micro spectrophotometer for Mid IR measurements.
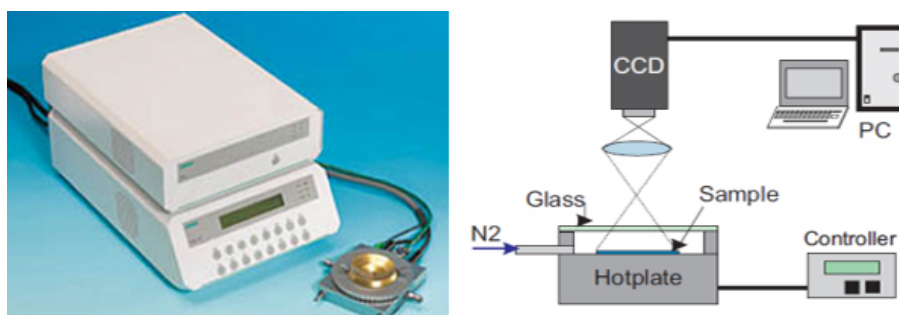
FIGURE 3.17: Heating stage enabling thermal optical microscopy.

transition can be measured using Differential Thermal Analysis (DTA), but bulk or powdered samples are required for this.

In this thesis, all of the above techniques have been used to characterise the chalcogenide phase change materials. Optical reflectivity measurements, as a function of temperature, were made on thin film samples by placing the sample on a thin film heating plate and measuring the intensity of the reflected light from the sample with a CCD camera.

The heating ramp rate can be controlled up to $100^oC/min$. The camera is mounted such that the whole of the sample is visible. The camera takes snap shots at a predetermined temperature resolution. To raise the temperature of the sample, a Linkham Scientific TK1500 microscope furnace was used (See Figure 3.17). One can observe the effect of high temperatures on devices and thin films, e.g the crystallisation and melting point of thin films can be observed very easily using this technique.

3.3.1 Differential scanning calorimetry

Differential Scanning Calorimetry (DSC) has been traditionally used to measure glass transitions, in a wide array of disciplines including food science, pharmaceuticals, and materials science. In a typical experiment, a few tens of milligrams of a sample encapsulated in an Al pan with a lid, and a second identical pan and lid with no sample used as a reference pan, are heated at a fixed scan rate typically of $10^oC/min$. The difference in heat flow between a sample and a reference displays an endotherm near a glass transition event as a sample softens and atomic mobility increases (Figure 3.18).

The basic principle underlying this technique is that when the sample undergoes a physical transformation such as phase transitions, more or less heat will need to flow to it than the reference to maintain both at the same temperature. Whether less or more heat must flow to the sample depends on whether the process is exothermic or endothermic. For example, as a solid sample melts to a liquid it will require more heat flowing to the sample to increase its temperature at the same rate as the reference. This is due to the absorption of heat by the sample as it undergoes the endothermic phase transition from solid to liquid. Likewise, as the sample undergoes exothermic processes (such as crystallization) less heat is required to raise the sample temperature. By observing the difference in heat flow between the sample and reference, differential scanning calorimeters are able to measure the amount of heat absorbed or released during such transitions. DSC may also be used to observe more subtle phase changes, such as glass transitions.

If the scan rate is lowered from e.g $10^oC/min$ to $3^oC/min$, the endothermic signal strength decreases by a factor of 3/10 and shifts to a lower temperature. The inflexion point of the endotherm is generally used to define Tg. The lowering of scan rate dT/dt (where t is the time) lowers the signal strength, but it also lowers Tg because of the
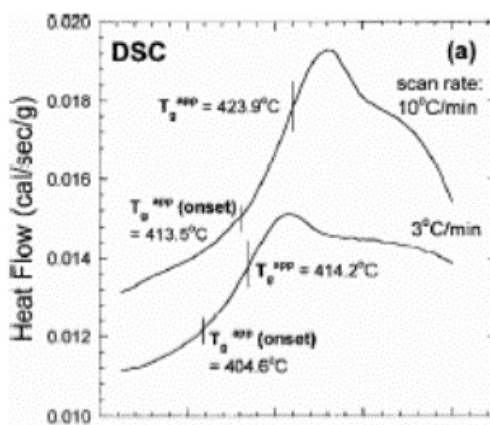
FIGURE 3.18: DSC curve showing glass transition,crystallisation and melting points as observed from such a measurement [Reprinted from (17)].

kinetic nature of the glass transition. The rate of heat flow can be written as

$$dH/dt = mCp^k(dT/dt),$$

where H designates the quantity of heat flow to a sample of mass m with a kinetic specific heat Cp^k. To increase dH/dt, it is customary to increase the scan rate (dT/dt). This has the effect of up-shifting glass transition temperatures as well. Such shifts have been used to extract activation energies for enthalpy relaxation near Tg.

Chapter 4

Data Storage

4.1 Background

Phase change based data storage devices can be categorised into two main categories:

- Optical Recording (CDs, DVDs, Bluray Disks)

- Electrical Recording (Phase Change Memory)

Each has its own specific applications. Optical recording is a well-established technology in widespread use and will be discussed in chapter 6. However, the use of phase change as an electronic data storage medium has been the focus of a great deal of research in recent years. The prospect of having a low power, fast switching data storage medium that can be highly scalable with lower fabrication costs lends itself very well to the different properties of chalcogenides with phase change properties. Thus electronic phase change data storage has been touted as a possible replacement for FLASH memory, which is currently the market leader.

With a view to exploring the use of unconventional chalcogenide alloys as a means to producing low power phase change data storage devices, the work here was carried out with three main phase change alloys, namely germanium antimony telluride, gallium lanthanum sulphide and germanium antimony. A brief overview of current research in the area of electrical phase change is set out here followed by an account of the work carried out in this project.

4.1.1 Electrical phase change

Electrically induced phase change within chalcogenide alloys can be achieved when a specific electric field known as the threshold electric field is applied to a material and

the glass switches from a high resistance, amorphous state to a low resistance crystalline state.

Through the use of electrical switching two distinct phenomena occur depending on the characteristics of the material and the size and duration of the pulse or sweep being applied:

- Threshold Switching

- Memory Switching

Threshold switching is exhibited when on the removal of the electric field the chalcogenide glass reverts back to the initial high resistance state. This occurs if the current flow through the glass is below what is known as the holding current I_h; However if this current is exceeded memory switching occurs as the alloy remains stable in the new low resistance, crystalline state.

The underlying mechanism responsible for electrical switching within chalcogenides has been widely debated and investigated. Adler and Peterson proposed a model for electrical switching based on charge defect states known as Valence Alternation Pairs (VAP) which was later also shown experimentally by Henisch (96; 97). This model proposes that switching occurs when field excited charge carriers fill up the charge defect states within the alloy structure. When all the defect sites are filled, the lifetime of any further charge carriers being introduced increases significantly beyond the thickness of the material. Thus a sudden drop in resistance is observed as the material switches to a much more conducting state (98; 99; 100; 101; 102). Through experimental evidence it is shown that the switch to a much more conducting state within an amorphous chalcogenide alloy occurs in too short a time span to allow any significant thermal effects to take place. This model explains to a high degree the occurrence of threshold switching.

To explain the change from amorphous to crystalline within chalcogenide alloys one can refer to the evidence of a hot central filament being formed in the switched region due to Joule heating (74). If the heat within this current carrying filament is able to induce phase change in the material structure, a subsequent change from the amorphous to the crystalline state, i.e. memory switching occurs.

Amalgamating the two models, it can be derived that after the initial threshold switching stage, the increase in conductivity leads to increased power dissipation within the sample, this brings about a rise in the temperature of the conducting filament due to Joule heating. This rise in temperature in itself increases the conductivity of the filament, further increasing the temperature as a result. This intertwining cyclic series of events eventually leads to the temperature rising above the crystallisation temperature of the chalcogenide alloy and as a result phase change occurs and we observe a sudden drop in resistance.

4.1.1.1 Electrical switching parameters

Through the use of electrical switching a number of material properties can be observed. The snapback within the I-V characteristics is observed when the threshold voltage is reached and distinguishes between the high and low resistance states. It has been suggested that the snapback itself is not a material property parameter but as a result of the load resistance of the measurement systems reacting to the sudden change in resistance (103). These are discussed using a typical I-V characteristic for a phase change cell shown in Figure 4.1.

Parameters which are important to understand electrical switching are defined as:

- Threshold voltage is the voltage at which the material switches to a low resistance state. This depends on the sample thickness, type of switching source and natural resistivity of the material.

- High/Low resistance ratio: the resistance of the high resistance state can be obtained by looking at the inverse of the gradient of the I-V curve below the threshold and by doing the same for the post threshold region the ratio can be obtained.

- Switching time: the time that the material takes to change its state from amorphous to crystalline and vice versa.

- Delay time occurs when the threshold voltage is exceeded, the alloy will not switch to a low resistance state immediately, thus this delay between the application of the pulse and the switch is known as the delay time. The higher the voltage is above the threshold voltage the shorter the delay time.

- Lock time is determined when the phase change alloy switches to a low resistance state; to do so it should be held in this state to stabilise, this period of time is known as the lock time. If the switching is initiated by a pulse and if the pulse
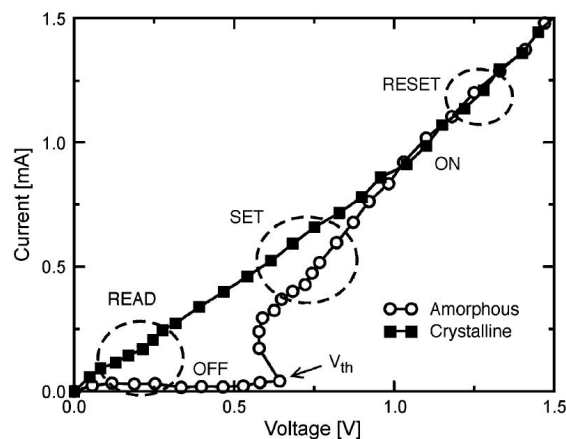
FIGURE 4.1: Typical I-V Characteristics of an OUM cell [Reprinted from (18)].

width is less than the sum of the delay and lock time, the memory switch will revert back to its initial high resistance state. The lock time is a characteristic of the sample and it also depends on the applied over voltage.

- Recovery time is the post threshold switching time needed for the material to recover to its initial higher resistance state when the current is reduced.

Of particular interest in phase change memory cells is the set and reset times, which is the electrical characteristic needed in a pulse or sweep to crystallize and subsequently melt and quench the sample in order to bring back to an amorphous state. The biggest challenge to the commercialisation of PCRAM devices is the high set and reset currents required to program these devices between the two resistance states, as well as their low stability at elevated temperatures. The focus of this work is addressing these paramters by using more thermally stable high resistance chalcogenide alloys.

4.1.2   Electrical phase change devices

4.1.2.1   Materials

Some chalcogenides are stable in both amorphous and crystalline phases (104; 83). These materials are of particular interest for phase change data storage applications. As such a great deal of work has been done around the GeSbTe family of materials for electronic data storage. The lowest current consumption reported thus far for a GeSbTe based electronic phase change memory cell has been demonstrated by Xiong et al (19) (Figure 4.2). In this instance carbon nanotubes have been used as nanoscale electrodes in a lateral line-type cell and as such the volume of phase change material needed in order to achieve on/off switching is minimised, lowering the current consumption considerably.

When reviewing the work done within the GeSbTe family of electronic data storage with a view to power consumption, one should also note the recent demonstration by Simpson
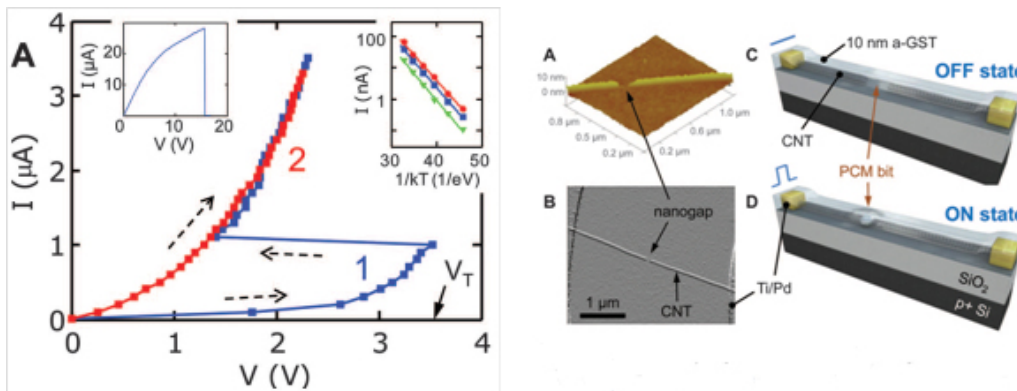
FIGURE 4.2: Carbon nanotubes as electrodes has been demonstrated as a means of achieving low current consumption devices [Reprinted from (19)].
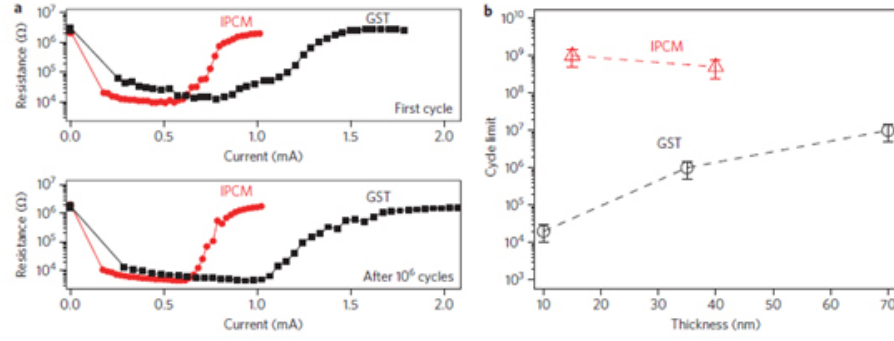
FIGURE 4.3: phase change memory concept known as iPCM exhibiting high stability
and low power consumption [Reprinted from (20)].

et al (20) of a "iPCM" (interfacial phase change memory) devices (Figure 4.3) which
rely on a GeTe/Sb$_2$Te$_3$ superlattice configuration through ultra-thin alternating GeTe
and Sb$_2$Te$_3$ layers in a crystalline phase. The mechanism proposed for these types of
cells, relies on a change in the angle of the germanium atom in the superlattice on the
interface of these ultra thin layers to achieve an On/off state, they show very low power
consumption and fast switching times, as well as, high relative stability compared with
Ge$_2$Sb$_2$Te$_5$ based memory cells.

Due to the problems discussed previously about the Te motion in the phase change
process, other materials have been explored as a Te free alternative. In particular GeSb
has been demonstrated as an ultrafast switching alternative to the conventional GeSbTe
based devices.
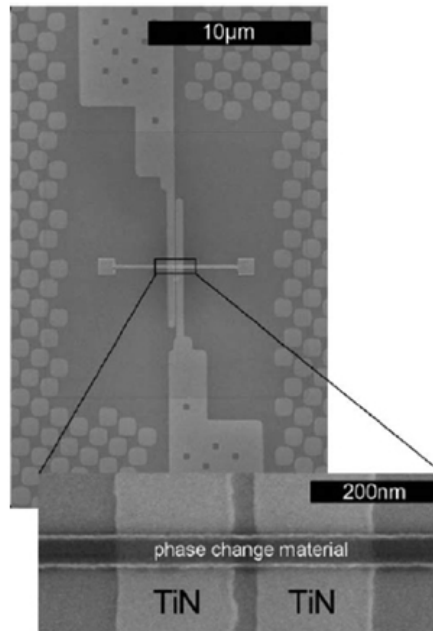
FIGURE 4.4: SEM picture of the demonstrated ultra thin GeSb phase change bridge
memory cell [Reprinted from (21)]

Chen et al (21), demonstrated the first example of a GeSb based phase change memory devices (Figure 4.4), where an ultra-thin nanobridge is used and data retention in the reset state of up to 175°C above that of GeSbTe is obtained along with 60ns set times. All showing a great promise for this novel material, in being a candidate for a highly scaled fast switching device. One should note that further studies have shown problems that can arise from phase segregation in this binary system, which results in the reduction of long term stability.

4.1.3   Sulphide phase change devices

Looking down the chalcogen group of the periodic table from oxygen to polonium, the atomic bonds become more metallic and isotropic, the energy gap decreases and electronegativities decrease. As a result, the electronic conductivity increases (105).

So it seems that in the search for a high thermal stability low power consuming phase change memory cell, sulphur can be a good candidate as a low current consuming alternative to Te and Sb based memory cells. One should keep in mind that low current consumption needs to be alongside a stable phase change as the material used needs to be stable in both amorphous and crystalline phases (104; 83).

In fact sulphide-based phase change materials using a number of physical methods have shown potential as the active medium for data storage. These mechanisms include storage of charges within deep levels in the semiconductor band-gap (106), sulphurization of metallic elements in the film (107) and structural phase transitions (108).

In the field of electronic phase change data storage it has also been demonstrated by Simpson et al (13), that using a copper doped GaLaS thin film, very desirable phase change characteristics can be achieved as seen in Figure 4.5.
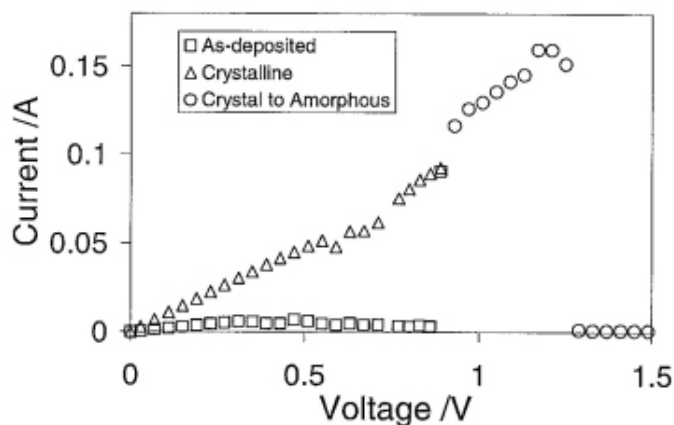
FIGURE 4.5:   I-V characteristics of the previously demonstrated GaLaS:Cu phase change cell [Reprinted from (13)].

The use of gallium lanthanum sulphide shows great promise as a very low power consumption phase change medium. However in this case the copper doping presents an undesirable material within the CMOS fabrication industry.

One should note that gallium lanthanum sulphide exhibits a very high crystallisation temperature with structural studies in crystalline and amorphous phases of the material, showing that GaLaS is made up of Ga-S bonds with a bond length of $2.26\mathring{A}$ and La-S bonds with a length of $2.93\mathring{A}$. The bond lengths are said to be the same in both crystalline and glassy state, during phase change only the bond angles need to change, giving rise to the hypothesis that GaLaS can be a stable fast switching material (83). However in the utilisation of GaLaS, one should note the high crystallisation and melting temperatures of the alloy. These high temperatures need to be accomodated when choosing the structure of the device, in order to be able achieve the desired temperatures and adequate quench rates during operation.

4.1.3.1 Structure

Electrical phase change memory device structures can be split into many distinct architectures, as follows:

- Vertical cells (e.g mushroom cell)

- Lateral phase change (e.g line-type cells)

The more widely used mushroom cell design relies on a heater at the back of the thin film of phase change chalcogenide being heated using electrical power and as a result inducing phase change through Joule heating.

The PCM cell is a two-terminal device consisting of a bottom electrode, a chalcogenide layer and a top electrode. Figure 4.7 displays a sketch of the cell layout for a very general vertical geometry and for the two logic states of the cell.

The cell operation is based on the thermally-induced change of phase in the active chalcogenide layer Figure 4.6. The amorphous phase of the chalcogenide material is characterized by a large resistivity, while the resistivity in the crystalline phase is about 3-6 orders of magnitude lower than in the amorphous phase, depending on the alloy being used. As a result, the chalcogenide phase can be easily recognized by a voltage or current sensing of the cell. The phase in the chalcogenide material can be changed by the application of electrical pulses: to transform the crystalline phase into amorphous, the pulse current must deliver enough Joule heating to raise the temperature above the melting point, thus allowing the transformation in the liquid phase during the pulse.

The liquid phase is then quenched into a disordered amorphous phase. The crystalline phase can be recovered by the set operation, namely with the application of a current
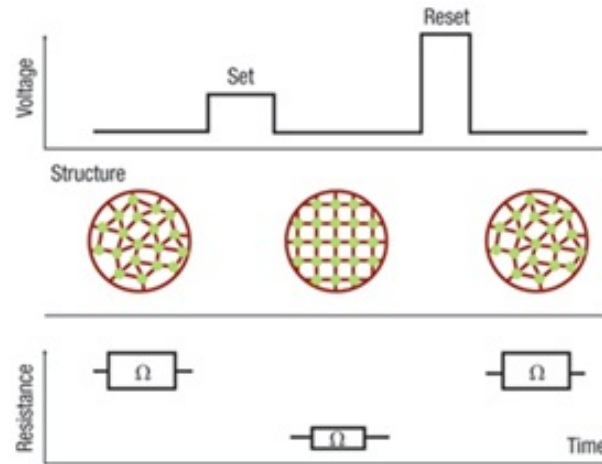
FIGURE 4.6: Set and reset pulses allow the controlled reversible phase change of the material from a high resistance amorphous state to a low resistance crystalline state [Reprinted from (22)].

pulse where Joule heating raises the temperature, high enough to allow for a fast crystallization of the amorphous structure, but below the melting point, in a 100 ns time frame. The amorphous phase occupies a typical dome-shaped volume. This is the case for the so-called mushroom cells (depicted in Figure 4.6).

For efficient Joule heating in the cell, a strong confinement of heat and electrical currents is needed. This is usually made possible by a narrow bottom electrode, also known as the "heater". The heater must dissipate a large power and sustain a large temperature gradient, thus high electrical resistivity and low thermal conductivity are required.

This structure can then be used as the resistance on one of the contacts of a conventional transistor and effectively act as a resistance which shifts the threshold of the transistor as the phase of chalcogenide is switched back and forth (Figure 4.7).
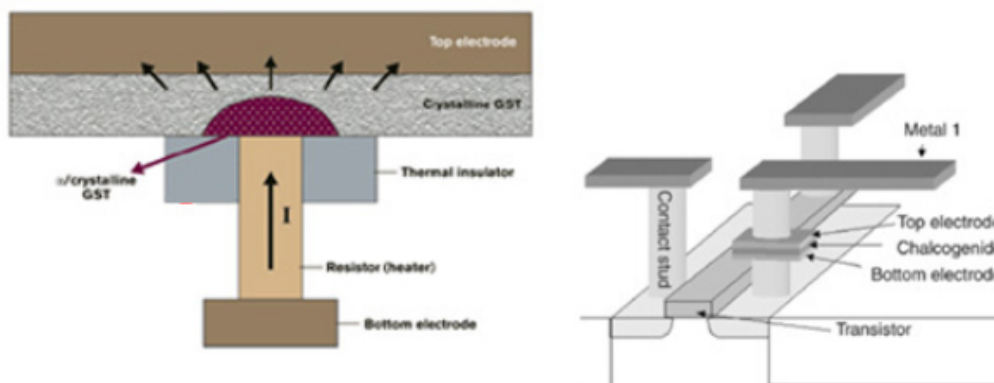
FIGURE 4.7: Typical schematic of a Mushroom cell design and integration into a wider PCRAM [Reprinted from (23)].
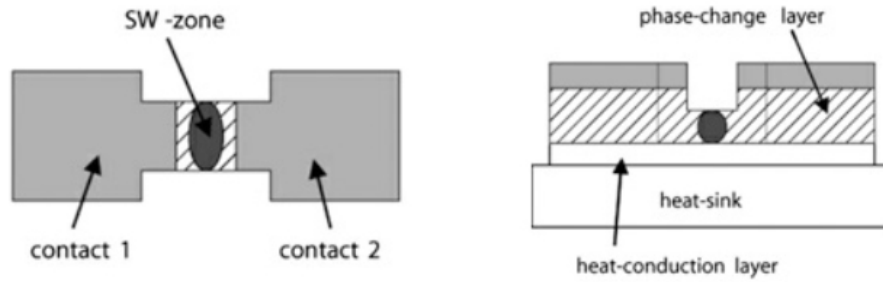
FIGURE 4.8: Typical diagram of a lateral phase change memory cell [Reprinted from (24)].

This is in contrast to the lateral phase concept (Figure 4.8) which is being presented as a low current consumption and higher thermal efficiency device, giving obvious advantages for long term scaling of these devices.

By using a doped SbTe material, researchers from Philips (now NXP) scaled the phase change material by using a lateral "line" type structure. The structure is shown in the (Figure 4.9) (25).

This design decouples the top electrodes from the phase change region which decreases the heat dissipation through the electrode itself as well as allowing rapid cooling using the heat sink which is important for RESET operation of the cell. The two electrodes were made by a TiN layer of 50 nm in thickness. The phase change material, doped SbTe, was deposited by sputtering and then patterned by electron beam lithography and reactive ion etching (RIE). The phase change material extends from the two electrodes and then shrinks to a narrow line structure in the middle between the two electrodes.
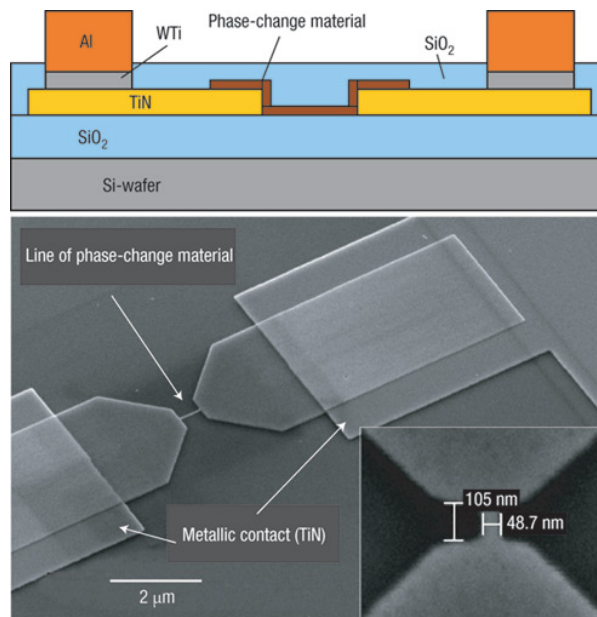
FIGURE 4.9: Schematic plot of the line structure (top) and SEM images of the structure after fabrication (bottom) [Reprinted from (25)].

The high glass transition, Tg, peak crystallisation, Tp, and melting, Tm, temperatures of sulphide based glasses indicates that more heat energy is needed for phase change. However, nanoscale cell dimensions are now possible using conventional fabrication techniques and these high temperatures are achievable. Using a novel line-type cell design, interface reactions can be limited and an increased quench rate is possible. With this in mind, for the investigation of GaLaS as an electronic phase change material, it is deduced that a lateral nanowire type cell, will give the best architecture for sulphide based phase change memory.

This scaling effect is reviewed here with a view of the different structures proposed for high scalability phase change cells. Table 4.1 (18) shows several prototype structures for phase change random access memory devices. The most common type for phase change memory scaling is contact scaling devices; Devices using sub-lithographic contact bottom electrodes and there are many variations of this structure. The edge contact structure is a structure using the advantage of thin film scaling, it is a lateral structure. The micro trench (μ Trench) structure also uses the thin film for scaling. The structure is not only advantageous in scaling the contact area but also in scaling the cell size as it is a vertical cell. The ring structure uses a hollow cylinder bottom electrode for the device. The distribution of the operating current is very tight compared with other structures.

Efforts have also been made in reducing the reset current. In addition to contact scaling cells, devices which scale the phase change materials are also discussed. In particular, the pillar structure is a vertical structure with only one additional mask step for the fabrication, it can reduce the reset current very efficiently with a relatively simple fabrication procedure. The other two lateral structures, line and bridge devices, use lateral thin films to scale down the volume of the phase change region. The cross-sectional area can be effectively reduced but the lateral structure is intrinsically larger than that of the vertical devices.

"Mixed mode" structures are also described. These structures combine different concepts to improve the cell performance. The cross-spacer structure scales both the phase change material and the contact size. The multilevel devices store multiple bits in one cell to increase the data density. The confined structure contains a recessed bottom electrode to reduce the RESET current and several special process technologies are used to fabricate this structure.

4.2   Motivation

The phase change technology behind rewritable optical disks and the latest generation of electronic memories has provided clear commercial and technological advances for the field of data storage, by virtue of the many well-known attributes, in particular scaling, cycling endurance and speed, that chalcogenide materials offer. While the
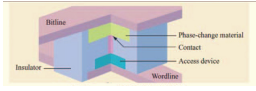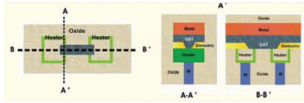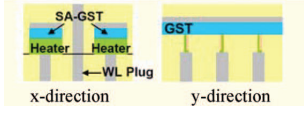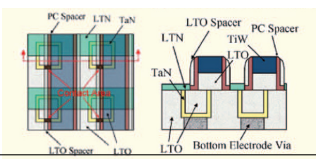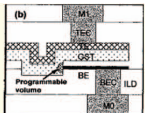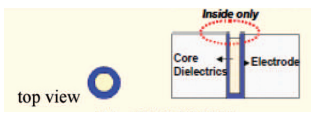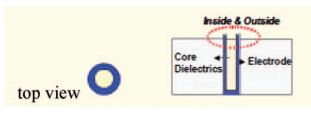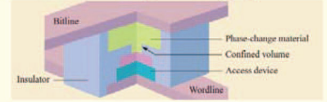
Schematic view	Structure	I_{reset} (μA)	Contact Area (nm^2)	Tech. Node (nm)	Ref.
	mushroom	50-1000	300-3000	N/A	(109)*
	mushroom	160	707	80	(110)
	mushroom	700	3000	90	(111)
	μ-trench	400	90	400	(111)
	μ-trench	600	N/A	180	(112)
	SA μ-trench (wall)	300	400	90	(113)*
	SA μ-trench (wall)	200	N/A	45	(114)
	pore	250	1257	180	(115)
	cross-spacer	80	500	180	(116)
	cross-spacer	230	1000	180	(116)
	edge	200	4000	240	(117)
	ring-shape contact	600	1300	100	(118)*
	ring-shaped contact	600	1300	90	(119)*
	advanced ring-shaped contact	450	1500	100	(120)*
	confined	700	4418	240	(121)
	confined	260	1963	45	(122)
	dash-typed confined	160	487.5	<20	(123)

TABLE 4.1: Different types of PCRAM architectures. * indicates the data was either extracted from figures or are estimated from referenced papers and not directly provided in the literature (18).

switching power and current consumption of established germanium antimony telluride based memory cells are a major factor in chip design in real world applications, often the thermal stability of the device can be a major obstacle in the path to the full commercialisation. In this work we show that phase change media based on the gallium and lanthanum chalcogenides can outperform the well know benchmark performance of germanium antimony telluride devices. Facilitated by high throughput screening of gallium lanthanum sulphides and tellurides, we show these compounds offer set and reset currents over an order of magnitude lower than an equivalent germanium antimony telluride device, while at the same time offering improved thermal stability and the potential for improved endurance.

Our particular interest in the field of phase change memory (PCM) is the discovery of new chalcogenide alloys to potentially outperform the commonly used GeSbTe (GeSbTe). There is a wide range of chalcogenide alloys, range from pure chalcogenides, to pnictogen-chalcogen, tetragen-chalcogen, metal chalcogenides to halogen-chalcogenides (124). Many of these compounds are covered within high-level patent literature, within which a vast array of potential compounds suitable for phase change memory are proposed, yet with relatively few studied in detail (125). Indeed, even among phase change memory cells fabricated with the most conventional GeSbTe compounds, the reasons why these compositions provide us with useful and attractive physical properties are still veiled (126). It is therefore our belief that the field and material space is ripe for a thorough analysis of the compositional space to provide both a better understanding of the range of properties the numerous chalcogenide alloys offer and to optimize the compositions to meet the demands of practical solid state memory.

It has been indicated that GeSbTe based phase change memory devices with a high level of scaling may suffer from very poor thermal stability (71); moreover as applications of GeSbTe based memory cells extend to harsh operational environments such as aerospace and automotives, device performance as temperatures fluctuates will be compromised. These factors along with high current consumption of memory cells based on this alloy pose the biggest obstacle in realising the full commercial potential of PCRAM. Improved stability has already been obtained using Ge-doped Sb:Te (127) and also by replacing Ge completely by Ga (128) ,which allowed device operation at 100°C.

In the work presented here we fully explore the relatively unknown gallium and lanthanum based chalcogenides with a particular focus on both performance and temperature stability. Nanowire memory cells were fabricated with a view to study the effect of high scaling on the power consumption of thermally stable low current consuming chalcogenide alloys. In order to do this device scaling was carried out in two main directions:

- Scaling of electrode contact area - This involves the reduction of the contact size between the electrode and the phase change material by applying techniques to

form sublithographic contacts. Many fabrication techniques have been used in the course of trying to reduce the contact area, along with the structures fabricated will also be presented.

- Volume of phase change material - An alternative method is to scale the volume of the phase change material itself. The size and the thickness of the phase change material were found to influence the RESET current. Hwang et al. explained that the reduction of RESET current is due to current localisation (121). Since the size of the GeSbTe is much larger than the heater, the shape of the current path may affect the RESET current. In addition to the horizontal size, the thickness of the phase change material is also very important for reducing the RESET current.

Through this, a direct comparison of cells with identical geometries and architectures, across a range of phase change volumes, width, lengths and active areas are fabricated and characterised. The only difference in these cells is the active phase change alloy used; one set, using GaLaS and the other utilising GeSbTe as the phase change medium. Therefore, this study, presents a direct comparison regarding the suitability of both materials for electronic phase change memory using cells sizes comparable to state of the art industrial critical features. Thus, this present a method to compare the two alloys for these high density novel electronic data storage technologies which require ultra low power consumption and high thermal stability for full commercial integration within existing computing architectures.

4.3   Micron scale devices

The fabrication work carried for phase change memory section of this project can be categorised into the following categories:

- Microheater structures.

- Nanowire memory cells in the GeSb, GeSbTe and GaLaS family of glasses.

4.4   Thin film devices

The devices created for investigating the effect of scaling on the current consumption of the phase change memory cells were created using a combination of photolithography and sputtering.

The mask shown in Figure 4.10 which contains a series of lines with varying width between 1μm up to 200μm was used as a bottom electrode of the devices.

The bottom electrodes were patterned on a borosilicate glass slide and subsequently a 300nm layer of molybdenum was sputtered on the patterned surfaces. While covering a section of these lines for contact in the characterisation stage, a subsequent second deposition of a 100nm of GaLaS to different alloys was carried out and lifted off to leave us with the devices shown in the Figure 4.11. These devices are characterised using an electrical probe station as shown in section 4.5.1.

4.4.1 Modelling

Electro thermal Joule heating simulations were carried out to better understand the switching dynamics of GeSb nanowires for the purpose of creating highly scaled lateral phase change memory cells.

The model is based on the heat equation as the basis for heat transfer calculations in solids:

$$\rho C_p \frac{dT}{dt} - \nabla.(k\nabla T) = Q,$$

where ρ is the density.
C_p is the heat capacity.
k is the thermal conductivity.   (4.1)
Q is the heat source.

The heat source in our case is an electromagnetic heat source which through an electric current creates a temperature rise as a result of Joule heating which is dependent on the materials electric conductivity, while the thermal conductivity of the material determines the heat distribution across the solid.

The Joule heating due to the electric current is proportional to $I^2 \times R$, where I is the electric current and R is the resistance (inverse of the electric conductivity). The electric conductivity of the material is temperature dependant and is calculated through
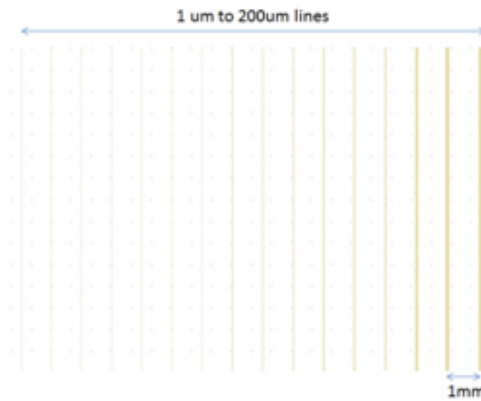
FIGURE 4.10: Lines used for electrodes with varying widths between 1μ and 200μm.
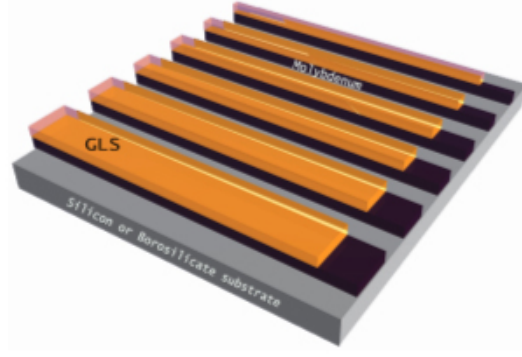
FIGURE 4.11: Simple diagram of final device with varying cell sizes.

the expression below:

$$ElectricConductivity = \frac{1}{p_0(1 + \alpha(T - T_{ref}))},$$

where T is the dependent variable for temperature.

p_0 is the resistivity at initial temperature

α is the temperature coefficient, and (4.2)

T_{ref} is the initial temperature.

The simulations used electrical sweeps to induce a temperature change and thermal mapping of the structures allowed the optimisation and better understanding of the structures and experimental results.

It should be noted that the models were verified experimentally by cross-referencing the predicted temperature of the structures to the optically observed change or electrically
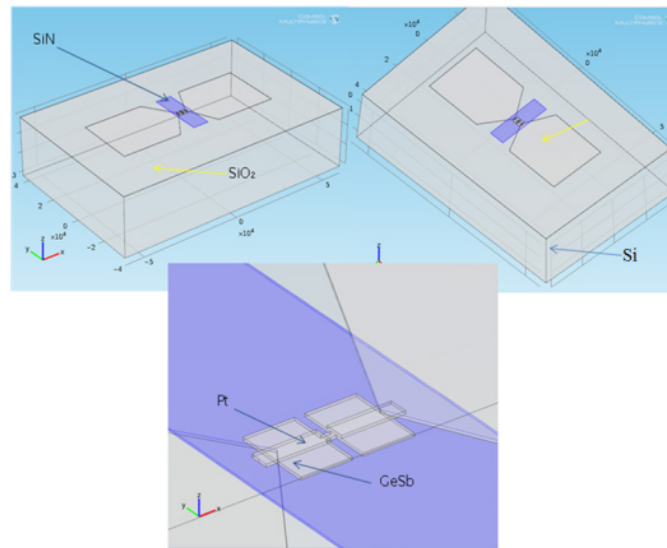
FIGURE 4.12: Overview of the multiphysics model made for the GeSb nanowire cells.

measured resistance change in the fabricated devices, which indicated the hotspot had reached crystallisation temperature.

4.4.1.1   Nanowire modelling

A number of nanowire phase change memory devices were fabricated using the alloy GeSb and characterised. A series of simulations were carried out to better both understand and reaffirm our understanding of the mechanism responsible for their switching ability as set out in our experimental work (see Figure 4.12).

The simulations were carried out across a series of different nanowire lengths and widths as set out in the Table 4.2. These were simulated across a range of different voltages and

Width	Length
100 nm	140 nm
200 nm	300 nm
300 nm	400 nm

TABLE 4.2: Geometries of the nanowires used in GeSb lateral nanowire memory cells.

taking into account the contact resistance of the different layers in relation to each other. Temperature data was taken at the hotspot of the nanowire. The initial temperature condition was set at 293.15 K at 0V.
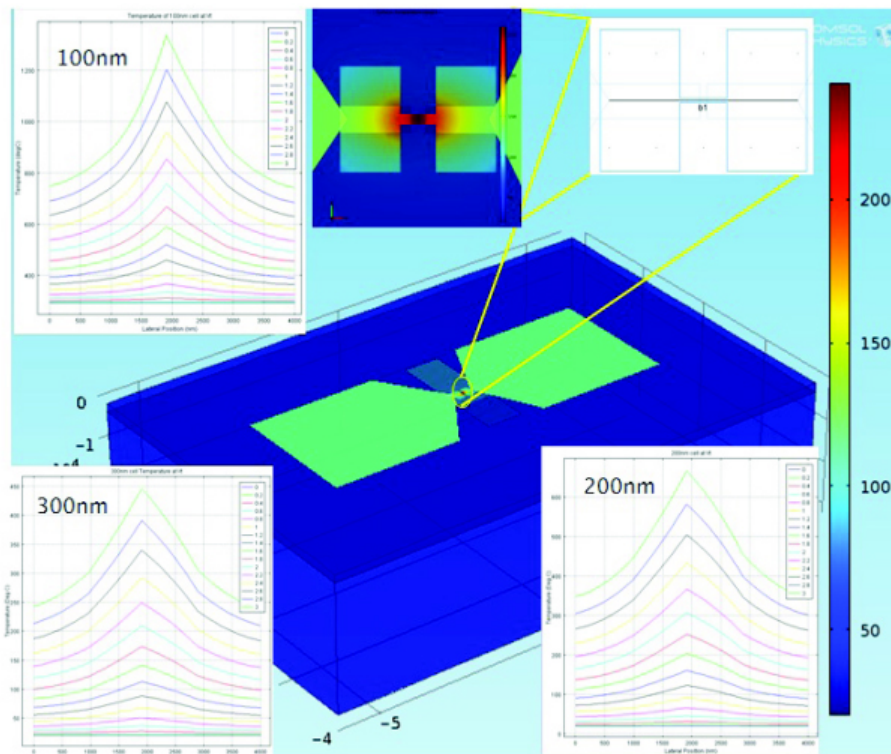
FIGURE 4.13: The multiphysics model and temperature gradient across the nanowire device simulated across the length of the memory cell.

As described previously the electrothermal dynamics of the DC electrical sweeps was modelled using COMSOL multiphysics as shown previously and temperature maps of the devices was obtained (see Figure 4.13). The temperature was simulated across the nanowire cells.

4.4.2   GeSb nanowire PCRAM

Based on the geometries and design concept modelled previously a series of nanowire memory cells with Ge:Sb as the active layer of the device was fabricated. These cells were fabricated in the eutectic composition 15Ge:85Sb.

4.4.2.1   GeSb thin film

Initially a thin film of GeSb was deposited in the in-house CVD system [see Chapter 3]. The microheater design shown previously was used to investigate the electrical phase change of the sputtered thin film. These relatively large cells showed a typical threshold voltage of 2–3.5 volts and set current of up to 100mA. The typical I-V characteristics of these devices is shown in Figure 4.15.

4.4.2.2   GeSb nanowire

Deposition by CVD was followed by FIB milling of the thin film to created isolated nanowire structures. This was followed by an ion beam as well as an electron beam deposition of platinum to contact the nanowire (Figure 4.16). Thus two sets of devices were created in order to also investigate the effect of the process parameters on the characteristics of the memory cells.
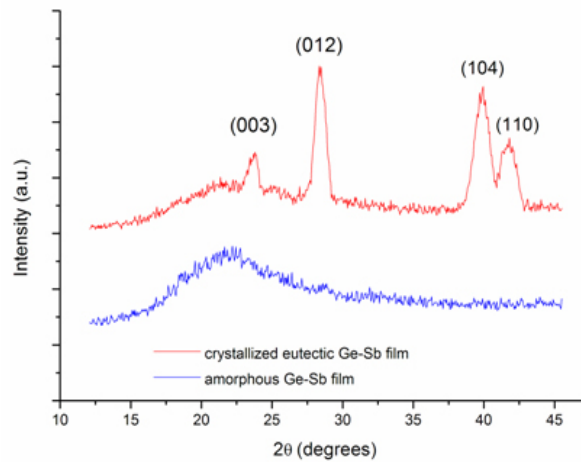
FIGURE 4.14: XRD spectra of amorphous and crystalline CVD grown eutectic Ge:Sb, measurement taken by Dr C. C. Huang.
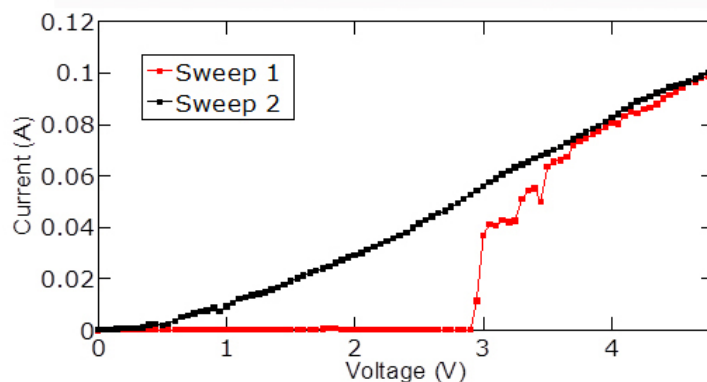
FIGURE 4.15: Typical current-voltage characteristics of a Ge:Sb thin film microheater device.

Next a lithography step was used to define a series of pads for subsequent contacting during the characterisation stage (see Figure 4.16). Once patterned the pads were created using a TiW sputtering deposition.

Finally, deposition of a SiN capping layer using RF Sputtering was performed in order to cap the hot spot of the device and ensure reversible switching (Figure 4.17).

4.4.3 GaLaS nanowire PCRAM

4.4.3.1 GaLaS thin film

For the GaLaS films, the sputtering targets were fabricated in-house by melt-quenching gallium sulphide and lanthanum sulphide powders in a vitreous carbon crucible.
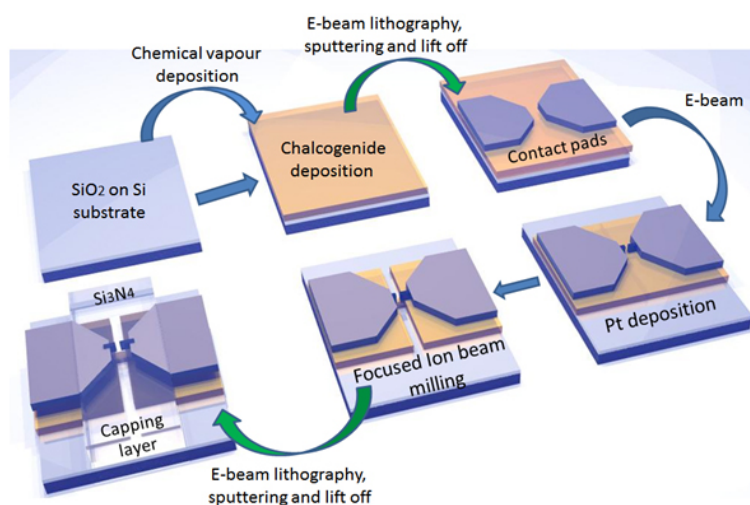
FIGURE 4.16: Process flow diagram showing the fabrication process used for the production of GeSb nanowires.
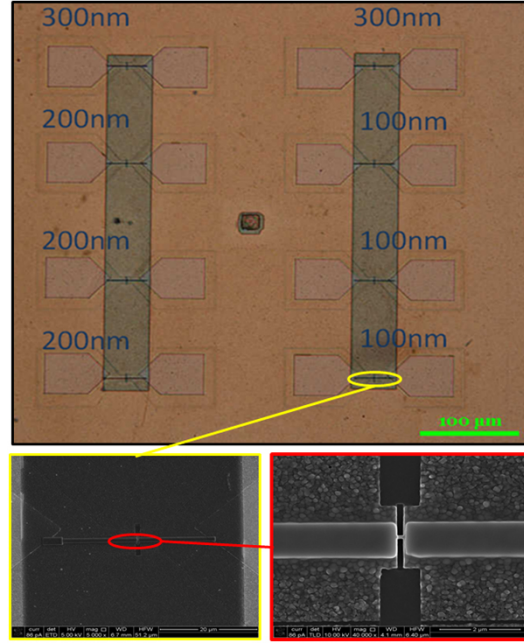
FIGURE 4.17: Microscopy images of GeSb nanowire memory cells.

Deposition took place in a Kurt J. Lesker NANO38- SPUTTER thin film deposition system with a background pressure of 3mTorr. High purity argon was used as the sputtering gas and the distance between the target and the substrate was 150mm. The substrate was kept at room temperature initially and $< 10°$ C temperature increase was observed while the film was being formed. For the GaLaS, the deposition power used was 60W and the argon gas flow was 15ccpm. The film thickness were confirmed using a KLA Tencor P16 Stylus Profiler. Film thicknesses of 15, 30 and 75 nm were deposited in both materials for the final devices.

The composition of the films was found to be 13Ga:7La:30S by EDX. The crystallisation temperature of the sputtered thin film was investigated by using thermal stage microscopy after deposition of a 100nm GaLaS thin film on a silicon substrate. Figure 4.18 shows the experiemtnal setup used. The surface of the sample was monitored using a CCD camera in order to observe the crystallisation and melting point of the thin film.

The electrical characterisation of the above GaLaS thin film device was carried out with a Cascade probe station and Agilent 4155C semiconductor parameter analyser shown in Figure 4.40(b & c). By introducing a voltage sweep between 0-20V, the current across the fabricated cell was measured using the source measure unit within the semiconductor parameter analyser. It should be noted that an internal load resistance within the instrument provides current limitation in order to protect the device. The I-V characteristics of the sputtered GaLaS thin film device are shown in Figure 4.19. These were obtained using a voltage sweep whilst measuring the current as well as using a current sweep whilst measuring the voltage. This revealed three states of the film with
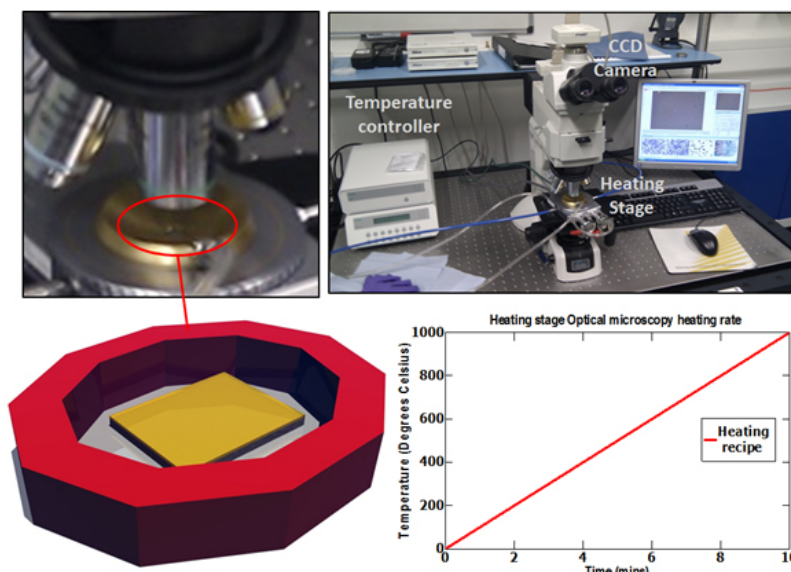
FIGURE 4.18: Thermo-optical microscopy of crystallisation and melting characteristics of thin film chalcogenide films.

a threshold of around 10.1-10.3 V. Starting at a high resistance state and applying the sweep, which at the threshold gives way to the stable phase change (memory switching) by virtue of the Joule heating to above the crystallisation point of the material, subsequent sweeps reveal that the low resistance crystalline state is stable unless switched back to the high resistance through electrically melt quenching the layer. This electrical switching between amorphous and crystalline phases is reproducible at least ten times. The resistance contrast between the two phases is in the order of 10^6, making this result very promising for PCRAM application.

The microheater design shown previously was used to investigate the electrical phase change of the sputtered thin film. These relatively large cells showed a typical threshold voltage of 10–15 volts and set current of up to 10mA, which showed the promise that a sulphide based phase change memory cell holds, in terms of low current consumption (See Figure 4.19). This allowed the continuation of this work in attempting to realise the potential of such thermally stable chalcogenides in highly scaled devices.

4.4.3.2   GaLaS nanowire

A series of devices were fabricated using standard photolithography, reactive ion etching, ion beam milling and ion beam deposition to yield a total of 100 individually addressable cells of varying sizes in the compositions 13Ga:7La:30S. Devices were fabricated on a SiO_2/Si wafer on which the GaLaS was deposited by RF sputtering. A brief overview of the fabrication process used for these devices is set out in the following.
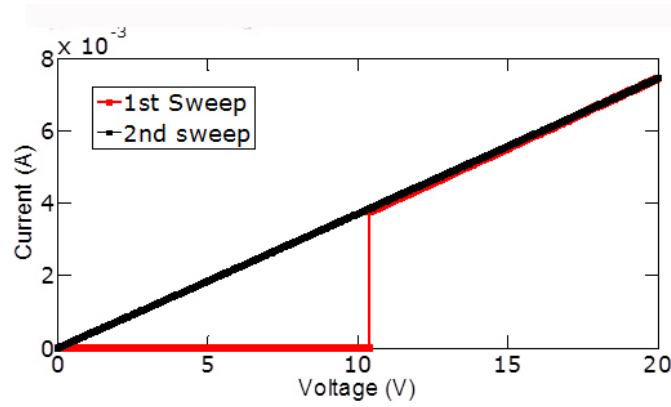
FIGURE 4.19: Typical current voltage characteristics of GaLaS thin film microheater devices.

4.4.3.2.1 Contact fabrication Electrical contacts were provided by molybdenum metal pads which were deposited by sputtering using the process described earlier. The substrate was kept at room temperature and the deposition power used was 100W, with argon gas flow of 15ccpm. The contacts were patterned using photolithography using a positive photoresist (S1805) and the lift-off technique with a pre-deposition oxygen plasma ash (using a 100W plasma power and 10ccpm Oxygen flow), the ashing was also repeated post lift-off to clean the samples of any residue photo resist. The deposition power used was 45W and the argon gas flow was 37cc. Platinum electrodes were then created using electron-beam assisted platinum deposition using a FEI Helios 600 Focused Ion beam. The gap between these electrodes formed the final nanowire or memory cell. A scanning electron microscopy image of a typical cell is shown in Figure 4.21.
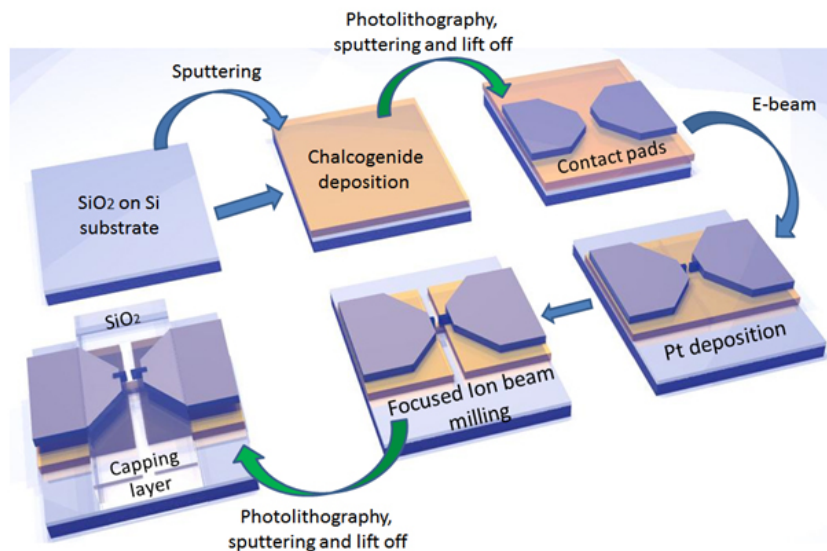
FIGURE 4.20: Process flow diagram showing the fabrication process used for the production of GaLaS nanowires.
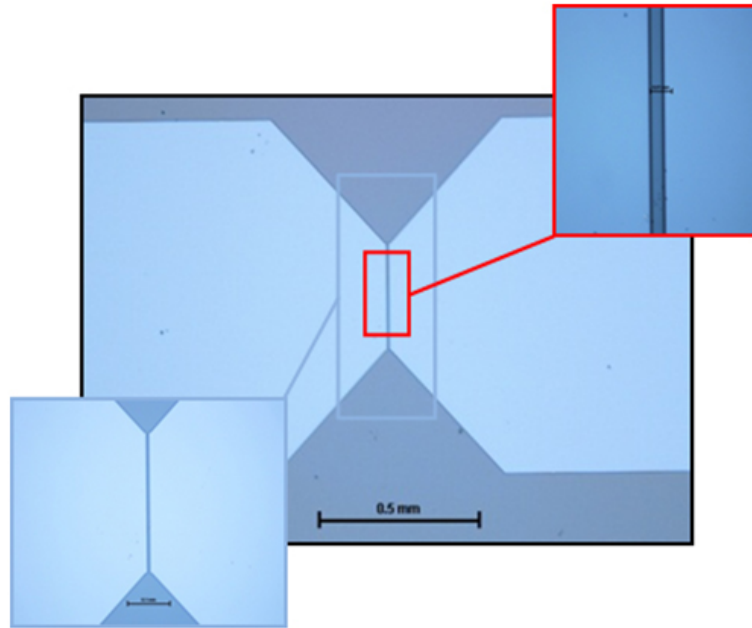
FIGURE 4.21: Optical microscopy images of contact pads fabricated using photolithography, sputtering and the lift-off technique.

4.4.3.2.2 Nanowire fabrication   Trenches were etched in the chalcogenide layers in order to obtain the desired nanowires. These isolated nanowires were created using ion beam milling [see Chapter 3] of the chalcogenide layer to obtain restricted nanowires of different geometries (see Figure 4.22). The resulting nanowires ranged from 40 to 375 nm in length and 50–300 nm in width.

4.4.3.2.3 Capping layer fabrication   To cap the active zone of the memory cell with an appropriate capping layer, a further photolithography step was carried out, followed by a sputtering deposition to produce a SiO_2 capping layer as shown in Figure 4.23.
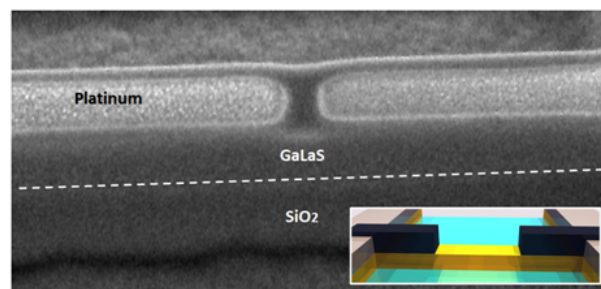
FIGURE 4.22: Scanning electron microscope (SEM) image of GaLaS memory cell formed from two platinum electrodes spaced apart. The chalcogenide layer has been milled away to form the nanowire cell.
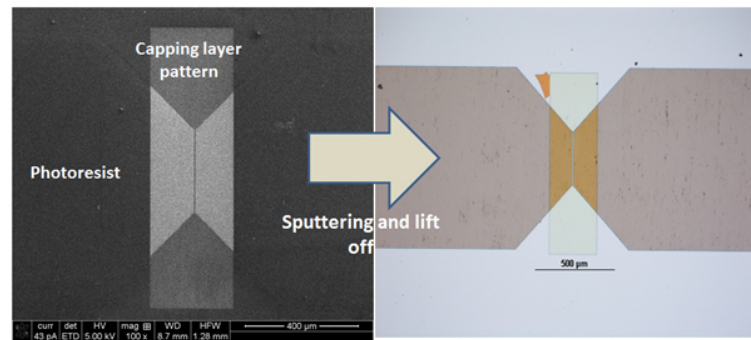
FIGURE 4.23: Fabrication of the capping layer of the memory cells using photolithography, sputtering and lift-off technique, followed by an ashing step to remove any residue photoresist on the sample surface.

4.4.4 GeSbTe nanowire PCRAM

In order to provide a direct comparison of switching parameters with the GaLaS nanowire devices fabricated, the same structure was used in order to fabricate identical memory cells with GeSbTe sputtered film as the active layer. The memory cells shown in Figure 4.28, were produced using the method outlined previously.

4.4.4.1 GeSbTe thin film

The GeSbTe sputtering targets were obtained commercially (Testbourne Ltd. UK) and were nominally of the composition $Ge_2Sb_2Te_5$ (atomic %).

Deposition took place in a Kurt J. Lesker NANO38- SPUTTER thin film deposition system with a background pressure of 3mTorr. High purity argon was used as the sputtering gas and the distance between the target and the substrate was 150mm. The substrate was kept at room temperature initially and minimal $< 10°$ C temperature increase was observed while the film was being formed. For the GeSbTe, the deposition power used was 45W and the argon gas flow was 37cc. The film thickness were confirmed using a KLA Tencor P16 Stylus Profiler. Film thicknesses of 15, 30 and 75 nm were used in both materials in the final devices. EDX and XRD was also used to confirm the composition of the film deposited and crystallised (see Figure 4.24 and Figure 4.25).

Element	Atomic %
Ge K	28.02
Sb L	20.65
Te L	51.33
Totals	100.00
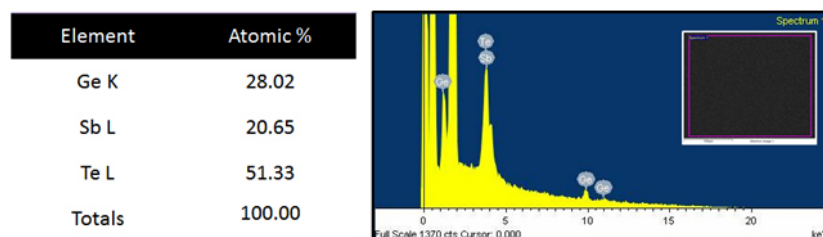
FIGURE 4.24: Energy dispersive X-ray of sputtered 100nm GeSbTe thin film.
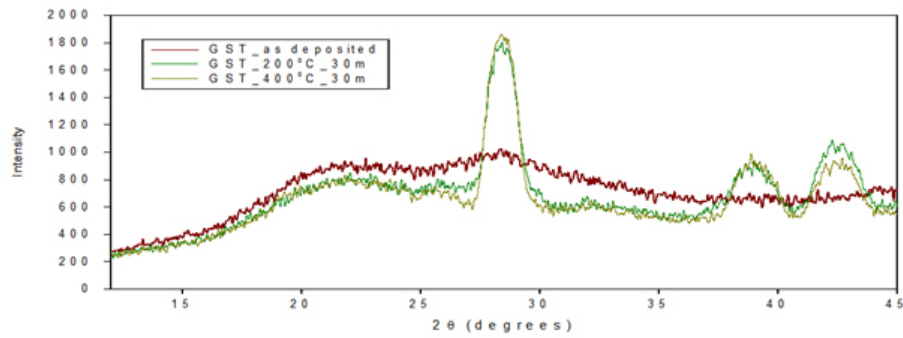
FIGURE 4.25: XRD spectra of GeSbTe thin film with different annealing temperatures.

The microheater design shown previously was again used to investigate the electrical phase change of the sputtered thin film. These relatively large cells showed a typical threshold voltage of around 1.5 - 2.5 volts and set current of up to 50mA, this is in good agreement with literature on electrical phase change of GeSbTe. The typical I-V characteristics of a GeSbTe based device is shown in Figure 4.26.
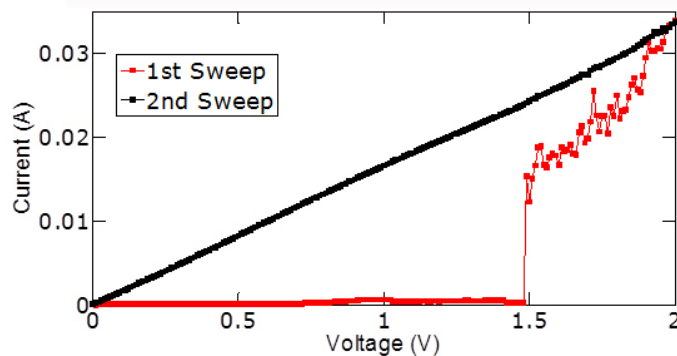
FIGURE 4.26: Typical current-voltage characteristics of GeSbTe thin film microheater device.
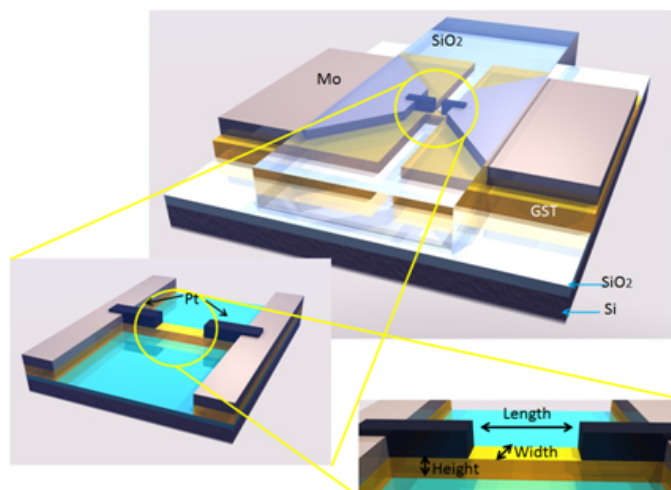
FIGURE 4.27: model of the GeSbTe and GaLaS NW memory cells.

The electrical characterisation of the above Ge-Sb-Te thin film device was carried out with the Cascade probe station and Agilent 4155C semiconductor parameter analyser shown in Figure 4.26. By introducing a voltage sweep between 0–4.5 V, the current across the fabricated cell was measured using the source measure unit within the semiconductor parameter analyser. It should be noted that an internal load resistance within the instrument provides current limitation in order to protect the device. The I-V characteristics of the CVD grown Ge-Sb-Te thin film device are shown in Figure 4.26. These were obtained using a voltage sweep whilst measuring the current as well as using a current sweep whilst measuring the voltage. This revealed three states of the film with a threshold of around 1.5–1.7 V. Starting at a high resistance state and applying the sweep, which at the threshold gives way to the stable phase change (memory switching) by virtue of the Joule heating to above the crystallisation point of the material, subsequent sweeps reveal that the low resistance crystalline state is stable unless switched back to the high resistance through electrically melt quenching the layer. This electrical switching between amorphous and crystalline phases is reproducible at least ten times. The resistance contrast between the two phases is in the order of 10^2 Ohms, making this result very promising for PCRAM application.

4.4.4.2 GeSbTe nanowire

The memory cells fabricated from the thin films deposited used the same fabrication process as those with GaLaS as an active layer. The structure is shown in Figure 4.27.

Scanning electron microscopy images of the NW memory cells before being the deposition of the capping layer is shown in Figure 4.28.

4.4.4.3 High throughput depositions

After configuring and calibrating the system for the GaLaS family of glasses, the HT-PVD (see chapter 3) method was employed to produce films covering the full pseudo-binary range from gallium sulphide to lanthanum sulphide (Figure 4.29 & Figure 4.30).
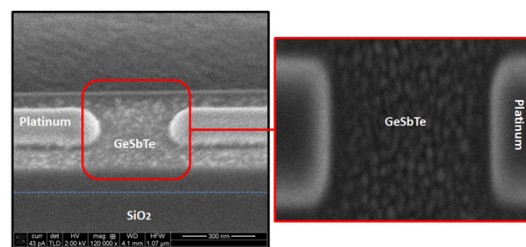
FIGURE 4.28: Scanning electron microscope (SEM) image of GeSbTe memory cell formed from two platinum electrodes spaced 375 nm apart. The chalcogenide layer has been milled away to form the nanowire cell.
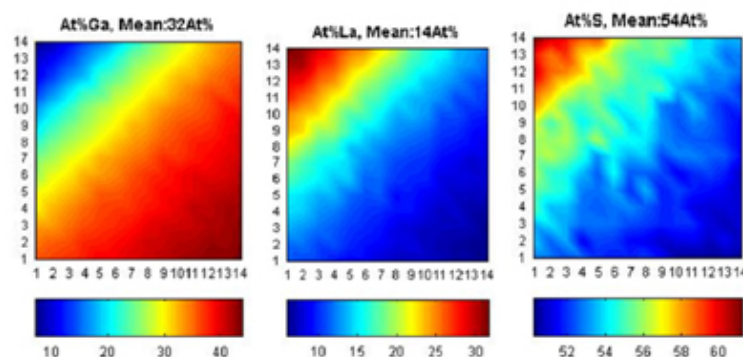
FIGURE 4.29: Energy dispersive xray across a 35 x 35 mm sample deposited with the compositional gradient of the ternary family of GaLaS.

The process was optimised by varying substrate temperature during deposition and the evaporation temperature of each of the source materials. The films' annealing and crystallisation were subsequently studied to gain further insight into the material system. Figure 4.31 shows X-ray diffractograms illustrating the difference between films prepared with different sulphur sources (either "native" sulphur present in the deposition chamber or sulphur produced by a specialist sulphur cracking K-Cell) but under otherwise identical conditions. During the early stages it was realised that the fact that the phases formed in these two cases are completely different - there is only one match between XRD traces and these are at very different annealing temperatures demonstrates that precise, highly-informed control over deposition is required to reliably fabricate these complex materials. Phase transition temperatures (and therefore switching energies and thermal stability) are a strong function of chalcogenide composition. The thermal properties of the chalcogenide films were investigated using a system for High Throughput Optical Measurement of Phase Transitions (HTOMPT), which derives crystallization temperatures for each composition from an analysis of changes in optical reflectivity as a function of temperature. Figure 4.32 shows the HTOMPT crystallisation temperature map for a GaLaS gradient sample and a translation of this information to a ternary compositional plot. The electrical phase-switching characteristics of GaLaS have also
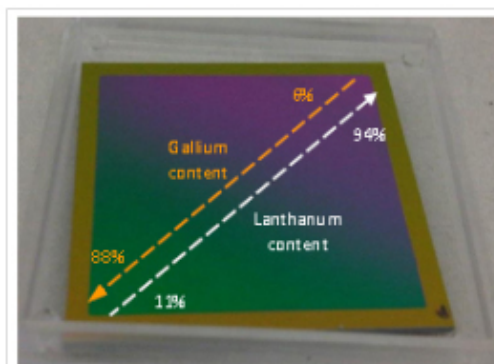
FIGURE 4.30: Compositional gradient GaLaS sample prepared by high throughput physical vapour deposition.
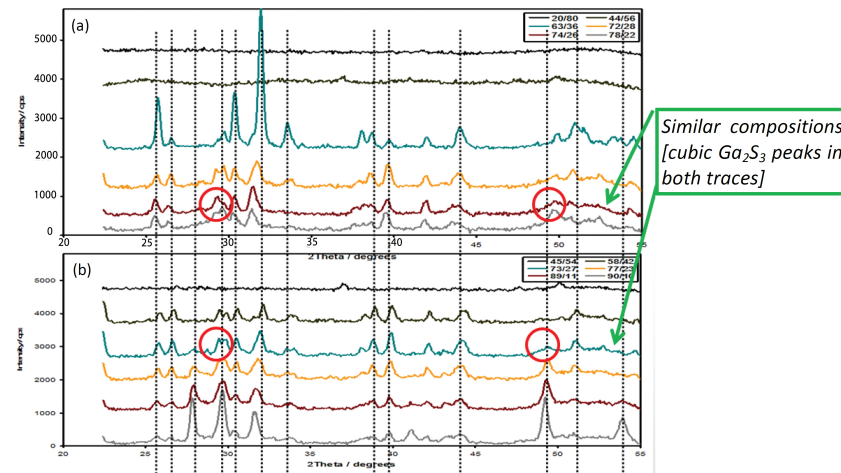
FIGURE 4.31: XRD of GaLaS samples (a)deposited at 200°C using native sulphur in PVD chamber annealed to 650°C. (b) deposited at 200°C using a sulphur cracking k-cell annealed to 700°C.

been analysed as a function of glass composition using the high-throughput methodology. Photolithographic and focused ion beam milling processes were employed to define an array of GaLaS nanowires between Mo electrodes across a compositional gradient of GaLaS (see Figure 4.33). These were then screened for threshold voltage, set/reset current and amorphous/crystalline state resistance (section 4.6.2).

4.4.4.4 High throughput PC-NW chip

Using the PVD thin film with a compositional gradient of GaLaS, a series of NW cells were fabricated in order to investigate the optimal phase change composition of highly
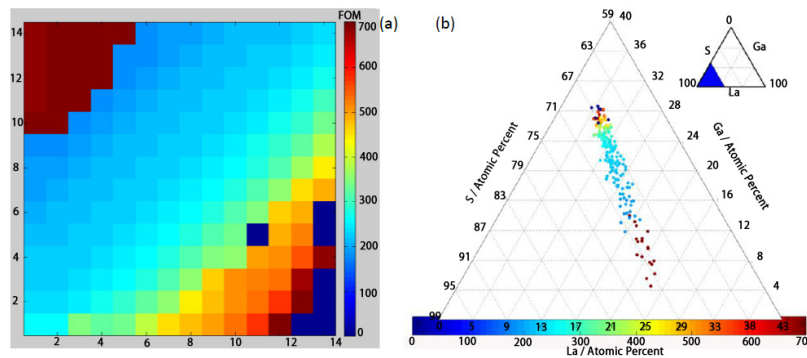
FIGURE 4.32: Crystallisation temperature of GaLaS (a) as a fucntion of position across a compositional gradient samples varying from lanthanum sulphide top left to gallium sulphide bottom right. (b) translated to a ternary composition plot.
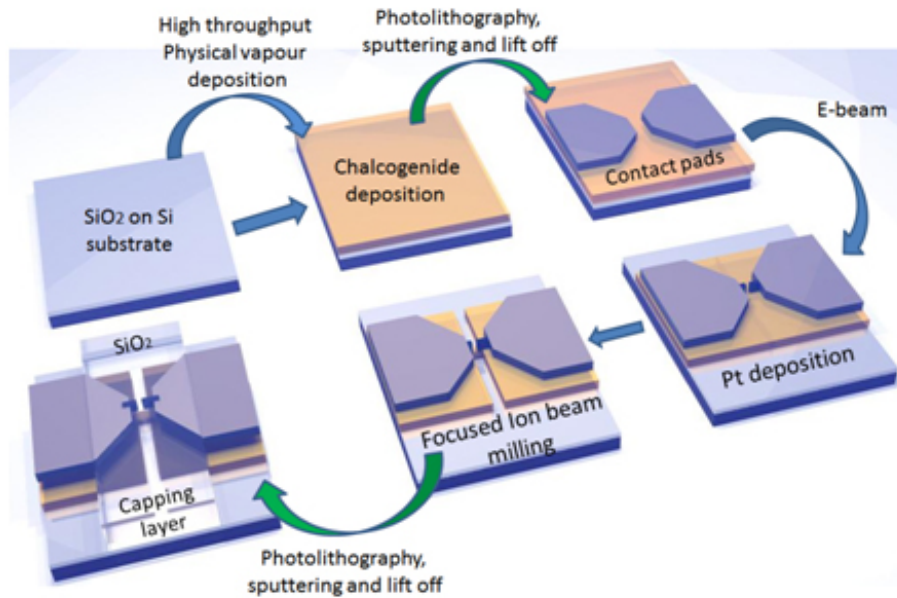
FIGURE 4.33: Process flow diagram showing the fabrication process used for the production of nanowires across compositional gradient thin film.

scaled phase change memory as well as assessing the influence of the different elements in the ternary alloy on the electrical phase change behaviour.

The fabrication process is shown in Figure 4.33. The results obtain from the high throughput nanowire memory chip are discussed in the results and discussions section of this chapter.

4.5   Characterization

4.5.1   Electrical characterization

In order to measure the electrical properties of the phase change devices, several testing circuits have been proposed that need to fulfill specific criteria for testing PCRAM devices:

- The resistance of the device is usually as low as several kΩ in the SET state and as high as several MΩ in the RESET state. A system should be able to measure these two very different states accurately.

- The RESET pulse is usually in the order of nanoseconds, so the temporal resolution of the testing system should be in the nanosecond range with a sharp trailing edge to enable melt-quenching.

- The RESET current is typically in the μA region in an advanced device, and the tester should be able to measure the current trace properly.

- Fast phase change devices can be SET in several tens of nanoseconds. The rise time and fall time of the pulses should be as short as possible.

To fulfill the requirement, several approaches have been proposed and the most practical circuits are shown in Figure 4.35 .

In Figure 4.35, the switch is used for separating the pulse generator (PG) and the direct current (DC) measurement tool. To characterise and understand the switching mechanism in these devices two types of electrical switching regimes were used:

- Electrical Sweep (129)

- Dual Pulse (130; 131; 27; 132; 133; 69; 134)
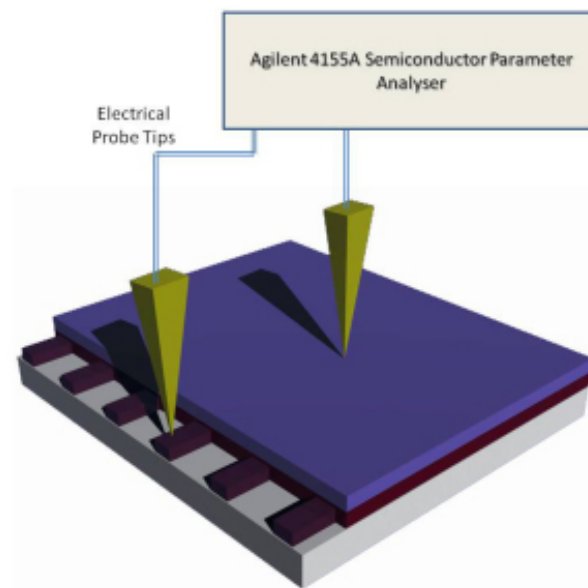
FIGURE 4.34: Experimental setup used for the electrical sweep measurements.
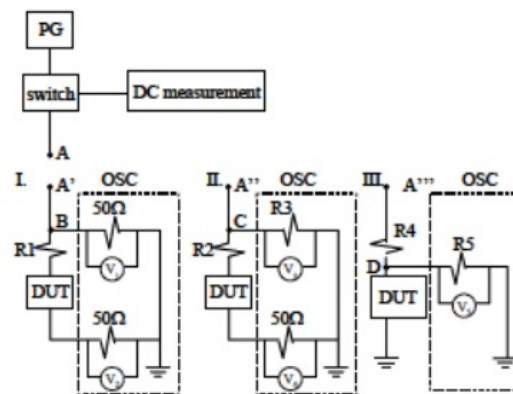
FIGURE 4.35: Typical configurations of a memory cell testing setup [Reprinted from (17)].
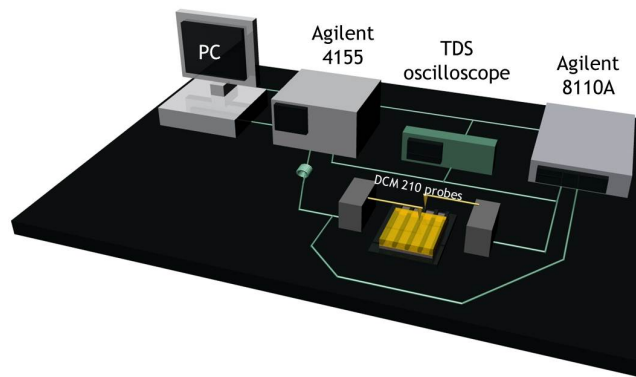
FIGURE 4.36: Experimental setup used for the dual pulse switching measurements.

The electrical sweep across the thin film effectively raises the temperature through Joule heating and given enough power being put through the crystallization temperature of the alloy should be reached thus allowing the electrical switching of the thin film. This can be verified by simultaneously recording the current-voltage characteristics of the device, which gives indications as to the type of switching occurring (threshold or memory switching).

To apply this method of electrical characterisation the experimental setup shown in Figure 4.34 was used in order to both supply the energy required for crystallisation as well as, simultaneously measuring the relevant electrical parameters. The other possible electrical switching regime is the use of two pulses, which depending on their duration and power will allow the crystallization and melt/quenching of the chalcogenide thin films (Figure 4.35).

One pulse can increase the temperature to the crystallization temperature, whilst the shorter higher energy pulse melts and quickly quenches the alloy back to a glassy state. By measuring the resistance one can observe the difference between the crystalline and
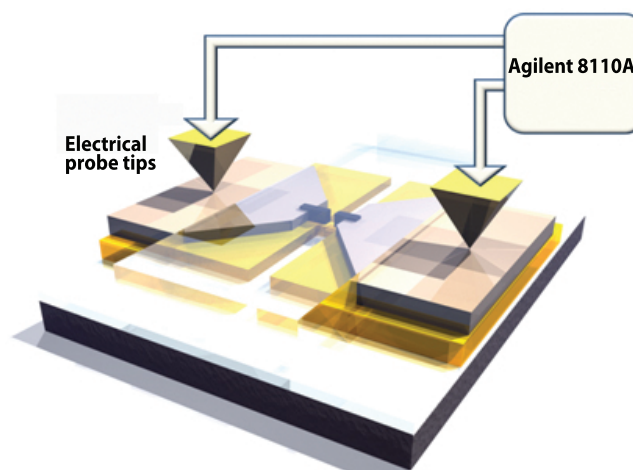
FIGURE 4.37: Simple setup used for characterising the phase change nanowire memory cells.
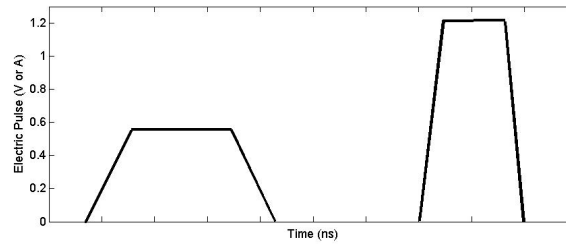
FIGURE 4.38: Two pulses are provided to allow switching between the two states of the phase change layer.

amorphous states, which is very important for non-volatile memory applications. The experimental setup shown in Figure 4.36 was used in order to introduce the appropriate pulses, verify the pulse integrity as well as, measure and store the resistance across the cell as a result of these pulses. The other setup used specifically to pulse switch the nanowire lateral cells where a series of incrementally increasing pulses were introduced to switch the cells is shown within Figure 4.37.

Two different set of experimental setups were used in order to induce phase change within each phase change alloy used (Shown in Figure 4.36 and Figure 4.37). The dual pulse mechanism used to crystallise and melt quench the phase change layer is shown in Figure 4.38. The longer pulse with a lower energy crystallises the alloy while the shorter higher energy pulse re-amorphises the phase change layer. Through the use of this method one can also measure the switching speed of the memory cell. In order to do this one needs to use the incrementally increasing pulse setup shown in Figure 4.43. The alternative method of investigating electrical switching is using a DC sweep method of characterising the phase change memory cells. The sweep setup is shown in Figure 4.39. The electrical sweep method raises the temperature of the phase change layer to the crystallisation and melting point of the alloy. Using this, one can observe the threshold voltage and re-amorphisation voltage of the alloy while also allowing the derivation of
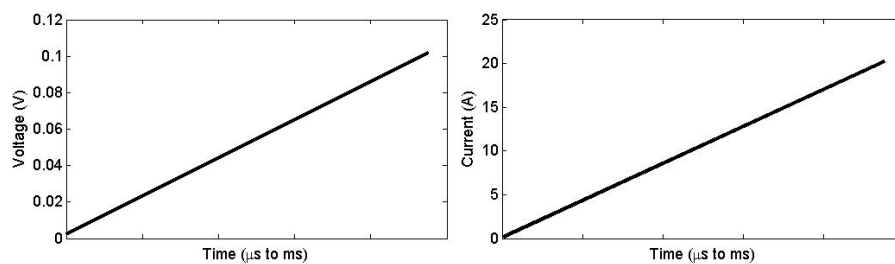
FIGURE 4.39: The two sweep mechanisms used to switch the phase change layer. The current sweep is limited to 0.1A on the Agilent 4155C and to 1A on the Keithley 238 and the voltage sweep is limited to 25V on the Agilent 4155C and 110V on the Keithley 238.

the resistance in the low resistance and the high resistance states and the subsequent resistance ratio which is an essential parameter in the use of these alloys for non-volatile PCRAM devices. The resistance can be derived through calculating the inverse of the slope of the I-V curve, pre and post threshold:

$$Cell\ resistance = \frac{1}{gradient\ of\ IV\ curve}.$$

The resistance ratio (R_{on}/R_{off}) is obtained by calculating the pre-threshold amorphous state resistance and the post threshold crystalline state resistance separately. This allows us to arrive at a high/low resistance ratio which is an indication of the memory switching contrast, a key parameter in memory cell characterisation.

4.5.2   Thermal stability measurements

To assess device performance at elevated temperatures, a series of device based studies have been conducted with both GaLaS and GeSbTe devices. In these experiments, phase switching is investigated at temperatures up to 600°C, several hundred degrees higher than the stable operational window of conventional PCRAM devices. The experimental setup used to record the electrical switching parameters as a function of cell temperature to understand the thermal stability of the different chalcogenide alloys used within phase change memory, is shown in Figure 4.40.

The temperature of the sample was increased using a Linkam Scientific Thermal microscopy stage whilst recording the I-V characteristics of the device. This allowed the
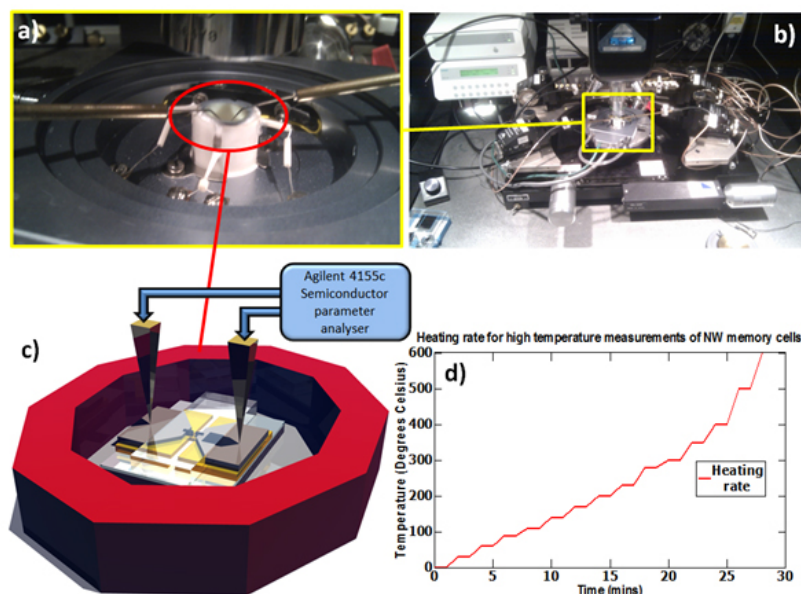
FIGURE 4.40: Experimental setup used to obtain current voltage characteristics of the memory cells across different device temperatures.

observation of the change in threshold voltage and R_{on}/R_{off} as a function of the temperature change.

4.6 Results and discussion

In this section an account of the results obtained from the devices fabricated is presented with a discussion of the contextual significance of the different attributes observed within the said devices. The nanowire memory cell results made from GeSb, GaLaS and GeSbTe are presented in chronological order, ending with a comparison of the GaLaS based cells with those using GeSbTe as the active layer. The results observed through scaling of these devices is also presented with specific focus on volume and lateral scaling (active area, length and width) of the nanowire active zones.

4.6.1 Nanowire memory cells

4.6.1.1 Electrical characterization

4.6.1.1.1 GeSb nanowire The I-V characteristic of the devices fabricated was measured simultaneously whilst supplying the sweep. This was done by supplying a voltage sweep and measuring the current with a selection of the result shown in Table 4.3. The typical current voltage characteristics of the nanowire memory cells is shown in

Width (nm)	Set Current (A)		Set Voltage (V)	
100 nm	1.01×10^{-4}	1.60×10^{-4}	1.46	1.39
200 nm	1.294×10^{-3}	2.414×10^{-3}	1.65	1.668
300 nm	3.96×10^{-3}	1.11×10^{-3}	2.048	2.396
Width (nm)	Reset Current (A)		Reset Voltage (V)	
100 nm	1.764×10^{-3}	3.08×10^{-4}	3.66	2.35
200 nm	5.31×10^{-3}	4.173×10^{-3}	2.907	2.874
300 nm	6.08×10^{-3}	2.21×10^{-3}	3.19	3.316

TABLE 4.3: Table of typical results of different GeSb nanowire cells fabricated and measured experimentally showing the reduction in relevant operational parameters during nanowire width scaling. The reduction in current consumption is much more pronounced than the reduction in threshold voltage, this is as a result of the effect of smaller nanowires widths of current localisation during set and rest operation. While the current consumption shows as much as a 6 times change from the smallest to the largest cell sizes, the threshold voltage shows a much less pronounced dependance on the reduction in width of the nanowires.

Figure 4.41. The current consumption of the devices in the low resistance state is in the high μA to very low mA region (e.g below 1mA set current in the 100nm cell). This along with the stackable geometry of these lateral nanowire cells makes these structures and the use GeSb as the phase change active layer a very promising and advantageous option for highly scaled future memory devices. For the three nanowire cell sizes shown
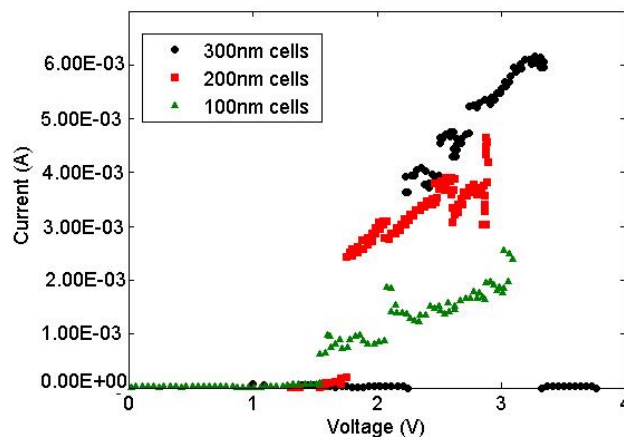
FIGURE 4.41: The current-voltage characteristics of the nanowire memory cells with different effective cell sizes.
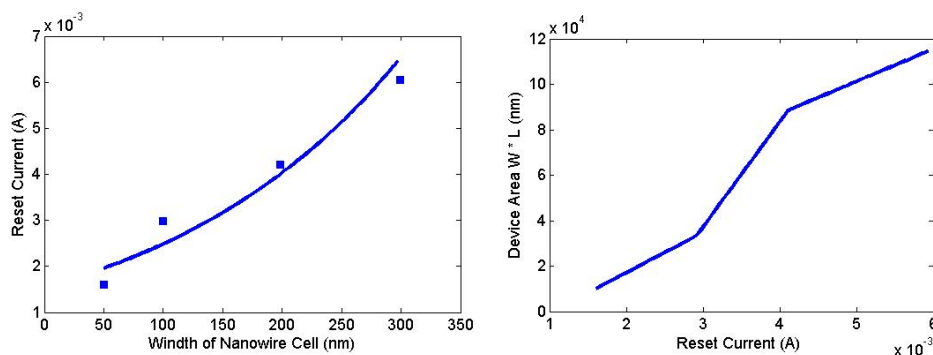
FIGURE 4.42: (left) The reset current measured across the different nanowire memory cells with different widths (right) The reset current measured across the different nanowire memory cells with different areas.

in Figure 4.41, there is clear reversible memory switching in the devices. There is a reduction in threshold voltage with decreasing cell size. These readings were repeated across different nanowire sizes arriving at comparable current-voltage characteristics for different nanowire cell sizes. Average parameters across different measurements and device sizes are also shown in Figure 4.42.

The reset current within high density memory cells is an important parameter, which determines both how low power the device will be as well as how thermally stable the high density nanowire devices will be; as, the higher the reset current, the higher the heat generated and passed on from cell to adjacent cell. The reset current in this case decreases with smaller nanowire width, achieving close to 1mA reset current at the 50nm cell size

Reset currents for different nanowire memory cells with different areas given the same height shows a reduction in the reset current with smaller area devices which is as a result of the lower energy needed to both crystallise a smaller area and to eventually
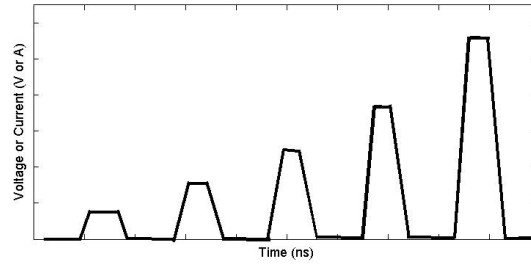
FIGURE 4.43: Incremental electrical pulses used to arrive at a single pulse switching speed used for the memory cells.
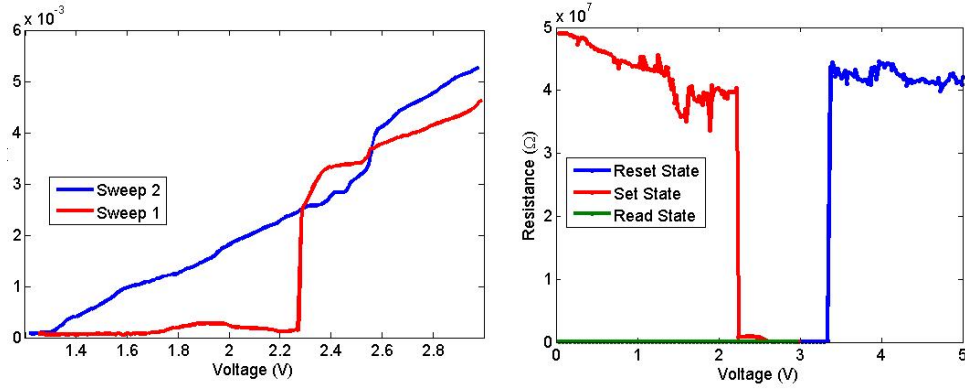
FIGURE 4.44: (left)Current-voltage characteristics of a 200nm memory cell recorded simultaneously whilst attempting pulse switching of the device.(right) Resistance - Voltage characteristics of a GeSb nanowire cell, showing a Ron/Roff ratio of the order of $10^3\Omega$.

melt/quench the phase change nanowire, these range of measurements demonstrating the different nanowire cells with different areas and lengths and their effect on the current consumption shows the potential for using these devices for low power consumption, more thermally stable alternatives to conventional GeSbTe for highly scaled, high density memory cells. As mentioned before, the nanowire memory cells were also switched using an incrementally increasing pulse to determine their switching speed (shown in Figure 4.43). The I -V characteristics of the cell were measured simultaneously and the results shown in Figure 4.44 were observed.

The V_t was observed to be 2.27 V and R_{on}/R_{off} ratio of the order of 103 (Figure 4.44). The threshold voltage corresponds very closely to the DC sweep method of switching shown previously and the switching pulse used is 300ns. This shows a fast switching speed for an unpackaged and rather large geometry device (200nm) further highlighting its potential for very fast switching non-volatile phase change memory cells.

As described previously two sets of devices were fabricated, the results above were observed on the electron beam deposited samples. The ion beam deposited samples showed the behaviour shown in Figure 4.45 when utilising the sweep mechanism to switch the cells.
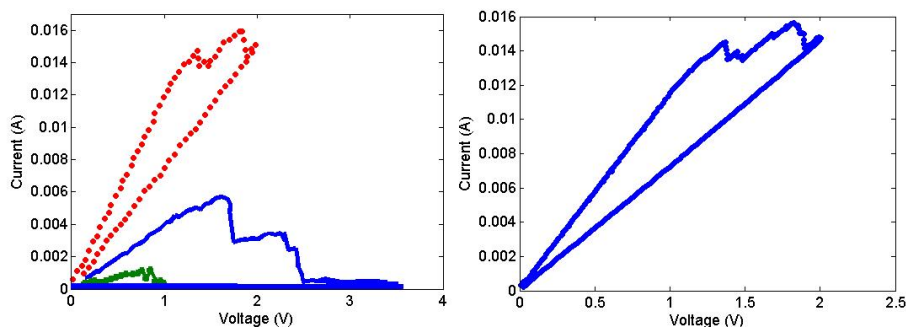
FIGURE 4.45: (left) Current-Voltage characteristics of Ion beam deposited nanowire memory cells. They all show a lack of a threshold voltage with a much lower resitance ratio between on and off state.(right)Current-voltage characteristics of the gallium contaminated device as a result of ion beam induced deposition.

When repeating the measurements for other ion beam deposited samples, one can observe the lack of threshold voltage and gradual change in resistance of the cell. Also the cells start in a much more conductive state than the electron beam deposited samples. This can be attributed to the gallium implanted into the cells during the fabrication process, as a result of the ion beam induced deposition. A set of repeated measurements of these cells is shown in Figure 4.45. These results correspond very closely to those reported by Meister et al (135). However based on the results obtained here and comparing with the results we obtained for the electron beam induced deposition it can be deduced that the typical IV characteristics shown in literature for nanowire cells maybe as a
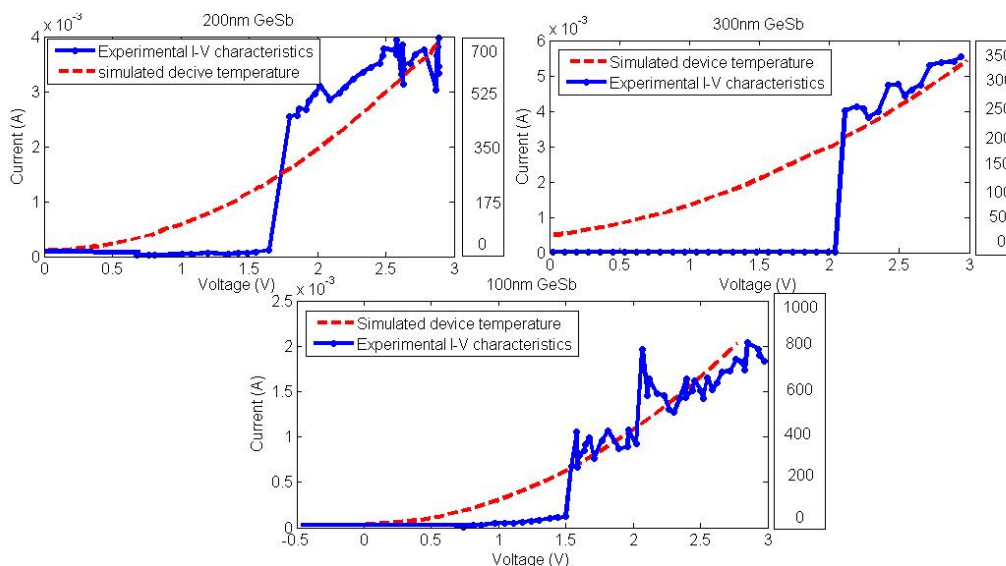
FIGURE 4.46: The current-voltage characteristics and corresponding modelled device temperatures for different nanowire cell sizes. It can be observed that at the onset of the threshold voltage where the experimental results show a change from a high resistance amorphous state to a low resistance crystalline state, the modelled device temperature indicates that the hot zone of the chalcogenide nanowire should be reaching temperatures very close to the crystallisation temprature, this reaffirms our understanding that phase change is responsible for the on/off switching observed in these memory cells.

result of gallium ion contamination by the FIB during the fabrication process and as such do not show a clear threshold as is expected from phase change memory cells. Our results conclusively show that by using electron beam induced deposition during fabrication true phase change nanowire memory cells can be obtained which show clear threshold voltages and a very high R_{on}/R_{off} ratio. Making them much more ideal for mass produced commercial nanoscale high density phase change memory devices. The current-voltage characteristics of the different cell sizes can be seen alongside the corresponding temperature of the devices as obtained from the simulations described previously (Figure 4.46). It can be observed that at around the threshold voltage of the devices the simulated temperature of the device reaches the crystallisation temperature of GeSb thin films. This in itself explains the current-voltage characteristics observed experimentally as at around this voltage resistance changes indicating the change in the crystal structure of the GeSb thin film, i.e phase change.

4.6.1.1.2 GeSbTe nanowire
A series of devices were fabricated using standard photolithography, reactive ion etching, ion beam milling and ion beam deposition to
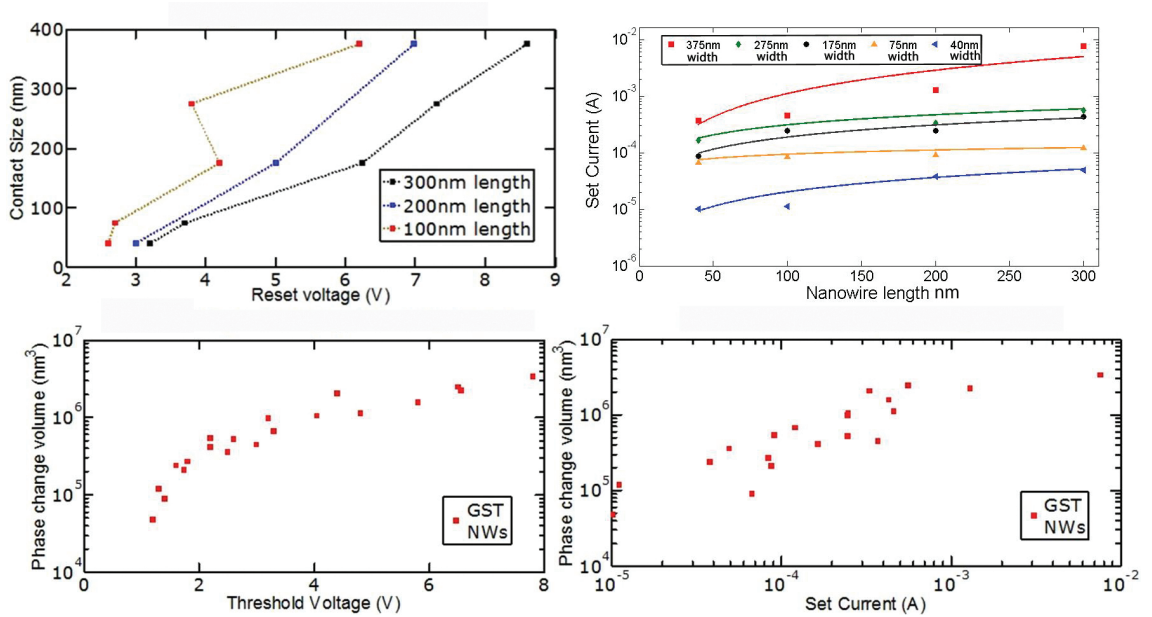
FIGURE 4.47: Scaling of the GeSbTe memory cells has been accompanied by a study of the effect of scaling on the different memory paramaters of these devices (top left) Reduction of the voltage required to reset the device with decreasing contact size is seen (top right) The shorter the length of the nanowire phase change active area, the lower the current required to set the device to a low resistance state, the reduction in the width of the nanowires shows a much more pronounced and direct effect on the reduction in current consumption, as current localisation is directly related to the width of the nanowires, as a result of the greater change in phase change volume in width scaling (bottom left and bottom right) The reduction in the volume of the phase change material, brings about a lower power requirement as less energy is needed to phase switch the memory cells. As a result, the reduction in both threshold voltages and set currents can be clearly observed here.
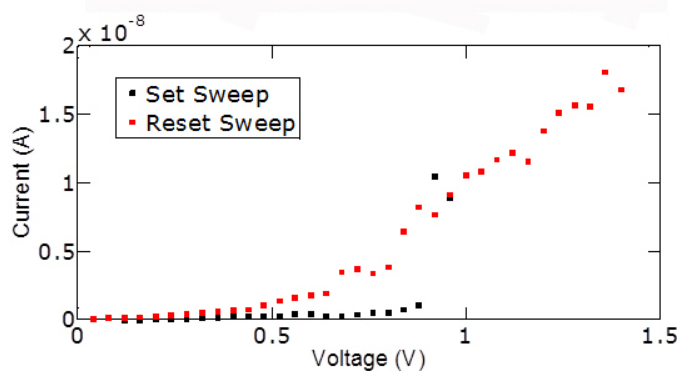
FIGURE 4.48: Smallest current consumption observed within the GaLaS NW memory cells.

yield the device structure shown previously. As set out previously, the scaling study carried out on the nanowire memory cells concentrated on two different types of scaling. The reduction in the contact size can reduce current consumption as it increases the efficiency of the memory cell in terms of joule heating. The results shown in Figure 4.47, show the reduction of the different switching parameters of the memory cell with a reduction in the contact size of the memory cell. It has been suggested that as the volume of phase change material is scaled a reduction in the switching current and voltage can be observed due to current localisation in a smaller volume of material. Figure 4.47 shows the effect of phase change volume scaling on the different parameters of the memory cells.
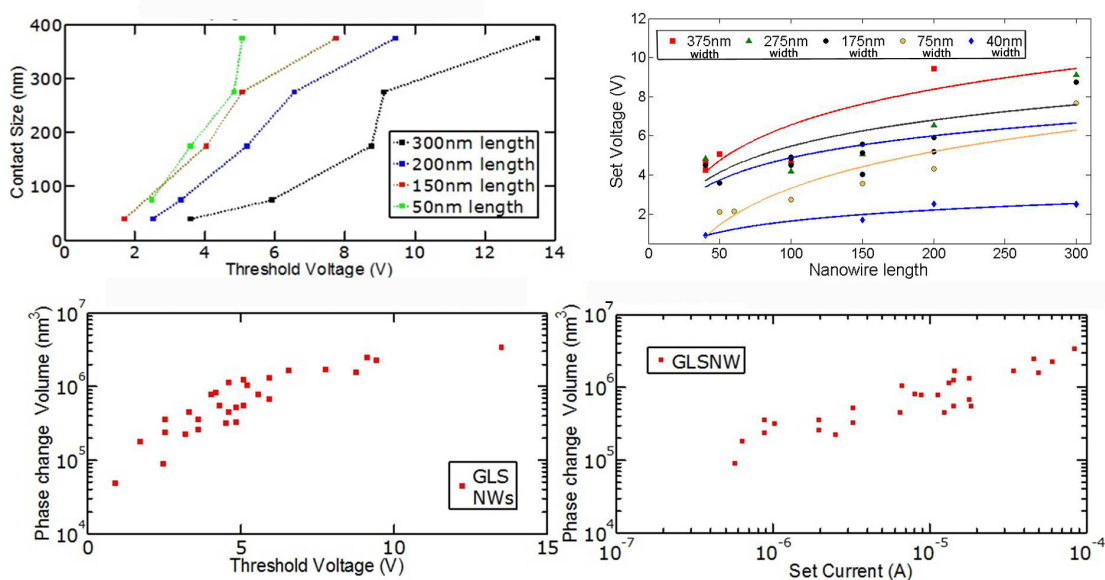
FIGURE 4.49: (left)Reset voltage of GaLaS NWs with decreasing volume of phase change material.(right)Reset current of GaLaS NWs with decreasing volume of phase change materials.
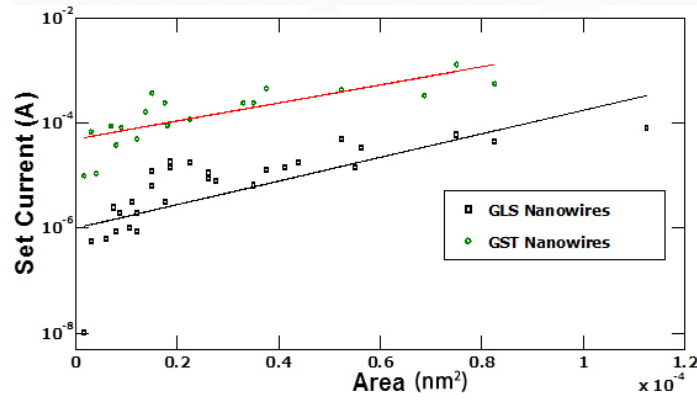
FIGURE 4.50: Set current of NW memory cells with decreasing effective area.

4.6.1.1.3 GaLaS nanowire By introducing voltage sweeps between and measuring the current across the fabricated cell using the source measure unit within the semiconductor parameter analyser as set out previously. The memory cells were electrically switched successfully. The I-V characteristics of a GaLaS cell with ultra low current consumption are shown in Figure 4.48. The resistance of the material in its amorphous state was on the order of $3 \times 10^9 \Omega$. Once the voltage was increased above the threshold, the resistance switches to a more conductive state showing a resistance of $3 \times 10^5 \Omega$. As set out previously, the scaling study carried out on the nanowire memory cells concentrated on two different types of scaling. The reduction in the contact size can reduce current consumption as it increases the efficiency of the memory cell in terms of joule heating. The results shown in Figure 4.49 shows the reduction of the different switching paramters of the memory cell with a reduction of in the contact size of the memory cell.As expected, one can observe that as the volume of phase change material is scaled a reduction in the switching current and voltage can be observed due to current localisation in a smaller volume of material. Figure 4.49 show the effect of phase change volume scaling on the different parameters of the memory cells.
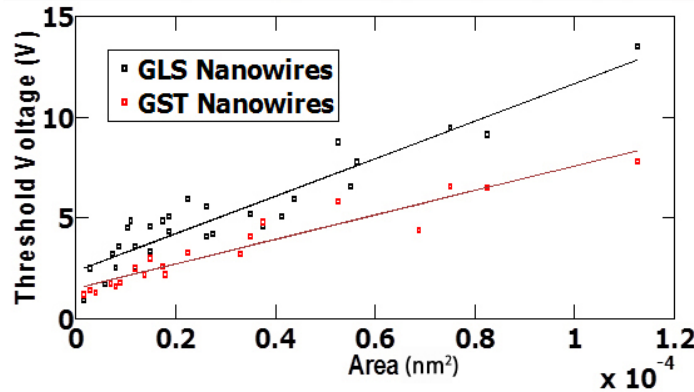
FIGURE 4.51: Threshold voltage of NW memory cells with decreasing effective area.
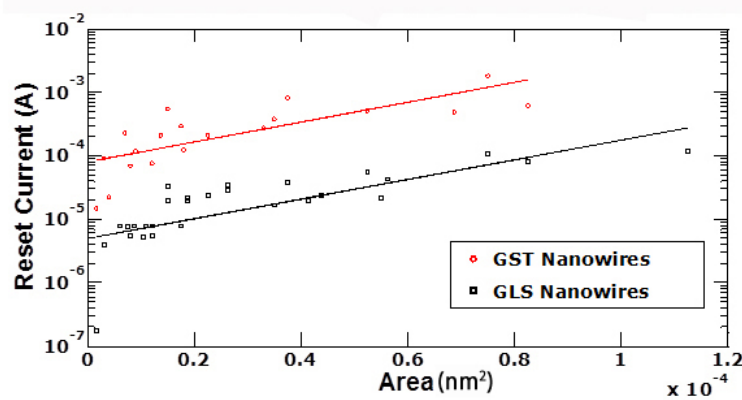
FIGURE 4.52: Reset current of NW memory cells with decreasing effective area.

4.6.1.1.4   Comparison   A more detailed and statistical study of set and reset operations was made on approximately 50 cells in each of the GaLaS and GeSbTe designs. Pulse widths for the set were said to be in excess of the expected switching time, typically 200ns for set and 100ns for reset. The threshold voltage could be measured for the set and reset function. This data is plotted as a function of cell area, i.e the active area of the chalcogenide between the platinum electrodes and the representative data is shown in the Figure 4.50 to Figure 4.53.

Despite some overlap in the data at small cell sizes for the set operation, it is clear that there is a difference in the performance of the two materials, when used in identical cell designs. A curve was fit to each set of data, for which N, the number of cells measured, varied between 20 to 50.

To allow direct comparison of the performance of the two materials a cell area 12x 10^{-6} nm^2" was chosen. This is above the region of small cell sizes where our experimental uncertainty was relatively large, but significantly smaller than the largest of the cell that
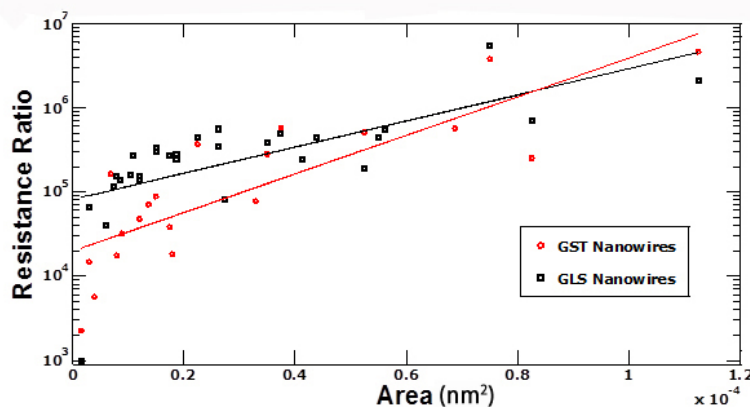
FIGURE 4.53: Resistance ratio of NW memory cells with decreasing effective area of the memory cell.
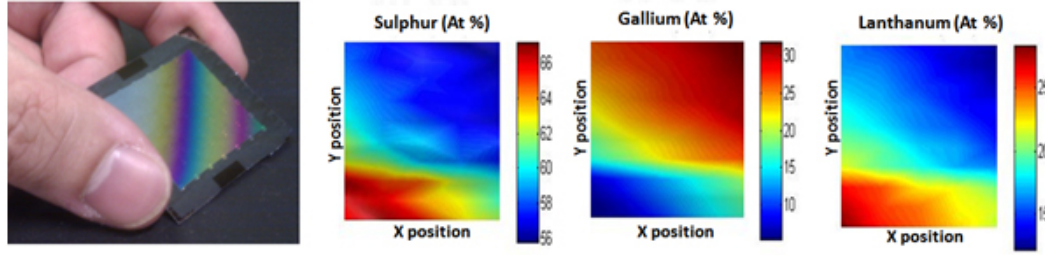
FIGURE 4.54: Energy dispersive X-ray of nanowires across compositional gradient.

were fabricated, some of which were an order of magnitude larger. The result of these comparison are shown here.

The results indicate that there is an enhancement of the resistance contrast of approximately an order of magnitude with GaLaS offering a 10^4, difference between the amorphous and crystalline states. This is due in part from the relatively large resistance in the glassy state resistance (approximately 10^9 Ohms), which manifests itself also in a slightly higher threshold voltage.

Due to the high crystalline state resistance of GaLaS, efficient joule heating allows a reduction in the reset current as well as making this material a very suitable candidate for ultra low power data storage applications.

4.6.2 NW PCRAM composition optimization

For the GaLaS family of glasses, that offer vastly higher thermal stability and lower current consumption than conventional GeSbTe, the full ternary was deposited by physical vapour deposition and all compositions on the phase diagram were screened using high throughput techniques (see Figure 4.54).

This was followed by the fabrication of an array of nanowire memory cells across the compositional gradient, giving us the ability to investigate the change in threshold voltage, set and reset currents as well as other relevant parameters for phase change memory across the full compositional range.

This high throughput method of composition optimisation for memory materials, gives one the ability to optimise an entire ternary on one chip. Each memory cell fabricated on predesignated places along the compositional gradient allows us to study the suitability of the material for different data storage parameters, as well as giving an insight into the dependance of the different phase change memory parameters on the elemental constituents of the glass family being studied.

The devices fabricated on the compositionally varying GaLaS thin films, were studied for relevant parameters to phase change memory. The resistances in both phases
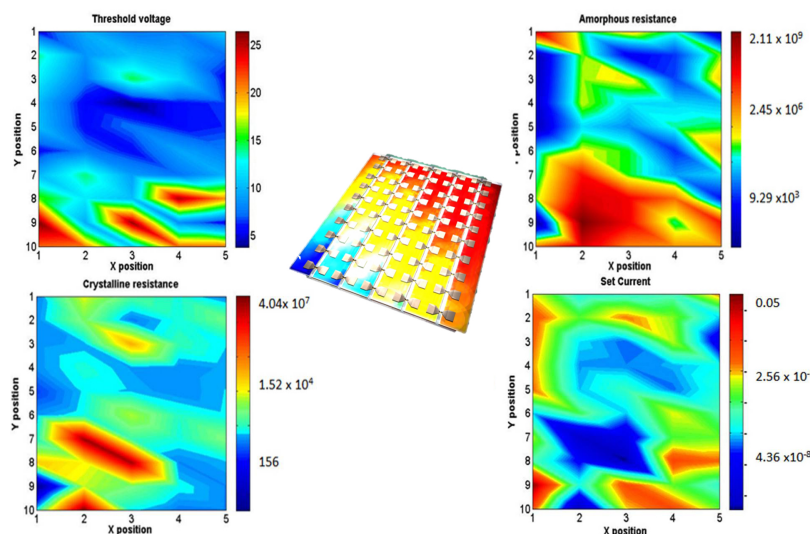
FIGURE 4.55: Memory attributes of GaLaS nanowires across a compositional gradient chip.

was investigated (Figure 4.55), along with threshold voltages and current consumption. High resistances in both amorphous and crystalline phases is a desirable feature for electronic phase change memory, as it allows efficient joule heating for both set and reset operation and ensures low power consumption and integratability with low current consuming CMOS architectures. In the devices fabricated, there is a clear trend between amorphous resistance and lanthanum and sulphur in the composition. A high amorphous resistance is observed in compositions with high concentrations of these two elements. The crystalline resistance follows this trend with the highest crystalline resistances being exhibited in sulphur rich compositions. Also noteworthy is the observation that, the threshold voltage (a parameter which should be minimised in low power electronics) in cells fabricated with compositions that contain a higher gallium concentration exhibit the lowest threshold voltages.

The different compositions studied in this way can allow a database of information to be created through which exact compositions are designated to particular applications in need of tailor made material properties, this allows the optimisation of material properties for a number of different device platforms.

4.6.3 Elevated temperature operation

To assess device performance at elevated temperatures, a series of device based studies have been conducted with the most promising alloys (See Table 4.4). GaLaS glasses for example exhibit characteristic thermal properties over 200°C higher than GeSbTe alloys. Figure 4.56 shows a typical measurement in which the threshold voltage as a function of temperature is plotted for both a GaLaS and GeSbTe device.

Phase change alloys	Tg (°C)	Tx (°C)	Tm (°C)
Ga:La:S	550	640	830
GeSb	-	260	650
$Ge_2Sb_2Te_5$	120	160	610

TABLE 4.4: Thermal stability of GaLaS family of glasses compared with the GeSb and GeSbTe alloys, exhibiting characteristics several hundred degree higher than the GeSbTe alloys.

The thermal stability measurements were characterised using the DC sweep method over increasing temperatures. The I-V characteristics of the cell was measured throughout assessing at what temperature the devices begin to fail.

The conventional alloys used in phase change memory is GeSbTe with a crystallisation temperature of $200^{o}C$. Most phase change memory devices which utilise this alloy suffer from being highly unstable at elevated temperatures. As high density chips made for commercial applications need to be stable and still allow phase change at high temperatures this study has aimed to investigate and demonstrate the suitability of GaLaS as a high temperature phase change alloy where GeSbTe cannot be used.

As can be seen from Figure 4.56, using measurements taken up to $600^{o}C$ (well above the GeSbTe crystallisation temperature) electrically induced phase change is observed. At such temperatures GeSbTe would be volatile and effectively unusable. However, as is shown, GaLaS with a crystallisation temperature of $\approx 650^{o}C$ as a thin film shows high thermal stability.

For the GeSbTe device, functionality (loss of threshold switching) occurred at approximately 160° C whereas for this example, repeatable threshold switching continued to 600° C with the GaLaS device. Although this data only indicates enhanced temperature operation in a prototype device rather than real world application, it does clearly indicate that significant difference in temperature stability can be achieved through
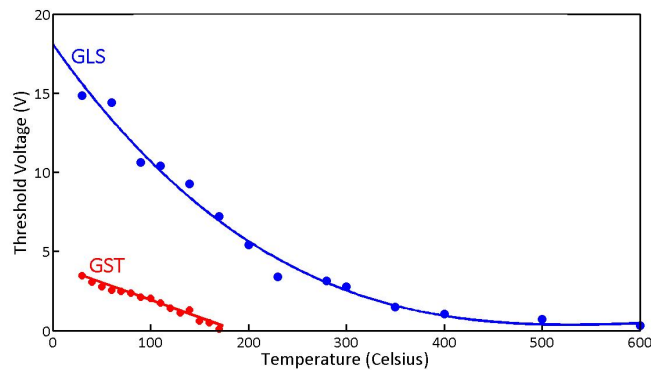
FIGURE 4.56: Observation of switching and threshold voltage change with increasing device temperature.

compositional modification and exploring novel material as increased thermal stability is essential for commercial applications.

4.7 Summary

The primary objective of this work was to investigate the suitability of sulphide based chalcogenide memory cells for thermal stable, low current (power) consumption electronic phase change memory applications. To this end, memory cells incorporating GeSbTe, GeSb and GaLaS have been designed, fabricated and characterised, whilst also scaled devices were used to investigate the effect on power consumption parameters.

In reaching this goal, significant landmark results have included:

- Fabrication and characterisation of GeSbTe, GeSb lateral nanowire memory cells with identical geometries and device structures.

- First demonstration of gallium lanthanum sulphide nanowires with

    - Low current consumption (one of lowest reported).
        * Set currents $<1\mu$A
        * Reset current 1-10μA
    - High thermal stability (operation of up to 600°C)
    - High resistance contrast up to 10^4.

- High throughput nanowire phase change memory chip fabrication and characterisation for the optimisation of the GaLaS phase change ternary.

The knowledge and expertise derived from these achievements set a strong foundation for the continuation and expansion of research work in the field of chalcogenide phase change data storage, where directions may include synthesising sulphide based nanowires through Vapour Liquid Solid (VLS), [see Chapter 7] techniques allowing high endurance highly scaled devices. The use of highthroughput technique also allows rapid optimisation of optimal compositions for nanowire data storage.

Chapter 5

Information Processing Devices

5.1 Background

With the soaring price of custom electronics in use for different consumer and industrial applications, reconfigurable electronics are becoming even more important. In reconfigurable electronics, versatile architectures allow customized functions to be implemented after fabrication. This paradigm of software-definable hardware offers intriguing benefits that include flexibility through in situ reprogramming, fault tolerance, and rapid response solutions to be formed by configuring pre-built components. The other example in current practice is the field programmable gate array (FPGA), which has evolved from being a curiosity to a multi-billion dollar disruptive technology. Phase change materials have not traditionally played a role in reconfigurable electronics, but offer powerful advantages by virtue of their non-volatility, durability, and the possibility of multi-state configurations. These concepts lead potentially to more compact computation architectures based on threshold logic, or more ambitiously dense arrays of artificial neurons and other novel hybrid (digital plus analog) signal processing architectures (17).

5.1.1 Logic gates

Logic gates are primarily implemented using diodes or transistors acting as electronic switches, but can also be constructed using electromagnetic relays (relay logic), fluidic logic, pneumatic logic, optics, molecules, or even mechanical elements. With amplification, logic gates can be cascaded in the same way that Boolean functions can be composed, allowing the construction of a physical model of all of Boolean logic, and therefore, all of the algorithms and mathematics that can be described with Boolean logic.

A programmable logic device or PLD is an electronic component used to build reconfigurable digital circuits. Unlike a logic gate, which has a fixed function, a PLD has an

undefined function at the time of manufacture. Before the PLD can be used in a circuit it must be programmed, that is, reconfigured.

For small-scale logic, designers now use prefabricated logic gates from families of devices such as the TTL 7400 series by Texas Instruments and the CMOS 4000 series by RCA, and their more recent descendants. Increasingly, these fixed-function logic gates are being replaced by programmable logic devices, which allow designers to pack a large number of mixed logic gates into a single integrated circuit. The field-programmable nature of programmable logic devices such as FPGAs has removed the "hard" property of hardware; it is now possible to change the logic design of a hardware system by reprogramming some of its components, thus allowing the features or function of a hardware implementation of a logic system to be changed(17).

The logical AND and OR which operate as logical conjunction or disjunction, respectively (simply put, conjunction outputs a "1" when all inputs are "1", and disjunction outputs "1" when any input is "1"), and other functions operate according to the rules of Boolean logic. Simple gates, if not constructed directly in the transistors as circuit layouts, are built as cascades of simpler building blocks. All Boolean functions are expressable by some (nonunique) compositions of gates drawn from complete basic sets of Boolean functions (such as AND, NOT, OR, NOT, etc.).

5.1.1.1   Processors

There is a rich body of work on configurable digital systems, such as processors, memory, and field programmable gate arrays (FPGAs) which have become incredibly complex systems over the past decades, while configurable analog concepts remain a relatively fragmented body of work. Here the use of multi-valued phase change resistive elements is explored in realising cognitive quasi-analogue architectures which can have both electrical and optical inputs and outputs. The presented class of devices have been developed with a specific view to boolean reconfigurable logic circuit and memristive information processing elements applications (17).

Boolean networks based on cascades of simpler functions are sometimes called combinational logic. Combinational logic networks compute "statelessly", meaning that for any static input combination, final output values are produced (after accounting for finite signal propagations through the gate-networks) that never change so long as the inputs to the network are frozen, but lose these values when the inputs are removed (17). In order to hold the outputs computed by Boolean networks so that they do not continue to change, a mechanism to store Boolean state is required. The addition of storage elements and feedback dramatically expand the utility of digital systems. Storage provides a registration mechanism, conveying the notion of states that, once locked in, do not change even as inputs continue to vary. Feedback provides the ability to modify future

states even when inputs do not vary. It is possible to capture all of these concepts in the generalization of a clocked-domain digital system. Here, a combinational Boolean circuit computes outputs (y_c and y_d) from inputs (x_a and x_b). A flipflop array (one deep) registers all outputs. Through the inclusion of feedback, we achieve history-dependent behavior (17). This history-dependent behavior, being an advancement of the circuit behavior from one state to another (the description is sometimes called the state transition matrix), is captured by dedicating some of the inputs and outputs to the computation of state using feedback. The output states of the flip-flop array latch the outputs of the combinational Boolean circuit in synchronization with a clock, freezing both state and outputs between clock pulses (17).

Clocking digital systems emerged as a means of coping with the complexities of digital systems with feedback in the presence of non-uniform delays. Not all paths in classical real-world combinational circuits are isochronal, leading to some parts of a complex calculation of an input taking longer than others. In circuits with feedback, race conditions can result, leading to erroneous calculations or circuit states that are difficult to control and in fact become dependent on circuit layout, temperature, and other factors. In effect, the introduction of clocking produces a temporal firewalls, a discipline that eliminates race conditions by construction (17). Obviously, the clocking interval is typically chosen so that enough time has elapsed for the worst-case (slowest) timing path to complete its calculation. Clocked-domain sequential design, the practice of design circuits with clocks, is the dominant form of digital design today, and most synthesis tools expect this style of design. Disciplines for clockless (asynchronous) and wavepipelined systems are much rarer and have evolved separately. These arcane approaches achieve performance through self-timed circuitry. In clockless circuitry, output states change only in response to specific changes in input. Wave pipelining exploits the latency of signal propagation in deeply-staged combinational logic to "launch" multiple computations within an overall clocking cycle. Clockless approaches are promising but less comfortable to designers due to their additional complexity and limited support in electronic design automation today. Hence, sequential digital design involves memory. Non-volatility plays at least three major roles in Boolean systems (17):

- Finite state machines (FSMs), in which memory cells (flip-flops / registers) are dispersed throughout combinational logic, which computes the values of these memory cells. The design objective in FSMs is to maximize performance of state machines, for some combination of power, density, and latency (the latter dictating the operating speed of calculations).

- Bulk storage, where large amounts of state information in the form of user data are to be preserved and retrieved. In this case, combinational logic is used primarily to access the stored data for reading or writing. The design objective in bulk storage is to maximize the density of memory bits available to a user.

- Configuration storage, where state information is used to customize the functions of circuits. The design objective is to minimize the overhead of circuit added to manage configuration.

  These computing requirements for efficient information processing has brought about a rejuvination in the area of quasi analogue "multi-valued" resistive elements. Phase change technologies based on chalcogenide alloys have an inherently unique role to play in these technologies, its natural non-volatility, ability to host active ions within its amorphous lattice and allow field induced movement within this environment in effect allows their utilisation as a "solid electrolyte" in resistive memory applications. Furthermore, their ability to work effectively in both the optical and electronic domains makes the pursuit of information processing elements based on these alloys a promising and worthwhile field of research. An overview of cognitive and memristive technologies follows as a stepping stone to the research done within this project and presented in this chapter (17).

5.1.1.2   Resistive memory

Ionic conduction arises from the movement of negative (anions) or positive (cations) ions when an electric field is applied across an ionic material. The ions are effectively placed in gaps within a glassy structure. The gaps allow the ions an extent of freedom to move under the influence of an electric field. In a typical vitreous material, below the glass transition temperature the ionic conduction tends to be thermally activated and it is possible to calculate an activation energy. At temperatures greater than the glass transition temperature this fitting to an Arrhenius plot is not observed (136).

The chalcogenide based resistive memories in essence rely on a polarity dependent, resistive switching at a low write threshold voltage. The most effective of these technologies, is the nanoionics resistive RAM demonstrated by Kozicki et al (26; 27), where memory switching is achieved after a redox reaction driving metal ions in the chalcogenide glass forming metal-rich clusters that lead to a conductive bridge between the electrodes (Figure 5.1).

The memory element can be switched back to the off-state by applying a reverse bias voltage. In this case metal ions are removed and due to that size and number of metal-rich clusters are reduced resulting in an erased conductive bridge (resistance increase).

These technologies have demonstrated very small threshold voltages and high R_{on}/R_{off} ratio as well as low current consumption making it a promising candidate for future memory applications (Figure 5.2).
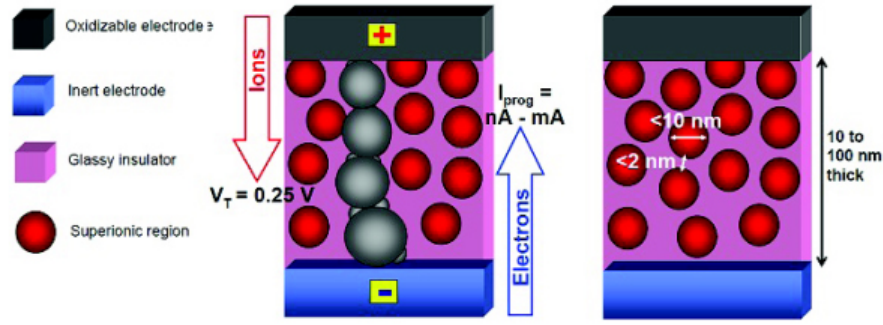
FIGURE 5.1: Representation of ionic movement across the RRAM structure as a function of electrical input [Reprinted from (26; 27)].
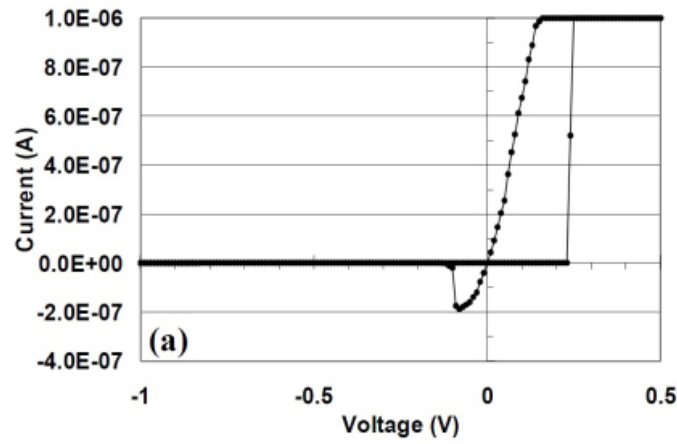
FIGURE 5.2: Typical current-voltage characteristics of a solid electrolyte RRAM device [Reprinted from (26; 27)].

5.1.1.3 Neuromorphic computing

5.1.1.3.1 Cognitive behaviour   Cognitive memory is the regime where the evolution of the state of the material does not change in a steep passage between an insulating to a conducting state. In such a regime a series of applied voltage pulses gradually change the state of the material giving almost endless intermediate states rather than the binary digital conventional memory and logic in use today. In a chalcogenide alloy on applying a set of voltage pulses crystallization occurs by nucleation and growth of phases as a result of the action of each current pulse. Thus, the nano-crystalites generated following a sequence of pulses build a coherent sequence of states. The nano-crystalites are randomly distributed in the amorphous chalcogenide material. As they increase and spread in the mass of the amorphous layer the conduction modifies in growing steps and in the end the current finds its way between electrodes through percolation. Once the percolation regime is achieved the material leaves the amorphous-cognitive regime to reach the multiple crystalline-cognitive regime, i.e. switches from the insulating state (bit:0) to the conductive state (bit:1), see Figure 5.3.

The essential feature of the step memory method is that it simulates the operation of the neuronal cell of a living being. A neuronal cell (a multiple memory, cognitive element) is operated by biochemical pulses coming from the neighbour cells. Only when enough pulses are accumulated the so-called "firing" state is formed in which the cell discharges and sends further the accumulated pulse. Thus, the neuronal cell operates by low accumulations and sudden discharges over a threshold level (137).
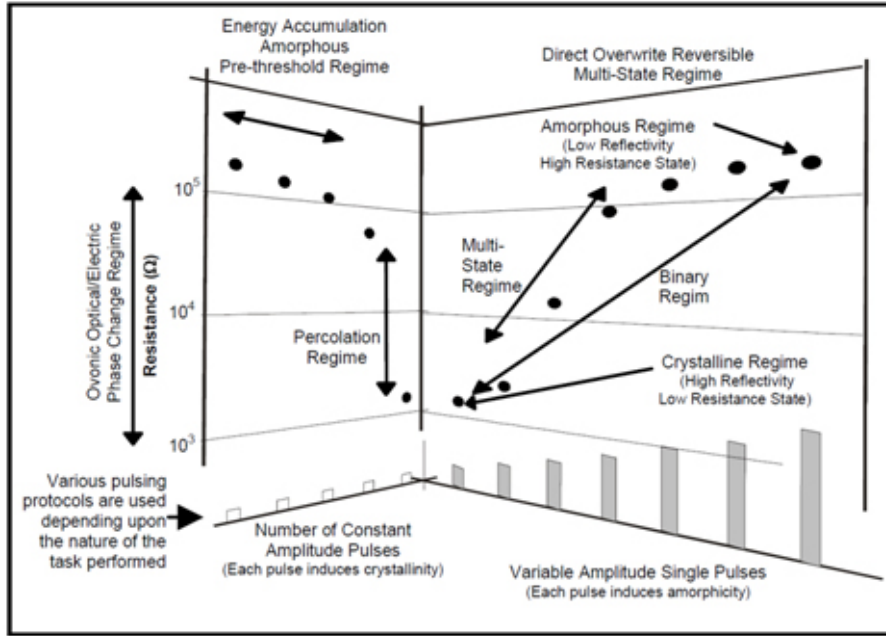
FIGURE 5.3: Representation of a typical characteristics of the cognitive behaviour within chalcogenides [Reprinted from (28)].

Chalcogenide can be deposited in a low-cost, thin film fashion in a continuous manufacturing process. They can also be integrated and embedded, that is hybridized with conventional silicon circuitry. Very importantly, they are scalable. A single device can operate at extremely small dimensions, for example less than 100 Angstroms. At the same time, its performance characteristics may improve the smaller the dimension. Therefore, as photolithography goes to smaller sizes it is advantageous to our device operation (137). Most notably both their binary phase change and cognitive behaviour can be induced both optically and electrically making the perfect candidate for future optoelectronic and all optical computing purposes.

5.1.1.3.2 Memristive behaviour   Originally theoretically proposed as one of the four basic electrical circuit components by Leon Chua in his landmark 1971 paper (138), a memristor is short for a "memory resistor" and is formally defined as a two-terminal element in which the magnetic flux Φm between the terminals is a function of the amount of electric charge q that has passed through the device. The relationship of this fundamental circuit with more familiar electronic elements is shown in Figure 5.4.
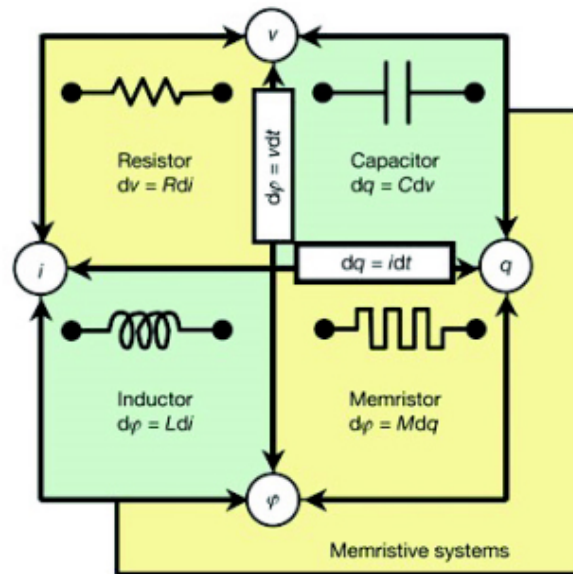
FIGURE 5.4: The four fundamental circuit elements in electronics [Reprinted from (29)].

A memristor shares many of the properties of resistors and shares the same unit of measurement (Ohms). However, unlike a resistor, in which the resistance is permanently fixed, memristance may be programmed or switched to different resistance states based on the history of the voltage applied to the device. This phenomenon can be understood graphically in terms of the relationship between the current flowing through a memristor and the voltage applied across the memristor (Figure 5.5).
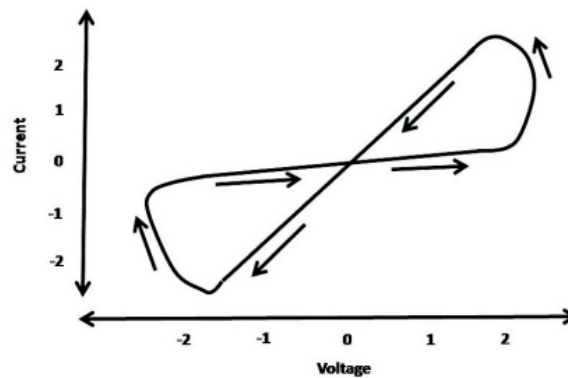
FIGURE 5.5: Typical current-voltage characteristics of a memristor given a generic AC signal [Redrawn from (30)].

Simply put, "memristance" is charge dependant resistance. Memristance defines a linear relationship between current and voltage, as long as charge does not vary. Of course, nonzero current implies instantaneously varying charge. Alternating current, however, may reveal the linear dependence in circuit operation by inducing a measurable voltage without net charge movement-as long as the maximum change in q does not cause much

change in M:

$$V(t) = M(q(t)) \times I(t).$$

Such a device was not demonstrated experimentally until 2008 by Strukov et al at HP Labs (Figure 5.6), where they developed a simple model of binary switch based on the coupled movement of both charge dopants and electrons in the semiconductor titanium oxide which resembled those proposed by Chua (138; 30). This device was fabricated
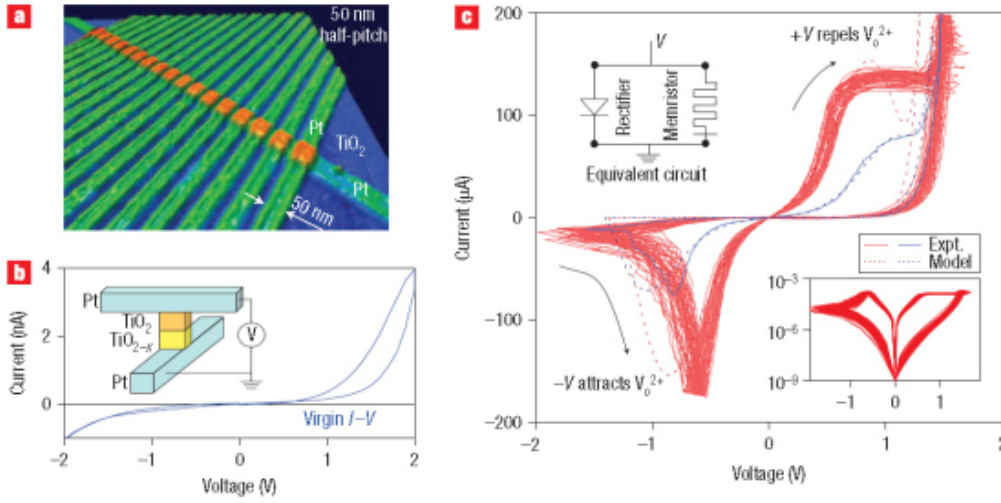
FIGURE 5.6: Schematic and typical current-voltage characteristics of a HP memristor
[Reprinted from (31)].

by nano-imprint lithography with a linewidth of 50nm or 150 atoms and the typical "pinched hysteresis" I-V characteristics proposed by Chua as the expected behaviour of the elusive memristor is observed through the device (139; 140; 141).

Titanium dioxide (TiO_2), which is also a semiconductor, has high resistance, just as in the case of intrinsic silicon, and it can also be doped to make it conducting. If an oxygen atom, which is negatively charged, is removed from its lattice site in TiO_2, a positively charged oxygen vacancy ($V0^+$) is created , which acts as a donor of electrons. These positively charged oxygen vacancies ($V0^+$) move in the direction of current applying electric field. Taking advantage of this ionic transport, a sandwich of thin conducting and non-conducting layers of TiO_2 are used to realise this memristor. Consider, we have two thin layers of TiO_2, one highly conducting layer with lots of oxygen vacancies and the other layer undoped, which is highly resistive. Suppose that good Ohmic contact is formed using platinum electrodes on either side of sandwich of TiO_2 (29). The electronic barrier between the undoped TiO_2 and the metal looks broader. The situation remains the same, even when a negative potential "I", is applied across electrode A, because the positively charged oxygen vacancies are attracted towards electrode A and the length of the undoped region increases. Under these conditions the electronic barrier at the undoped TiO_2 and the metal is still too wide and it will be difficult for the electrons to cross over the barrier.
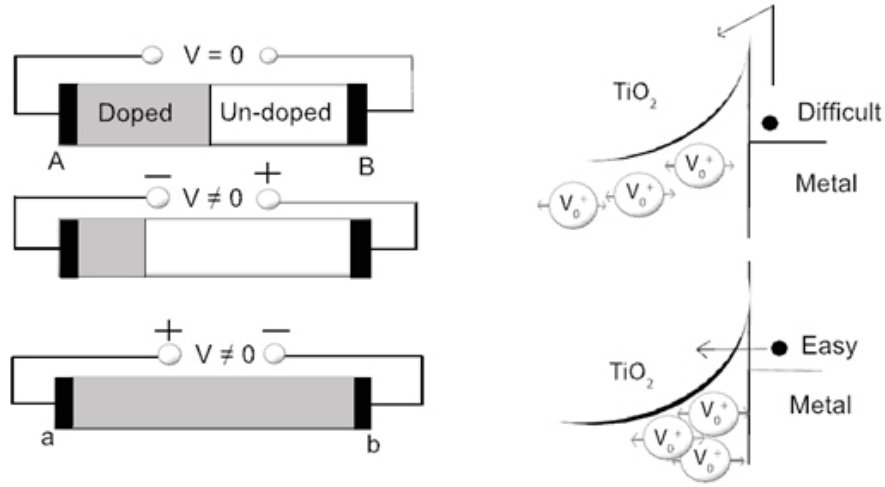
FIGURE 5.7: Ionic conduction mechanism in a titanium oxide based memristor.

However, when a positive potential is applied at electrode A the positively charged oxygen vacancies are repelled and moved into the undoped TiO_2. This ionic movement towards electrode B reduces the length of undoped region. When more positively charged oxygen vacancies ($V0^+$) reach the TiO_2 metal interface, the potential barrier for the electrons become very narrow, as shown, making tunnelling through the barrier a real possibility. This leads to a large current flow, making the device turn ON. In this case, the positively charged oxygen vacancies ($V0^+$) are present across the length of device. When the polarity of the applied voltage is reversed, the oxygen vacancies can be pushed back into their original place on the doped side, restoring the broader electronic barrier at TiO_2 metal interface. This forces the device to turn OFF due to an increase in the resistance of the device and reduce possibility for carrier tunnelling (Figure 5.7).

It is imperative to also note that this form of electrically induced oxygen vacancy movement is not unique to titanium oxide and has been demonstrated for different applications within what are known as OxRRAM (Oxide Resistive RAM) devices (142; 31; 143)(See Table 5.1).

Binary Metal Oxide	TiO_2, NiO, Cu_x, ZrO_2, MnO_2, HfO_2, WO_3, Ta_2O_5, Nb_2O_5, VO_2, Fe_3O_4
Perovskite	PCMO ($Pr_{0.7}Ca_{0.3}MnO_3$), LCMO($La_{1-x}Ca_xMnO_3$) BSCFO($Ba_{0.5}Sr_{0.5}Co_0...Fe_{0.2}O_3$-...), YBCO($YBa_2Cu_3O_{7-x}$), ($Ba_1Sr$)$TiO_3$(Cr, Nb-doped), $SrZrO_3$(Cr, V-doped), (La, Sr)MnO_3 $Sr_{1-x}La_xTiO_3$, $La-1-xSr_xFeO_3$, $La_{1-x}Sr_xCoO_3$,$SrFeO_{2.7}$, $LaCoO_3$, $RuSr_2GdCu_2O_3$, $YBa_2Cu_3O_7$
K_2NiF_4	$La_{2-x}Sr_4NiO_4$, La_2CuO_{4+}

TABLE 5.1: Overview of different material exhibiting resistive oxide based switching

The memristor both represents a new paradigm in logic circuits and cognitive computing as well as memory applications. This is possible as a memristor can both be turned on or off as well as remember the previous state of the device. Within the HP memristor, when the applied bias is removed, the positively charged Ti ions (which are actually the oxygen deficient sites) do not move anymore, making the boundary between the doped and undoped layers TiO_2 immobile. When we next apply a bias (positive or negative) to the device , it starts from where it was left.

In the case of a memristor both the ionic and the electron movement, into the undoped TiO_2 and out of undoped TiO_2 are responsible for the hysterisis in its curent-voltage charactericstics.

As with the cognitive switching of chalcogenides this also follows the performance of biological neural networks as the synaptic response also alter their response according to the frequency and strength of the signals.

5.2   Motivation

Lithium containing glasses have been investigated for solid state battery applications. Therefore, ionic storage in such materials can be useful also for data storage; a functional solid electrolyte consisting of crystalline metallic islands of Ag_2Se dispersed in amorphous semiconducting materix of Ge_2Se_3 has been studied extensively and has become a candidate host material as part of solid electrolyte data storage. However technologies exploiting phase change and electrolytic chalcogenide devices present an exciting opportunity at developing novel information processing devices, going beyond the world of memory into cognitive computing and reconfigurable logic circuits. In this work through exhibiting significant ionic conductivities, chalcogenide glasses are utilised for the fabrication of high densitivity oxide based information processing devices.

Using novel device architectures and switching regimes a number of devices are presented in this chapter where, both electronic and optoelectronic non-volatile reconfigurable circuits has been pursued with an outlook on the potential for simultaneous information storage/processing devices and the possibility of achieving cognitive computing using chalcogenide phase change and ion conduction as the basis for its operation contributing to the fields of ReRAM and FPGAs.

In this chapter an overview of the current technologies and concepts which exhibit great potential for future cognitive computing systems is presented. Subsequently, the devices designed and fabricated are presented followed by the operational characteristics of the said devices, finishing with a contextual summary of the results.
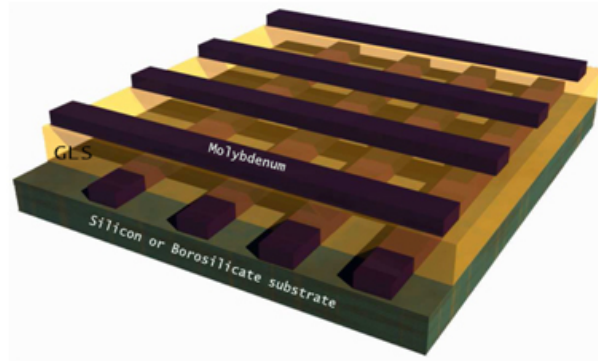
FIGURE 5.8: Representation of cross array cells used for cognitive switching, with molybdenum electrodes and a GaLaS active layer in between.

5.3 Fabrication

The work on neuromorphic devices set out in this report is divided into two main categories:

- Cognitive switching

- Memristive behaviour

The fabrication process used for the production of the devices used for each investigation is described here.

5.3.1 Cognitive switching

5.3.1.1 Electronic cognitive switch

Using the selective sputtering technique and a physical contact mask, a series of electrodes were created on glass substrates. This allowed the subsequent deposition of GaLaS (through sputtering) as the active layer. This was capped by a further electrode deposition stage at 90° to the original to allow for simple devices to be created for electrical characterisation of the different alloys (see Figure 5.8).

5.3.2 Memristive devices

The mask shown in Figure 4.10. which is a series of lines with varying width between 1μm up to 200μm was used as a bottom electrode of the devices.

The bottom electrodes were patterned on a borosilicate glass slide and subsequently a 300nm layer of molybdenum was sputtered on the patterned surface. While covering a section of these lines for contact in the characterisation stage, a subsequent second
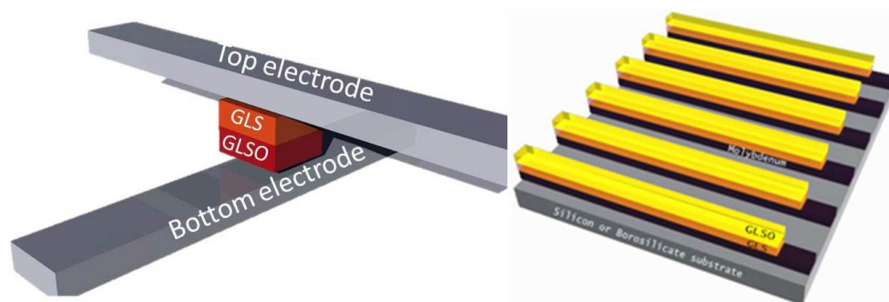
FIGURE 5.9: Molybdenum-GaLaS-GaLaSO- hybrid Test Sample used for memristive/RRAM switching.
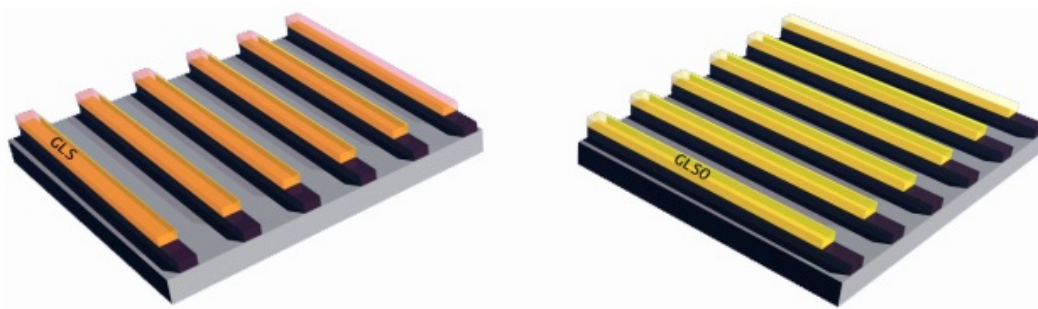
FIGURE 5.10: Pure GaLaS and GaLaSO control samples fabricated with molybdenum bottom electrodes.

deposition of a 100nm of GaLaS was carried out followed by a 70nm GaLaSO deposition and finally the photoresist was lifted off to leave us with the devices shown in Figure 5.9. These devices are characterised using the setup shown in Figure 4.34 as set out previously. Alongside this sample two control samples were also fabricated using the same process, one with only a GaLaS active layer, the other with a GaLaSO active layer (shown in Figure 5.10).

5.3.3   Logic gates

The reversible high to low resistance switching within chalcogenides used for phase change memory purposes can be used as a simple non-volatile switch. This enables the use of this phenomenon for information processing devices, such as programmable arrays as set out previously. In order to show the capability of this method for information processing, a series of logic gates were fabricated capable of basic Boolean operation. These series of proof of principle devices were fabricated with the potential to be used within all electronic or optoelectronic applications, demonstrating the versatility that using chalcogenides brings to the field.

5.3.3.1   Electronic gates

Electrical contacts were provided by molybdenum metal pads which were deposited by sputtering using the process described earlier. The substrate was kept at room temperature and the deposition power used was 100W, with argon gas flow of 15ccpm. The contacts were patterned using photolithography using a positive photoresist (S1805) and the lift-off technique with a pre-deposition oxygen plasma ash (using a 100W plasma power and 10ccpm oxygen flow), The ashing was also repeated post lift-off to clean the samples of any residue photo resist. The deposition power used was 45W and the argon gas flow was 37ccpm. Platinum electrodes were then created using electron-beam assisted platinum deposition using a FEI Helios 600 Focused Ion beam. The gap between these electrodes formed the final nanowire or memory cell. Scanning electron microscopy images of typical cells is shown in Figure 5.11.

A series of electronic logic gates were fabricated using photolithography to fabricate contact pads which converged to within 2μm of each other. This was followed by an oxygen plasma reactive ion etch to clean(ash) the sample. The devices were fabricated at the centre of this zone. E-beam induced platinum deposition was used to fabricate the nanowire electrodes.

Once the devices were patterned at the active zone, a photolithography step was carried out to define the zone in which chalcogenides were to be deposited to cover the previously fabricated nanowire electrodes with a nanogap as the active zone.

5.3.3.2   Optoelectronic gates

The optoelectronic logic gates were fabricated by using a photolithography step to define the grid electrodes followed by a sputtering and lift-off step. This was followed by a further photolithography step to define the area where the chalcogenide was to be deposited leaving the contacts clear for characterisation. This was followed by a two-step sputtering deposition, where the chalcogenide and capping layer are deposited and a final lift-off and ashing step to clean the device, see Figure 5.12. It should be noted that all the logic gates reported were fabricated on a variety of substrates to provide different information during process optimisation.

5.4   Characterization

5.4.1   Electronic logic gates

The experimental setup shown in Figure 5.13 was used in order to introduce the appropriate pulses, verify the pulse integrity as well as, measure and store the resistance
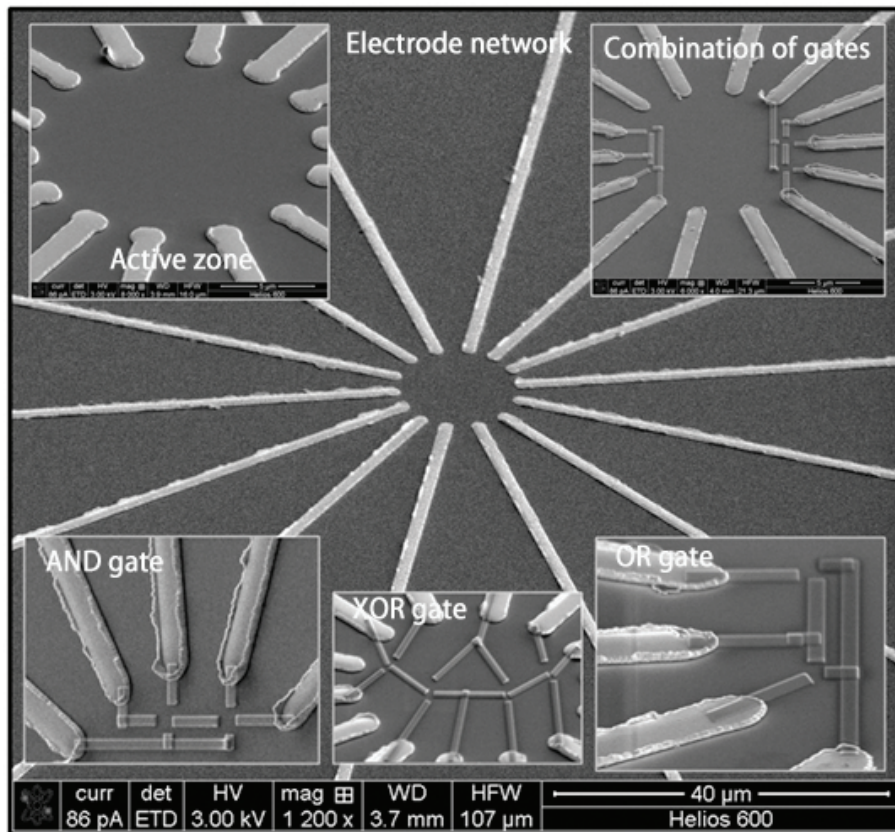
FIGURE 5.11: Scanning electron microscopy images of fabricated electronic logic gates before final sputtering of the chalcogenide and capping layers. The nanogaps between the nanowires deposited provide the switchable area in the final devices.
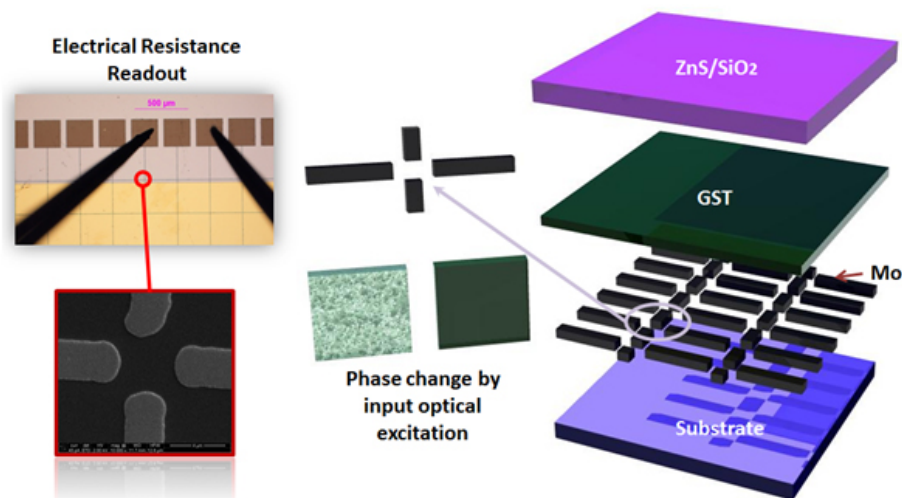
FIGURE 5.12: (top left) optical microscopy image of the optoelectronic logic gates during characterisation with electrical probes visible on contact pads. (bottom left) scanning electron microscopy of nanogaps in the programmable array which act as optoelectronic switches on the application of optical phase transition pulses. (right) Model of the structure of the optoelectronic gates showing the electrodes in a programmable array architecture with a phase change GeSbTe layer and ZnS/SiO2 capping the device.
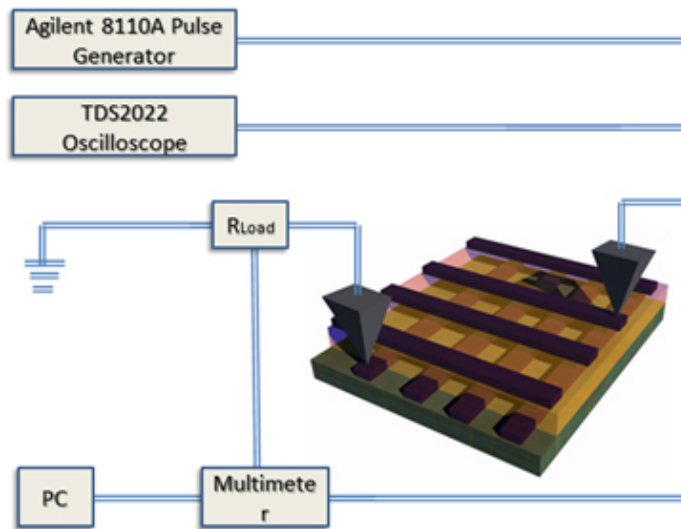
FIGURE 5.13: Experimental setup used for the dual pulse switching measurements.
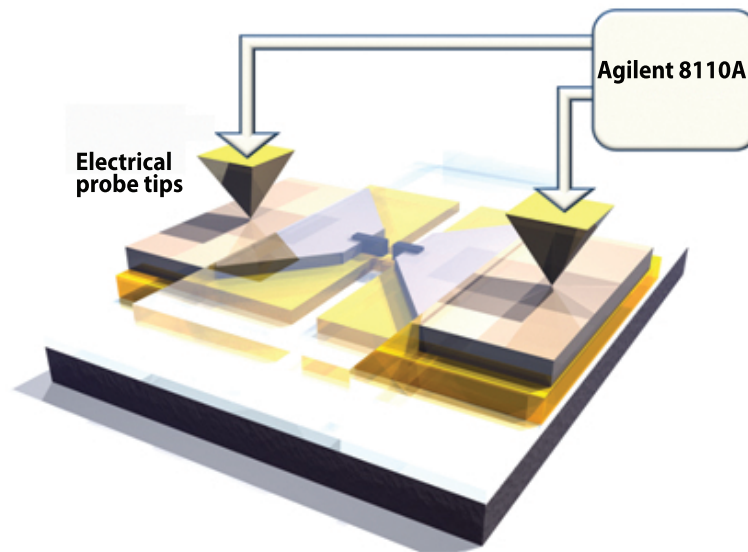
FIGURE 5.14: Simple setup used for characterising the phase change nanowire memory cells

across the cell as a result of these pulses. The other setup used specifically to pulse switch the nanowire lateral cells where sweeps were introduced to switch the cells is shown within Figure 5.14. Two different set of experimental setups were used in order to induce phase change within each phase change alloy used (Shown in Figure 5.13 and Figure 5.14). The dual pulse mechanism used to crystallise and melt quench the phase change layer is shown in Figure 5.15. The longer pulse with a lower energy crystallises the alloy while the shorter higher energy pulse re-amorphises the phase change layer.
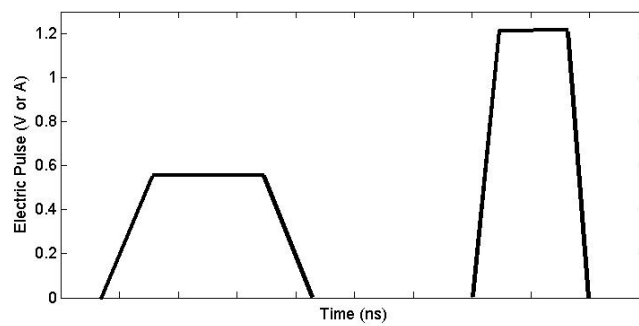
FIGURE 5.15: Two pulses are provided to allow switching between the two states of the phase change layer.

5.4.2   Electrical cognitive switching setup

The setup shown in the previous section was used to induce electronic cognitive switching by using a train of nanosecond sub-threshold pulses to slowly crystallise the active layer.

The pulsing system used to induce cognitive switching within the device fabricated previously is shown in Figure 5.16.
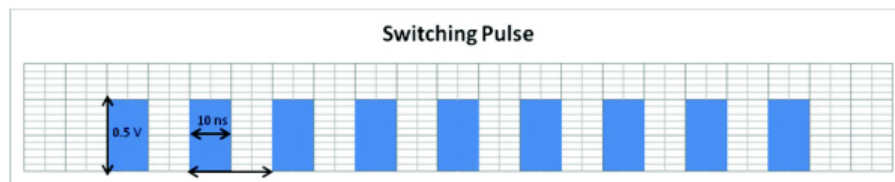
FIGURE 5.16: Pulses used for cognitive switching of the cross array GaLaS cells with 10ns pulse width and 10us period.

It should be noted that a single pulse within this pulsing system supplied to the device does not have enough power or the required duration for switching of the cell. The resistance of the cell was recorded simultaneously to allow the observation of the state of the cell as a function of the number of electrical pulses sent through the cell.

5.4.3   Memristive switching setup

This setup was also used to observe the memristive properties of the GaLaS-GaLaSO hybrid devices. The difference being that a low frequency AC signal is used at the input. As such the AC signal shown in Figure 5.17 was used and the current-voltage characteristics of the device were measured simultaneously.
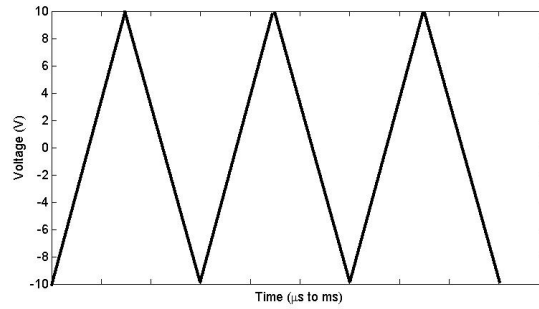
FIGURE 5.17: Low frequency AC signal sent through the system with a period of 22.5 seconds and amplitude of 10V.

5.4.4 Optoelectronic gate setup

The setup shown in Figure 5.18 was used to characterise the optoelectronic logic gates. This provided the capability for targeted spatial excitation of structural transitions in the thin film phase change layer at the interconnections of the electrodes, thereby effectively making and breaking a circuit. This system is based on a 660 nm diode laser focused to a spot size at target of up to 50 μm diameter. Electrical probe micro positioners were used to contact the devices and the resistance is measured via a multimeter simultaneously.
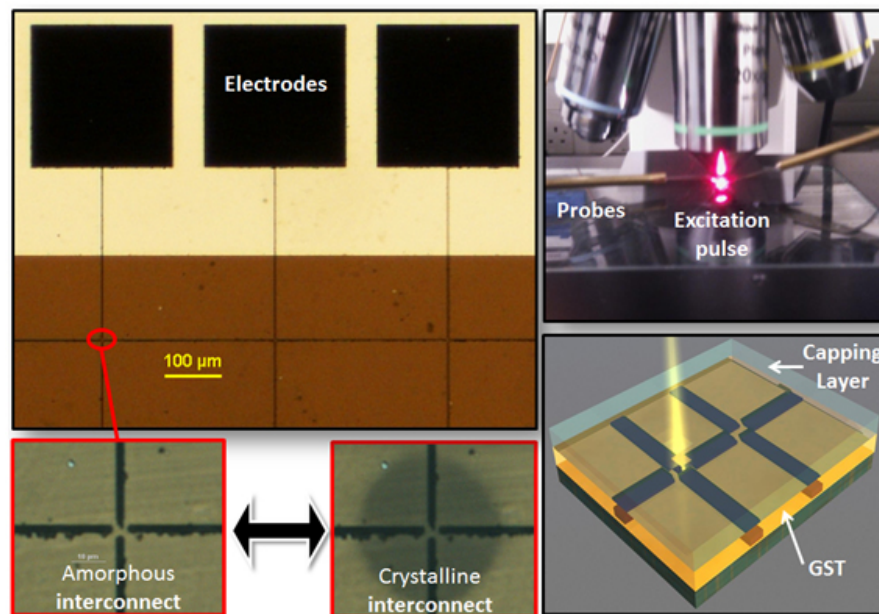
FIGURE 5.18: schematic of the experimental setup. Top left) Transmission optical microscopy of chalcogenide optoelectronic gates. Lower left) Amorphous and crystalline interconnect representing an open and closed switch respectively. Upper right) photo of experimental setup showing the optical phase change laser input and the electronic probes measuring the resistance of the circuit. Bottom right) Artistic model of optoelectronic gate with optical input excitation.

5.5   Results and discussion

5.5.1   Electronic logic gates

The dual pulse setup described previously was used to switch active zones A and B, while monitoring the output. This can be seen in Figure 5.19. One can observe that the resistance of the output current-voltage characteristics is in the high resistance state until both A and B have been switched to a low resistance showing the characteristics of an AND gate. The AND gate is a basic digital logic gate that implements logical conjunction. A HIGH output (1) results only if both the active zones to the AND gate are crystalline. If neither or only one active zone on the AND gate is amorphous, a low output is observed. In another sense, the function of AND effectively finds the minimum between two binary digits, just as the OR function finds the maximum.

Therefore, the output is that the circuit is never complete and thus the output is always 0 except when all the input active zones are in a low resistance crystalline state. This architecture presents obvious advantages to CMOS transistor based recognfigurable logic circuits as one can process information with as little as two nano grains, with additional advantages in terms of fabrication due to its simpler and cheaper fabrication process. Figure 5.19 shows the four states of the gate while also monitoring the output signal.
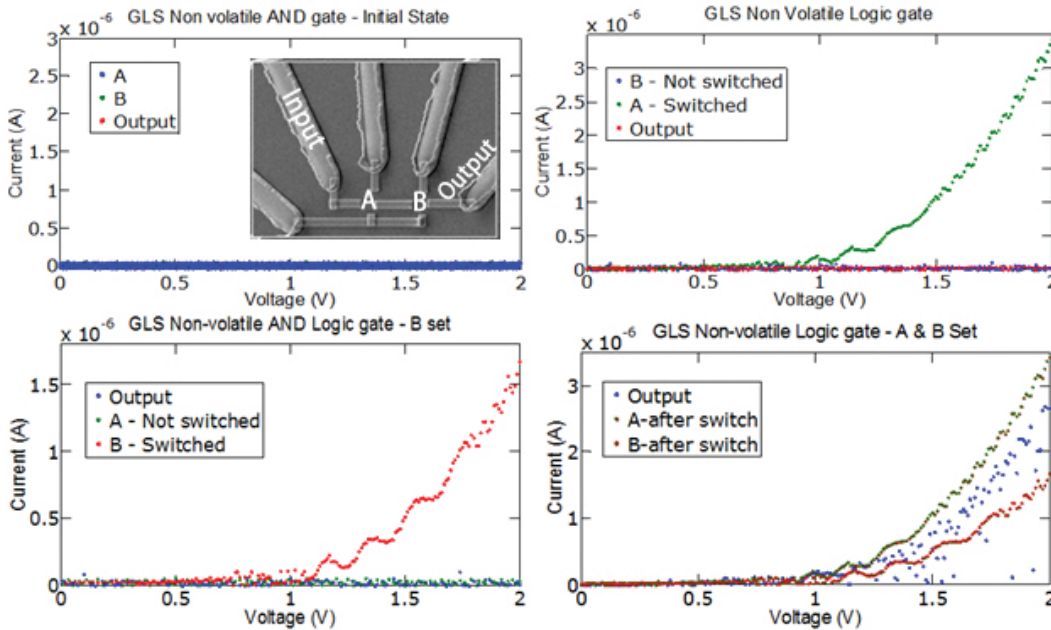
FIGURE 5.19: The four states of the GaLaS non-volatile AND gate. When both A and B have been switched to a low resistance crystalline state the output resistance is lowered drastically.
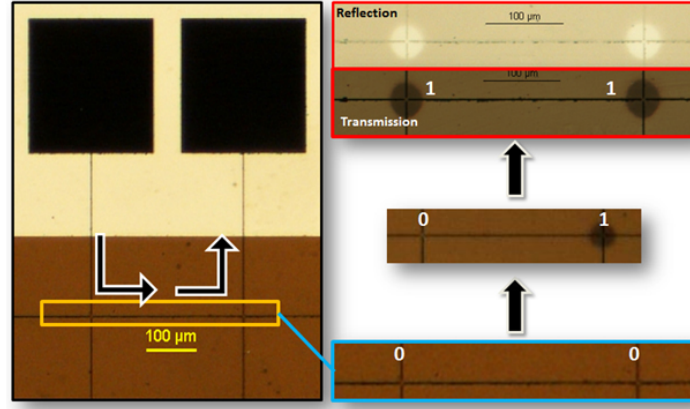
FIGURE 5.20: Optoelectronic nonvolatile AND logic gate using GeSbTe. Right) Reflection and transmission optical microscopy images show the different states of the logic gate.

5.5.2 Optoelectronic logic gates

The concept of reconfigurable logic gates is further extended to a cross platform optoelectronic device where the switching excitation input is optical pulses at 660nm wavelength for 200ns and 100ns pulse widths to crystallise and amorphise the active zones as shown in Figure 5.20 and Appendix A. The operational principle is universal across both the electronic and optoelectronic gates. For instance, as a brief description of the AND gate was provided previously, here we may focus on the OR optoelectronic gate architecture as shown in Figure 5.21, works on the principle that upon the crystallisation of either zone A or B the output sensed at the output will be high.

The output of the gate will only be low when both zones A and B are in an amorphous high resistance state. As such one can observe the full truth table in the observed resistance reading in Figure 5.21 and Appendix A as well as Table 5.2, as cycling between the four states of the inputs of the gate one can observe that the resistance remains low unless both input zones are in their amorphous state, if any or both of the inputs are
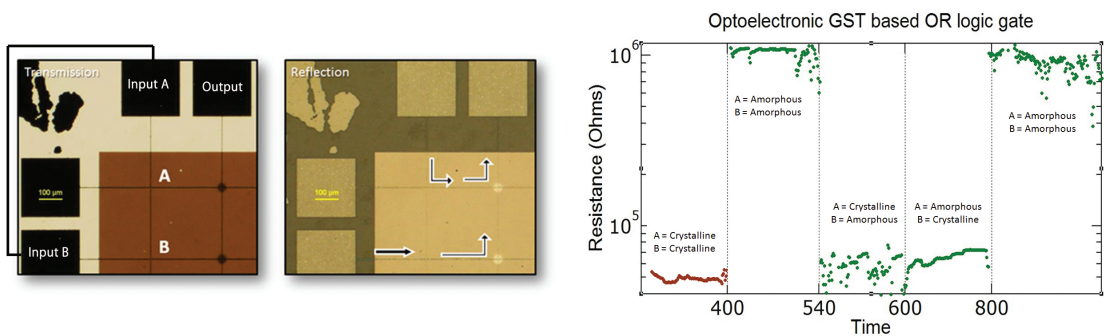
FIGURE 5.21: Optoelectronic nonvolatile OR logic gate using GeSbTe. (left) Reflection and transmission optical microscopy images show the different states of the logic gate.(right) Resistance reading of the device in the four possible states of its respective boolean truth table.

A		B		Output
Amorphous	0	**Amorphous**	0	0
Crystalline	1	**Amorphous**	0	1
Amorphous	0	**Crystalline**	1	1
Crystalline	1	**Crystalline**	1	1

TABLE 5.2: OR optoelectronic logic gate. Amorphous(0)=High resistance state, Crystalline(1) =Low resistance state

crystallised, in this instance through optical excitations that output will be in the low resistance, high (1) output level.

The use of the resistance change accompanying the phase transition from amorphous to crystalline and vice versa provides a novel platform for reconfigurable logic arrays, the unique physical properties of the chalcogenide alloys which makes them the most versatile optoelectronic material and the universality of the phase change phenomena in both the optical and electronic regimes, has been the basis for the proof of principle devices demonstrated. The demonstrated operational characteristics further highlights the potential which these materials hold beyond the world of pure data storage into the field of ultra low power non-volatile data processing.

5.5.3   Cognitive behaviour

5.5.3.1   Electronic

As set out previously this behaviour was observed while exciting the device with sub-threshold pulses whilst the resistance of the cell was recorded simultaneously to allow the observation of the state of the cell as a function of the number of electrical pulses sent through the cell. The results are shown in Figure 5.22.
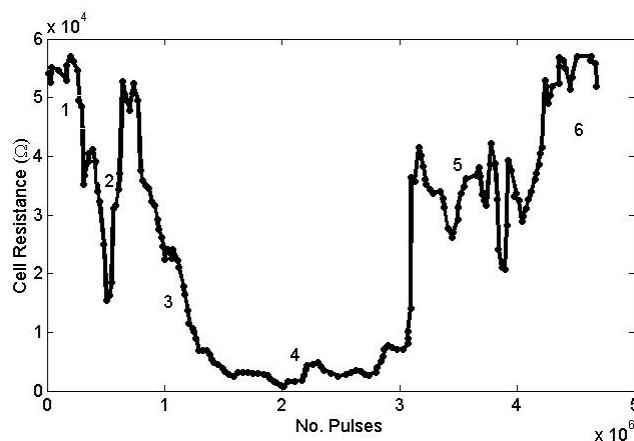
FIGURE 5.22: Cognitve behaviour of GaLaS cross array cell as a function of a train of pulses.
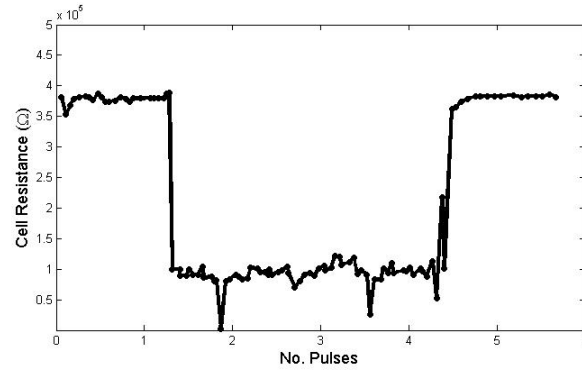
FIGURE 5.23: Single pulse switching of GaLaS cells as a control experiment.

Within the resistance characteristics four distinct regions can be observed, which can be explained through the following. The cell starts in the high resistance amorphous state, this turns into the oscillations observed in region 2. In this region threshold switching is being induced, as the resistance drops and returns to its original high resistance state as the power or duration of the pulses is not enough to memory switch the cells. During this state the electrons are filling the vacancies of the chalcogenide, but no phase change has occured. Once all the vacancies between the two electrodes are filled, the gradual change in resistance observed in region 3 begin, where the resistance does not return to its original amorphous state, but a gradual cognitive analogue phase change occurs. During this stage nanocrystals are being formed within the chalcogenide layer, the more pulses are sent the higher the number of these nanocrystals. Once enough nanocrystals are formed to bridge the gap between the two electrodes, the cell enters region 4 observed in the characteristics. In this region a crystal filament bridges the gap between the two electrodes, thus a stable low resistance is observed. As more pulses are sent through the cell the temperature of the filament rises, this incremental rise in temperature with each pulse sent through, ends in the eventual change jump to a high level resistance, as the cell melt quenches to its original amorphous state. The intermediate stage between the low and high resistance state is the crystal filament being melt quenched gradually starting from the area closest to electrode until the filament is phase changed in its entirety to its original amorphous state. It should be noted that this is a possible mechanism and other physical mechanisms such as multiple filament formation may also be responsible for the characteristics observed.

Further experiment was carried out where single pulse switching on the same cells was induced by a series of incrementally increasing pulses until the cell could be switched with one pulse whilst the resistance was recorded simultaneously. The observed results are shown in Figure 5.23.

The pulse duration used in this experiment was 20ms. A simple calculation discussed below reaffirms the idea that the material in fact "remembers" the pulses sent through it and like a neuron only changes when a certain threshold is reached. If we consider that
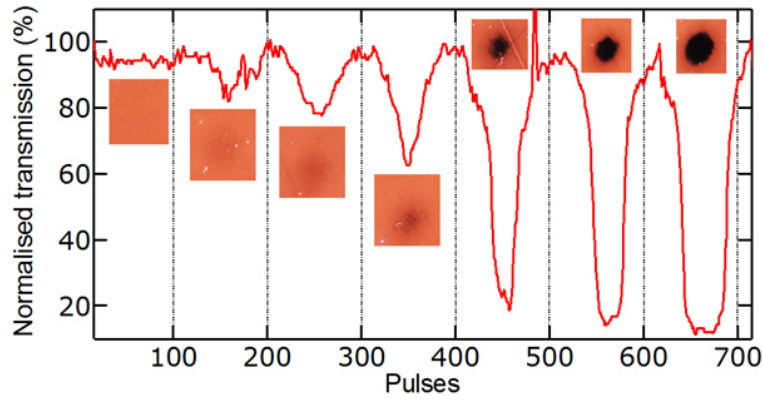
FIGURE 5.24: Multi-level quasi analogue transmission change in optically phase changed GeSbTe spot. Insets are transmission optical microscopy images of the different levels of switching observed on the GeSbTe film, with the corresponding graphs at each stage showing the line scan of the detector, exhibiting the multi-level change in the transmisssion of the phase change film as a result of the different number of pulses in the train of pulses being used to switching the film.

2×10^6 pulses of 10ns duration yields a low resistance state (as shown in Figure 5.22), then the cumulative duration of the pulses is 20ms. This corresponds with the single pulse switching results where after a 20ms pulse the high resistance of the cell changes to a stable low resistance state.

5.5.3.2   Optical cognitive switching

One can also use optical pulses in precisely the same fashion in order to induce multi-level gradual quasi analogue crystallisation as opposed to a simple on/off state in optical switching (Figure 5.24), this can act as a perfect platform for a number of next generation logic and information processing devices.

This precise control over the level of optical change which can be induced in the phase change thin film can lend itself very well to the concept of ultra thin metamaterial optical switches discussed in Chapter 6.

It should also be noted that recently Wright et al (144), have also demonstrated cognitive switching of GeSbTe films for biologically inspried arithmetic operation, which shows the great promise that crystallisation in such a manner can hold for next generation information processing devices.

5.5.4   Memristive/RRAM behaviour

The hybrid GaLaS-GaLaSO sample fabricated, (Figure 5.9) as set out previously demonstrated resistive switching in what can be described as both OxRRAM switching (Figure 5.25) as well as memristive in nature, although one can categorise both distinct
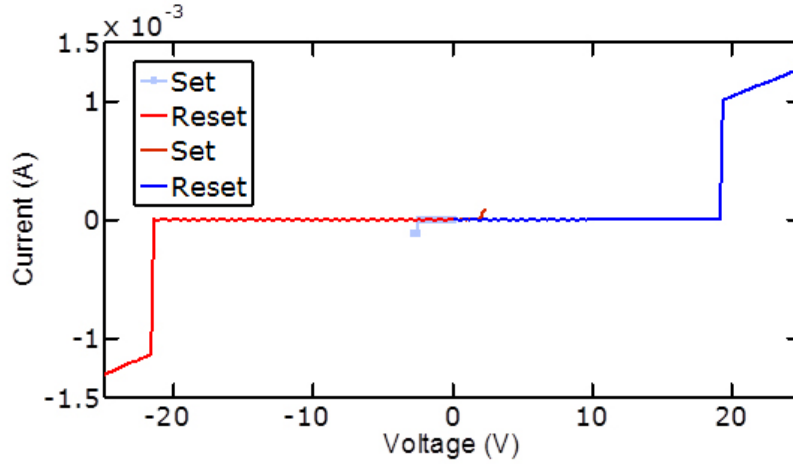
FIGURE 5.25: Bidirectional set and reset current voltage characterstics of the GaLaSO based device.

phenomena as memristive behaviour in the AC and DC regimes .

The sample was characterised by sending different sweeps through the device whilst in parallel the I-V characteristics of the device were recorded in order to observe the varying resistance of the device as a result of the electrical power being put through it (memristance). The current-voltage characteristics of the device over many sweeps in both positive and negative polarities is shown in Figure B.2.

A bidirectional resistance change is observed in these characteristics (Figure 5.26) which indicates that this is not in fact electrically induced phase change switching. Typical read state current voltage characteristics is shown in Figure 5.26, with the corresponding resistance memory window of operation, showing a resistance ratio of up to 10^6 ohms.

For a further investigation of the resistance switching behaviour in GaLaSO-based
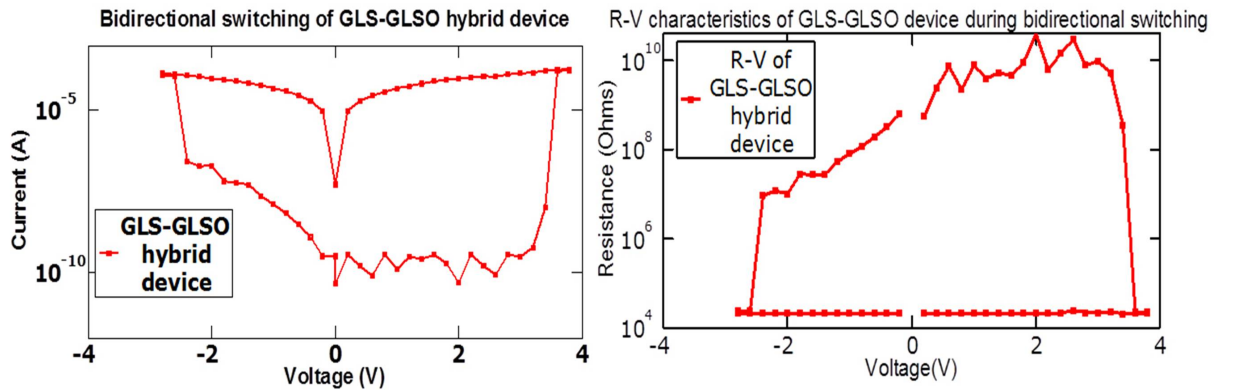
FIGURE 5.26: (left)current voltage characteristcs of the device in the ON state in both polarities, showing the non-volatilitiy of the resistive switching. (right) The corresponding resistance memory window showing up to and above 10^8 ohms resistance change in both directions.
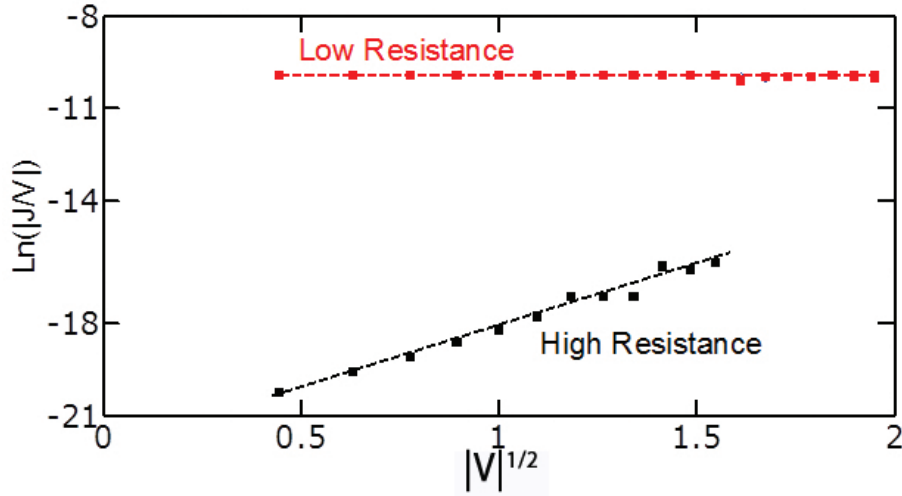
FIGURE 5.27: Ln(J/V) versus $V^{1/2}$ for the high and the low resistance states. Showing Poole-Frankel emission in the low resistance state.

ReRAM devices, various conduction mechanisms, including Schottky emission, Poole-Frenkel emission, space charge limited conduction, and Ohmic conduction were analysed based on the characteristics, among them, evidence of Ohmic and PooleFrenkel conduction behaviour was observed.

It was observed that Poole-Frenkel emission is dominant in a high electric field. This behaviour is related to the crystalline defects formed in the GaLaSO layer, e.g., oxygen vacancies or metal ions. On the other hand, the low resistance state showed a good linear fit to the Ohmic conduction curve, as shown in Figure 5.27. These results may be due to the conducting filament generation during the set process. Among the many proposed resistance switching models, the filamentary mechanism can be applied to explain the resistance switching behavior observed in this study. According to the filamentary model, tiny conducting elements, such as oxygen vacancies or metal ions, congregate to form stronger and more localized conducting filaments, which then lead to a transition from HRS to LRS. Therefore, the conduction of the LRS shows the Ohmic behavior because the current can be transported through the metallic filaments.

After reset switching, the conducting filaments can be ruptured by a Joule heating effect and the resulting device was transited from LRS to HRS. In HRS, conduction shows PooleFrenkel emission that is related to the charge transport in a bulk material filled with electrically charged defects. The filament model suggests that crystalline defects, such as grain boundaries and dislocations, provide easy diffusion paths for oxygen or metal ions in oxygen heavy chalcogenides and metal oxides materials. Hence, these defects congregate easily around the grain boundary and assume localized conducting filament forms. Therefore, resistance switching can be achieved even under a low electric field.
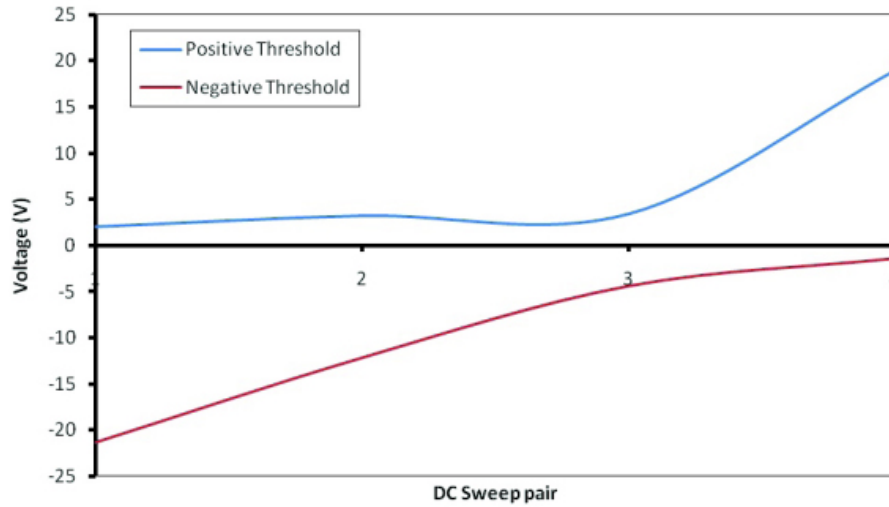
FIGURE 5.28: Threshold voltage of the device across several DC sweeps, is a good indication of the switching region of the device with 0V original being the boundary between the GaLaS and GaLaSO layer.

Furthermore, the bidirectional resistance switching can also be manually reset to a desired polarity state by a further sweep (see Figure 5.25). Subsequent to this sweep the I-V characteristics of the device are shown in Figure B.3. The observation shows that the current-voltage characteristics of the device are reset to its original threshold voltage and R_{on}/R_{off} ratio. However, as the polarity set sweep was in the positive direction the threshold voltage is in the positive direction this time instead of the negative polarity as before.

This can be observed much more clearly by observing the relationship between the positive and negative threshold voltages as a function of the DC sweeps and the polarity reset sweep put through the device. This is effectively an observation of the depletion region of the device and can be seen in Figure 5.28.
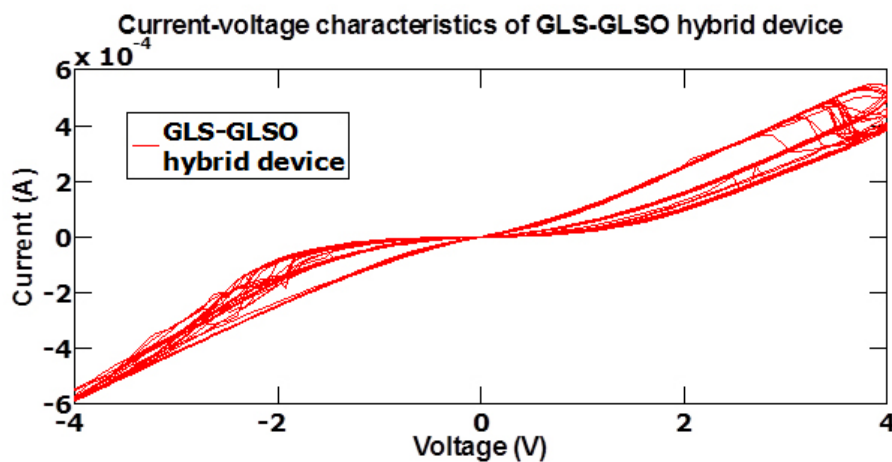
FIGURE 5.29: Repeated measurements of the memristance of the hybrid device over many cycles.
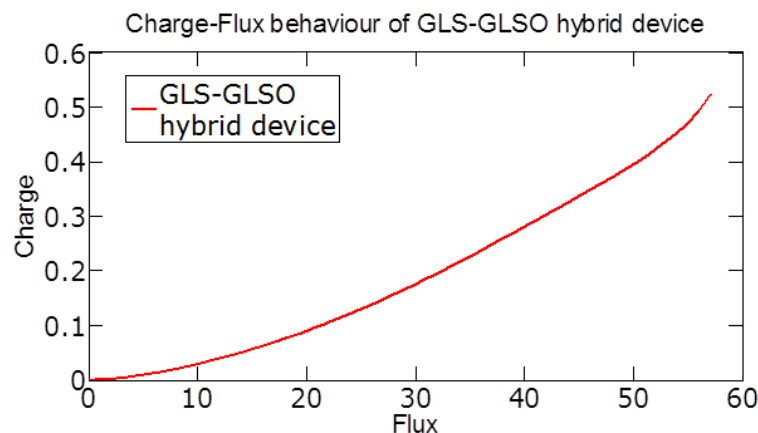
FIGURE 5.30: Charge-flux characteristics of the device showing the non-linear relationship arising as a result of the memristive nature of the behaviour of the GaLaS-GaLaSO hybrid device.

Based on the experimental results it is understood that at any given point the device has two threshold voltages in both polarities. The position of these threshold voltages can be changed based on the electrical power and polarity put through the device. This in essence can move the cloud of oxygen vacancies between the two electrodes.

When in the low resistance state, by applying a low frequency AC signal, one can observe a different type of behaviour as shown in Figure 5.29.

The nonlinear relationship between the charge and flux across the device can be better observed in Figure 5.30, where the reciprocal of the slope is the varying memristance of the device with respect to the charge input. This is a clear indication of the memristive nature of the behaviour of this hybrid device.
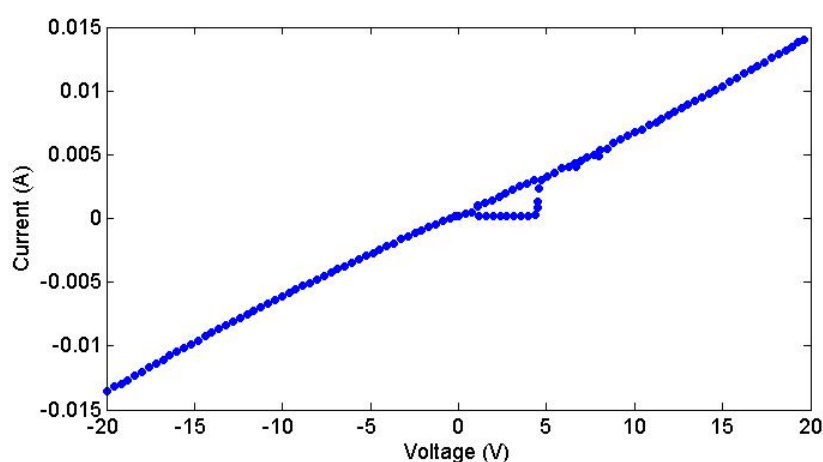
FIGURE 5.31: Current-voltage characteristics of single active layer GaLaS based device for control experiment purposes.
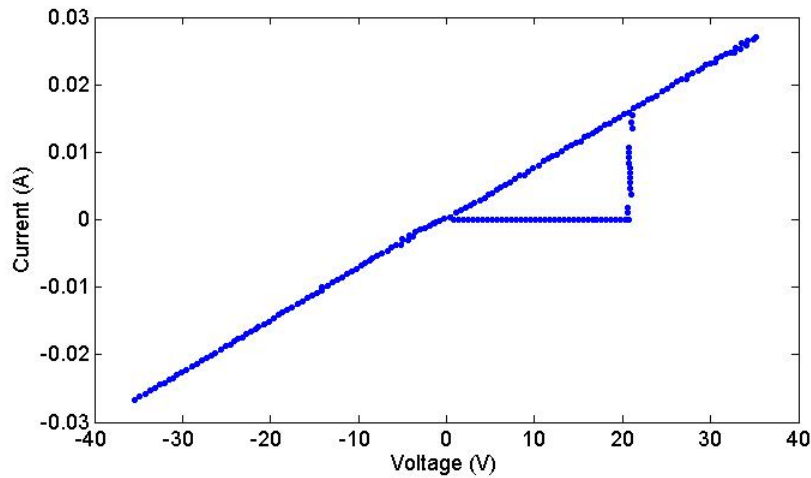
FIGURE 5.32: Current-voltage characteristics of single active layer GaLaSO based device for control experiment purposes.

The I-V characteristics of the device along with the simulated behaviour of how a memristor would behave given the parameters of our device are shown in Figure B.5.

The experimental results and ideal simulation results show a high degree of agreement and reaffirm the idea that this in fact is a memristor.

A series of control experiments were also carried out with single layers of GaLaS and GaLaSO instead of the hybrid two active layer device (Figure 5.31 and Figure 5.32). These show the typical phase change behaviour with two resistance states expected from a phase change alloy, which is distinctly different from the behaviour observed on the hybrid devices.

These experiments highlighted the difference between unidirectional phase change current-voltage characteristics and that of nanoionic bidirection resistive/memristive behaviour exhibited by the hybrid device.

The GaLaS-GaLaSO hybrid device is essentially a memristor and ReRAM in one material device both satisfying synaptic logic and memory switching given different electrical inputs and shows a device capable of one material solution that brings phase change and resistive RAM together with cognitive memristive logic through material properties. Making it an unprecedented way of achieving a universal memory/logic chip and realising the dream of inorganic neuromorphic computers.

The need for such devices is becoming increasingly apparent as future memory and processing architectures are being proposed and investigated for ultra low power device applications. In this pursuit, nanocrossbar arrays consist of a set of parallel bottom electrodes and perpendicular top electrodes with a thin layer of resistive switching material in between is the most promising. The simplicity of the geometrical structure and the absence of transistors make the concept extremely interesting for low power non-volatile

memory concepts and high integration, because the cell size can be reduced to $4F^2$ (F=minimum feature size) . The integration density can be further increased to $4F^{2/n}$ by stacking n crossbars on each other, whose cells can be operated without influencing each other. However, as all the cells in a row are connected to each other by the top electrode and all cells in a column are connected to each other by the bottom electrode, sneak paths, are still an inherent disadvantage of passive crossbar arrays. They significantly limit the size of a crossbar array (maximum numbers of rows and columns), as the current and voltage drop over the addressed element is strongly dependent on the current through multiple parallel sneak paths. Furthermore, the overall resistance of the crossbar array depends on the numbers of 0s and 1s stored in the array and, thus, the power consumption increases, if the resistive cells are mainly in the low resistance state. The integration of a rectifying element would solve the sneak path problem. The low current consumption and bipolar switching ability of the GaLaSO based devices provides a unique path to forming an ultra low power chalcogenide phase change memory cell with an integrated diode of the same material with a highly doped layer to act as a rectifying thin film selector diode in future computer architectures.

5.6   Summary

The primary objective of this work was to investigate the suitability of chalcogenides for more exploratory information processing devices. Proof-of-principle demonstrations of novel devices providing AND and OR logic operations in electronic and optoelectronic modes of operation has been pursued. Observations of bidirectional resistive switching in more complex sulphide based structures also indicate the possibility of utilising these thermally stable chalcogenide films in resistive memory applications.

In reaching these goals, significant landmarks have included:

- Electronic non-volatile phase change logic gates
  - AND gate

- Optoelectronic programmable logic gates.
  - AND gate
  - OR gate

- Observation of bidirectional switching in oxygen rich gallium lanthanum sulphide (GaLaSO) hybrid device.

- Optical cognitive multilevel transmission switching of GeSbTe thin film

- Observation of bidirectional resistive switching of GaLaSO hybrid device.

- Observation of memristive response of GaLaSO hybrid.

The knowledge and expertise derived from these achievements set a strong foundation for the continuation and expansion of research work in the field of chalcogenide information processing devices, in particular the marriage of optical multilevel switching and opto-electronic logic elements with metamaterials(metamaterials are described in Chapter 6), can bring about full memristive information processing capability as well as multi-level cognitive operation which allows low footprint processors, whilst the non-volatility allows "true sleep" computing using ultra low power consumption.

Chapter 6

Metamaterial Phase Change Optical Switches

6.1 Background

The phase change technology behind the current rewritable optical disks and the latest generation of electronic memories has provided clear commercial and technological advances for the field of data storage, by virtue of the many key attributes chalcogenide materials offer (145). New generations of optoelectronic devices are being driven by the merging of optics and electronics, as photons and electrons begin to cooperate in a single material platform. As a part of this evolution, plasmonics and metamaterials bring with them the ability to focus and manipulate light on the nanoscale, far beyond the diffraction limit of conventional optics. With such strong credentials in the 'parent' fields of photonics and electronics, it is more than reasonable to assume that chalcogenides have much to offer in the plasmonic domain as well. With these considerations in mind the use of chalcogenide glass media in active plasmonic switching devices are considered and proof of principle demonstrations of nanophotonic switching in the near and infrared domain based on reversible photo-induced changes in the optical properties of a chalcogenide thin film is presented (34; 146).

6.1.1 Metamaterials

Metamaterials comprise a rapidly advancing research field, with new directions constantly emerging. As a result, it is not an easy task to coin a universally accepted definition without risking to exclude important areas of research (143). We therefore adopt the rather loose definition of (147), according to which metamaterials are artificial media consisting of electromagnetic resonators in crystal-like arrangements with a pitch smaller than the wavelength of excitation (32).
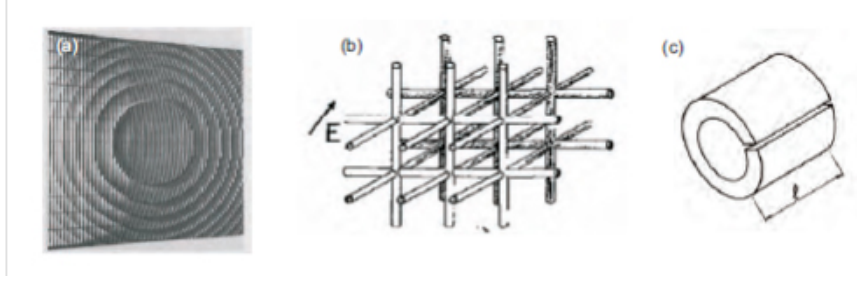
FIGURE 6.1: (a) Lens comprised by metallic plated in refractive index less than unity. (b) Array of dielectric rods exhibiting plasma behaviour. (c) Primitive form of the split-ring resonator [Reprinted from (32)].

Owing to their sub-wavelength structuring, metamaterials appear as effective media to an incident wave with constitutive parameters defined to a large extent by their geometry. Hence, by appropriate patterning, the constitutive parameters of metamaterials can be tailored across a wide range surpassing the properties of naturally available materials (32).

Probably the first metamaterial is the jute composite used by Bose in his polarization rotation experiments (32; 148). Almost fifty years after Bose, it was suggested that a lens consisting of stacked metallic plates acts as an artificial dielectric with refractive index less than one, while soon after it was realized that metallic and dielectric rod can simulate plasma behaviour at microwave frequencies (32; 149; 150) (see Figure 6.1). Almost another forty years had to pass before the next step in metamaterials research, when Sir John Pendry suggested that an ensemble of split-ring resonators (SRRs) -introduced earlier to create a magnetic resonance at GHz frequencies (32; 151), can constitute an effective magnetic medium described by a macroscopic permeability (32; 152). Armed by artificial media with controllable electric and magnetic response, structures that present simultaneously negative electric permittivity and magnetic permeability were realized (32; 153) (see Figure 6.2(a)), a concept considered earlier but remained a theoretical peculiarity due to a lack of appropriate materials (154; 155; 156; 157). The potential of such media was realized by Pendry who suggested that they can be used to build a perfect lens, i.e. a lens that harvests both propagating and evanescent fields and hence is not limited by the wavelength of light (158). Pendry's theoretical predictions were soon followed by an experimental demonstration of the concept at microwave frequencies (159).

Microwave metamaterials were successfully scaled down to operate at mid- and near-infrared wavelengths with moderate efforts and no significant change in their electromagnetic properties (160; 161). However, transferring the metamaterial concept in the optics domain was hindered by unforeseen obstacles. On one hand the technical difficulties of structuring materials at the nanoscale restrict visible metamaterials in thin layers, in contrast to their three-dimensional infrared and microwave counterparts. On the other hand, the high losses associated with metals at optical frequencies and the
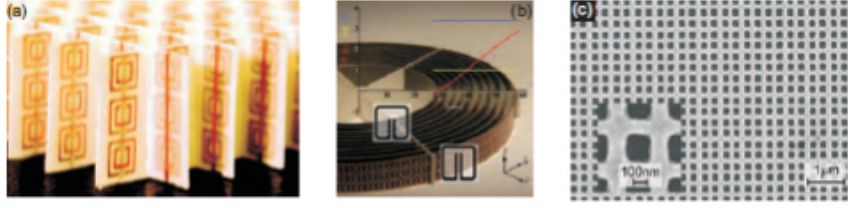
FIGURE 6.2: (a) First realization of a negative refractive index medium. (b) Mircowave metamaterial with invisibility cloak functionality. (c) An optical negatively refractive metamaterial based on the first-net structure [Reprinted from (32)].

saturation of the magnetic response of SRRs degrades metamaterial performance significantly (32; 162). The solution was given by a radical change in the geometry of metamaterial resonators, replacing SRRs with metallic elements of appropriate shape. Following this approach optical negative refractive index metamaterials were demonstrated based on pairs of metallic rods (32; 37) and on its complimentary structure, namely pairs of voids on metal films (32; 163), as well as on variations of the latter (164) including the so-called fishnet structure (32; 165). Although the main body of metamaterial research has focused so far in achieving a negative refractive index, a number of different directions have emerged.

Most notably, metamaterials have enabled experimental investigations of the newly founded field of transformation optics (166; 167), where electromagnetic waves are guided and redirected at will, promising applications as from nanophotonic information processing to exotic topics such as the invisibility cloak. Such effects are made possible by carefully tailoring the permittivity and permeability of the medium surrounding the metamaterial, in order to guide incident radiation around the lattice, rendering it virtually invisible. Experimental demonstrations of cloaking by metamaterial devices have been performed successfully so far in microwave by metal- dielectric metamaterial composites (168) as well as in the visible part of the spectrum by all-dielectric metamaterials (169).

Recently, it was demonstrated that the metamaterial response can be controlled through symmetry breaking in split-rings (see Figure 6.3(a)) by employing coupled resonances, thus introducing the concept of trapped-mode metamaterials, i.e. artificial structures
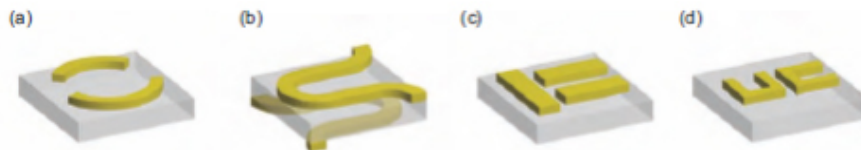
FIGURE 6.3: Unit cells of metamaterials exhibiting EIT-like behaviour:(a) Asymmetrcally split-rings, (b) bi-layered fish-scale, (c) coupled metallic stripes, and (d)coupled split-ring resonators [Reprinted from (32)].

exhibiting narrow-band resonant response resulting from strong interference of its constituents (32; 170). This lead to a first demonstration of a metamaterial analogue of electromagnetically induced transparency (EIT), where a bi-layered metamaterial was rendered transparent by a resonant anti-phase excitation of the two layers (32; 171) (see Figure 6.3(b)). Similar behavior was soon observed for plasmonic metamaterials (32; 172) and experimentally demonstrated in the optical (173) based on the coupling of radiative and dark, sub-radiant elements (see Figure 6.3(c) & Figure 6.3(d)). Finally, EIT-like behaviour was also observed in the THz regime (174) on a scaled-down version of the metamaterial employed in (170), while an omni-directional metamaterial analog of EIT was demonstrated in (175).

Metamaterial analogs of EIT are expected to play a key role in future developments in metamaterial research. In a first instance, low-loss metamaterials based on this concept have been predicted (176). Trapped-mode metamaterials, in particular, can be tailored to exhibit coherent or incoherent behaviour, namely collective or individual response, enabling novel applications and alleviating fabrication restrictions. Coherent metamaterials are especially important in view of the recent advances in the active metamaterials.

6.1.1.1 Switchable metamaterials

The mentioned ability of metamaterials to create electromagnetic responses absent in nature has initiated the new research field of transformation optics (177; 178) which has applications ranging from electromagnetic cloaking (167) to subdiffraction imaging (179). Most notably frequency-agile metamaterials, which allow one to adjust the electromagnetic response in real time, are emerging as an important part of this field.

What is clear is that future nanophotonic applications, in particular photonic data processing circuits, will undoubtedly require active devices of sub-wavelength dimensions (180; 32; 181). Unfortunately, electro-optic modulation of light in a device of nanoscale thickness is not a trivial problem.

In conventional electro-optic modulators exploiting for example the most widely used Pockels effect, the polarization switching involved requires the interference of two propagating modes to develop over distances far in excess of the wavelength of light. The dimensions of such modulators in the propagation direction are often in the centimeter range (182).

Signal modulation via control of the waveguide absorption coefficient or refractive index is another possibility. However, this approach also requires substantial propagation lengths over which an amplitude or phase change accumulates, or it involves resonators and/or interferometric arrangements that are inherently longer than the wavelength of light. The typical dimensions of electro-absorptive quantum well (QW) structures for example GaAs ring resonators are a few micrometers (183). Similar compact (10 -12

μm) structures based on refractive index modulation of silicon electro-optic modulators have also been demonstrated (184; 185).

As it has been mentioned, the resonant characteristics of metamaterial structures are highly sensitive to the local environment. Because of this, a small change in the properties of an active medium adjacent to the metamaterial can translate to a dramatic change in the properties of the combined hybrid structure

As such it has recently been suggested that strong signal modulation may be achieved in truly nanoscale photonic devices, despite very short propagation lengths, through the use of materials that show a substantial change in absorption or refraction in response to a control excitation (180; 181) in conjunction with photonic metamaterials. The relative change in the real and/or imaginary parts of the refractive index must be of the order of unity and this can only be achieved in metals, where phase changes can bring about significant changes in optical properties.

Such functionality has been extensively studied and demonstrated with elemental gallium, which can exist in several phases with radically different optical properties. In this case, phase changes led to the modification of the plasmon and interband absorption to provide a platform for various nanoscale active devices (180; 181; 186). Such demonstrated devices among others consist for example of a high-contrast plasmonic modulating device, where light control by light was achieved by changing the efficiency of light coupling into a plasmon polariton wave (187; 188). Another device that has potential applications in phase change memory and data storage technologies operating at extremely low power levels was demonstrated first by light induced structural phase transitions in a single gallium nanoparticle (189), followed by the demonstration of electron beam induced structural phase transitions of individually addressable gallium nanoparticles (190; 146).

Generally, the hybrid metamaterial approach (191; 192), in which natural materials are integrated into the metamaterial composite, has been particularly successful in enabling frequency-agile metamaterials that respond to the application of voltage (193; 194), external electric field (195), light (161; 196), and heat (197). This tuning ability helps make metamaterial devices more versatile, adapting to shifting input or changing target parameters. However, all these methods for enabling frequency-agile metamaterials require the continuous application of an external stimulus to maintain altered metamaterial properties. Once the external stimulus is removed, the metamaterial returns to its original response.

Essentially, any functionality derived from metamaterials would benefit greatly if the metamaterial tuning persisted once the triggering stimulus disappeared. Metamaterials that are tuned mechanically or geometrically should retain their tuned properties (198; 199; 146), but such techniques are likely to be difficult to implement at higher frequencies or for complex designs.
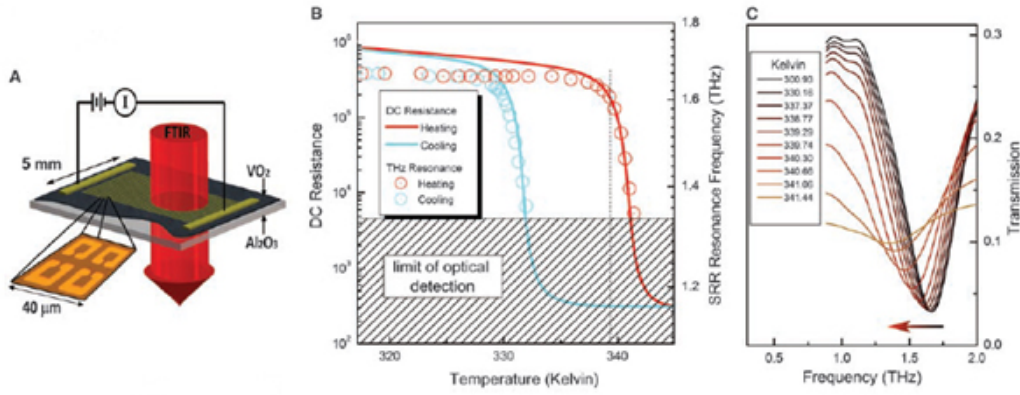
FIGURE 6.4: Memory-oxide hybrid-metamaterial device. (A) The device consists of a gold SRR array that has been lithographically fabricated on a VO$_2$ film. Electrodes are attached allowing in-plane current-voltage relation transport, and the device is mounted to a temperature-control stage. (B) Simultaneous dc-transport and far-infrared probing of the metamaterial demonstrate that as VO$_2$ passes through its insulator to metal transition, resistance drops and the SRR resonance frequency decreases. (C) Spectroscopic data from which the metamaterial resonance frequencies in (B) are identified (heating cycle shown). Data in (B) and (C) were obtained by performing a complete temperature cycle (300 to 350 to 300 K) with temperature stage on which the sample is mounted [Reprinted from (33)].

The persistent frequency tuning of a memory metamaterial device can be illustrated by use of a single-layer gold split-ring resonator (SRR) array patterned (16) on a 90-nm-thin film of vanadium dioxide (VO$_2$) (Figure 6.4). VO$_2$ is a correlated electron material that exhibits a volatile insulator-to-metal (IMT) phase transition that can be thermally (200), electrically (195; 201), or optically (202) controlled.

Driscoll et al (33) demonstrate electrically controlled persistent frequency tuning of a metamaterial, which allows the lasting modification of its response by using a transient stimulus. This work demonstrates a form of volatile memory capacitance (see Figure 6.4).

A non-volatile metamaterial electro-optic device has been demonstrated here at the ORC by Samson et al (34). It exploits the frequency shift of a narrow-band Fano resonance mode in a plasmonic planar metamaterial induced by a phase change in the dielectric properties of an adjacent chalcogenide glass layer. An electrically stimulated transition between amorphous and crystalline forms of the glass brings about a 150 nm shift in the near-infrared resonance providing transmission modulation with a contrast ratio of 4:1 in a device of subwavelength thickness.

Transmission switching was demonstrated by applying pulses of incrementally increasing voltage between the patterned gold layer and an electrode brought into contact with the top surface of the GaLaS (38) (see Figure 6.5). This method was further refined in this project.
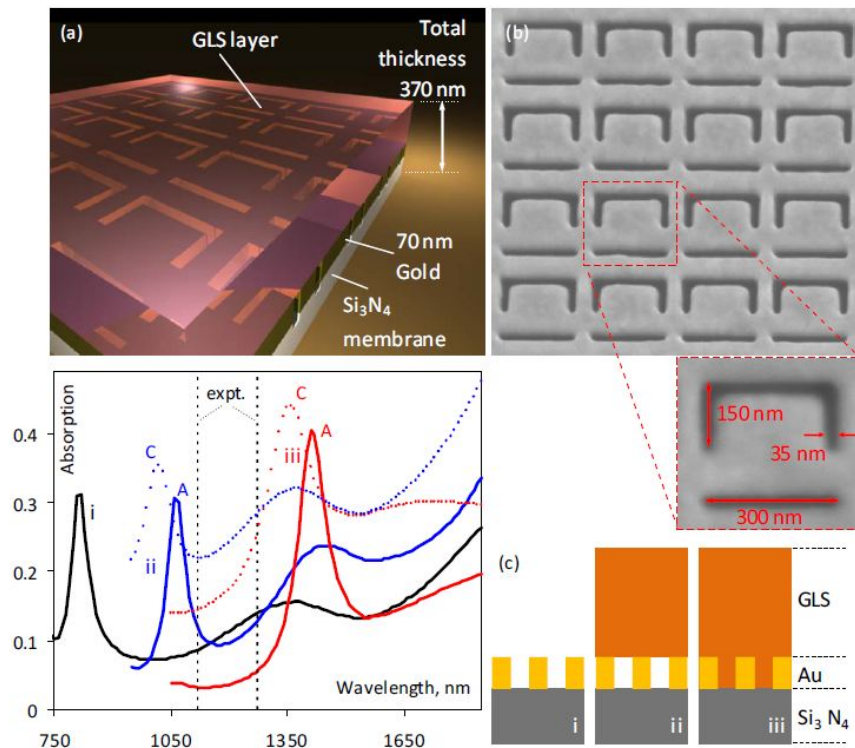
FIGURE 6.5: GaLaS hybrid metamaterial [Reprinted from (34)].

It should be noted that as an alternative to switching the dielectric medium in contact with the metamaterial attempts have been made to adjust the distance between several planar metamaterial layers in which efficient transmission change was achieved but the tuning originated from a change in the layer structure rather than a change in metamaterial molecule (203). Recently, another interesting work demonstrated the modification (204) of the optical properties of a metamaterial by reorienting the metamaterial molecules (35) (see Figure 6.6). This has given rise to the concept and design
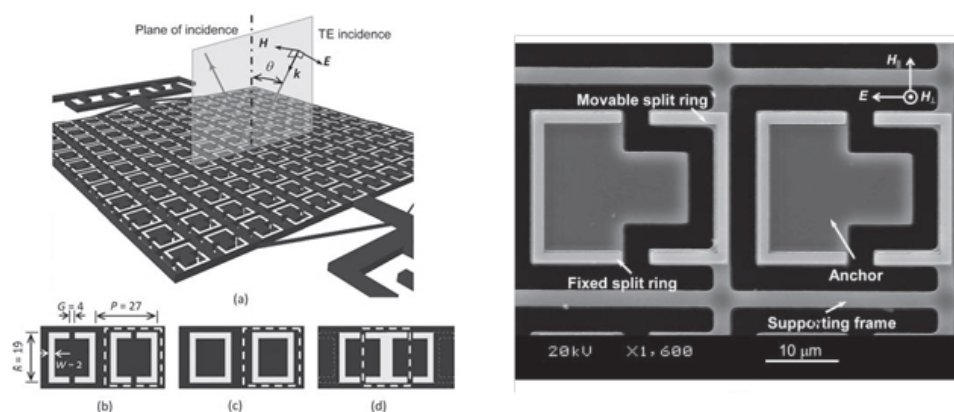
FIGURE 6.6: Switchable metamaterial achieved through creating movable split rings as a way of modifying the resonant response of the metamaterial, achieved using micromachining techniques [Reprinted from (35)].

of switchable magnetic metamaterials by directly reshaping the metamaterial molecules using micromachining technology and present working devices with switchable magnetic responses. The schematic diagram of the switchable magnetic metamaterial is shown in Figure 6.6(a). Each metamaterial molecule consists of two semi-square split rings. One is anchored on the substrate while the other can be moved by micromachined actuators. As a result, the gap between the split rings can be altered and thus the geometric shape of the metamaterial molecule can be changed, altering its resonant response.

The incidence exemplifies the transverse electric (TE) state, i.e., the E field is perpendicular to the plane of incidence. Figure 6.6(b) Each metamaterial molecule consists of two semi-square split rings separated by a gap. One is movable and the other is fixed. In the open-ring state, the metamaterial molecule is in the "[ ]" shape. The metamaterial molecule can be changed to Figure 6.6(c) the closed-ring state with the shape "[]" and Figure 6.6(d) the back-touch state with the shape "I" by simply translating all the movable semi-square split rings at the same time.

This method is fascinating in its design, however does not present a non-volatile method of switching metamaterial responses and the difficulty of the fabrication process needed to realise such complex structures suited for lower wavelength operation make it a less than suitable candidate for photonic metamaterial switching.

However when it comes to practical phase change functionality, the obvious switchable dielectric candidates for the realization of the nanophotonic optical switch concept are the chalcogenide glasses found in the heart of today's re-writable optical disc technologies and non-volatile electronic memories.

The research areas explored in this project is using chalcogenide thin films and through incorporating them with metamaterial arrays. Metamaterials are artificial man-made materials which have been engineered to have properties that may not be found in nature. They gain their properties from structure and geometrical inhomogeneity in order to create effective macroscopic behaviour.
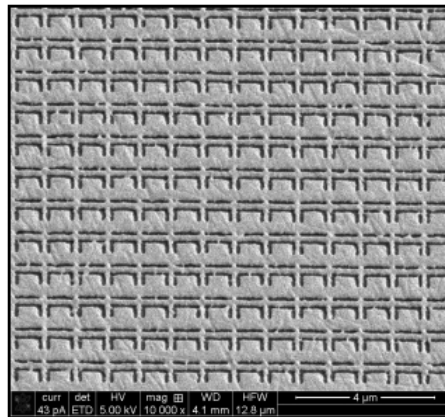
FIGURE 6.7: A photonic metamaterial array designed for use with chalcogenide alloy GeSbTe.

The research in the area of metamaterials is vast and involves many different structures and applications. Within this project we incorporate phase change thin films with what are known as photonic metamaterials (Figure 6.7); an artificially fabricated, sub-wavelength, periodic structure, designed to interact with optical frequencies (mid-infrared). The sub-wavelength period distinguishes the photonic metamaterial from photonic band gap structures (see section 6.3).

6.1.2 Optical phase change devices

Optical phase change of chalcogenide thin films has been an area of intense research for the past 3 decades bringing about great commercial success with the production of CDs, DVDs and Bluray discs. At the centre of these technologies is the inherent change in the optical properties of these thin films in the amorphous and crystalline states. This reversible non-volatile change seems very well suited to the field of nanophotonic transformation optics. Using the optical phase change of chalcogenide glasses as the switchable dielectric medium in contact with the metamaterial molecules can allow the drastic and controlled change of the resonant response of the metamaterial in a reversible manner. As this project utilises this method of phase change, one needs to take into account the incredible wealth of knowledge available on optical phase change of chalcogenides.

By studying the structure of phase change optical discs which can be seen in Figure 6.8 a great deal of knowledge can be obtained. The phase change layer is typically sandwiched between two dielectric layers which protect the film and this is capped with a reflective layer for optical phase change recording and the whole structure is deposited on a polycarbonate disk. This is improved upon by also incorporating two interface layers which promote the nucleation rate as well as prevent the possible sulphur diffusion
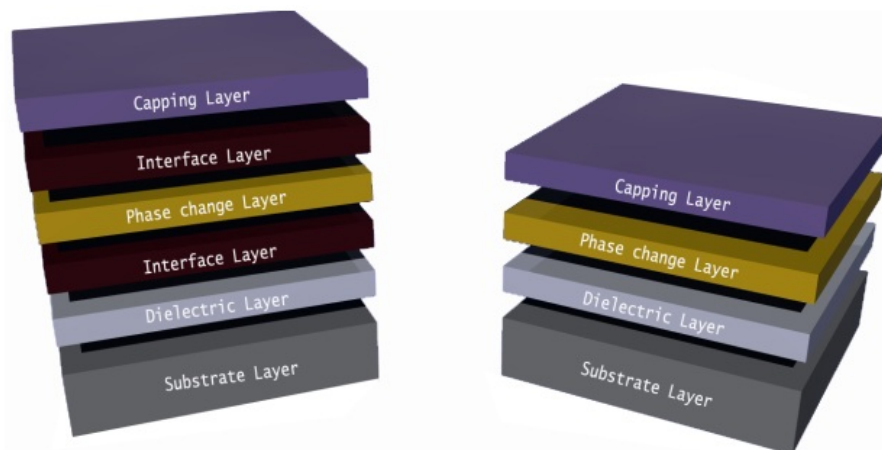
FIGURE 6.8: Schematic of the layer stack used in a conventional optical disk. The difference between the 4 and 6 layer stack are the introduction of the interface layers in the 6 layer disks which aim to aid crystallisation and prevent layer diffusion.

into the phase-change film from the sulphur containing dielectric layers. It should be noted that the above motioned methods to improve the nucleation rate are based on the growth-driven (GeSbTe) materials and may not be compatible for the nucleation-driven (doped SbTe) materials.

The principle of phase-change optical storage is based on the concept that some physical property of a microscopic area of the recording layer on the disc surface is altered due to crystallographic structure changes when the films are irradiated by laser pulses. The reproduction of the recorded information takes advantage of the difference in reflectivity due to the difference in refractive index and extinction coefficient between the two phases. Although there are two possible types of phase change (one is between amorphous and crystalline phases and another is between two different crystalline phases) the one applied in rewritable phase-change optical discs is only the first type. Before recording data on the phase-change optical discs, the as-deposited writing process, the crystaline state is achieved by heating the phase-change thin films with sufficient laser power above its melting point and then rapidly quenching it to room temperature. Because the atoms of the phase-change material after melting are in a disordered state and the cooling rate of the area irradiated by laser pulses is very high, the time is not sufficient for the atoms to be arranged into the ordered crystalline structure. Thus amorphous marks are formed. The absolute minimum quenching rates required for amorphization are different for various materials, ranging from 10^6 to 10^{11} K/s.

In the erasing process as shown in Figure 6.9, the crystalline phase is realized by annealing the phase-change films at the temperature between the crystallization temperature Tc and the melting point Tm with a medium power laser irradiation. During the irradiation period, the atoms of the phase-change media are rearranged into an ordered structure; thus the amorphous region can be changed to the crystalline state. The phase
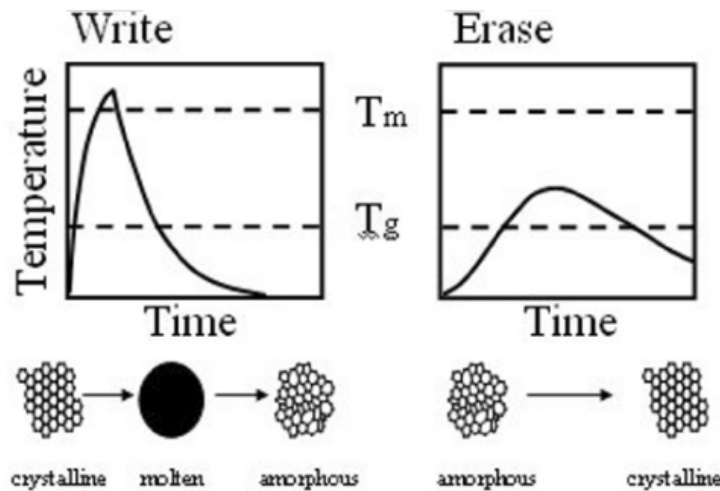
FIGURE 6.9: Schematic of the temperature time profiles associated with formation of amorphous dots (left panel) and crystallisation on (right panel) of amorphous marks in a crystaline layer [Reprinted from (17)].
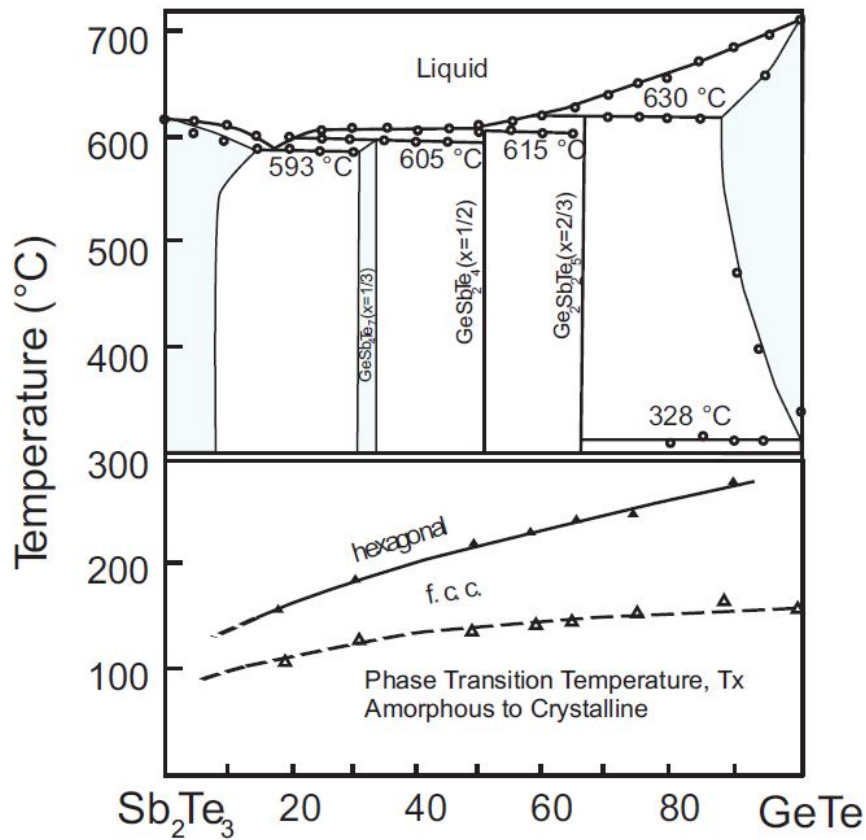
FIGURE 6.10: Phase diagram for pseudo binary system Sb_2Te_3 -GeTe [Reprinted from (13)].

changes in the phase-change optical discs are accomplished by using the irradiation of laser light which typically has a diameter on the order of 1 μm. When a laser beam having a 1 μm diameter moves on the recording thin films at a linear velocity of 10 m/s, the irradiation time of a point on the film is only 100 ns. Hence, the available time for the energy deposition is also within this irradiation time duration.

In this work, $Ge_2Sb_2Te_5$ has been utilised as an optical phase change dielectric. The crystallisation of $Ge_2Sb_2Te_5$ is a nucleation driven process as the optical power has been found to be constant for Complete Erase Time (CET) of different diameter amorphous marks. This behaviour is indicative of a nucleation dominant process. As further proof, inspection of the crystallised marks with a TEM also revealed that as the crystallising pulse power was increased the number of crystallites present increased and, at the threshold power for complete erasure, the mark was found to be filled with non-crystalline grains with sizes ranging from 10nm to 30nm, indicating that the nucleation occurs before growth from the surrounding crystalline background (87).

The CET of $Ge_2Sb_2Te_5$ decreases with increasing film thickness, this is understood to be a result of competing interface and bulk effects. Below a threshold thickness the film crystallisation characteristics are dominated by interface effects. As the film

is made thicker, the CET becomes less sensitive to these effects and bulk nucleation is predominantly the influencing factor. Consequently, below a critical thickness the interface material, surface energy and roughness all influence the nucleation rate of $Ge_2Sb_2Te_5$ (87).

Having discussed the logistics of optical phase change in chalcogenide thin films with a focus on GeSbTe as the material of choice in this instance, it becomes clear that when one considers that amorphous-crystalline phase transitions in chalcogenides may bring about a relative index change of 0.1 on nanosecond timescales, the great potential held by chalcogenides in the plasmonic domain becomes clear.

6.2   Motivation

Nanophotonic applications, in particular, photonic data processing circuits, require active devices of subwavelength dimensions. However, modulation of light in a device of nanoscale thickness is not a trivial problem. In conventional modulators exploiting the Pockels or Kerr effects, the polarization switching involved requires the interference of two propagating modes to develop over distances far in excess of the wavelength of light. The dimensions of such modulators in the propagation direction are often in the centimeter range. Signal modulation via control of the waveguide absorption coefficient or refractive index is another possibility.

However, this approach also requires substantial propagation lengths over which an amplitude or phase change accumulates, or it involves interferometric arrangements that are inherently longer than the wavelength of light. It has been suggested that strong signal modulation may be achieved in nanophotonic devices, namely photonic metamaterial nanostructures, despite very short propagation lengths.

Nanoscale electro-optic and all optical modulation that relies not on absorption modulation, but rather on a change in the refraction of a material associated with a control-input-induced phase change is pursued here. In a layer of nanoscale thickness, such a refractive index change would be insufficient to noticeably modulate the intensity or phase of a transmitted wave. However, it is widely recognized that by combining a nanoscale layer of phase change material with a planar plasmonic metamaterial (see Figure 6.11) one can exploit the fact that the position of narrow resonant absorption lines in certain metamaterials are strongly dependent on the dielectric environment. Switching the dielectric layer in contact with such a metamaterial produces a massive change in its resonance frequency. Importantly, given that the planar metamaterial also has a sub-wavelength thickness; the whole electro-optic modulating structure can be much thinner than the light wavelength. Moreover, the resonance frequency, and therefore the spectral band of high contrast switching, can be engineered by design and located anywhere within the entire transparency range of the dielectric phase change medium.

The primary objective of this work was to achieve proof-of-principle demonstrations of novel devices providing reversible nanophotonic switching functionality based on optically and electrically-addressed chalcogenide phase-change materials. In reaching this goal, significant achievements have included:

- The first demonstration of electrically-induced wide area ($> 50 \ \mu m^2$) phase-change switching in a gallium lanthanum glass (to our knowledge, the first demonstration of such switching in any phase-change memory material) via planar multi-terminal micro-ribbon heaters (an essential development for electro-optic metamaterial applications);

- The first demonstration of reversible, non-volatile, all-optical switching in a hybrid chalcogenide glass metamaterial structure: Using germanium antimony telluride (GeSbTe) glass and gold plasmonic nanostructures (metamaterial array) of sub-wavelength thickness, reversible switching in the 1-2 μm (Near infra-red) and 4-5 μm (Mid Infra-red) spectral range with modulation contrast exceeding 4:1 has been achieved at an optical excitation levels below 0.25 mW/μm^2;

- The development of high-throughput physical vapour deposition and analysis techniques for chalcogenide media and metamaterial hybrids have provided considerable insight into device fabrication/optimization and electrical/optical phase switching for the new chalcogenide system.

- The knowledge and expertise derived from these achievements set a strong foundation for the continuation and expansion of research work in the field of chalcogenide photonics, where directions may include the development of optically and electro-optically multi-element devices with parallel control (e.g. spatial light modulators for phase and intensity control) and photonic cognitive and data processing systems.

The following will set out the account of achieving these goals.

6.3 Metamaterial design

The selection of appropriate metamaterial geometries is crucially important to applications in photonic switching. The experiments in this chapter employ a planar structure belonging to a class of metamaterials that supports trapped mode plasmonic excitations (205; 206; 207). These structures support narrow reflection, transmission, and absorption resonances with asymmetric, Fano-type dispersion. In such metamaterials, weak coupling of the excitation mode to free-space radiation modes creates exceptionally narrow reflection, transmission and absorption resonances with asymmetric, Fano-like dispersion (208; 209). For example, finite element numerical modeling illustrates how
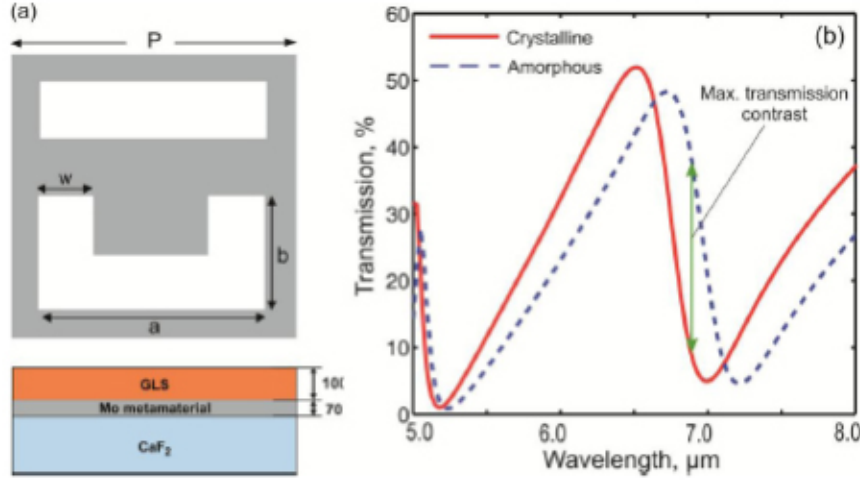
FIGURE 6.11: Numerical modelling of ASR metamaterials hybridized with chalcogenide phase-change media. (a) Plan view of ASR unit cell geometry and cross-section of hybridized device structure; (b) Optical transmission spectrum for the structure in (a) [P=4, a=3.2, b=1.6, w=0.8 μm] with GaLaS in its crystalline and amorpous phases.

the presence of an asymmetry in a split ring resonator provides narrow resonances, compared to the broad dipole resonance of a symmetrically split ring resonator. The earliest example of such a metamaterial displaying the so-called trapped mode resonance was a periodic array of metallic wire asymmetrically split ring (ASR) resonators that has found numerous applications where sharp spectral features are required (210; 207; 33; 211). It has also very recently been shown both theoretically and experimentally that the strong interactions between the magnetic moments of the oscillating trapped mode currents in an array of ASR resonators are able to create a light emission with high spatial coherence fueled by plasmonic current oscillations, coined as the lasing spaser (147; 212). Here, a complementary structure to the wire ASR metamaterial is used, a periodic array of ASR slits in a metal film.

In the present work we target resonances and associated optical switching functionality in the infrared spectral domain, this presents significant application opportunities (e.g. compact nanoscale electro-optic signal switching by other means is very challenging at IR wavelengths). This spectral range is also advantageous because dimensional constraints on metamaterial designs allow for device fabrication by photolithography as well as the more expensive and time-consuming processes such as ion beam milling and electron-beam lithography. Samples are thus more amenable to high-throughput processing and scaling to large-area and/or large volume production.

The family of ASR designs with IR resonances, have been developed through three-dimensional finite element numerical modelling (taking into account substrate, functional chalcogenide and buffer layers where relevant - Figure 6.11), previous to fabrication. Phase switching in the thin film chalcogenide component of these hybrid structures will bring about substantial shifts in the spectral positions of optical resonances, thereby modulating transmitted and reflected signals (as indicated in Figure 6.11).

6.4 Modelling

6.4.1 Large area crystallisation microribbons

As described previously two methods of switching the chalcogenide layer between its two structural phases has been demonstrated:

- Sandwiching the chalcogenide between two electrodes.

- Placing a probe on top of the chalcogenide layer with a bottom electrode having been deposited previously.

The first option is not suitable as the top electrode prevents us characterising the optical interaction of the metamaterial with the phase change layer during or after switching. The second option can be used, however placing the probe on top of the layer more often than not, will damage the surface and quality of the device or penetrate through the chalcogenide layer damaging the device completely.

As a result, using an electrothermal heater underneath the layer has been the approach used, as it presents a suitable option in achieving large area crystallisation without contacting the top surface and as such ruining the quality of the device or jeopardising the subsequent optical characterisation of the device.

A number of structures have been considered for this purpose and multiphysics modelling was carried out to determine their suitability in achieving the temperatures needed for the phase change of GaLaS. The two structures shown below were picked as:

- Due to their efficiency in achieving the required temperatures.

- Their ability to have the metamaterial array incorporated within the structures.

- Their versatility in both being used for metamaterial and also plasmonic applications.
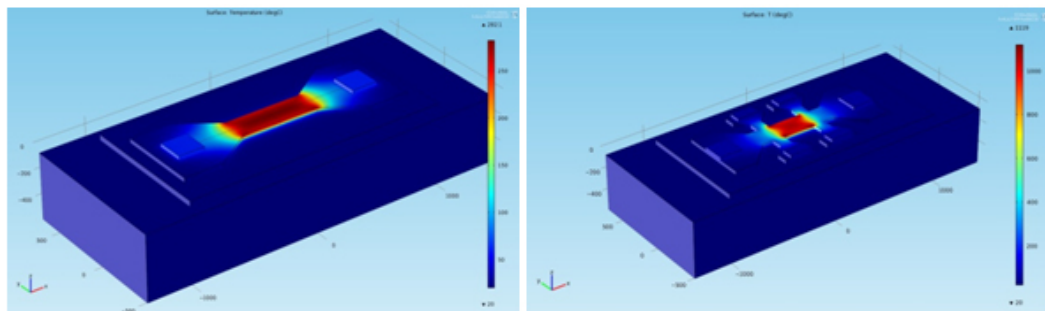
FIGURE 6.12: Initial micro-ribbons large area crystallisation structures multiphysics simulation.

The modelling carried out showed (Chapter 4) the ability of these structures to achieve the crystallisation temperature of GaLaS thin films, shown in Figure 6.12

6.4.2   Hybrid metamaterial device

As the structures shown previously (Figure 6.12) were eventually going to be patterned with a metamaterial array, this in itself would change the physics of Joule heating within the structures. As such, the addition of the array was modelled to observe the difference in the heating dynamics (see Figure 6.13).

The heating data is taken across the device in both the x and y direction to see the distribution across the metamaterial array and how this will affect the phase change chalcogenide layer on top of the sample.

6.4.3   Metamaterial integration modelling

As described previously the microribbon large area crystallisation cells were eventually going to be integrated with metamaterial arrays. To anticipate the change in thermal dynamics of the resulting structures some multiphysics modelling was carried out, with the results shown in Figure 6.14. For comparison, when simulating the same structure
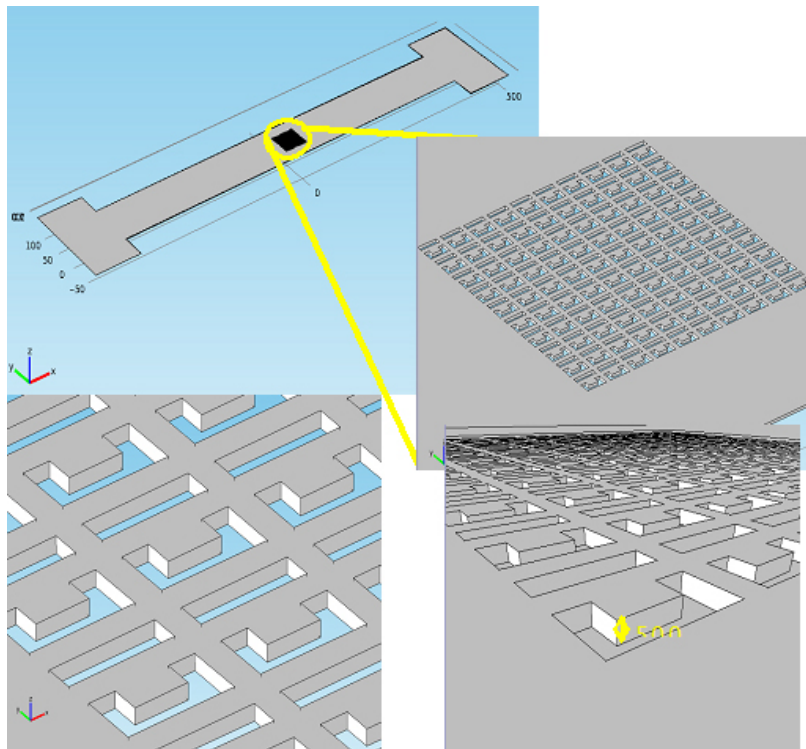
FIGURE 6.13: Models of metamaterial array integration into microribbon heater structure.
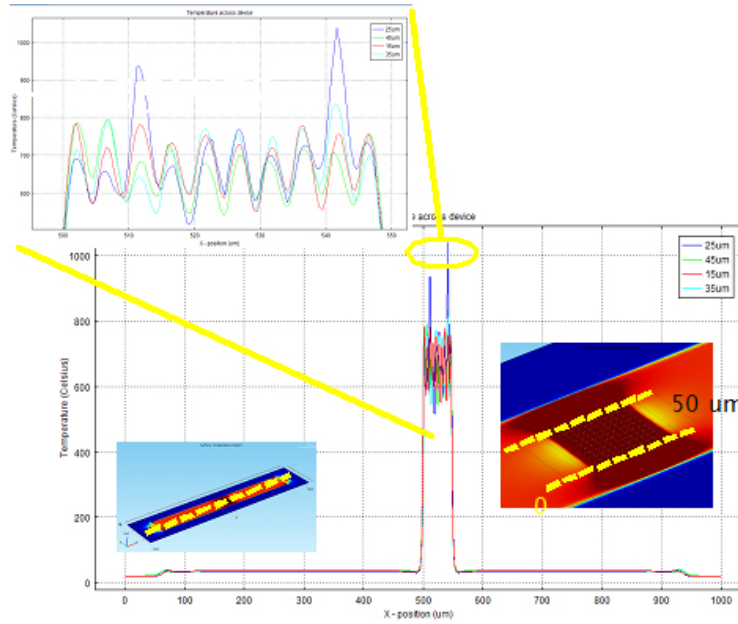
FIGURE 6.14: Diagramatical representation and results of the electrothermal modeling of the integration of the metamaterial array with the microribbon structures.
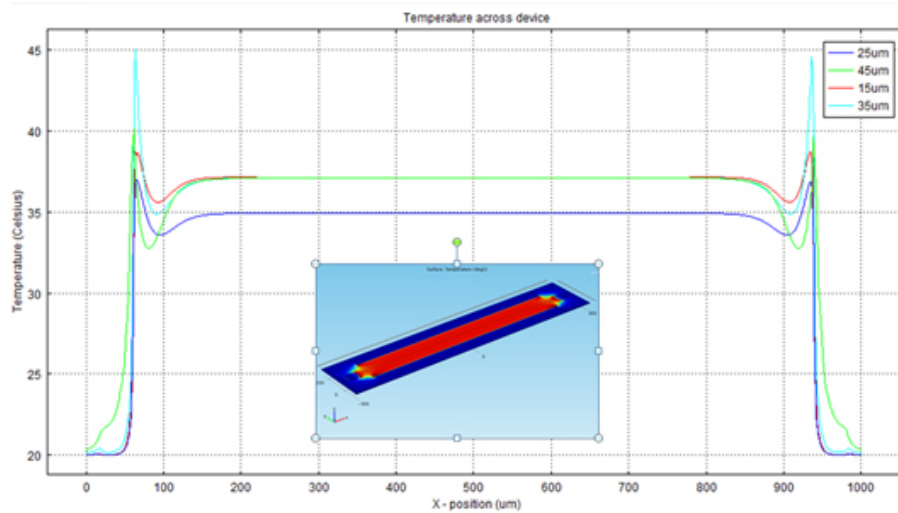
FIGURE 6.15: Diagramatical representation and results of the electrothermal modelling of the integration of the metamaterial array with the microribbon structures.

without the metamaterial array integrated within it, the results shown in Figure 6.15 are observed.

From the modelling results it can be predicted that due to the smaller spacing which the metamaterial array introduces in the path of the electric sweep a higher resistance is encountered by the electricity thus making the temperature increase much more rapidly, yielding the desired temperature at much lower voltages compared to a structure without the array integration. Furthermore, the area directly on top of the metamaterial array will be a hot spot, thus making the eventual crystallisation much more focused, giving a higher degree of control over the crystallised area.
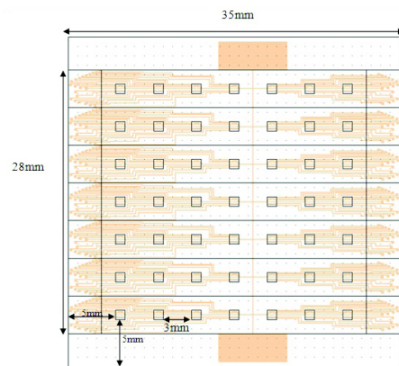
FIGURE 6.16: CAD image of electronic high throughput chip.

6.5 Fabrication

6.5.1 High throughput mask

The hybrid chalcogenide-metamaterial structures have also been integrated into a mask which will give us the ability to look at a high throughput method of identifying the best compositions of phase change alloys for a metamaterial electro-optic and all optical switch.
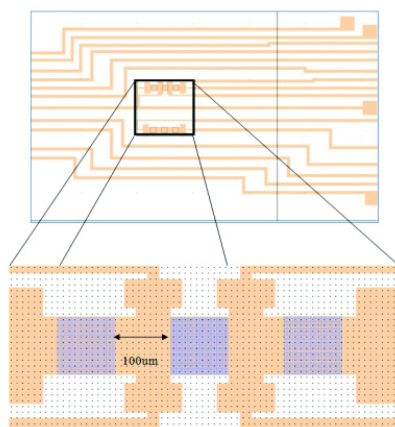
FIGURE 6.17: Individual window of the high throughput chalcogenide-metamaterial electrical switching chip.

An array of the structures shown previously is incorporated into a 35x35mm chip which will then be deposited with a chalcogenide phase change layer with finely controlled composition gradient in the x or y direction as well as a thickness gradient in this direction. The pads on the perimeter of the chip are used for electrical switching and contact of each device in the windows (see Figure 6.16).

Each structure is incorporated with three metamaterial arrays and each window of the device will represent a different composition or thickness and thus a high number of
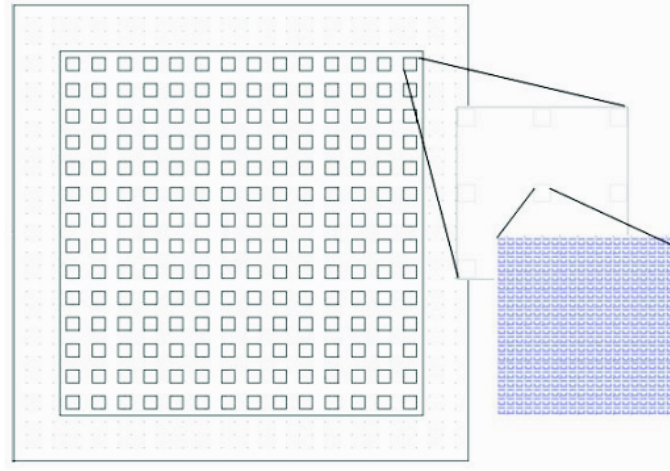
FIGURE 6.18: Individual window of the high throughput chalcogenide-metamaterial optical switching chip.

different devices can be investigated within one high throughput chip. (see Figure 6.17).

This mask is also advantageous as it removes the need to directly contact each structure to induce crystallisation. The pre-routed wires and pads on the perimeter of the chip will serve as the ports for crystallisation removing the damage caused by both the pressure placed on the structures from the probes and also static from the probe tip on the surface of the microribbons.

These high throughput chips were also developed with an alternative design for optical switching without the electrical pads on the perimeter as shown in Figure 6.18.

6.5.1.1 Fabrication processes

6.5.1.1.1 High throughput chip fabrication The optimised structures used for large area crystallisation which were modelled previously were fabricated using photolithography to pattern the substrate. Here a series of fabrication steps (photolithography, sputtering, e-beam, liftoff, PVD) were followed. This was carried out using S1805 positive photoresist. After exposure and development the structures shown in Figure 6.19 were created.

RF sputtering was subsequently used to deposit a 300nm layer of molybdenum for bottom electrode/heater for the devices. The lift-off method was used to take away the unwanted molybdenum (see Figure 6.20).

The remaining molybdenum was the well defined structure shown in Figure 6.21.

A 100nm layer of GaLaS was deposited on top of these structures using RF sputtering.
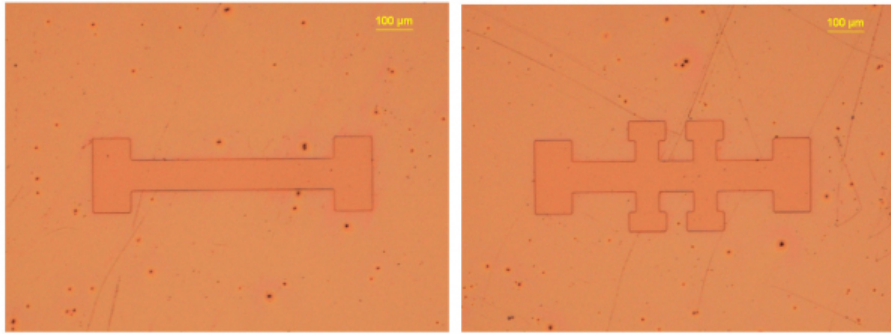
FIGURE 6.19: Testing of photolithography steps to realise microribbon structures, showing photoresist patterned silicon substrate.
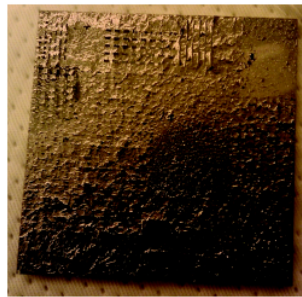
FIGURE 6.20: Molybdenum film during the lift-off process.
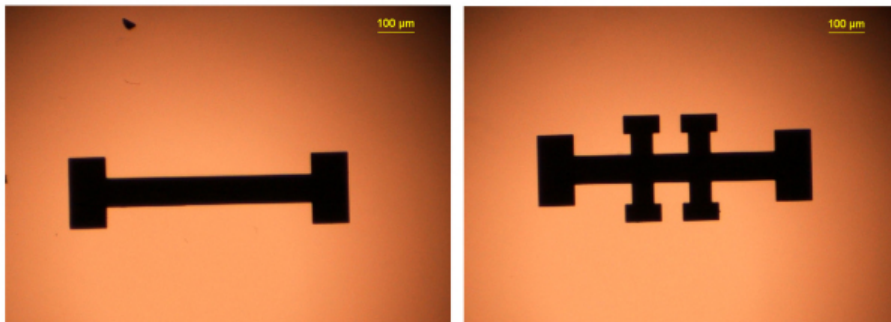
FIGURE 6.21:   Transmission optical microscopy of realised molybdenum structures post-liftoff.

A final photolithography step is needed to define the empty areas on top of the pads. Once this has been defined a final etch step is carried out to breach through the top GaLaS layer. This was carried out using reactive ion etching. The resulting final device is shown schematically in Figure 6.22.

A second set of devices was also fabricated which was the reverse of the previous device described here. In this alternative setup, first a 70nm layer of GaLaS was deposited using RF sputtering on a calcium fluoride substrate and this was followed by a photolithography step where the patterns of the electrodes was defined as before (Figure 6.9) and this was followed by a 300nm deposition of molybdenum and lift off to produce a device which is the reverse of the previous devices fabricated (Figure 6.22). These latter devices were fabricated as the utilisation of CaF as the substrate allows the observation
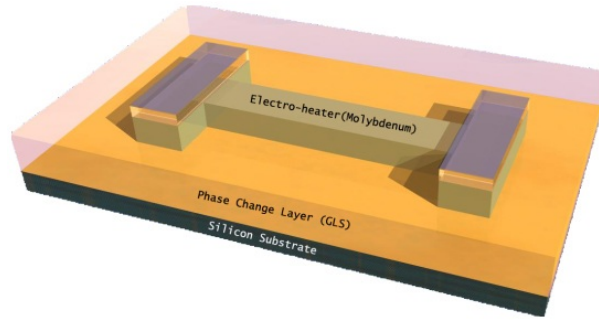
FIGURE 6.22: Representation of the different layers of the first set of devices fabricated.

of both reflection and transmission across the device after switching has occurred giving more information about the nature of the change which can be induced electrically or optically (Represented in Figure 6.23).

The work carried out here resulted in the fabrication of the high throughput chalcogenide metamaterial chip (shown in Figure 6.24). This included the integration of metamaterial arrays in the heater structures in the electro-optic chip. A fully optical chip (Figure 6.25) is also fabricated with metamaterial arrays across the chip which will have a compositionally variant chalcogenide deposited on afterwards using the high throughput physical vapour deposition technique.

As part of this work large area optical switching was also pursued, for this purpose a series of devices were made to allow optical switching and optimisation of conditions for the eventual integration with metamaterial arrays (Figure 6.26).
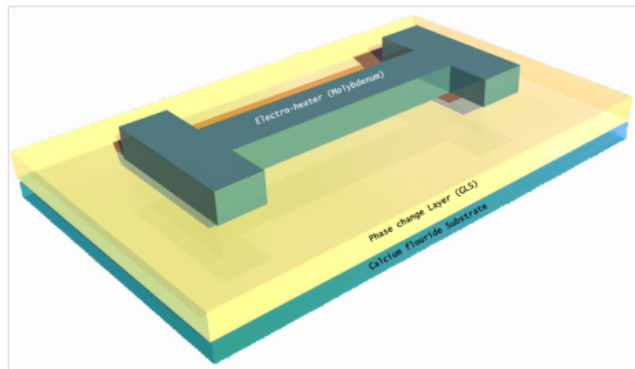
FIGURE 6.23: Representation of the second generation of structures fabricated with CaF substrate.
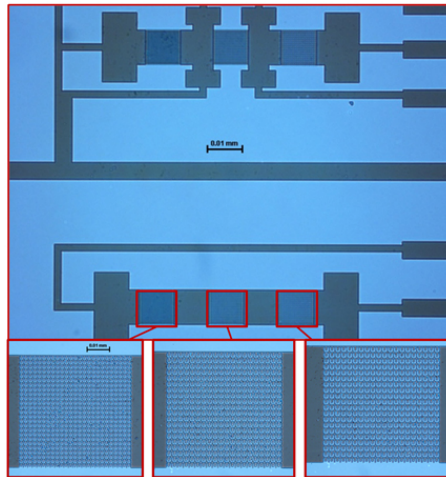
FIGURE 6.24: High throughput metamaterial electrical chip.

6.5.2 GeSbTe metamaterial optical switches

6.5.2.1 Design

The great advantage of using metamaterials in an optical switch of this nature is that they allow the tuning of the wavelength of operation to whichever wavelength is needed for the device that the switches will be used in. As such this presents an unprecedented way of realising nanoscale versatile integrated photonic circuits which are not wavelength specific in their operation but can be tuned to the part of the electromagnetic spectrum which is needed in a specific application.

As discussed previously, in this first demonstration of such a family of devices, the objective spectral ranges for the optical switches were chosen to be the near and mid infrared, due to their significance in telecommunication and other commercial application. As such two types of cells were utilised (Figure 6.29). The advantage of using
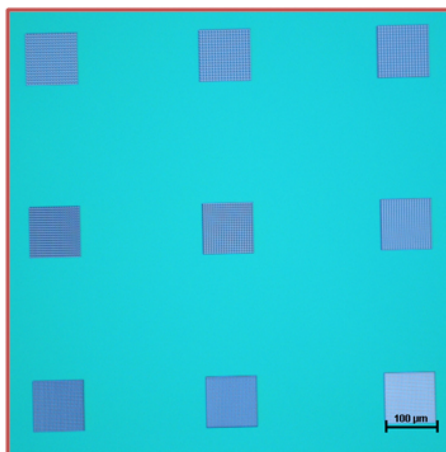
FIGURE 6.25: High throughput metamaterial optical chip.
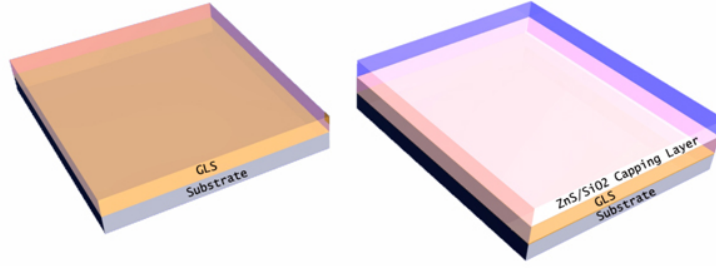
FIGURE 6.26: Optical switching Samples - with and without a capping layer.

such a metamaterial design is that it has specific responses in the x and y polarisation of light. Thus two operational modes can be utilised depending on the polarisation of the incident light.

6.5.2.2 Fabrication process (FIB and sputtering)

Figure 6.27 is an illustrative chart of progress made in scaling artificial magnetism, negative refraction and other novel phenomenon such as sub-diffraction imaging to optical frequencies. Ring resonator designs first demonstrated at microwave frequencies have been successfully scaled to mid-infrared (IR) frequencies using standard microfabrication and machining techniques, however; further scaling requires a different approach as the cell sizes need to be scaled beyond the diffraction limit.

Among the first distinguished designs with near-IR resonant magnetic activity was demonstrated using a wire sandwich structure, in which a dielectric layer is sandwiched
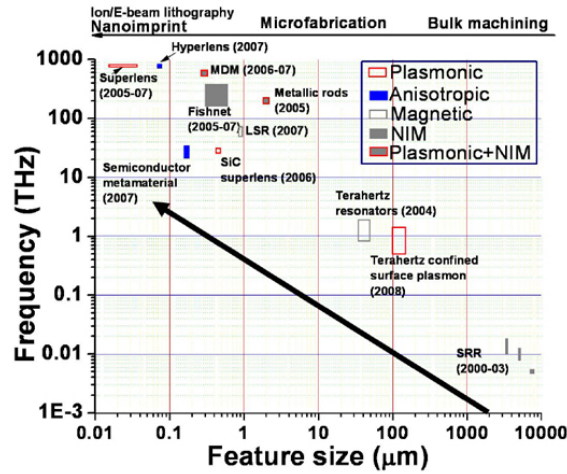
FIGURE 6.27: Progress made in scaling metamaterials from microwave to optical frequencies. Feature size denotes lattice or unit cell size as appropriate. Suitable fabrication tools corresponding to feature size are listed at the top. Note: LSR is L-shaped resonator,14 MDM is metal-dielectric-metal, 17, 18 SRR is split-ring resonator 4, 7, 8 and NIM stands for negative index materials. [Reprinted from (36)]
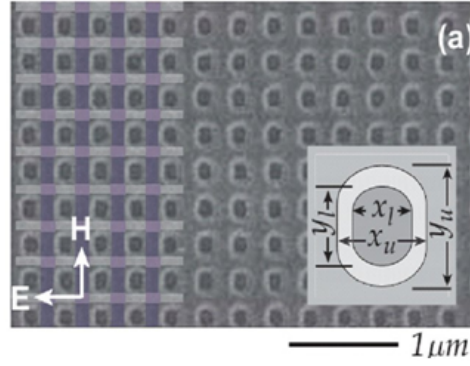
FIGURE 6.28: Metamaterial developed by Vladimir Shalaev and collegues at Purdue University. The holes are about 120 nm across and are separated by about 300 nm (37).

between two metal films. The magnetic response in this sandwich configuration originates from the antiparallel current supported by the wire pair. when combined with long metal wires, this structure, popularly known as a "fishnet", was shown to have negative refraction for a particular polarization at telecommunication wavelengths (1550nm). This demonstration involves the use of focused ion beam milling to realise the nanoscale patterns seen in Figure 6.28.

Development of metamaterials operating at telecommunication wavelengths is of significant practical interest as it can lead to novel optical components such as lenses, beam-splitters and optical modulators for fiber-optic communication industry as well as photonic integrated circuits for optical information storage and processing.

As seen in Figure 6.29, due to the restrictions in cell sizes and the goal to demonstrate operation at telecommunication wavelengths, the metamaterial structures were fabricated by focused ion beam milling through a 50 nm thick gold film evaporated on a calcium fluoride polished substrate. A gold film surface roughness of 2-3 nm was
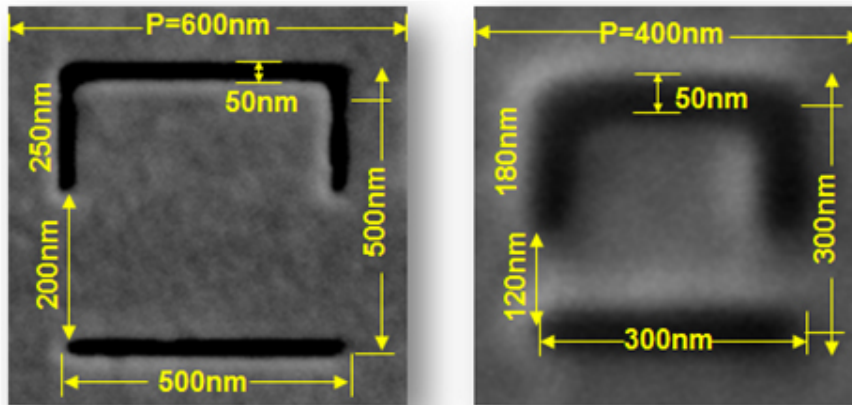
FIGURE 6.29: Scanning electron microscope of fabricated metamaterial cell designs.
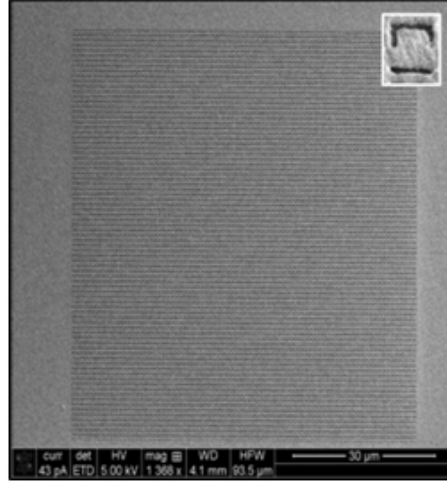
FIGURE 6.30: Scanning electron microscopy image of a 50×50 μm^2 metamaterial array.

generally obtained using low pressure 10^{-8} mbar thermal evaporation. 50x50 μm^2 metamaterial arrays with a square unit cell size of 400 and 600 nm were manufactured on the gold-coated membrane(see Figure 6.30). A ZnS/SiO$_2$ buffer layer is deposited on the patterned gold film. This is followed by a GeSbTe sputtered film of various thicknesses in the amorphous phase. This was sputtered under a 3 mTorr argon atmosphere onto the ZnS/SiO$_2$ buffer layer from a target of Ge$_2$:Sb$_2$:Te$_5$. This is followed by a final ZnS/SiO$_2$ or SiO$_2$ capping layer without breaking chamber vacuum in the sputtering system after the GeSbTe deposition (Figure 6.31).

On a standard chip fabricated through this process, between 6 - 10 arrays of metamaterials are fabricated. Scanning electron micrographs of a typical mid-IR and near-IR
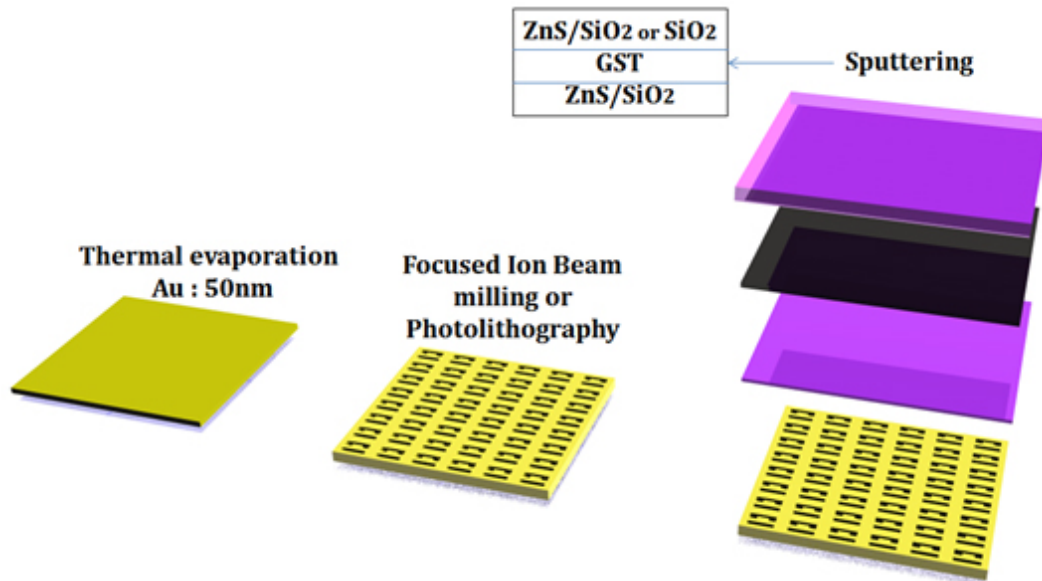
FIGURE 6.31: Process flow diagrams for the fabrication of phase change all optical metamaterial switch.
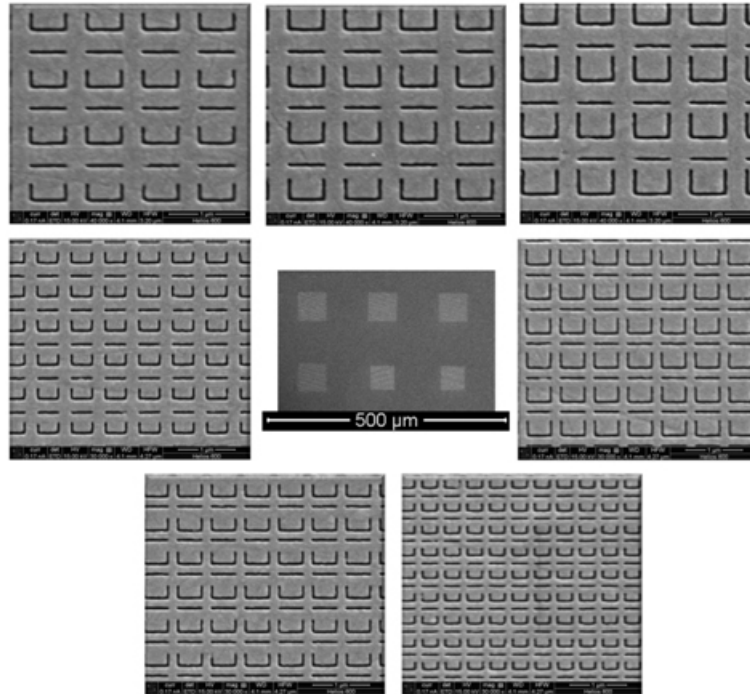
FIGURE 6.32: Mid infrared metamaterial fabricated on a 50 nm gold film.

chip is shown in Figure 6.32 & Figure 6.33.
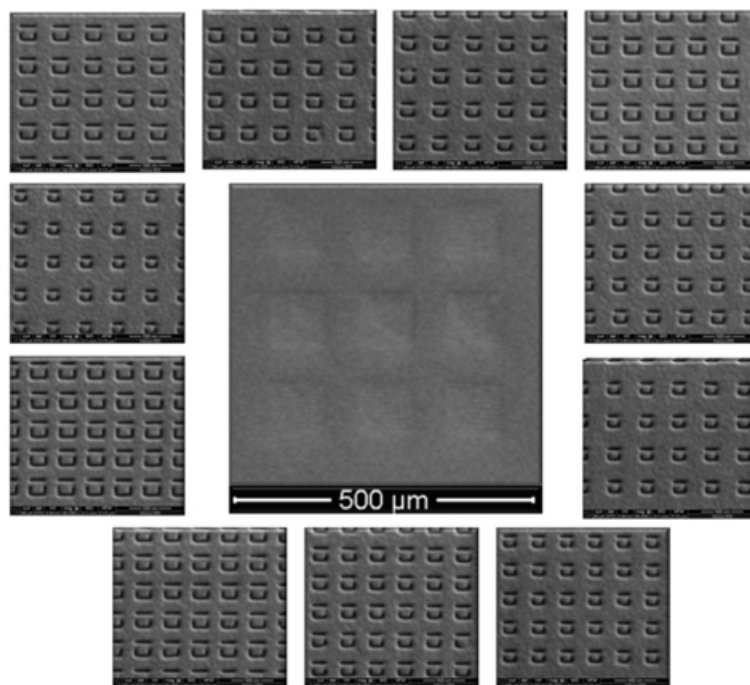
FIGURE 6.33: Near infrared metamaterial fabricated on 50 nm gold film.

6.5.2.3 Structural optimisation

With the capability to optically switch large areas of chalcogenide thin films (see above), we have demonstrated hybrid plasmonic metamaterial devices for all-optical switching in the near- and mid-infrared ranges using germanium antimony telluride (GeSbTe) glasses. These structures comprise (Figure 6.34):

- A substrate (CaF for mid-IR applications, fused quartz for near-IR);

- A metamaterial layer (an evaporated gold film with a typical thickness of 50 nm, patterned by photolithography with 50 μm x 50 μm spare arrays of asymmetric split rings);

- A functional thin film of GeSbTe sputtered under an argon atmosphere to a thickness of 15-40 nm;

- An inert buffer layer of SiO_2 or ZnS/SiO_2 between the metamaterial and chalcogenide to prevent diffusion of metal into the chalcogenide;

- A capping layer, again of SiO_2 or ZnS/SiO_2, on top of the GeSbTe to ensure that the chalcogenide does not deteriorate or react with air (especially at elevated phase transition temperatures). [Samples remain under vacuum throughout the process of buffer, chalcogenide and capping layer deposition].

It should be noted that the choice of polished calcium fluoride as the substrates was made due to the very high transmission of CaF (Figure 6.35) and as such its suitability in trying to minimise the effect of the substrate on the transmission performance of the final devices.
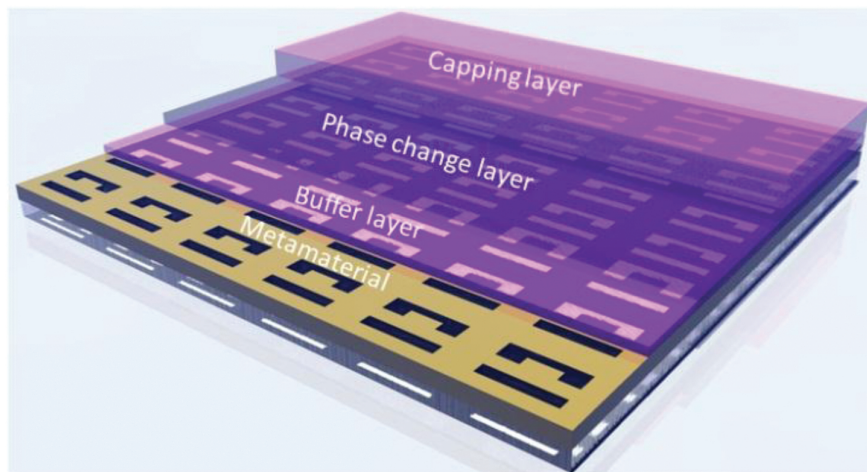
FIGURE 6.34: Layer structure of chalcogenide metamaterial switching device (artistic impression).
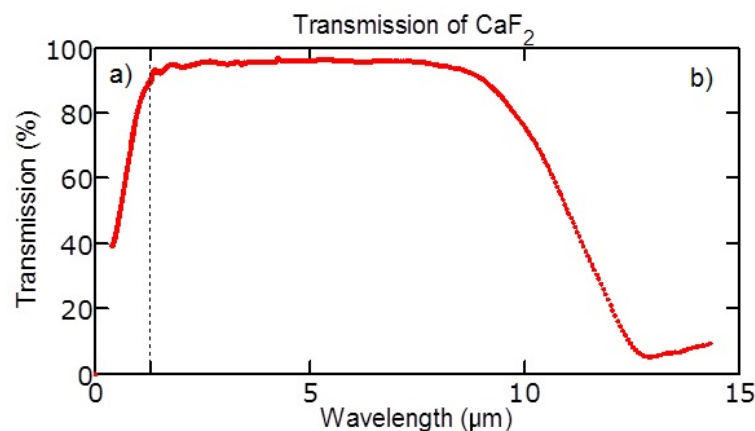
FIGURE 6.35: Transmission spectra of polished CaF substrate.

The production of the metamaterial pattern on a gold film is followed by a triple layer structure (Figure 6.34). The presence of the buffer and capping layers is essential to achieving reproducible, reversibly switching functionality but they also affect the optical and thermal properties of the structure. For example, by spacing the metamaterial and phase-change layers the buffer layer affects the spectral position and width of the structure's absorption resonance and is detrimental to contrast ratio. On the other hand, the presence of the buffer and capping layers allow more efficient optical Joule heating of the samples which enables switching with shorter optical pulses, thereby increasing the speed of the devices. Through practical testing and numerical simulation we have been able to optimize the layer structure of samples and associated metamaterial cell designs for mid- and near-IR applications to maximize switching contrast while retaining a physically robust device structure (Figure 6.36).
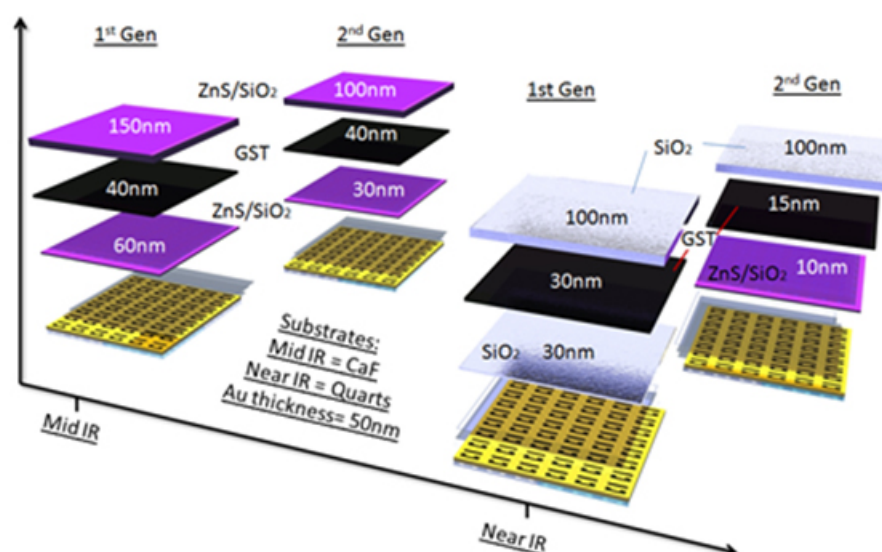
FIGURE 6.36: Evolution of chalcogenide metamaterial structures for optimal switching contrast in physically robust architectures.

6.6   Characterisation

6.6.1   Metamaterial heater switching setup

In order to switch an area of at least 50um x 50um, a setup needs to be used which supports high current and voltage switching and allows the observation of the device in order to determine if and when the device has switched. Based on this the setup shown in Figure 6.37.

6.6.2   Metamaterial optical switching

6.6.2.1   Rastor setup

Most conventional optical switching devices using chalcogenides (e.g. CDs and DVDs) achieve phase change marks on the order of 700 nm - 1 μm. In such systems a laser is typically focussed to a diffraction limited spot to provide sufficient power density and temperature increase to change the phase of the material. Large area optical switching of chalcogenides using only a diode laser has not previously been demonstrated.

In order to utilise phase changes as a mechanism for realizing all-optical switching through the integration of chalcogenide thin films with metamaterial arrays (having dimensions of order 50 μm x 50 μm) one must address the technical challenge of developing a method to achieve fast optical switching of chalcogenides over what is (in this field) a very large area.
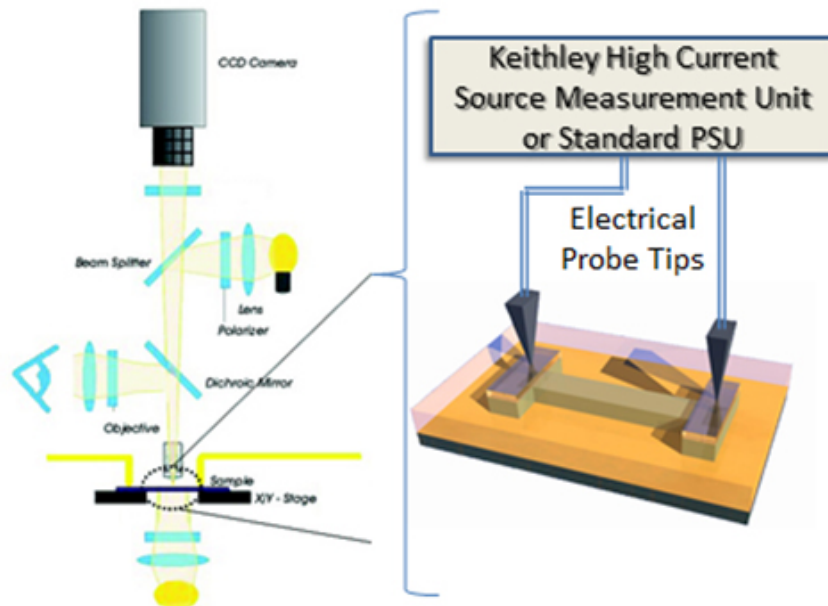
FIGURE 6.37: Large area crystallisation switching experimental setup.
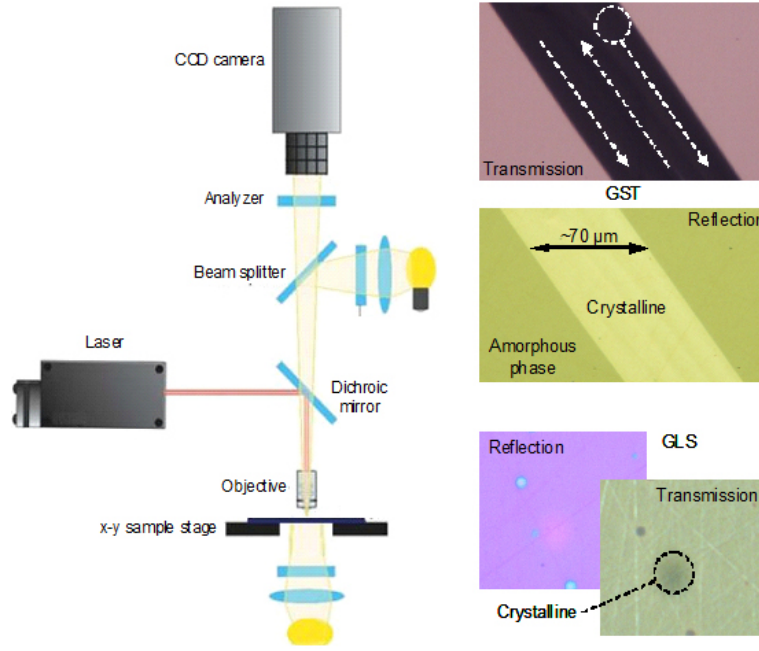
FIGURE 6.38: Experimental platform (left) for targeted optical phase switching of chalcogenide glasses. Right- preliminary tests on GeSbTe and GaLaS thin films (on CaF substrates, with ZnS/SiO_2 capping layers). As illustrated for the GeSbTe film, the laser spot can be scanned across a sample surface to convert large areas of material.

The first experimental setup used to optically induce large area crystallisation of GaLaS was achieved using the setup shown in Figure 6.38. Using this setup a spot size on the sample of 15um and an incident power on the surface of the sample as high as 1.10-12.0 mW, there was a need to rastor the beam in order to fully phase change a metamaterial array.

6.6.2.2 Single pulse large area switching

As the rastor method of large area switching was not very well suited to an integrated device, effort was made to create a setup that can be used for single pulses switching. To this end, a system has been assembled for routine large-area optically-induced switching. This provides capability for targeted excitation of structural transitions in thin film chalcogenide samples regardless of underlying metamaterial sample structure. This system (Figure 6.39) is based on a 660 nm diode laser focused to a spot size at target of up to 50 μm diameter (giving intensities up to 0.25 mW/μm2). Successful reversible switching of both germanium antimony telluride (GeSbTe) and gallium lanthanum sulphide (GaLaS) chalcogenide films has been demonstrated and switching of chalcogenide hybrid metamaterial devices has subsequently been achieved (see "Chalcogenide metamaterial all-optical switching" below).

Laser pulses (durations down to 50 ns) were shaped using an Agilent 8110A pulse generator while optical changes in the chalcogenide layer were monitored in real time to
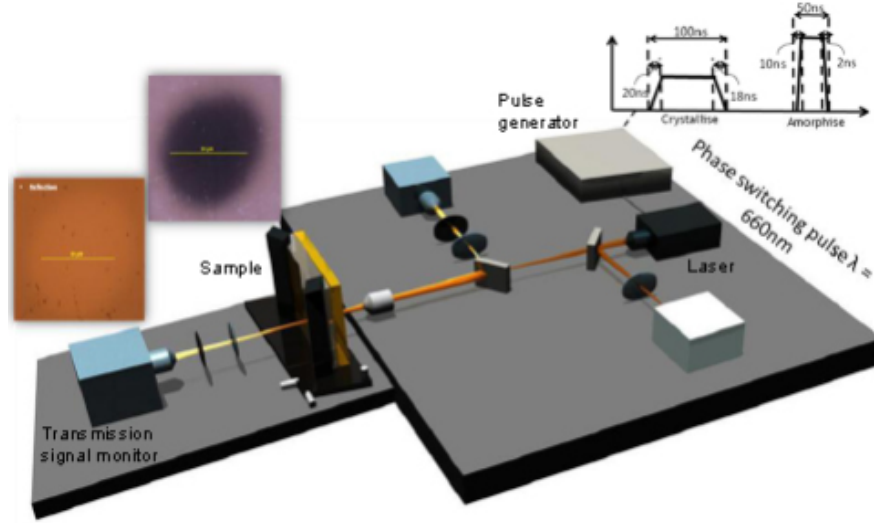
FIGURE 6.39: Experimental platform for single-pulse, large-area optical phase switching of chalcogenide glasses.

identify the phase transition points. In this way it was possible to optimize pulse energy and duration separately for the forward (amorphous-crystalline) and reverse (crystalline-amorphous) transition directions: the former requiring longer, lower power pulses; the latter shorter, higher power pulses.

6.7 Results and discussion

6.7.1 Large area crystallisation tests

In order to create a set of all optical and electro-optic metamaterial switches the experimental setup shown in Figure 6.39 and Figure 6.40 was used to create a series of DC sweeps in order to heat the chalcogenide thin film through Joule heating and to bring the temperature of the thin film directly on top of the metallic structure to the crystallisation temperature. The sweep shown in Figure 6.40 was initially used to investigate whether phase change could indeed be induced.

By gradually increasing the current going through the metallic back electrode structure and observing the change through optical microscopy and taking out the power as soon as a change is detected, the results shown in Figure 6.40 across both the two terminal and six terminal devices was observed.

In the first set of switching experiments it was observed that although a large area was crystallised, this crystallised area was inhomogeneous and the concentration of the crystallites was much higher in the perimeter of the structure than the central region. To improve this, a second set of switching experiments was carried out with the difference being that in this instance, when the switching of the device was observed optically the
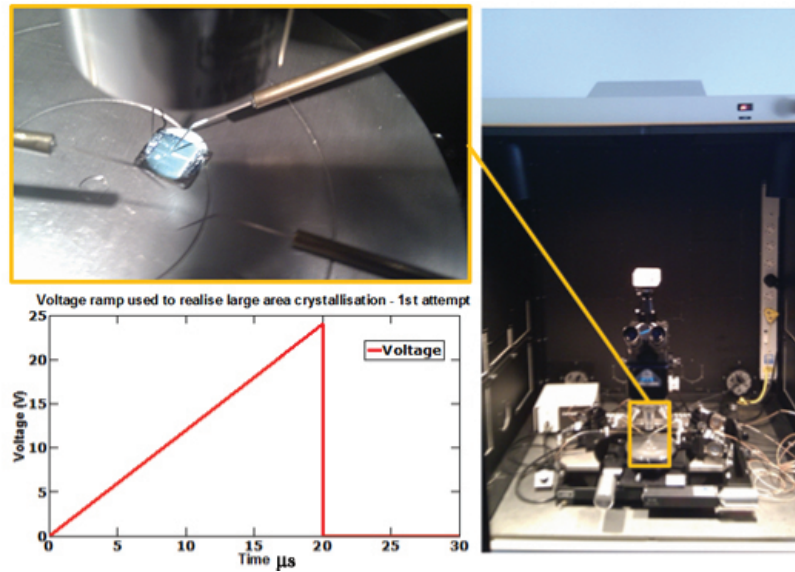
FIGURE 6.40: Voltage ramp used initially to observe large area switching, along with
the corresponding experimental platform used.

sweep was held at that point for period of time instead of stopping the electrical input,
as before (see Figure 6.42).

This new hold section added to the end of the sweep allowed the crystallites to grow
across the large area that had been heated through Joule heating, making the area
switched much more homogeneous. This produced a second set of switching results as
shown in Figure 6.43.
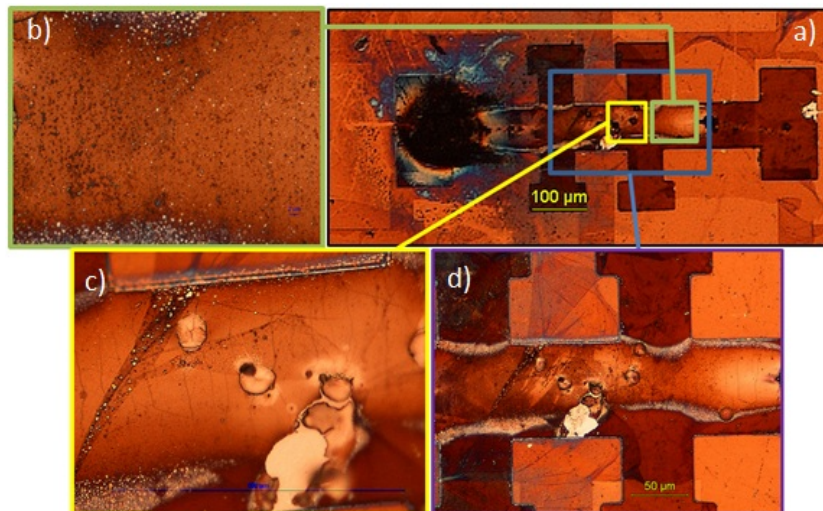
FIGURE 6.41: Optical microscopy image of the devices after switching using first voltage
ramp program showing a degree of crystallisation, with clear crystalites visible along the
hot region of the heater. a) The entirety of the structure is shown with the left contact
pad having been damaged by the probe. b, c and d show the structure with higher
levels of magnification. The increase in density of the crystals around the perimeter of
the structure can be observed clearly in d.
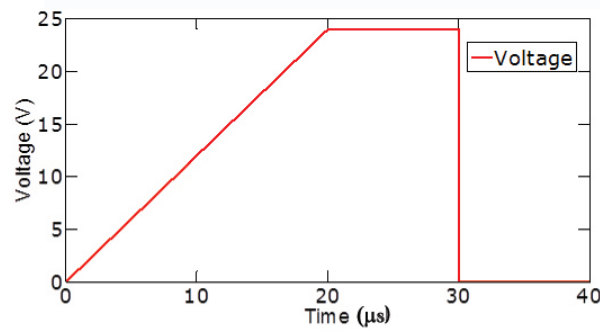
FIGURE 6.42: Second voltage ramp used, this time introducing a voltage hold section
to grow crystallites.

Comparing the two set of results, it can be observed that after the onset of switching
if the electrical input is kept on, the crystallites grow and create a much more uniform
crystalline layer at the hotspot. This observation both reaffirms the idea that this shows
a degree of crystallisation and phase change as well as the fact that the switching can
be controlled and its intensity and uniformity optimised.

The damage seen on the pads of the device are as a result of the electrical probe contacts
on the surface of the structure. Unstable and non-ideal contacting to the device results
in two major outcomes on the pads around the device:

- Excessive pressure on the structure by the probes can damage the structural integrity of the device pads.

- Unstable contacting to the device can result in minute electrical static discharge
  on the structures when a high voltage is put through.
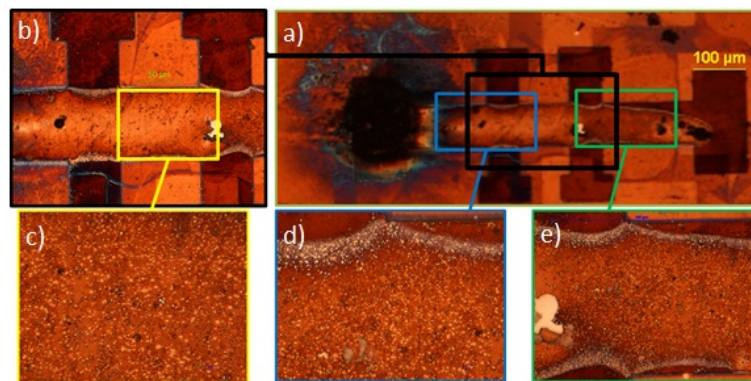
FIGURE 6.43: Samples after second voltage ramp showing a much denser and homogeneous crystallite surface as a result of the modified voltage ramp. a) shows the entirety
of the structure with the crystallised region across clearly observable. b, c and d are the
hotspot with higher magnification. Again the perimeter of the structure has a higher
density of crystals but the introduction of the hold section in the voltage sweep has
dramatically increased the density of the crystals that have grown across the structure
yielding a much more uniform crystallised layer.
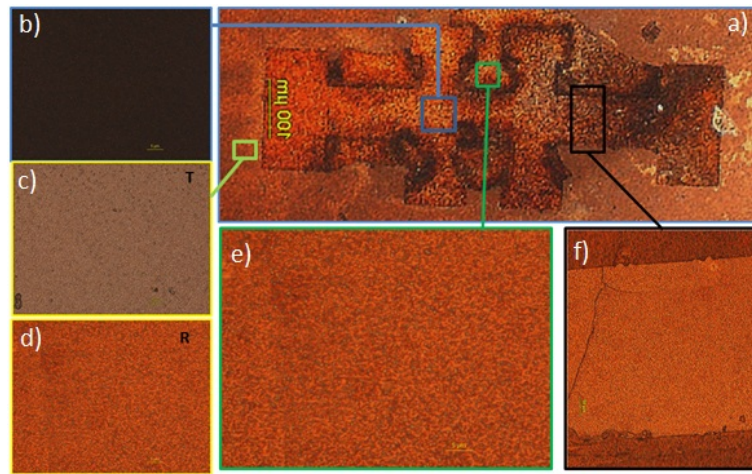
FIGURE 6.44: Transmission optical microscopy images on the second set of devices fabricated on a CaF substrate. a) shows the interface between where the molybdenum structure lies on top of the GaLaS layer and the bare GaLaS layer before switching showing smooth layers with little scattering or signs of crystals. b, c and d show the interface after being switches with the crystals grown on the previously smooth layer observable, these crystals can be seen to have grown underneath the molybdenum structure in d, showing a much more uniform switched layer with this design. This method also allows transmission optical microscopy as opposed to the previous design which only allowed reflection measurements.

These problems can be circumvented through a more complex high throughput chip described earlier in this chapter as well as using a more advanced electrical contacting system described in Chapter 5. The high throughput chip (described in section 3.1.3.1), allows the analysis of a range of different compositions arriving at the best composition for the refractive index change between phases and most desirable activation energy for crystallisation all on one chip. As described previously a second set of devices were also fabricated with a CaF substrate in order to be able to get transmission as well as the reflection data observed in the structures shown above. When the same DC sweep method was used to switch these devices the results shown in Figure 6.44 were obtained.
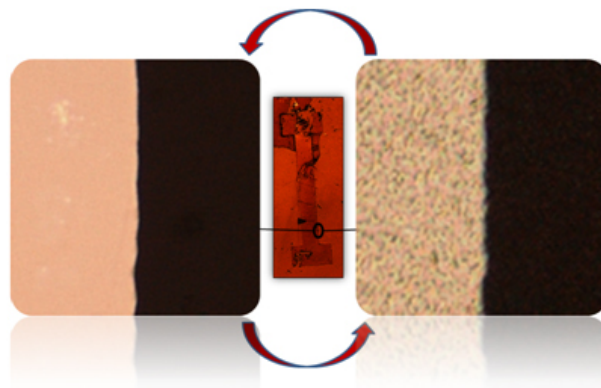
FIGURE 6.45: large area electronic phase change.
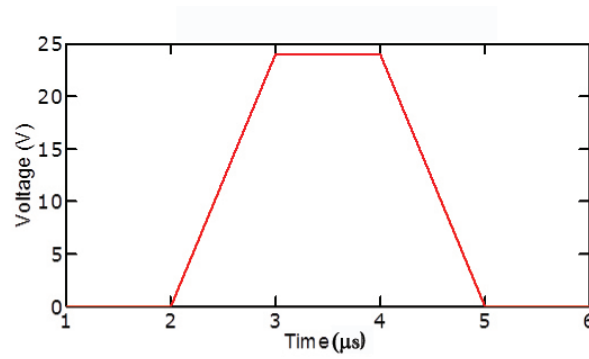
FIGURE 6.46: Voltage pulse used for large area switching of metamaterial high through-put chip.

These sets of results provide a good proof of principle and an indication that electrically induced large area crystallisation within chalcogenides is possible (Figure 6.45) and repeatable. The introduction of a metamaterial array within the heater structure would also, based on the simulations run both make the task of achieving large area crystallisation easier and bring the power requirements down considerably.

The high throughput metamaterial chips fabricated previously were deposited with an active layer of compositionally varying GaLaS using the physical vapour deposition technique set out in Chapter 3. In order to investigate the suitability of the metamaterial integrated large area heaters they were characterised with the voltage pulse shown in Figure 6.46. Optical microscopy images of the high throughput chip, and the two distinct structures used for large area metamaterial integrated phase switching is shown in Figure 6.47.
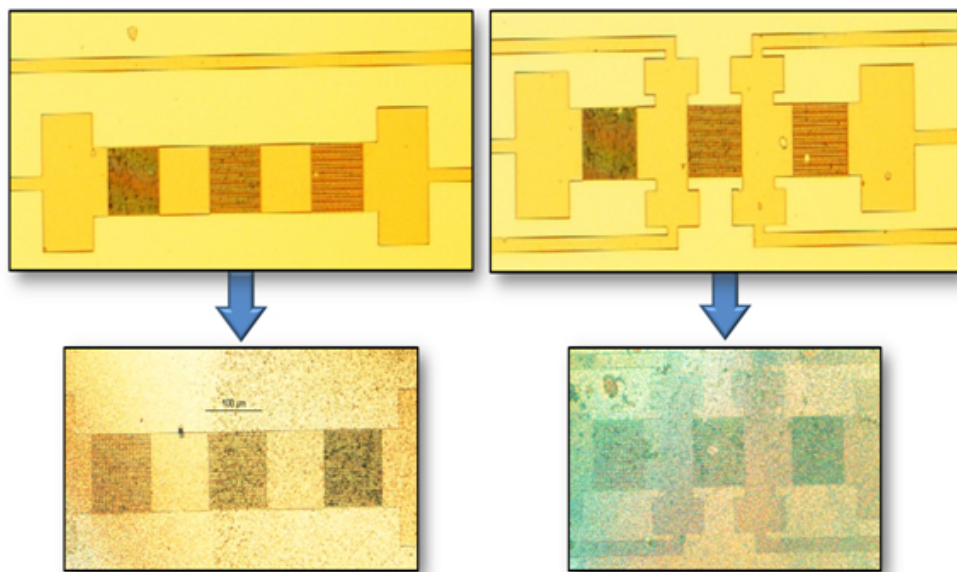
FIGURE 6.47: Optical microscopy images of High throughput chip in amorphous and crystalline form of the active GaLaS layer.
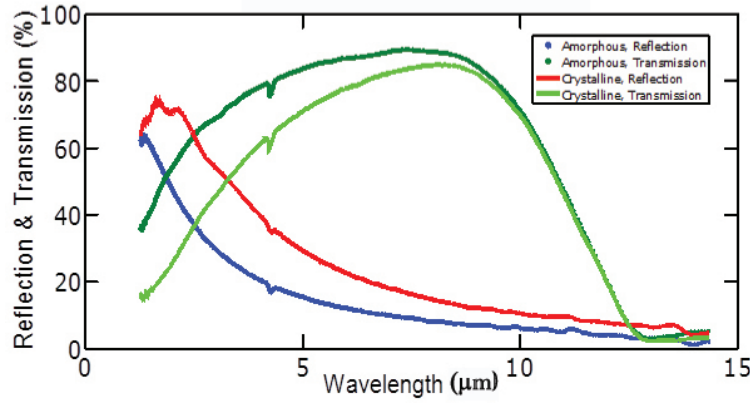
FIGURE 6.48: Spectrum of GeSbTe thin film on calcium fluoride substrate.

6.7.1.1   All optical GeSbTe metamaterial switches

The underlying concept used within these hybrid optical switches is the phase transition of GeSbTe between an amorphous and a crystalline state. It should be noted that in the first instance the phase switching behaviour of a GeSbTe thin film on a CaF is observed without the presence of a metamaterial array (Figure 6.48).

When looking at the transmission contrast between the two phases of the material, one can observe that the modulation is between 1:1 to 2:1 across the range measured.

The next step in the production of the device is the deposition of the confirmed phase change layer GeSbTe with the gold film used for metamaterial fabrication. Figure 6.49 shows the spectra for both transmission and reflection of a test device identical to the optical switching chips fabricated but without a metamaterial array. One can observe the enhancement in transmission and reflection at resonant wavelengths observed as a result of the introduction of the metamaterial arrays in both the near and mid infrared (Figure 6.50).
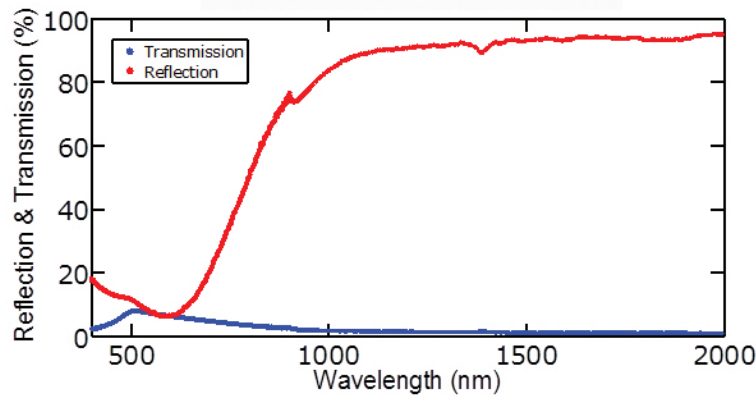
FIGURE 6.49: Spectra for GeSbTe/ZnS-SiO$_2$/Gold film without a metamaterial pattern.
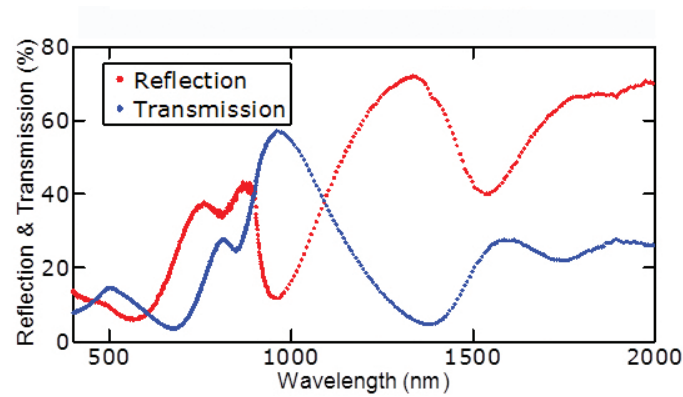
FIGURE 6.50: Typical as deposited Near-IR GeSbTe/gold metamaterial spectral response.

It had been anticipated that as a result of the optical phase change of the active GeSbTe layer a bidirectional shift in the resonant peaks of the metamaterial should be observed. This is due to the fact that phase switching the chalcogenide layer in the hybrid metamaterial produces a marked change in its resonance frequency of the structure. The GeSbTe transition from amorphous to crystalline increases its refractive index and redshifts the resonance frequency of metamaterial, bringing about a substantial change in optical transmission at wavelengths in the vicinity of the resonance.

As set out previously two methods of optical switching was pursued, initially rastoring
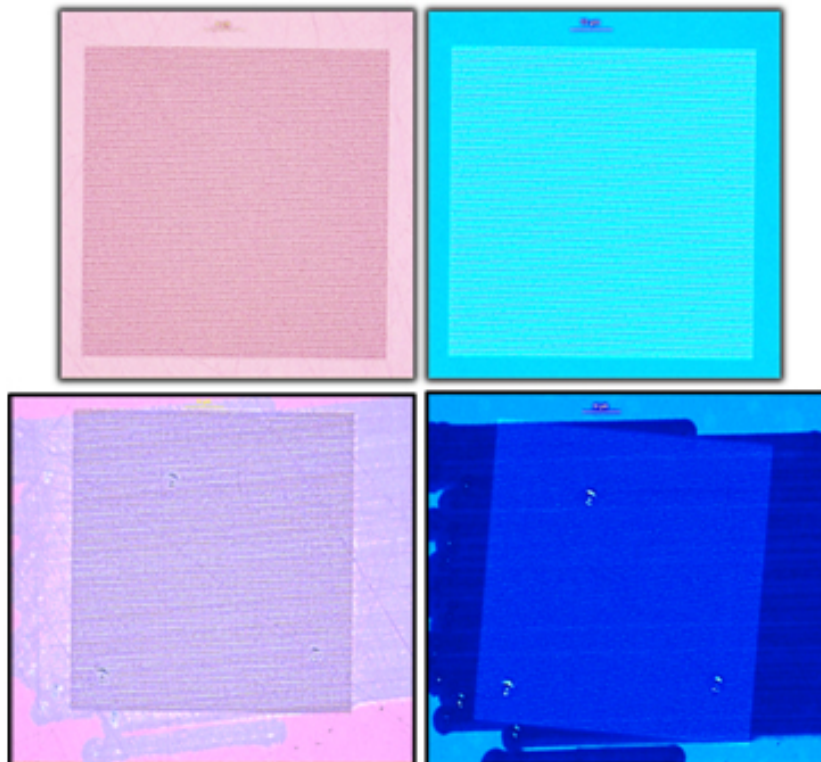
FIGURE 6.51: Optically switched chalcogenide hybrid metamaterial using a rastoring beam technique.
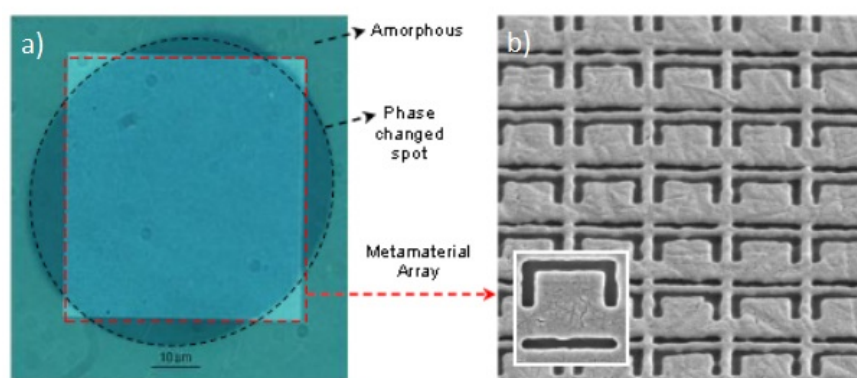
FIGURE 6.52: Large area optical switching in a chalcogenide thin film hybridized with a photonic metamaterial. a) Transmission optical microscopy image of optical switch with metamaterial array and single pulse switching footprint visible. b) Scanning electron microscope of the periodic structures milled into a 50 nm gold film, which make up the array shown in a).

the beam was used to optically switch the chalcogenide layer on top of a metamaterial array (see Figure 6.51).

As this was logistically undesirable in terms of an integrated device, as described earlier this was improved upon by using a spot size large enough to cover a substantial part of the metamaterial array. In the case of a chalcogenide metamaterial hybrid device this capability provided for single-pulse initiation of uniform phase transitions across entire nanostructured regions (Figure 6.52), bringing about dramatic changes in the spectral position of the metamaterial trapped mode absorption resonance and thereby the optical transmission of the structure. Figure 6.52 shows scanning electron microscopy (SEM) images of a metamaterial engineered for mid-infrared (2-10 μm) functionality. The pattern was fabricated by focused ion beam milling through a 50 nm thick gold film deposited on a calcium fluoride (CaF_2) substrate by thermal evaporation. The metamaterial was then coated with buffer, GeSbTe and capping layers as described and illustrated in Figure 6.36. Figure 6.52 shows a transmission optical microscope image of the sample after single-pulse laser excitation to induce crystallization of the GeSbTe over an area (the darker circular region) almost entirely covering the patterned domain (the square region). Crystallization is confirmed by further SEM imaging.

The metamaterial geometry can be scaled for functionality at any wavelength within the transparency range of the chalcogenide dielectric and we have demonstrated high-contrast modulation (up to a factor of 6) in both the mid-infrared (Figure 6.53) and near-infrared ranges (Figure 6.54) using structures <150 nm thick (excluding substrate).

The transition to the more reflective crystalline state (occurring through localized Joule heating) brings about a dramatic red-shift of around 200nm in the spectral position of the hybrid metamaterial's trapped mode resonance,in the spectral range 5 to 6.5μm.
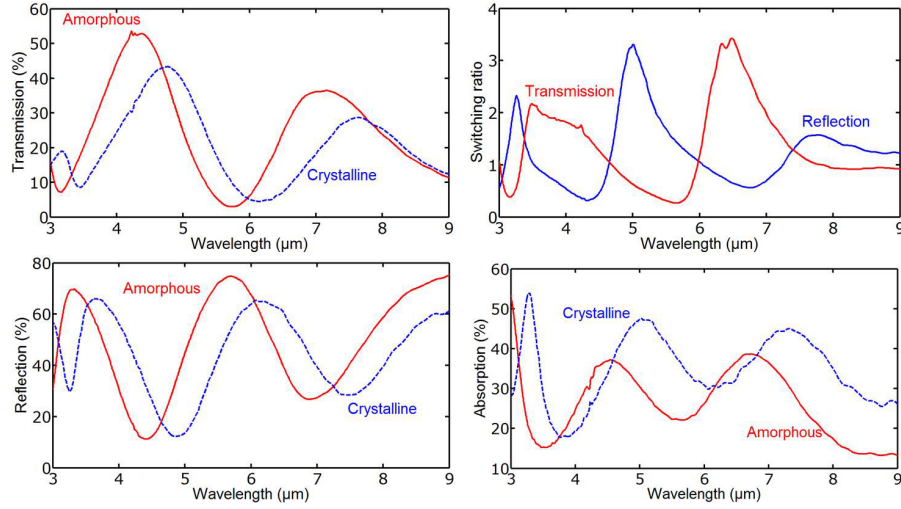
FIGURE 6.53: All optical mid-IR chalcogenide metamaterial switch : Metamaterial transmission and reflection resonances are spectrally shifted when GeSbTe undergoes transitions between amorphous and crystalline states giving strong modulation contrast [right] in wavelength bands around these resonances [Metamaterial unit cell sizes 600nm].

Figure 6.53 and Figure 6.54 show the corresponding transmission, reflection and absorption characteristics of the GeSbTe hybridized metamaterial, but in the new structural phase of crystalline. The resonance features were quantified again at normal incidence using the above mentioned microspectrophotometer.

As set out, to switch back the device, shorter higher powered pulses are used to switch the now crystalline GeSbTe layer on top of the metamaterial array back to an amorphous state. This, in effect brings about the melting and rapid quenching of the nanoscale
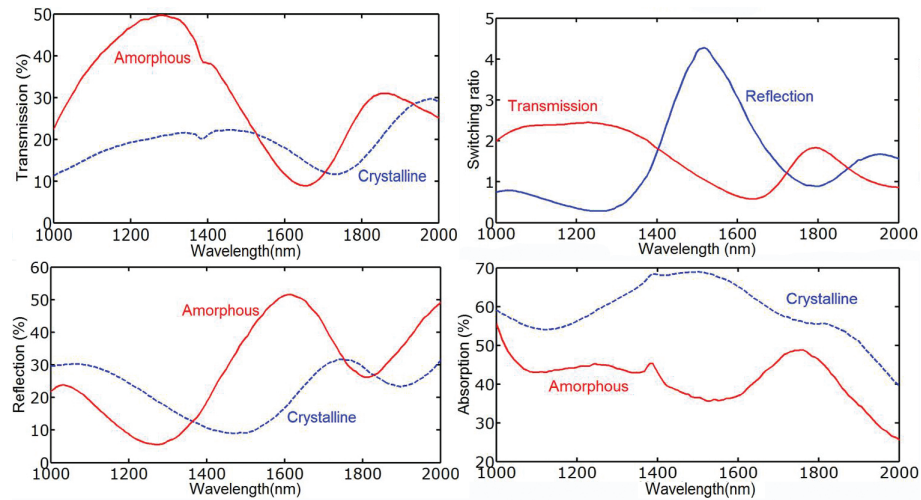
FIGURE 6.54: All optical near-IR chalcogenide metamaterial switch : Metamaterial tansmission and reflection resonances are spectrally shifted when GeSbTe undergoes transitions between amorphous and crystalline states giving strong modulation contrast [right] in wavelength bonds around these resonances [Metamaterial unit cell seizes 400nm].

chalcogenide layer allowing its transition back to a glassy state. This brings about a blue shift of 600nm in the trapped mode spectral range of 5 to 6.5μm.

Following hybridization with GeSbTe, the metamaterials' absorption spectrum, accrues a background associated with the additional absorption of the GeSbTe layer and the slight broadening of the plasmon peak due to increased damping. This is more pronounced in the more reflective crystalline phase, which inherently has larger extinction coefficients as well. The 600 nm resonance shift during structural phase transition from amorphous to crystalline (as highlighted in Figure 6.53), brings about substantial changes in the transmission and reflection of the hybrid structure at certain wavelengths. The transmission and reflection modulation contrast associated with chalcogenide phase switching in the hybrid structure are given as:

$$T_{mod} = \frac{T_a}{T_c}, \ R_{mod} = \frac{R_a}{R_c},$$

where 'a' and 'c' denotes to amorphous and crystalline form of GeSbTe during transmission and reflection measurements. For example, the transmission changes by around as much as a factor of four within a wavelength band centered at around 5μm (nearby the structure's trapped mode resonances during crystalline phase - see Figure 6.53). The reflectivity changes resulting from phase switching are also substantial, reaching around 4:1 at around 1500nm in the Near-IR switches (Figure 6.54). Thus, the hybridized metamaterial can act as a transmission and reflection switch, providing a contrast ratio of 4:1 in the near and mid infrared domains with device structures less than one eighth of a wavelength thick.

To summarize this section, for the first time, reversible, non-volatile, all-optical switching in a hybrid chalcogenide glass metamaterial structure is demonstrated; Using germanium antimony telluride (GeSbTe) glass and gold plasmonic nanostructures of sub-wavelength thickness, reversible switching in the near and mid-infrared spectral range with modulation contrast exceeding 4:1 has been achieved using nanosecond pulses at an optical excitation levels below 0.25 mW/mum2 (Figure 6.55).
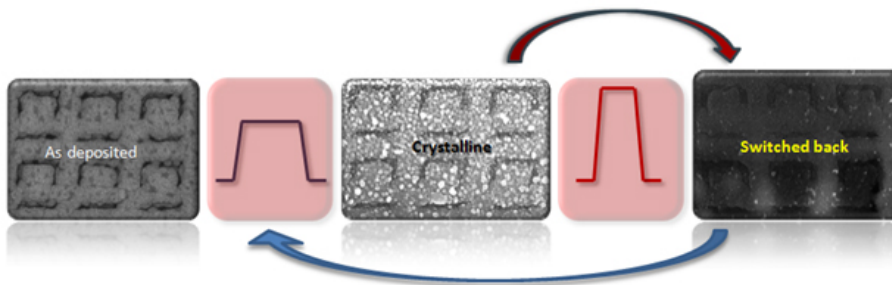
FIGURE 6.55: All-optical IR chalcogenide metamaterial switching: Single pules laser excitations convert the GeSbTe layer, across the entire metamaterial array (unit cell size = 400 nm), between amorphous and crystalline state, thereby switching the reflectivity and transmission of the hybrid structure with high contrast at wavelengths close to the metamaterial resonance.

6.8   Summary

The primary objective of this work was to achieve proof-of-principle demonstrations of novel devices providing reversible nanophotonic switching functionality based on optically- and electrically-addressed chalcogenide phase-change materials.

In reaching this goal, significant landmarks have included:

- Large area optical single pulse switching of Germanium antimony telluride thin films.

- Design and development of large area electrical heaters and integrating metamaterials.

  - First demonstration of Large area electro-optical switching of Gallium lanthanum sulphide thin films.

  - Design, fabrication and characterisation of a high throughput electro-optic and all optical metamaterial dielectric chip for high throughput optimisation.

- First demonstration of non-volatile reversible all optical metamaterial switch.

  - Demonstrated tunability in the near and mid infrared.

  - Thinnest all optical switch demonstrated thus far (thickness <150nm), an eighth of a wavelength thick.

  - Up to 4:1 switching contrast ratio .

  - 50 and 100ns reset and set switching times.

The knowledge and expertise derived from these achievements set a strong foundation for the continuation and expansion of research work in the field of chalcogenide photonics, where directions may include the development of optically and electro-optically multi-element devices with parallel control (e.g. spatial light modulators for phase and intensity control) and photonic cognitive and data processing systems, when taking advantage of the work set out in chapter 5 in conjunction with this work.

Chapter 7

Conclusions

7.1 Conclusion

The principal goal pursued within this research has been the application of chalcogenide thin phase change thin films for emerging optoelectronic data storage and information processing applications. Three material systems have been utilised, namely GeSbTe, GeSb and GaLaS. The devices demonstrated within this work show the great promise which chalcogenide phase change thin films show in providing novel solutions for next generation logic and memory devices which will take us in the short term beyond the limits of the silicon chip and, into the world of neuromorphic cognitive computing, computers that think and adapt, and also ultra-high speed optoelectronic switches to power the internet and future computers.

In its simplest form, next generation thermally stable phase change (PCRAM) and nano-ionic resistive (ReRAM) memory is pursued for ultralow power, non-volatile high density data storage and prcoessing. Additionally, the design of novel processing elements like next generation logic gates enabling neuromorphic cognitive processing and data storage in one structure based on material properties. Finally, the integration of phase change thin films with metamaterial arrays to produce electro-optic and all optical switches for future photonic computers and communication networks.

The original contributions of this work in the fields of data storage, information peocessing and nanophotonic applications are listed below and are now reviewed in more detail. They are also linked to the list of project aims given in Chapter 2.

7.1.1 Data storage

The primary objective of this work was to investigate the suitability of sulphide based chalcogenide memory cells for low current (power) consumption electronic phase change
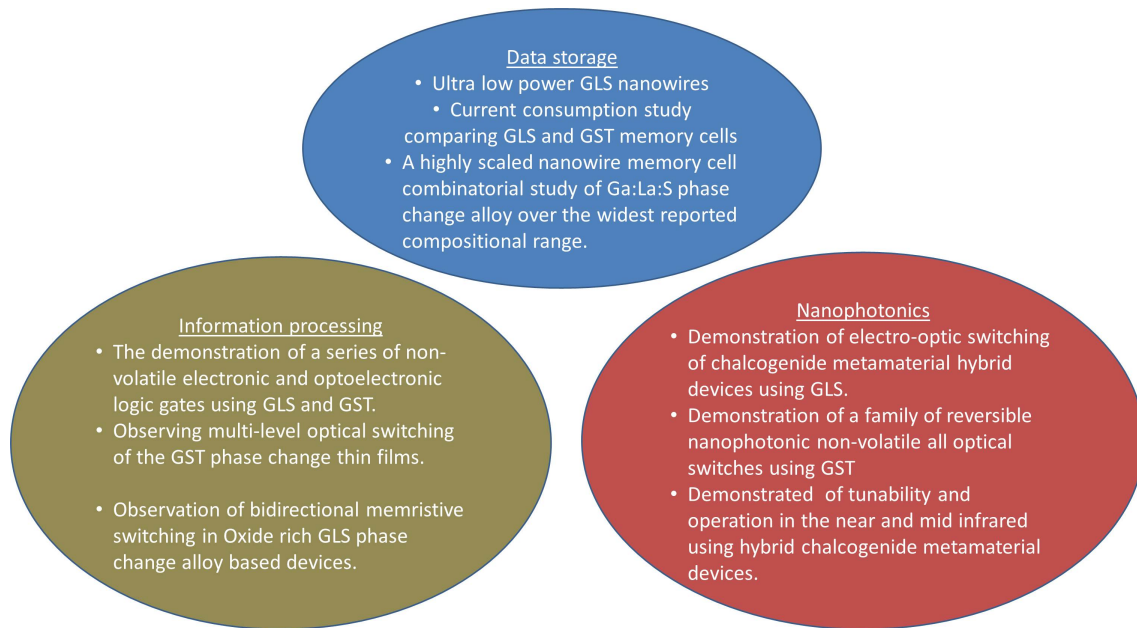
FIGURE 7.1: Project contributions to the different fields of information storage and processing within electronics, optoelectronics and nanophotonics.

memory applications. To this end, memory cells incorporating GeSbTe, GeSb and GaLaS have been designed, fabricated and characterised, whilst also scaling the devices to investigate the effect on power consumption parameters.

In reaching this goal, significant landmarks have included:

- Fabrication of GeSbTe, GeSb lateral nanowire memory cells.

- First demonstration of Gallium lanthanum sulphide nanowires.

    - Low current consumption (one of lowest reported).

        * Set currents $< 1\mu A$

        * Reset current ≈ 1–$10\mu A$

    - High thermal stability (operation of up to 600 celsius)

    - High resistance contrast up to 10^4.

- Highthroughput nanowire phase change memory chip fabrication and characterisation for the optimisation of the GaLaS phase change ternary. The knowledge and expertise derived from these achievements set a strong foundation for the continuation and expansion of research work in the field of chalcogenide phase change data storage, where directions may include synthesising sulphide based nanowires through VLS techniques [see Future work] allowing high endurance highly scaled devices. The use of highthroughput technique also allows rapid optimisation of optimal compositions for nanowire data storage.

7.1.2   Information processing

The primary objective of this work was to investigate the suitability of chalcogenides for more exploratory information processing devices. Proof-of-principle demonstrations of novel devices providing AND and OR logic operations in electronic and optoelectronic modes of operation has been pursued. Observations of bidirectional resistive switching in more complex sulphide based structures also indicate the possibility of utilising these thermally stable chalcogenide films in resistive memory applications.

In reaching these goals, significant landmarks have included:

- Electronic non-volatile phase change logic gates

    – AND gate

- Optoelectronic programmable logic gates.

    – AND gate
    – OR gate

- Observation of bidirectional switching in oxygen rich Gallium lanthanum sulphide (GaLaSO) hybrid device.

- Optical cognitive multilevel transmission switching of GeSbTe thin film.

- Observation of bidirectional resistive switching of GaLaSO hybrid device.

- Observation of memristive response of GaLaSO hybrid.

The knowledge and expertise derived from these achievements set a strong foundation for the continuation and expansion of research work in the field of chalcogenide information processing devices, in particular the marriage of optical multilevel switching and optoelectronic logic elements with photonic metamaterials, can bring about full memristive information processing capability as well as multi-level cognitive operation which allows low footprint processors, whilst the non-volatility allows "True sleep" computing using ultra low power consumption.

7.1.3   Nanophotonics

The primary objective of this work was to achieve proof-of-principle demonstrations of novel devices providing reversible nanophotonic switching functionality based on optically- and electrically-addressed chalcogenide phase-change materials. This has resulted in the first demonstration of reversible, non-volatile, all-optical switching in a hybrid chalcogenide glass metamaterial structures: Using germanium antimony telluride (GeSbTe) glass and gold plasmonic nanostructures of sub-wavelength thickness,

reversible switching in the 1-2 μm spectral range with a modulation contrast exceeding 4:1 has been achieved at optical excitation levels below 0.25 mW/μm2.

In reaching this goal, significant landmarks have also included, the first demonstration of electrically-induced wide area phase-change switching in a gallium lanthanum glass (to our knowledge, the first demonstration of such switching in any phase-change memory material) via planar multi-terminal micro-ribbon heaters (an essential development electro-optic metamaterial applications).

The development of high-throughput metamaterial dielectric chip and analysis techniques for chalcogenide media and metamaterial hybrids which will provide considerable insight into device fabrication/optimization and electrical/optical phase switching for the new chalcogenide system.

The knowledge and expertise derived from these achievements set a strong foundation for the continuation and expansion of research work in the field of chalcogenide photonics, where directions may include the development of optically and electro-optically multi-element devices with parallel control (e.g. spatial light modulators for phase and intensity control) and photonic cognitive and data processing systems.

7.2   Future work

Based on the work done and described in this report a number the future work for this project. This is briefly described in this section and is categorised within the same areas as the work carried out thus far.

7.2.1   Memristive work

Within the memristive/Resistive RAM work being done a number of investigations will be carried out:

The insitu doping of the GaLaS alloy during sputtering in two ways:

- In situ oxygen doping of the GaLaS layer during sputtering.Instead of depositing two discreet layers of GaLaS and GaLaSO as with the hybrid cell shown in this report. In situ oxygen doping of the chalcogenide alloy will be tested during sputtering by allowing oxygen into the chamber during deposition in a gradual incremental manor yielding a gradient of low to high oxygen doped GaLaS, which may yield a much more homogoneous and better quality active layer compared to the hybrid cell used here.

- The in situ doping of the chalcogenide layer deposited through RF sputtering with metal ions by sticking metal particle ingots onto the sputtering target will allow the investigation of GaLaS as a conventional RRAM. This method of in situ composition change was tested out during the past few months with successful results although optimisation of the process is required. Subsequently plans are in place to upgrade the facilities at the ORC allowing both guns on the RF sputtering machine to be operated simultaneously, giving rise to the possibility of both introducing dopants in a very controlled manor to conventional alloys as well as allowing the possibility to investigate increasingly interesting superlattice structures.

Characterisation of the mechanism responsible for the different types of logic and memory switching behaviour observed thus far in these devices can now also be investigated in a much more in depth novel manor through the use of the new four probe NANON-ICS AFM at the ORC. A number of propositions are made to investigate fundamental questions relating to memristive/nanoionic structures, through the use of the proposed experimental setup shown in Figure 7.2.
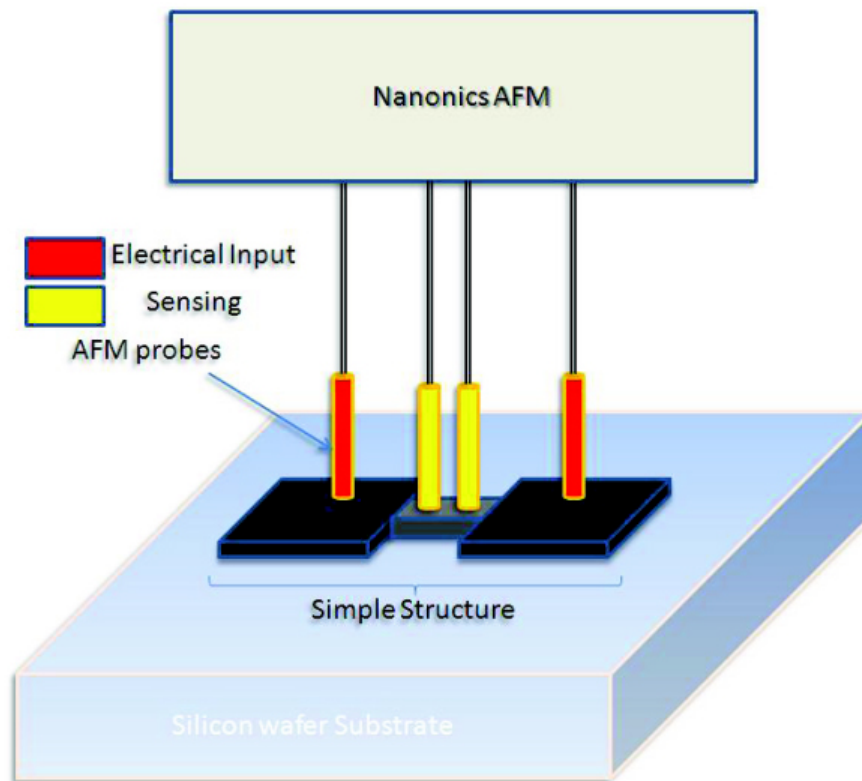
FIGURE 7.2: Single pulse switching of GaLaS cells as a control experiment.

Through the use of the multiprobe system, an electrical pulse can be sent through different lateral phase change, hybrid and oxygen or metal doped chalcogenide layers and by placing probes across the path of electricity one can observe the movement of ions or vacancies across the structure thus arriving at a model of how the ions move through the atomic structure of our chalcogenide systems.

7.2.2   Phase change memory

As scaling and thermal stability are both closely related to each other in high density chips, it is proposed that a series of cells at the nanoscale, be fabricated (as shown in Figure 89, with varying spacing between cells with GaLaS and GeSbTe as the active chalcogenide layer. This investigation is carried out in two different ways. First, the effect of switching a cell on its adjacent cell given different spacing and the temperature gradient radially around a cell that is being switched (the latter can be carried out by using the multiprobe AFM system). These simple experiments yield very improtant resutls that provide solutions to the major problems that need to be overcome in order to fully commercialise phase change memory devices. Second, a device that is based
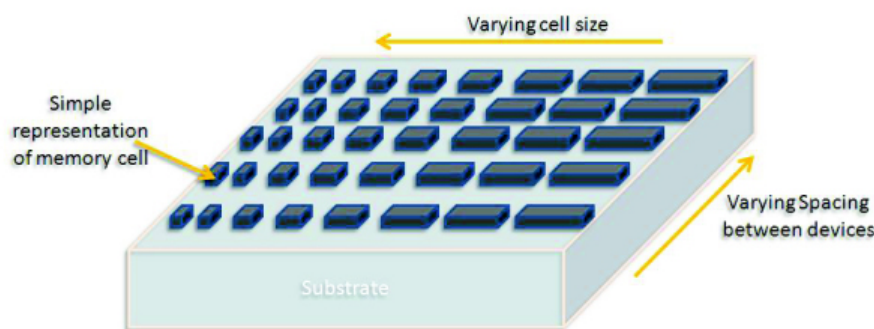
FIGURE 7.3: Proposed experiment for thermal stability vs scaling study.

on the NEMRAM structure (much the same way as Nantero Inc Carbon nanotube NEMRAM), by cutting out bridges of hybrid metal-chalcogenide layers and switching the phase of the chalcogenide through the use of the metal layer, the change in spacing of the chalcogenide should yield a geometrical change in the NEMRAM bridge, this can have many uses in both memory and optical switch applications(Figure 7.3).
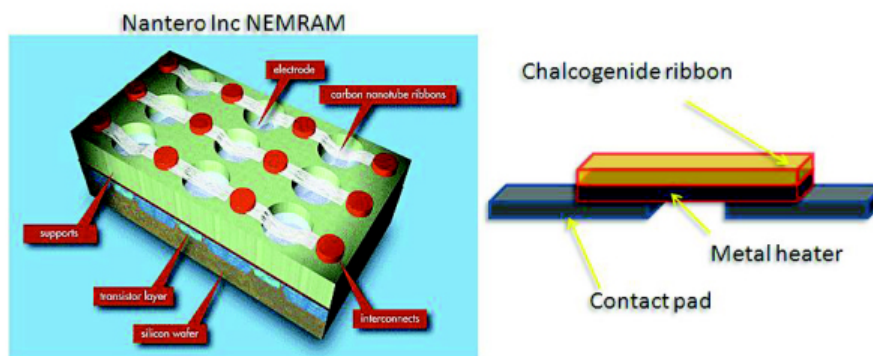
FIGURE 7.4: Chalcogenide NEMRAM proposed device inspired by Nantero Inc NEM-
RAM (9) device.

These are a brief overview of some of the investigations and experiments currently underway.

In the past, chalcogenide phase change materials based on sulphur have been ruled out due to their high crystallisation, glass transition and melting temperatures. However, the GaLaS materials utilised in this thesis have an extremely high electrical resistivity;this allows electrically efficient heating. Analysis and comparison with memory cells using $Ge_2Sb_2Te_5$ shows that the material has an order of magnitude reduction in electrical current to achieve each materials, respective, melting temperature. Further, in a practical PCRAM device, the reduction in write current allows the use of much smaller addressing transistors this mean that this material can be used in a highly scalable device. Due to the structural studies discussed previously, GaLaS is thought to be a fast switching medium as such the crystallisation speed and endurance limit of such material is an area of interest which should be explored to understand the limits of device performance made from this system.

Additionally the oxide rich devices should also be investigates with possible TEM and AFM electrical conductivity studies to understand the origins of the memristive behaviour observed, as they present a unique low power device for data storage and processing.

7.2.2.1 NWs with e-beam lithography

Electron beam lithography (often abbreviated as e-beam lithography) is the practice of emitting a beam of electrons in a patterned fashion across a surface covered with a film (called the resist), ("exposing" the resist) and of selectively removing either exposed or on-exposed regions of the resist ("developing"). The purpose, as with photolithography, is to create very small structures in the resist that can subsequently be transferred to the substrate material, often by etching. It was developed for manufacturing integrated circuits, and is also used for creating nanotechnology architectures.

The primary advantage of electron beam lithography is that it is one of the ways to beat the diffraction limit of light and make features in the nanometer regime. This form of maskless lithography has found wide usage in photomask-making used in photolithography, low-volume production of semiconductor components.

The key limitation of electron beam lithography is throughput, i.e., the very long time it takes to expose an entire silicon wafer or glass substrate. A long exposure time leaves the user vulnerable to beam drift or instability which may occur during the exposure. Also, the turn-around time for reworking or re-design is lengthened unnecessarily if the pattern is not being changed the second time.

E-beam lithography can minimise the effect of surface damage which can occur during ion beam milling on the chalcogenide layer in these lateral NW devices. As the chalcogenide can be deposited on pre-patterned substrates and is not exposed to any etching steps

to define nanoscale geometries, as a result surface defects and dopants into the active chalcogenide layer can be minimised.

It should be noted that in order to use such a method for fabrication, one needs to remember that sputtering cannot fill nanoscale vias and pores (e.g 50nm diameters), due to its non-conformal nature. As such, the chemical vapour deposition technique used previously for GeSb and GeSbTe depositions can be used by using the same technique for GaLaS depositions.

Through combining e-beam lithography and chemical vapour deposition, one can achieve very small geometries, with minimal etching damage to the active chalcogenide layer.

7.2.2.2   NW by VLS technique

Chalcogenide nanowires can be synthesized using the metal catalyst-mediated vapour-liquid-solid (VLS) process. For example, GeSbTe nanowires can be synthesised using Bulk GeTe and Sb_2Te_3 powders as precursors (213). The powders separately located inside a horizontal tube furnace in different temperature zones (GeTe in the middle and Sb_2Te_3 at the upstream side of the furnace) in order to simultaneously produce vapour-phased reactants. In this method a substrate covered with Au nanoclusters can be placed at the downstream side of the furnace and by ramping to 670^oC with a flow of Ar gas and maintained for 1 h. The local temperatures where Sb2Te3, GeTe and the substrate were placed should be approximately 575^oC, 670^oC and 520^oC, respectively from literature. This method both presents a very good method in producing nanowires due to its high yield as well as minimising any effects which lithography and ion beam etching can have on devices made from this. Using modifications to existing CVD apparatus used, one can produce these nanowires on pre-patterned gold substrates for direct device fabrication. In particular using GaS and LaS as precursors for the production of GaLaS nanowires is an interesting method to produce highly stable low power consuming NWs for memory applications. This method also allows the production of core-shell nanowires of different alloys, opening up a whole new world of possibility in producing novel devices with nanoscale optoelectronics and nanophotonic applications.

The high efficiency of high throughput deposition and characterisation is clear. In this thesis screening techniques have been exploited for screening of materials for nanophotonic and data storage applications. The VLS technique of producing NWs can also be used to produce NWs across a compositional gradient by using a gradient furnace and having gold catalyst loaded substrate across the temperature gradient producing a high yield of compositionally varying NWs.

7.2.3 Metamaterial logic devices (Radial structures)

Finally the work carried out in the field of information processing and chalcogenide metamaterial all optical switches provide a very promising base for the amalgamation of the two concepts in the pursuit of all optical and electro-optical nanophotonics information processing, which can yield devices several orders of magnitude smaller in scale than current technologies.

Modern semiconductor-based electronics is rapidly approaching fundamental limits caused by interconnect delays and large heat generation. Photonic devices and circuits could potentially solve these problems, because photons have intrinsically higher information-carrying capacity and produce low heat loads; but, the goal of all-optical computing has remained elusive. Previous developments have centred on two routes towards optical logic gates: the first one based on linear optical effects, such as interferometry, and the second one based on nonlinear processes, for example, tunable refractive indices or frequency mixing. However, the diffraction limit of light has presented a fundamental obstacle for reducing the dimensions of optical logic components to the length scales of electronic devices in integrated circuits. During the past decade, it has been proposed that photonics based on surface plasmons, that is, quanta of collective electron oscillations strongly coupled to photons in metal nanostructures, constitute one of the most interesting avenues towards further scaling down of photonic devices and simultaneous integration with solid-state electronics (214).

All-optical logic gates have received considerable attention in the field of optical networks (215); they can enable many advanced functions such as all-optical bit-pattern recognition (216), all-optical bit-error rate monitoring (217), all-optical packet address and payload separation (218), all-optical label swapping (219) and all-optical packet drop in optical time domain multiplexing (OTDM) networks (220). Many approaches have been proposed to achieve all-optical logic functions, based on the nonlinear effects either in optical fibre or in semiconductor material. Compared with their optical-fibre based counterparts (220; 221), all-optical logic gates based on semiconductor optical amplifiers (SOAs) are promising because of their power efficiency and their potential for photonic integration (215; 216; 217; 218; 219; 222; 223). In the literature most of the SOA-based optical logic gates employ interferometric structures, which requires several SOAs and makes the system complicated (215; 222; 223). A logic gate based on four wave mixing (FWM) in an SOA has also been demonstrated in (224). However, the scheme suffers from a low conversion efficiency, high input power and polarization dependence.

The all optical switches demonstrates in this work, showing both reflection and transmission switching present a unique building block, to achieve highly scaled, ultra-thin, wavelength tunable, high contrast all optical non-volatile switching. Additionally the multi-level optical switching of GeSbTe observed in this report and by others, can be

used as a means of achieving multi-level cognitive switching of metamaterials resonant responses.

By using composite metamaterial designs allowing two wavelength operation and switching the phase of the chalcogenide dielectric layer one can use two wavelength spatial multiplexing in such a structure.

Also by using stacked structures of nanostructured metamaterials, one could achieve a logical AND gate for example by focusing the laser beam on the dielectric layers independently switching each layer. This switching configuration would only show an overall change in transmission only when both the dielectric layers in the structure have been switched to a high transmission state.

Appendix A

Optoelectronic reconfigurable logic

The concept of reconfigurable logic gates a cross platform optoelectronic device where the switching excitation input is optical pulses at 660nm wavelength for 200ns and 100ns pulse widths to crystallise and amorphise the active zones.

The Optoelectronic reconfigurable logic circuits, in the particular the AND optoelectroni gate fabricated and discussed previously, is discussed here with an extension of the results being presented in order to provide a better understanding of the operation of the devices.

The truth table for the optoelectronic AND gate is shown here, indicating that when both inputs are in the low resistance crystalline state the digital state "'1"' is observed, as the resistance drops and a higher voltage is detected across the device grid.

A		B		Output
Amorphous	0	**Amorphous**	0	0
Crystalline	1	**Amorphous**	0	0
Amorphous	0	**Crystalline**	1	0
Crystalline	1	**Crystalline**	1	1

TABLE A.1: AND optoelectronic logic gate. Amorphous(0)=High resistance state, Crystalline(1) =Low resistance state

The resistance modulation of the device showing transitions between the different states of the truth table for the device is shown in Figure A.1. Showing characteristics needed for such reconfigurable logic circuits.
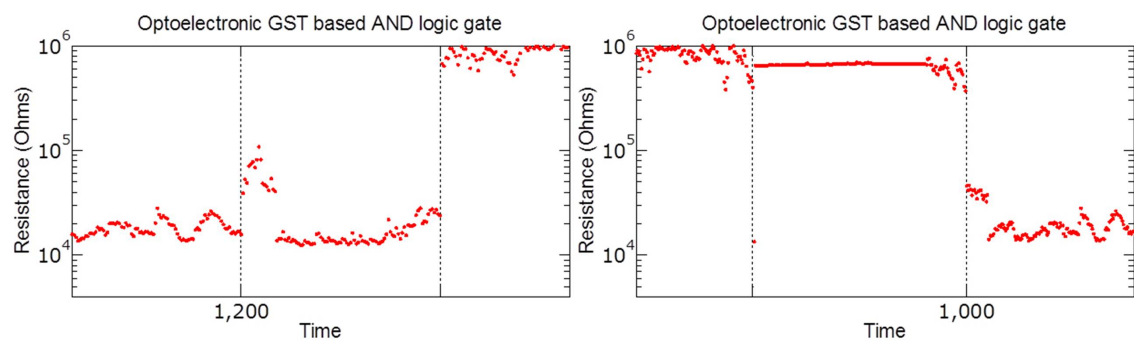
FIGURE A.1: Performance of the optoelectronic GST AND gate in transition through the different states of the boolean logic truth table.

Appendix B

Oxide rich GLS resistive switching

As discussed previously, using a hybrid GLS-GLSO cell, bidirectional resistive switching was observed with clear thresholds, an extension of the results shown previously is presented here, in the hope of providing a more in-depth analysis.

The as-deposited cell is in need of "'path forming"' as such a number of sweeps are used to form a switchin path between the electrodes within the chalcogenide layer. Figure B.1 shows the I-V characteristics of an as-deposited device.

Until a stable device performance is observed a number of sweep are made to stabalise the performance of the cells. Figure B.2 shows the bidirectional switching characteristics during this "'burn-in"' or "'path forming"' period.

Furthermore, the bidirectional resistance switching can also be manually reset to a desired polarity state by a further sweep (see Figure B.3). Subsequent to this sweep the
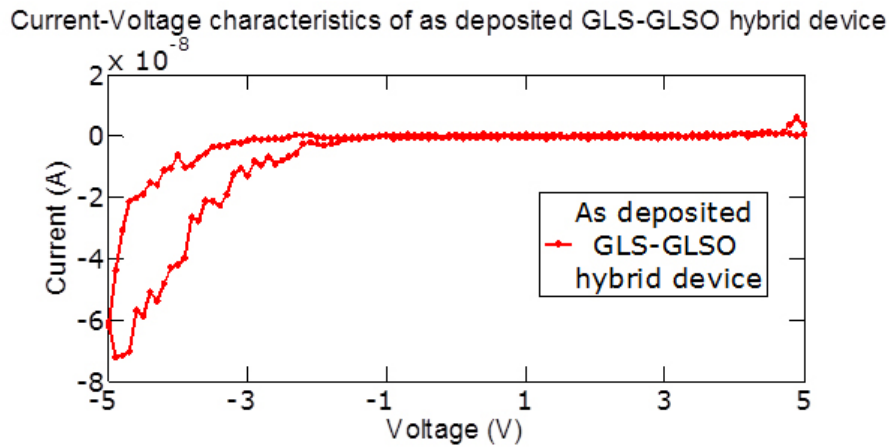
FIGURE B.1: I-V characteristics of the as deposited hybrid memristive device.
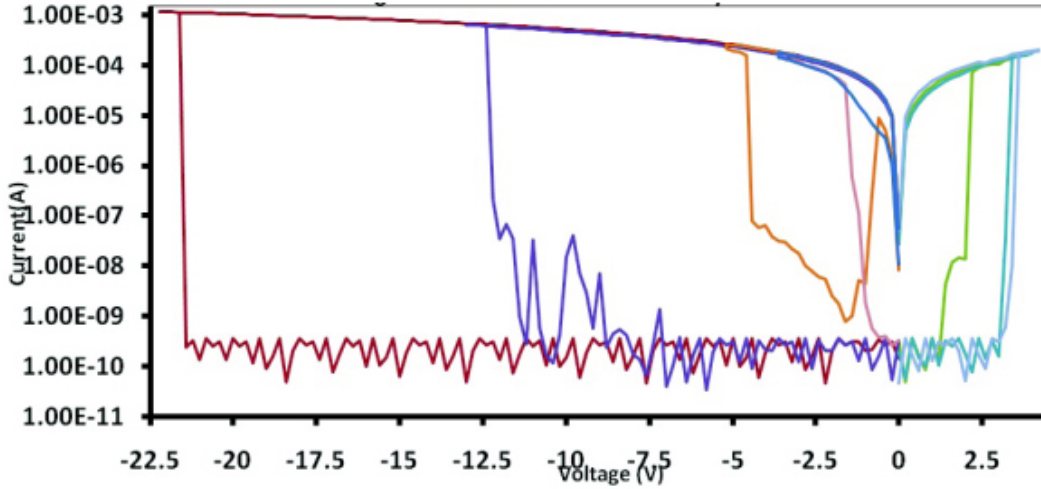
FIGURE B.2: Current-voltage characteristics of the device across different DC sweeps pre polarity Reset sweep

I-V characteristics of the device are shown in Figure B.4. The observation shows that the current-voltage characteristics of the device are reset to its original threshold voltage and R_{on}/R_{off} ratio. However, as the polarity set sweep was in the positive direction the threshold voltage is in the positive direction this time instead of the negative polarity as before.

When an AC signal is applied a "pinched hysteresis" characteristics is observed showing a high degree of resemblance to the typical memristor curve demonstrated in the literature (29). A numerical simulation was also carried out assuming this is an ideal memristor making use of oxygen diffusion within the semiconductor lattice given the
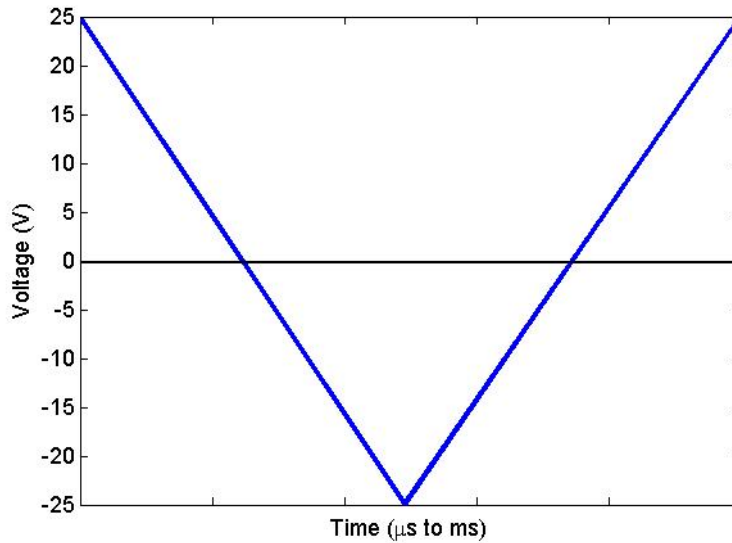
FIGURE B.3: Polarity reset sweep used to set the polarity of the current-voltage characteristics of the device
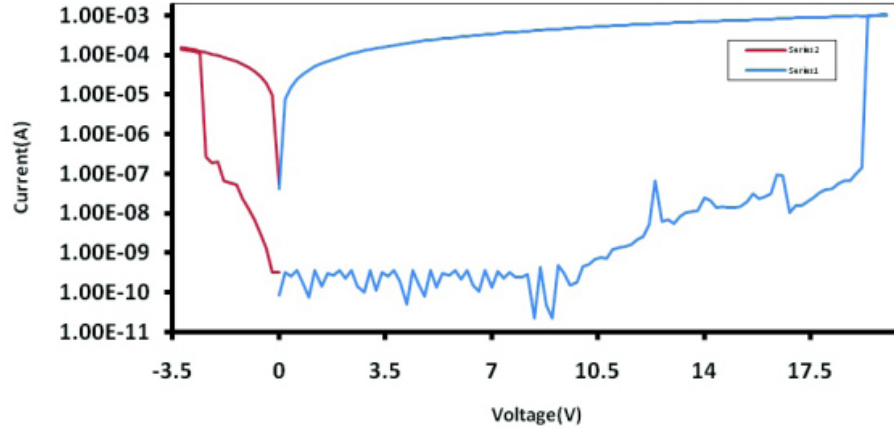
FIGURE B.4: The new IV characteristics following the Polarity reset sweep used to set the polarity of the current-voltage characteristics of the device
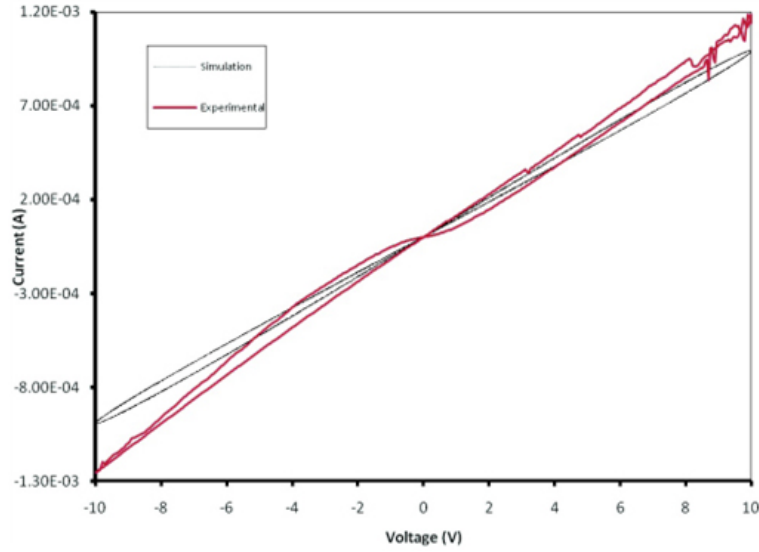
FIGURE B.5: The memristive behaviour of the system when in low resistance state and comparison with numerical simulations using basic memristor theory given the geometrical parameters of the device.

device geometries and thickness described previously one can obtain the characteristics of an ideal memristor and cross-reference this to our experimental results.

The I-V characteristics of the device along with the simulated behaviour of how a memristor would behave (based on memristor theory described in chapter 5) given the parameters of our device are shown in Figure B.5.

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