Development of Epitaxial Interdigitated Back Contact (IBC) Solar Cell as a Test Platform for Novel Antireflection and Light-trapping Schemes

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Abstract

The design of a test platform for novel antireflection and light trapping schemes, based on the interdigitated back contact (IBC) solar cell concept, is presented. Two enhancements to the front surface of the basic cell design are explored: Addition of a thin SiO_2 passivation layer between the thin film antireflective (AR) coating and incorporation of a front surface field via the formation of an n^+ floating emitter. PC2D simulations predict that power conversion efficiency values up to 17.4% can be achieved by incorporating these enhancements into the IBC cell design.

Introduction

The desire to increase solar cell efficiency and therefore drive down the cost-per-watt of PV has stimulated research into novel sub-wavelength scale antireflection (AR) and light trapping (LT) schemes including biomimetic 'moth-eye' structures [1], plasmonic metal nanoparticle arrays [2] and Mie resonator arrays [3]. The latter scheme has been shown to reduce the average reflectivity of silicon to as low as 1.3% over the 450-900nm range. This has led to the requirement of a solar cell test platform to facilitate the comparison of these new AR and LT methods with more traditional thin film and micron-scale texturing approaches. Since the front surface of the cell is free of any contacts, the interdigitated back contact (IBC) monocrystalline silicon solar cell design is well suited to fulfil this need [4].

IBC cells offer potentially higher efficiency compared with conventional solar cells. Complete elimination of the front contacts leads to a higher short circuit current due to the absence of shading losses and lower resistive losses. The front and back of the cell can be fully utilized for optical and electrical improvement, respectively. The cell design offers easier interconnection and increased packing density within a module [5]. Furthermore, the approach also improves aesthetics, increasing the likelihood of large scale adoption in building integrated PV. The concept has been used to manufacture large-area cells with efficiencies of more than 24% by Sun Power Maxeon cell [6].

In this paper, further steps towards the development of a planar Hot Wire Chemical Vapour Deposition (HWCVD) based IBC cell for testing novel AR and LT schemes against traditional thin film and micron-scale texturing are described. In the IBC solar cell design, most of the photo generation takes place near to the front of the cell. These light generated carriers can be easily lost by recombining at the front surface. Two enhancements to the front surface of the basic design are therefore investigated in this work: Addition of a thin SiO_2 passivation layer between the thin film AR coating and incorporation of a front surface field via the formation of an n^+ floating emitter.

Using experimental data from carrier lifetime, four point probe and reflectance measurements, PC1D and PC2D simulations are used to quantify the improvements to the design of the front surface and to predict the performance of the IBC solar cell.

Cell Design

The basic IBC cell design used in this work is presented in Figure 1 and an outline of the fabrication process flow is given in Figure 2.

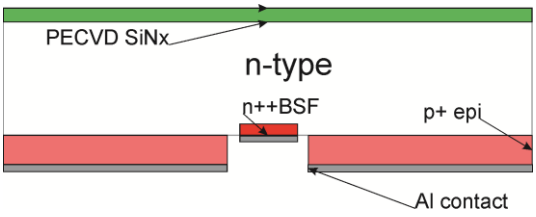

Figure 1: Schematic of the simple IBC cell designs for this study.

The process begins with cleaning of a silicon wafer (n-type, <100>, 1-10 Ω.cm). A photolithography and dry etch stage is then used to define the n-type contact pattern on the rear of the cell, through which the n^+ back

surface field (BSF) is formed by $POCl_3$ diffusion at $900^{O}C$. This is followed by deposition of an 85 nm thick silicon nitride AR layer by Plasma Enhanced CVD (PECVD). A second photolithography and dry etch stage is then used to define the p-type contacts. The epitaxial p^+ contacts are then fabricated by HWCVD deposition and lift-off. Finally, a third photolithography process followed by aluminium evaporation and lift-off forms the ohmic contacts to the n and p regions. The wafer is then diced to form 1 cm × 1 cm individual devices. The process listing includes the option of texturing the surface with a KOH etch after the initial wafer cleaning stage, however the results presented here are from the planar version of the device design.

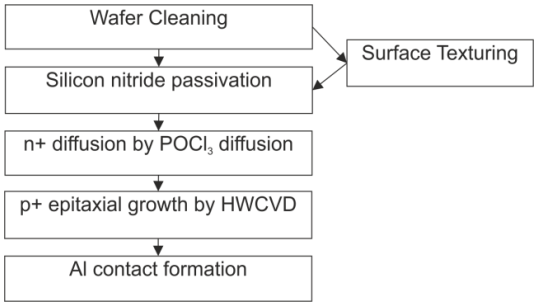

Figure 2: Process flow of IBC solar cell fabrication

Thin Film Coating Optimization

In order to optimize the coating design considering both antireflection and surface recombination reduction, an optical analysis was combined with an experimental investigation using a Sinton WCT-120 carrier lifetime characterization system, where the quasi steady state (QSS) measurement method was used for injection dependent lifetime measurement. In this measurement, a slowly decaying pulse of light is used and the effective lifetime is determined as a function of excess carrier density, Δn, using (1), where *G(t)* is the generation rate [7].

$$\tau_{eff} = \frac{\Delta n}{G(t)} \qquad (1)$$

Several materials were considered for front surface thin film coating including alumina (Al_2O_3), PECVD nitride, and also a combination of oxide and nitride (DLAR). The thin film coating was optimized by considering two factors: (1) ability to provide good passivation, characterised by a high carrier lifetime, and (2) ability to provide good AR ability, characterised by a low average reflectance, weighed to the AM1.5 spectrum (R_w). Table 1 shows the lifetime measured for the different passivation layers considered. The resulting optimized design consists of a 10 nm layer of thermally grown SiO_2 beneath a 85 nm layer of PECVD deposited SiN_X. This thin film coating exhibits a weighted average reflectance R_w, of 5% and a carrier lifetime of 182.4 µs when deposited on an n-type Si test wafer. This compares to an R_w of 33.5% and carrier lifetime of 6.5 µs on the untreated wafer (Figure 3).

Table 1: Measured carrier lifetimes of thin film materials deposited on silicon considered for passivation of IBC solar cell front surface.

Material	Lifetime (µs)
Bare silicon	6.5
4 nm Al_2O_3	91.4
30 nm PECVD SiN_X	60
10 nm SiO_2	86.3
10 nm SiO_2 beneath a 85 nm PECVD SiN_X	182.4

The improvement in lifetime when oxide and nitride layers are combined in a double layer is thought to be due to the enabling of two mechanisms that reduce surface recombination. Firstly, chemical passivation is provided by the thermal oxide layer that saturates dangling bonds at the surface. Secondly, fixed positive charges in the nitride as a result of non-stoichiometric growth repel minority carriers (holes) in the n-type material away from the surface. The hole concentration at the front surface is therefore lower, reducing recombination rate.

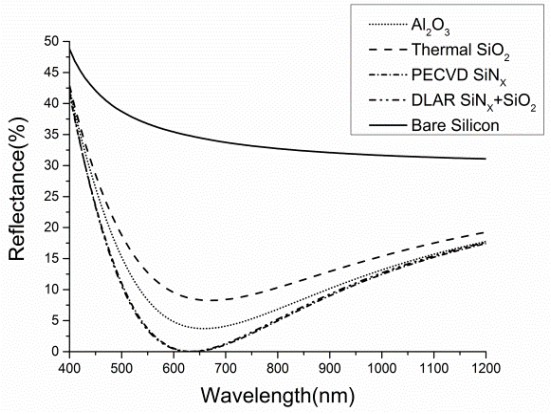

Figure 3: Simulated reflectance spectra for different thin film coatings on silicon (including bare silicon)

Floating Emitter Front surface field (FSF) Optimization

In addition to passivation provided by the thin film coating, formation of a FSF by incorporation of a floating emitter into the design is a well-known method to further reduce front surface recombination by repelling minority carriers from the surface [8]. A standard front contact c-Si solar cell was modelled in PC1D, firstly without a floating emitter and then with a floating emitter providing a sheet resistance of 150 Ω/sq. This value of sheet resistance was chosen from an optimization study on floating emitters for IBC cells reported in the literature [8]. The surface recombination velocity value was varied and the IV characteristics of the device were simulated. The results reveal that addition of a FSF decreases the sensitivity of the cell to the surface recombination velocity, as shown in Figure 4.

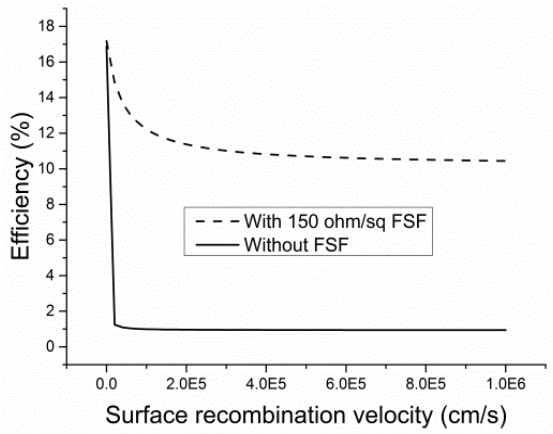

Figure 4: PC1D simulation results showing the variation of power conversion efficiency as a function of surface recombination velocity with and without a front surface field

The floating emitter clearly improves the device efficiency and so a process for forming a floating emitter using $POCl_3$ diffusion was developed for incorporation into the full cell fabrication flow illustrated in Figure 2. The floating emitter is formed by $POCl_3$ diffusion carried out at 750°C for 20 mins, followed by an anneal at 1000°C for 8 mins. The annealing process is combined with the thermal oxidation step to produce a floating emitter with a passivating 10 nm thick thermal oxide. The resulting measured carrier lifetime of the sample following this process was 370 µs, which is over twice the lifetime of the best sample from the thin film passivation study (Table 1). A further increase in lifetime may be possible with the addition of the PECVD nitride layer although this has yet to be tested.

To obtain a value for sheet resistance of the floating emitter to input into the device model, the thermal oxide was stripped and then a four point probe measurement was carried out. The resulting sheet resistance was 147 ohm/sq, which is close to the target value of 148 ohm/sq identified from the literature [9]. This value was used in a PC1D device model to obtain values for emitter saturation current (J_0) for input into the PC2D full cell IBC simulation.

Full cell simulation in PC2D

PC1D is limited to modelling cells in one dimension. Analysis of IBC cell designs involves effects in two dimensions and as such cannot by modelled using PC1D. Basore et al. thus developed PC2D, a circular reference solar cell device simulator in spreadsheet form that enables simulation of IBC and other complex cell designs [10]. PC2D was employed to simulate the IBC cell in this work, with input from experimental results, parameters from literature, and values from PC1D simulations. The input parameters used for the PC2D simulation are listed in Table 2.

Table 2: Simulation parameters for PC2D simulation

DEVICE PARAMETERS	VALUES
[a]**Device area**	1 cm^2
[a]**Base doping**	5×10^{14} cm^{-3}
[a]**Effective lifetime**	375 µs
[a]**Base Thickness**	275 µm
[a]**AR layer**	85 nm SiN_x + 10 nm SiO_2 DLAR
[b]**J_0 at metal contacts**	1.00×10^{-12} A/cm^2
[a]**J_0 at passivated surface**	1.00×10^{-14} A/cm^2
[c]**J_0 at passivated FSF**	4.00×10^{-16} A/cm^2
[a]**J_0 at p^+ region**	1.14×10^{-13} A/cm^2
[a]**J_0 at n^{++} region**	2.6×10^{-13} A/cm^2

[a] **Measured value**
[b] **Taken from literature**
[c] **From PC1D simulation using measured values**

The simulated I-V curve for the IBC cell design with the front surface improvements described in this study in comparison with IBC cell without FSF is presented in Figure 5. The simulated power conversion efficiency for optimized design is 17.4% compared to 14.6% for cell without a floating emitter. The simulated EQE spectrum of the optimized cell design with a FSF (Figure 6) shows values above 80% over the spectral range 450nm-1000nm. Good

performance of the device in the blue part of the spectrum indicates that front surface recombination has been effectively suppressed with the improvements to the design presented in this work. Fabrication of this optimized design is currently underway.

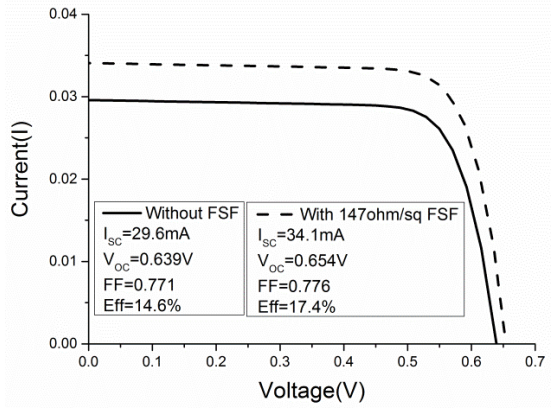

Figure 5: I-V curve simulated by PC2D

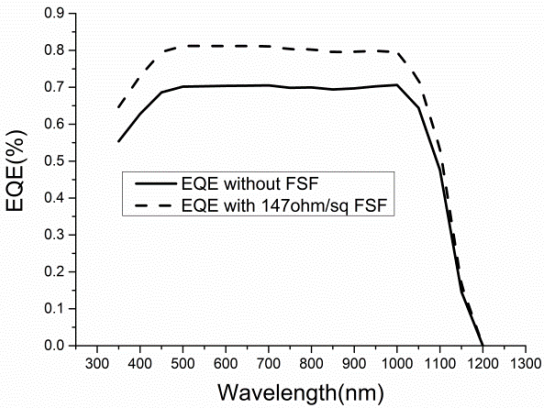

Figure 6: EQE of optimized IBC cell simulated by PC2D

Conclusions

A HWCVD-based epitaxial IBC solar cell for use as a test platform for novel antireflection and light trapping schemes is being developed. In this work, the optimization of the front surface is described. The thin film AR coating was optimized for both front surface reflection reduction and front surface recombination reduction, leading to a coating design consisting of 85 nm of silicon nitride on top of 10 nm of silicon dioxide. PC1D simulations reveal that addition of a floating emitter to create a FSF decreases the sensitivity of the IBC cell to surface recombination velocity. An experimental process for formation of a FSF using a $POCl_3$ diffusion was developed which incorporated a process to grow a thermal oxide. The carrier lifetime of the wafer with floating emitter and thermal oxide was measured to be 370 µs. This shows a large improvement compared to an untreated wafer which exhibited a lifetime of just 6.5 µs.

A PC2D model of an IBC cell with this improved front surface treatment predicts a power conversion efficiency of the IBC cell of 17.4% with FSF compared to 14.6% for the IBC cell without FSF. The next step is to fabricate a cell based on this optimized device design. If the reasonably high predicted efficiency can be achieved in practice, this would provide a good baseline device to be used as a test platform for investigating novel AR and LT schemes.

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