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Local charge trapping in conjugated polymers resolved by Scanning Kelvin Probe Microscopy

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ABSTRACT

The microstructure of conjugated polymers is heterogeneous on the length scale of individual polymer chains, but little is known about how this affects their electronic properties. Here we use Scanning Kelvin Probe Microscopy with resolution-enhancing carbon nanotube tips to study charge transport on a 100 nm scale in a chain-extended, semicrystalline conjugated polymer. We show that the disordered grain boundaries between crystalline domains constitute preferential charge trapping sites and lead to variations on a 100 nm scale of the carrier concentration under accumulation conditions.

KEYWORDS Conjugated polymers; Field-effect transistors; Scanning Probe Microscopy

The charge transport properties of conjugated polymer semiconductors continue to reveal interesting phenomena. Recent results have included the realization of high carrier mobilities approaching $1 \text{ cm}^2/\text{Vs}$ in semicrystalline films of poly(2,5-bis(3-alkylthiophen-2-yl)thieno(3,2-b)thiophene) (pBTTT)¹ and the observation of nonlinear, metallic transport at high carrier concentrations² which can be described in terms of a one-dimensional Luttinger liquid³. Charge transport is usually probed by electrical measurements over a length scale of several micrometers using field-effect transistor (FET) structures. However, the polymer microstructure varies on the length scale of individual polymer chains (10-100 nm)⁴, and the effect of such lateral heterogeneity on charge transport and electronic properties needs to be better understood. Nanoscale electrode structures have proved to be of limited use due to contact resistance effects.⁵ A closely related question, which is becoming of considerable technological importance as polymer FETs are being introduced into real world applications, is the question of charge trapping. Organic FETs exhibit a shift in threshold voltage during prolonged gate operation.⁶ This is attributed to population of long-lifetime trap states by the charges accumulated at the organic semiconductor - dielectric interface. Although in several materials systems the threshold voltage shift is of comparable magnitude than that of amorphous silicon (a-Si) thin film transistors, such operational degradation remains a concern because the microscopic understanding of charge traps in conjugated polymers remains very elusive.⁷ The complex, spatially non-uniform microstructure makes it difficult to identify specific trapping sites with measurements performed over micrometer length scales.

There is therefore a need for experimental techniques able to probe the electrical properties on a length scale of the polymer chain length. Scanning Kelvin Probe Microscopy (SKPM) can be used to measure lateral variations in the surface potential of organic electronic devices,⁸⁻¹⁰ but the spatial resolution of most SKPM setups is worse than 100 nm. This is because SKPM relies on an electrostatic interaction between the sample and a conducting atomic force microscopy (AFM) cantilever, which comprises significant contributions not just from the apex of the tip, but also from the body of the cantilever¹¹. In

this work we have used AFM tips with single-walled carbon nanotubes (CNTs) attached to the apex to reduce the capacitive coupling between the surface and the body of the cantilever and to improve the spatial resolution to better than 50 nm.

As a material system we selected pBTTT as it is not only one of the highest mobility semiconducting polymers, but also one of the most highly ordered systems due to interdigitation between polymer side chains¹². It forms two distinct liquid-crystalline mesophases upon annealing, a widely studied ‘terrace’ phase¹³ and a characteristic ‘ribbon’ phase induced by annealing at 260°C. In the latter the mobility is slightly lower, but the polymer chains are chain-extended and form regularly spaced crystalline ribbons with a width of 80 - 90 nm corresponding to the molecular chain length.¹⁴ In between ribbons the polymer chains are more disordered due to imperfect packing of chain ends arising from molecular polydispersity (inset of Fig. 1(b)). Here we investigate the influence of these well-identifiable grain boundaries on the trapping and transport of charges in the channel of an FET.

We used standard bottom-gate, top contact pBTTT FETs with gold source-drain electrodes on Si wafers with a 300 nm SiO₂ gate dielectric (channel length L = 20 μm, channel width W = 1 mm). An 80 nm pBTTT film was spin-coated from a 1,2-dichlorobenzene solution onto an unmodified SiO₂ surface. The FETs were well behaved with field-effect mobilities on the order of 0.03 cm²/Vs, comparable to those observed previously for the ribbon phase¹⁴. The frequency-modulated SKPM measurements were performed with a commercial Omicron variable-temperature AFM in ultrahigh vacuum (UHV). Previously, we achieved 100 mV surface potential and 100 nm lateral resolution with this system¹⁵ which was insufficient to resolve the 80 nm wide pBTTT ribbons. To improve spatial resolution single-walled CNTs were attached to the ends of commercial metal-coated AFM tips (Force modulation pointprobes, Nanoworld) using the “pick-up” method.¹⁶ Fig. 2(f) shows a scanning electron microscopy (SEM) image of a CNT modified tip. In addition, the potential resolution of the SKPM setup has also been improved by using a Nanonis OC-4 phase-locked loop for both the topography and potential

feedback loops. We now achieve spatial resolution better than 50 nm and lower noise potential measurements with a resolution of 10 mV.

We studied charge trapping by subjecting the device to a gate bias stress of $V_g = -80\text{V}$ for 60 minutes to fill deep trap states while the device was kept in the UHV SKPM chamber. During the stress the current decays by 55% (Fig. 1(a)) reflecting a pronounced negative threshold voltage shift associated with the trapping of about half of the gate induced charges. After the stress the gate voltage is turned off and the recovery of the device is monitored by pulsing the applied voltages periodically to measure the current. We observe an initial fast recovery to about 65% of the original current value in the first few minutes after turn off. Over the next 4 - 6 hours the current then further recovers to about 80% of its original value, which is very similar to the behavior reported for polythiophene.⁶

In SKPM measurements performed during the recovery (Fig. 1(b)) the presence of trapped charges manifests itself in that the spatially averaged surface potential V_s^{ave} after turn-off ($V_g = V_d = 0\text{V}$) is not close to 0V as one would expect if there were no charges remaining in the channel, but $V_s^{ave} \approx 8.5\text{V}$. This indicates that some 6×10^{11} positive charge carriers Q_t remain trapped in the channel ($Q_t = C_i V_s^{ave}$, where $C_i = 11 \text{ nF/cm}^2$ is the areal gate dielectric capacitance). A two-dimensional SKPM scan takes about 30 minutes, i.e., we cannot time-resolve accurately the fast detrapping process immediately after turn-off. As detrapping continues V_s^{ave} decays back to zero over a period of 6 hours comparable to the time scale over which the device current recovers. We have not yet investigated why the device current does not recover to its original value, but note that some irreversible device degradation unrelated to charge trapping has been observed in polythiophene FETs during prolonged bias stress.¹⁷

In AFM topographs the network of polymer ribbons can be clearly resolved (Figure 2(a)). In the corresponding surface potential map (Figure 2(b)) taken immediately after the gate bias stress there are well-defined regions in which the surface potential is more positive. These appear white with the chosen

color scale. They are directly correlated with the ribbon morphology of the film. In contrast, before the stress the potential landscape is smooth with little structure that does not correlate with the ribbon topography (Fig. 2(c) and (d)). This proves that the periodic surface potential contrast seen in Fig. 2(b) is only appearing after the bias stress, and is therefore directly related to the trapping of charges. Charge trapping does not occur homogeneously throughout the film, but there are well defined sites at which charges are trapped preferentially. Through analysis of single-line cross sections (Fig. 2(e)) we find that the positive peaks in the surface potential coincide with the troughs in the ribbon topography and the regions of more negative potential coincide with the peaks in the topography. Based on the analysis in Ref. ¹⁴ we assign the topography peaks to the ordered polymer ribbons and the troughs to the disordered grain boundaries. This implies that the trapped charges preferentially occupy the disordered grain boundary regions between the crystalline pBTTT ribbons.

The surface potential image taken 1 hour after device turn-off (Fig. 3(b)) still shows this distinct correlation with the topography, but during device recovery the amplitude of the surface potential variations correlated with the ribbon topography decays together with the average surface potential (Fig. 3(c)). After 5 – 6 hours the surface potential image exhibits no features correlated with the ribbon morphology and looks similar to that before the stress (Fig. 2(d)). To quantify the timescale of the decay we have evaluated Fourier transforms of surface potential line scans (such as Fig. 2(e)). The amplitude of the peak in reciprocal space corresponding to the ribbon periodicity decays on a similar time scale as the average surface potential (Fig. 1(b)). A similar conclusion is drawn from the analysis of histograms of surface potential images as a function of time during device recovery (Fig. 3(d)). 1 hour after removal of the stress the potential histogram exhibits two distinct peaks. Over the following 6 hours the two peaks merge and move to less positive potential values. We can associate the peak at more positive potential with charges trapped in intergrain regions with higher trapped charge density while the peak at less positive potential is due to a background of trapped charges for which we are unable to identify the structural origin. Whether this background is in fact due to the presence of other,

more uniformly distributed trap states not related to grain boundaries or whether it is a consequence of potential screening and limited spatial resolution is not known at present. In any case the results show that there is merely a higher density of trapped charges associated with the grain boundary regions, but the rate of detrapping, i.e., the trap energetics and kinetics, is similar for both distributions of trapped charges.

Finally, we discuss SKPM experiments in the on-state with a FET current flowing in response to a small source-drain voltage. If one could assume the charge carrier concentration induced by the gate voltage to be locally uniform, i.e., accurately screening the gate potential everywhere, one would expect a potential profile resembling a staircase with a small potential gradient in the presumably higher mobility / lower resistance, crystalline ribbons and a larger potential gradient in the lower mobility / higher resistance grain boundaries. This is not what we observe. In the potential profiles (Fig. 4) well defined positive potential humps are superimposed on top of an average potential gradient due to the applied source-drain bias. The positive potential humps coincide again with the disordered grain boundaries in between ordered ribbons. This is clear evidence that the hole carrier density in the channel during operation is in fact not uniform on a 100 nm scale, but charges moving in the channel appear to get “stuck” and “pile-up” in the disordered grain boundaries. This behaviour is fully consistent with the observation of preferential charge trapping in the grain boundaries described above. In fact, in the potential profile acquired at $V_d = 0$ V of Fig. 4, which was taken at the end of this voltage sequence, we can see a similar potential contrast due to a non-uniform charge distribution in the channel. Some of these charges would remain trapped in the channel if the gate voltage was switched off at this stage and would produce the trapped charge contrast discussed above. The positive potential humps are primarily a consequence of the gate bias stress, not the current flow. They are also observed when imaging the channel during gate bias stress without applied source drain voltage (data not shown).

Our results raise the intriguing question about the microscopic nature of such grain boundary related trap states. The enhanced charge trapping could be due to specific structural traps caused by the increased disorder in the grain boundaries. Yang et al.¹⁸ have used density functional theory calculations to investigate the effect of disorder on the electronic density of states of the highest

occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) states of clusters of poly-phenylenevinylene (PPV) oligomers. For PPV oligomers configurations with intramolecular distortions in bond angles and bond lengths were found to lower both HOMO and LUMO energies while intramolecular cis-configurations in the vinylene linkages were found to symmetrically reduce the HOMO-LUMO gap. Such intramolecular disorder primarily leads to a broadening of the HOMO states, but not to creation of hole traps. On the other hand intermolecular electronic interactions were found to push both HOMO and LUMO states to higher energy and thus create hole traps. However, we cannot exclude the influence of extrinsic impurities. The observed trap states could also be due to grain boundaries constituting a preferred ingress pathway for chemical contaminants such as oxygen or water or such impurities being expelled from the crystalline regions, i.e., the trap state could be associated with a chemical impurity⁷. We note that our experiments were performed after several days in UHV where we would expect most volatile, not chemically bonded impurities such as water to be removed from the film.¹⁹ An alternative explanation might be that the different electronic structure in the grain boundary region is not directly responsible for the trapping of charge, but causes the rate of injection into an otherwise homogeneously distributed trap state at the SiO₂ interface to be higher than that in the crystalline ribbons.

In any case our results show unambiguously that the disordered grain boundary regions constitute preferential charge trapping sites and lead to significant lateral non-uniformity on a 100 nm length scale of the induced carrier concentration under accumulation conditions. For an in-depth understanding of the charge transport properties of high-mobility, semicrystalline polymers it is essential to take these spatial variations in the electronic structure on a 100 nm scale into account.

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FIGURE CAPTIONS

Figure 1 (a) Normalized drain current of ribbon phase pBTTT FET during and after 1 hour continuous gate bias stress at gate voltage $V_g = -80V$, drain voltage $V_d = -5V$. The device is turned off at time $t = 0$ hours, after which the current recovery is monitored periodically by pulsed current measurement at the same voltage conditions. The molecular structure of pBTTT and the device architecture with the source (S), drain (D) and gate (G) electrodes are shown as insets. b) Average SKPM surface potential as a function of time after the stress. The dotted line indicates the surface potential measured before the stress. The red points show the amplitude of the surface potential variations associated with the ribbon phase as determined from FFT of potential line scans. The inset shows a schematic diagram of the pBTTT ribbon phase. The polymer chains are drawn as red lines, and the transition regions between the chain-extended crystalline ribbons and the grain boundaries are indicated by dashed blue lines.

Figure 2 a) AFM topograph of an 80nm thick ‘ribbon phase’ pBTTT film. b) Corresponding surface potential image after 1 hour stress at $V_g = -80V$; c&d) Topography and surface potential of an unstressed pBTTT device. e) Topography (black) and potential (red) linescans of a stressed device; f) SEM image of a metal coated AFM cantilever with a single walled CNT attached.

Figure 3 Topography (a) and corresponding surface potential images associated taken 1 hour (b) and 3 hours (c) after a 1 hour stress at $V_g = -80V$. Images are not corrected for lateral drift. d) Histograms of the surface potential distribution taken from SKPM images as a function of recovery time.

Figure 4 Surface topography line scan (top) and surface potential profiles along the FET channel during operation at $V_g = -30V$ with different values of V_d .

FIGURES

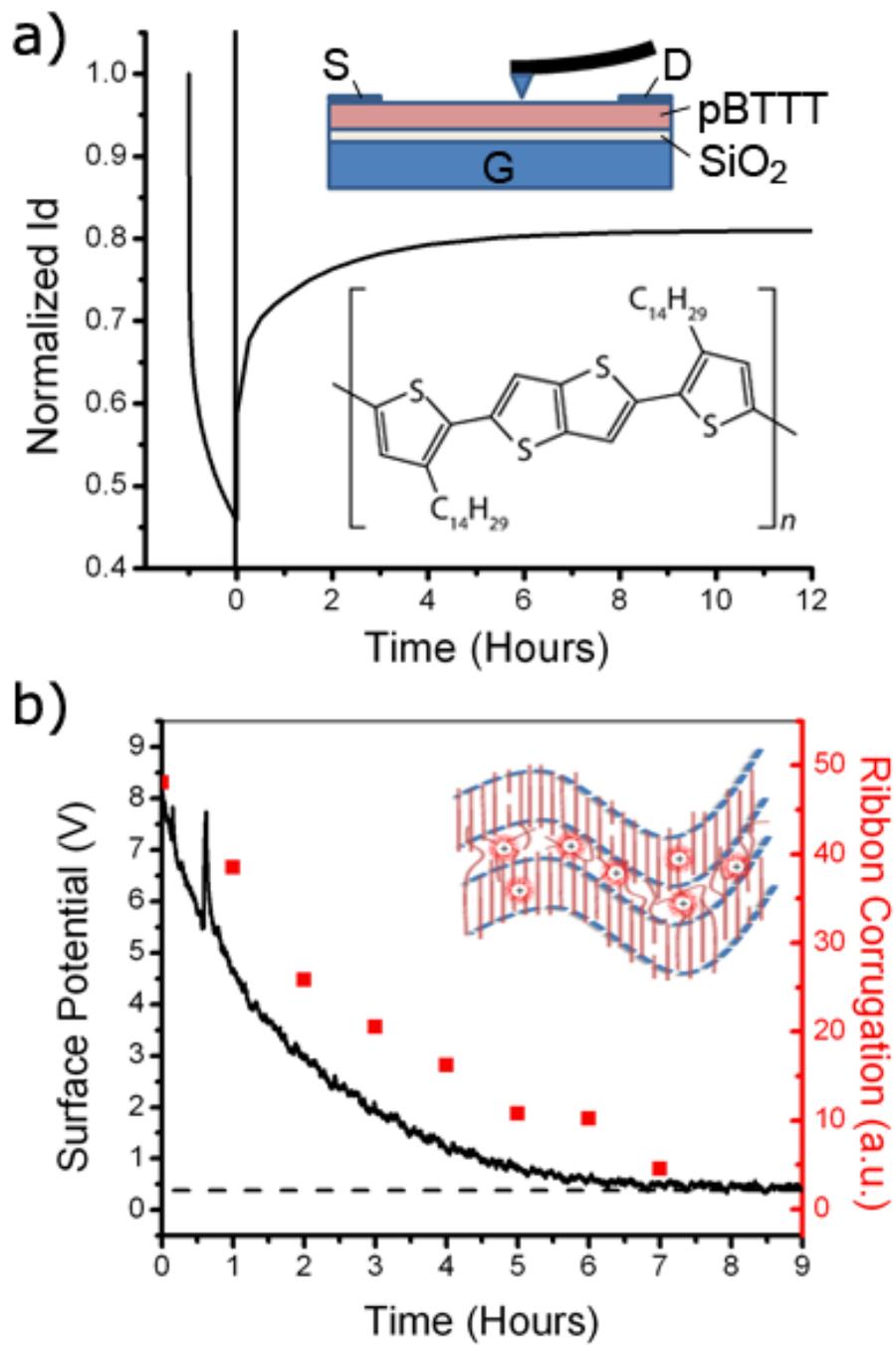


Figure 1

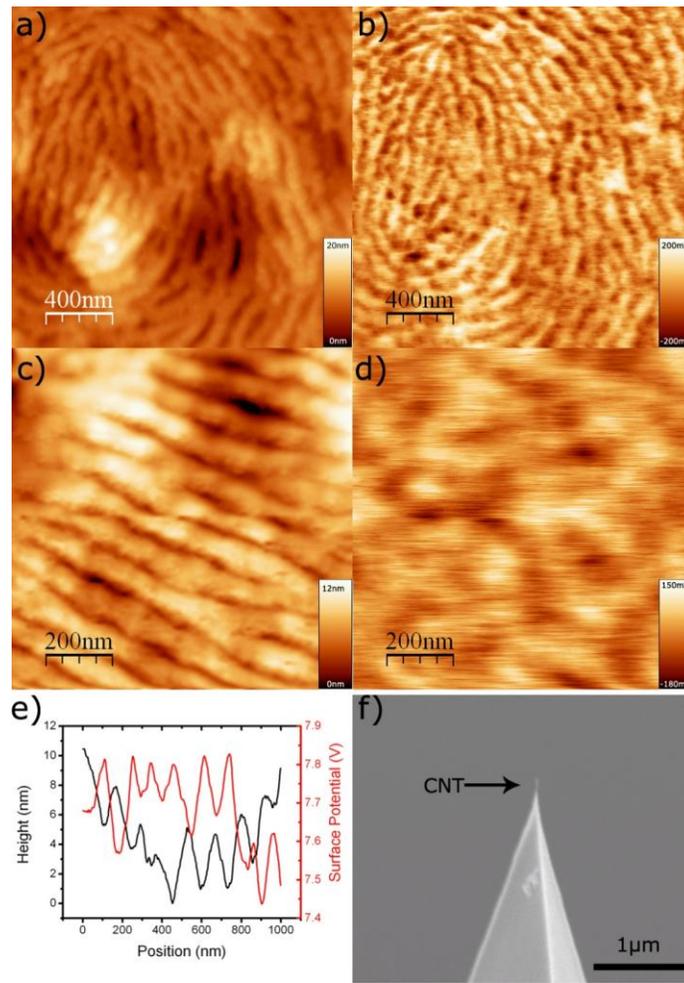


Figure 2

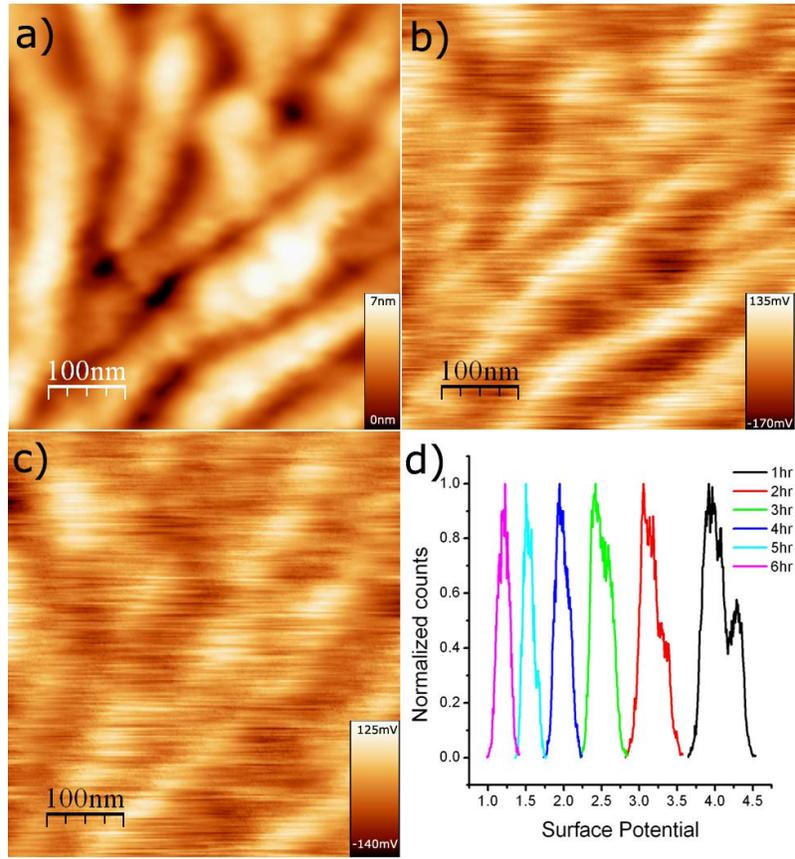


Figure 3

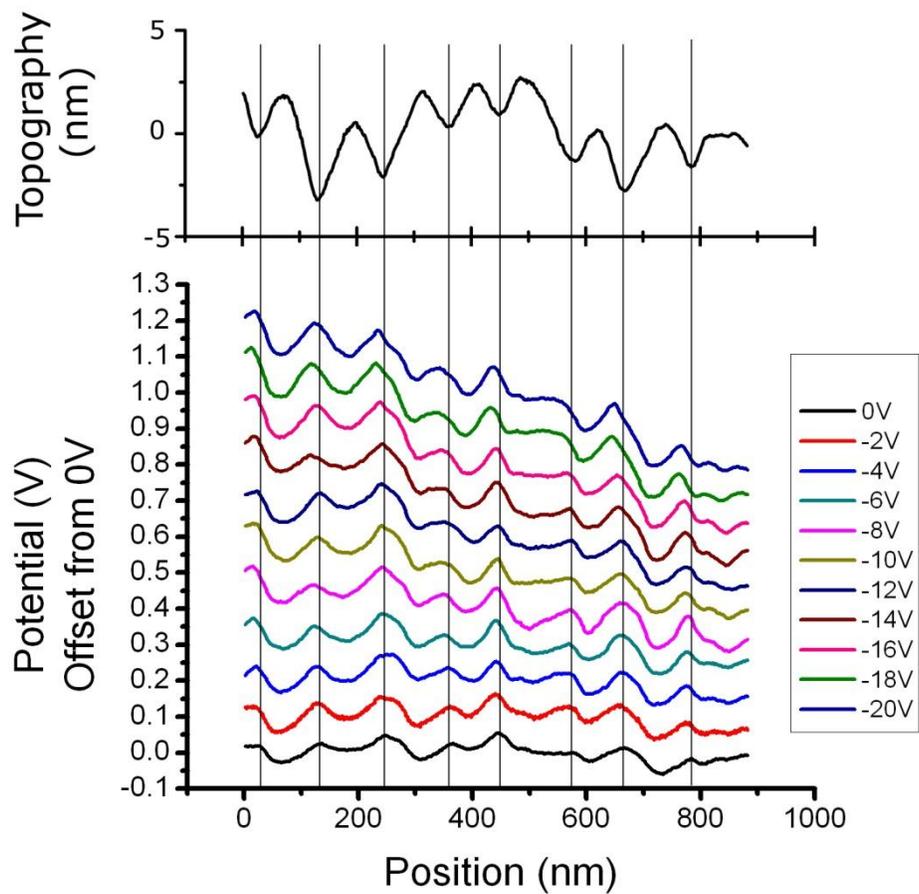


Figure 4

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