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Development of a Spring-Less RF MEMS Switch
by
Kian Shen KIANG

Thesis for the degree of Doctor of Philosophy
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ABSTRACT

FACULTY OF PHYSICAL AND APPLIED SCIENCE

SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

Doctor of Philosophy

DEVELOPMENT OF A SPRING-LESS RF MEMS SWITCH

by Kian Shen KIANG

This thesis reports on the development of a novel 77GHz low loss MEMS switch with a mechanically unrestrained armature, over a RF transmitting coplanar waveguide. Electrostatic actuation is used during the switching operation. The attractive force from the electrostatic field is generated by a pair of the actuation electrodes on both sides of the armature, depending on the direction of the movement.

A Simulink model is employed to simulate the mechanical response of the switching armature. Different damping models are deployed into the Simulink model, yielding different actuation time for the switch. This model is also employed to design the dimensions of the MEMS switch in the mechanical domain. The effect of Van der Waal force between the dielectric layer and designed armature is also discussed.

An electrical model of the RF MEMS switch is represented using lumped RLC components and characteristic impedance of the transmission line. The relationship between the electrical model and the scattering parameters is explained with the effects of the individual component on the S-Parameter being studied. Electromagnetic simulations have shown that the designed switch has potential of being employed in automotive collision avoidance system or in Doppler radar application. The proposed design is also capable of operating in lower frequency bands after some tuning, through different armature design.

A clean room fabrication flow is described as part of the development process of this novel switch. This is based on two Pyrex wafers and a SOI wafer utilising a double bonding and DRIE processes. RF characterisation of the coplanar waveguide and the micron-scale prototype at DOWN state is also discussed.

An alternative rapid prototyping technique based on high-frequency PCB and microscopic glass slide has been developed. This process is cheaper and requires shorter turnover time as compared to the clean room prototype. Electromechanical and S-Parameter measurements of the rapid prototype device are reported. These results are verified through simulations. The minimum actuation voltage of the prototype is 93V, with a rise and fall time of 165ms and 180ms. Switching is possible for frequencies from 2.8-5.5GHz and 6.6-10GHz, with the optimum frequency at 3.3GHz and 6.9GHz. The insertion loss and isolation of the prototype are -26.5dB and -38.5dB at 6.9GHz respectively. Although this is far from the state of the art for RF MEMS switches, it nevertheless proves the fundamental concept of a MEMS switch with an unrestrained armature by a prototype realised using a rapid prototype methodology.

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List of Symbols

A	cross sectional area of the armature
A_{ap}	total area of the actuation pad
A_{arm}	area of the armature
A_c	contact areas between armature and contacts the signal line
$A_{contact}$	total contact area between the armature and dielectric layer
A_r	contact areas between armature and contacts the ground line
α	attenuation of the transmission line
α_c	attenuation constant due to conductor loss
α_d	attenuation constant due to substrate loss
b	damping coefficient
c	speed of light
C_{air}	capacitance in absence of the substrate per unit length
C_{cpw}	capacitance of the transmission line per unit length
C_d	down state capacitance
C_{down_rou}	down state capacitance considering the effect of surface roughness
C_{ratio}	capacitance ratio
C_s	switching capacitance of the armature
C_u	up state capacitance
η	factor for the average damping pressure in a cell caused by air flow
D	distance between the contact surfaces of the two materials
$\epsilon_1, \epsilon_2, \epsilon_r$	dielectric constant of the materials
ϵ_0	permittivity of free space
f	frequency of the RF signal
F	electrostatic forces between the bottom electrode and the armature
F^+	electrostatic forces between the top electrode and the armature
F_{act}	electrostatic actuation force
$F_{contact}$	surface adhesion force
F_{damp}	damping force
$F_{electrostatic}$	electrostatic actuation force
F_{ext}	external applied inertial force
F_{mg}	gravitation force acting on the armature.
F_{mg}	gravitational force acting on the armature
f_o	LC series resonating frequency

g	earth gravity
G	width of the signal line
G_f	earth's gravity
g_o	initial capacitive gap
h_{sub}	substrate thickness
H_{vdW123}	hamaker constant
I	ionization potential
k	spring constant
k	spring constant of the MEMS armature.
K_n	Knudsen number,
k_z	mechanical spring constant
l	characteristic length
L	length of the conducting path
l_a	actuation electrode length
l_m	length of armature
L_b	inductance of the armature
λ_o	free space wavelength
λ_o	mean free path of the air molecules at atmospheric pressure
m	mass of the armature
v_{ph}	phase velocity
μ	absolute magnetic permeability
μ	mean free path of the air molecules at atmospheric pressure
μ_{eff}	pressure dependent effective viscosity
n_1, n_2	refractive index of materials
p	ambient pressure
P_a	atmospheric pressure
Q_o	nominal small displacement quality factor
R_b	resistance of the armature
r_c	pitch between adjacent holes
r_o	radius of the perforated hole
R_c	resistance of the centre signal line
R_g	resistance of the ground plane
ρ	density of material
ρ	resistivity of the material
S_{11}	magnitude of the return loss
S_{21}	magnitude of the isolation and insertion loss
σ	electrical conductivity of the material

σ	squeeze number
$T_{actuate}$	switch-on time
$\tan\delta$	dielectric tangent loss of the substrate
t_d	thickness of the dielectric material
t_m	armature thickness
$T_{release}$	switch-off time
V_{act}	actuation voltage
$V_{act(min)}$	minimum actuation voltage
V_b	bottom electrode voltage
V_{Pin}	pull-in voltage
V_t	top electrode voltage
W	slot width
w_m	width of armature
ω	angular frequency of the RF signal
ω_o	resonating frequency of the armature
x	displacement of the armature
Z_b	impedance of the armature
Z_o	characteristic impedance of the transmission line
z_o	gap between the armature and the electrodes at nominal position

List of Abbreviations

AC	Alternating Current
ADS	Advanced Design System
ALD	Atomic Layer Deposition
BAW	Bulk Acoustic Wave
CB-CPW	Conductor Back Coplanar Waveguide
CBFW-CPW	Conductor Back Coplanar Waveguide With Finite Width Ground Plane
CD	Constant Damping
CMOS	Complementary Metal-Oxide-Semiconductor
CPD	Critical Point Drying
CPW	Coplanar Waveguide
DC	Direct Current
DFR	Dry Film Resist
DRIE	Deep Reactive Ion Etching
DUT	Device Under Test
DUV	Deep Ultraviolet
FNA	Fuming Nitric Acid
FW-CPW	Coplanar waveguide with finite width ground plane
GSG	Ground-Signal-Ground
IC	Integrated Circuits
ICP-RIE	Inductively Coupled Plasma Reactive-Ion Etching
MEMS	Micro Electro Mechanical System
MIM	Metal-Insulator-Metal
PCB	Printed Circuit Board
PECVD	Plasma-Enhanced Chemical Vapour Deposition
Q factor	Quality Factor
RF	Radio Frequency
RLC	Resistor-Inductor-Capacitor
SMA	Sub Miniature version A
SOI	Silicon On Insulator
S-Parameter	Scattering Parameter
STS	Symmetric Toggle Switch
STS	Surface Technology Systems

TEM	Transverse Electromagnetic Mode
UV	Ultraviolet
VD-NP	Variable Damping without Considering Perforated Holes
VD-P	Variable Damping with Perforated Holes

Declaration of Authorship

I, KIAN SHEN KIANG declare that this thesis and the work presented in it are my own and has been generated by me as the result of my own original research.

Development of a Spring-Less RF MEMS Switch

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;
2. Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
3. Where I have consulted the published work of others, this is always clearly attributed;
4. Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
5. I have acknowledged all main sources of help;
6. Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
7. Either none of this work has been published before submission, or parts of this work have been published as: [please list references below]:

Journal Publication

1. Kiang, K.S., Houlihan, R., Gindila, M., Damrongsak, B. and Kraft, M. Design and simulation of a spring-less micro switch. *Electronics World*, Vol. 112, Iss.1844, pp. 30-34, 2006.

Conference Publication

1. Kiang, K.S., Chong, H. M. C. and Kraft, M. A Novel Low Cost Spring-Less RF MEMS Switch Prototype. *Proc. Eurosensors XXIV Conference*, Linz, Austria, Sept. 2010.
2. K. S. Kiang, H. M. H. Chong, C. J. Hwang, L. B. Lok, K. Elgaid And M. Kraft, Development of a low actuation voltage RF MEMS switch. *Proc. Eurosensors XXII Conference*, pp. 1462-1465, Dresden, Germany, Sept. 2008.

3. Kiang, K.S. and Kraft, M. Development of a low voltage MEMS switch for RF applications. Proc. MME 2006 Conference, pp. 105-108, UK, Sept. 2006

Signed:

Date: 21ST JANUARY 2011

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Chapter 1

Introduction

The overall Micro Electro Mechanical System (MEMS) market value was approximately US\$12 billion in 2004 [1] with more than 70% of the market shares belonging to the read/write heads and the inkjet heads. In a market forecast [2] published in 2007, the overall market was predicted to grow from US\$6.8billion in 2006 to approximately US\$11billion in 2011 without the consideration of read/write heads. The forecast [3] was later revised in 2009 with the considerations of the global financial downturn. The size of the market as illustrated in Figure 1.1 remained stable from 2007 to 2009 and the size of the Radio Frequency (RF) MEMS sector is expected to double when the economy recovers.

The majority of the market on RF MEMS are for Bulk Acoustic Wave (BAW) devices [4]. In 2001, a duplexer made commercial debut by Agilent, was costing US\$1,000. Since then, the price has decreased significantly in view of a mass production due to strong demand. At present, a similar duplexer is selling at only US\$2 each, thus becoming an attractive alternative to the ceramic counterparts.

RF MEMS switches can be used in many applications, such as phase array antenna/radar [5-7], portable wireless systems [8], switching networks [9], satellite communication systems [10] and tunable filters [11]. These applications can be grouped into four main categories namely aerospace and defence, test and instrumentation, telecom infrastructure and mobile phones. The market value for RF MEMS switches was US\$6 million in 2006 and is expected to increase to US\$210 million in 2011 [12]. The

forecasted market value for each category can be found in Figure 1.2, with demand in test and instrumentation leading the pack.

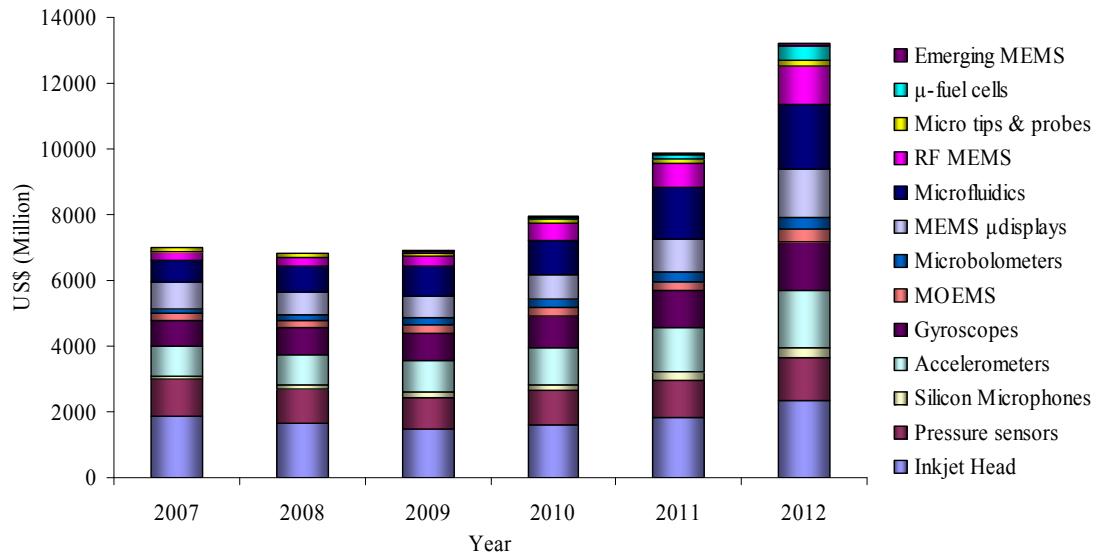


Figure 1.1: Turnover forecast for MEMS market with breakdown into different categories of product from 2007-12 as given in [3].

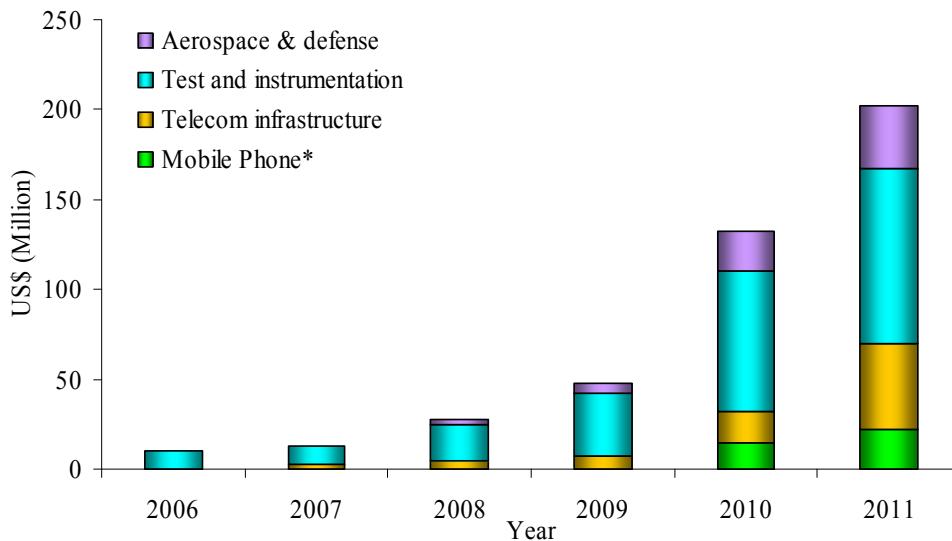


Figure 1.2: Turnover forecast for RF MEMS market with breakdown into different categories of product from 2006-11 as given in [12].

Although there are several commercial manufacturers of RF MEMS switches, they are generally not available for sale as a stand alone product. Advantest is one of such

companies who employ the RF MEMS switches into the company's automated test equipment. Omron, Wispry and Radant MEMS are the very few companies which are selling commercial RF MEMS switches as a product, as illustrated in Figure 1.3. The selling price varies from US\$25-US\$100 per unit depending on the specifications and volumes [12]. Therefore, implementation of RF MEMS switches in every mobile phone is still not realisable in the foreseeable future. The main obstacles preventing such implementation are the complex fabrication and packaging processes, control voltages, switching speed and manufacturing costs of the device [13]. A selected list of commercially available RF MEMS switch is tabulated in Table 1.

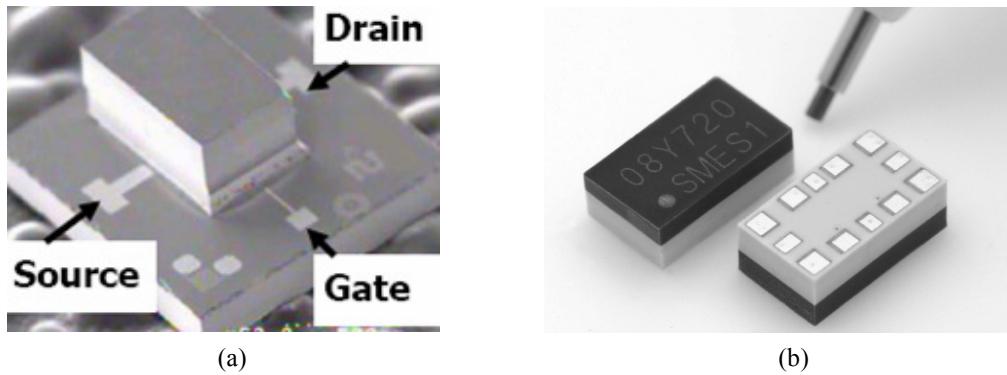


Figure 1.3: Commercial RF MEMS switch from (a) Radant MEMS [14] (b) Omron 2SMES-01 [15].

1.1 Motivation

The main objective for this work is to design a MEMS switch with an unrestrained armature for RF applications, which uses an electrostatic force to actuate the armature of the switch. The proposed design aims to introduce a novel MEMS switch that theoretically uses a smaller actuation voltage than conventional RF MEMS switches, where the typical actuation (pull in) voltage ranges from 20V to 100V. Switches reported with the low actuation voltage of 5V-15V require a complex mechanical suspension system, which makes it difficult to design and fabricate [16-19]. This novel design aims to ease the design process while mitigating the need for high voltage.

Another issue with existing RF MEMS switches is that low actuation voltage designs are often slow in switching. The new design has the potential to overcome this limitation, resulting in a faster switching response time. The packaging of the device under vacuum condition, if employed, would enhance the mechanical response of the switch. The electrostatic force used to actuate the armature will just need to overcome the earth's gravity and the inertia force of the device.

A low actuation voltage can also increase the reliability of the RF MEMS switch. High actuation voltages of 40V-80V have been used in many designs resulting in higher probability of stiction due to dielectric charging. The high electric fields formed across the dielectric due to the high actuation voltage, cause the dielectric to charge up or accumulate charges within the layer. The proposed low voltage design reduces the risk of this problem, so as to increase the functional life span of the device.

The proposed design also mitigates the built-up of intrinsic residual stress during the fabrication of the switch. Contrast to the conventional MEMS switches fabricated on a single wafer, the proposed design is fabricated on three different wafers before encapsulating them together. A scaled up rapid prototype switch, based on a simplified fabrication process and used as a proof of concept, is also introduced. This will allow scaling down into the encapsulated design in the future.

The high capacitive ratio of the design gives a relatively good RF performance. The novel design also provides a possibility of using conventional IC package methods, for example, glass-to-glass anodic bonding to resolve the high cost in packaging the device.

The state of art low actuation voltage RF MEMS switches, as tabulated in Table 4, shows that most switches operate at hundreds of microseconds with insertion loss less than -1dB and with isolation no better than -55dB. The proposed switch design should perform similar if not better than conventional designs be designs. The aim of the proposed switch should operate with an actuation voltage of <3.5V and an actuation and release time of less than 300 μ s and 200 μ s respectively. The proposed insertion loss should be less than -1dB and isolation better than -40dB at its electrical resonance.

1.2 Thesis Outline

Chapter 2 gives a general overview of MEMS technology. The basic operating principle of the RF MEMS switch is reviewed. Descriptions of a series contact switch and a capacitive shunt switch will be detailed. In addition, the performance differences between semiconductor switches and MEMS switches are discussed. In the last part of this chapter, recent researches and reliability issues of RF MEMS switches are summarized.

Chapter 3 presents the concept and design of the proposed RF MEMS switch. The theory of the electrostatic actuation of a mechanically unrestrained armature is discussed. It is not possible to implement the electrostatic actuation mechanism for a mechanically unrestrained armature, using a single top and bottom electrode configuration. The problem is addressed by implementing two pairs of the electrodes, one pair on the each side of the armature. The dimensions of the switch parameters are optimised based on the theoretical actuation voltage and the switching time of the switch. The surface adhesive force which affects the armature on the minimum actuation voltage is also reported. The chapter also documents the MATLAB/Simulink implementation of a one-dimensional electromechanical model of MEMS switch. It also highlights the different damping models and their impacts on the actuation time of the switch.

Chapter 4 discusses the radio frequency aspect of the MEMS switch, with the performance represented in scattering parameters. The transmission line and RF MEMS switch are represented as a lumped Resistor-Inductor-Capacitor (RLC) circuit. The effect of each component is individually varied and examined. These factors are then modelled in electromagnetic simulation software to derive the RF performance of the switch.

Chapter 5 proposes a clean room fabrication process for the proposed MEMS switch. The clean room fabrication prototype design is based on two Pyrex wafers and a silicon on isolation wafer, where the Pyrex wafers sandwich the silicon wafer. They are bonded together using anodic bonding and UV adhesive bonding processes. The fabrication issues encountered are discussed and solutions are presented. The chapter also describes a rapid prototyping process, which utilizes little clean room equipment and uses

cheap substrate materials, e.g. prototype circuit board and microscope glass slide. The selection process of dielectric material is also presented.

Chapter 6 reports on the RF characteristic of the designed coplanar waveguide as well as the S-Parameter of the proposed switch. The UP and DOWN state of the proposed switch are simulated by moving the armature away or in contact with the dielectric layer on the transmission line. During the UP state with a large capacitive gap, the RF MEMS switch is assumed to be a transmission line without an armature. Therefore, when the armature is manually manipulated by placing or removing the armature across the transmission line, the S-Parameters of the RF MEMS switch can be measured. The chapter also reports on the RF characteristic and the mechanical response of the rapid prototype device.

Chapter 7 concludes the present work and recommends potential areas for future research and development.

Company	Type of Switch	Actuation Mechanism	Actuation Voltage (V)	Insertion loss (dB)	Isolation (dB)	Operating RF Frequency	Switching Speed (μs)
Radant MEMS [14]	SPST	Electrostatic	90 V	< 0.24	>11	DC to 12 GHz	5
Radant MEMS [20]	SPDT	Electrostatic	90 V	< 0.8	>13	DC to 40 GHz	5
Omron [15]	SPDT	Electrostatic	34V	1.0dB @10GHz	30dB @10GHz	1 to 10 GHz	-

Table 1: A compilation of commercially available RF MEMS switches.

Chapter 2

Background and Literature Review

2.1 MEMS: A General Overview

The miniaturisation of integrated circuits (IC) devices motivates researchers to develop new ways to integrate and downsize discrete active components constantly. Technological barriers have been encountered by researchers in the device reduction to further integrated passive components into ICs. Integrated passive components are not able to provide high quality characteristics which are offered by their discrete counterparts.

The development of micromachining enables the fabrication of mechanical structures at the micrometer or millimetres scale. This fabrication technology, also known as Micro Electro Mechanical System (MEMS), uses advanced lithography and etching techniques which are similar to those of the IC fabrication technology. Leverage with existing IC technology gives MEMS the advantages of batch fabrication, device-to-device consistency and low cost of manufacturing.

MEMS uses materials similar to that of IC technology, its mechanical components can therefore be monolithically integrated with the electronics. The advantage is the possibility of fabricating integrated circuit and MEMS devices on a single die, which allows them to interact with other physical devices at the outside world. Studies shows that silicon is a suitable material for numerous applications including radio frequency (RF), optical, physical sensors and actuators among many others [21-23].

In the areas of RF MEMS, there are several devices under research; these are switches, high Quality (Q) factor inductors, tunable capacitors, high-Q mechanical resonators and filters.

The RF MEMS devices have better performances in terms of a lower power consumption, lower losses, higher linearity and higher Q factor compared to the existing semiconductor components. They have similar performance to the discrete RF components and can be integrated directly into active circuits on semiconductor wafers.

The subsequent topics of this chapter will focus on previous research carried out on RF MEMS switches.

2.2 RF MEMS Switches

A RF MEMS switch is a micro-scaled mechanical switch used in communication devices. It comprises of a movable switching membrane, which is called the armature, is suspended over a transmission line. The armature moves during the switching operation to change the state of the circuit.

MEMS switches can be designed using different actuation mechanism, type of contact, position of the armature, driving and circuit configuration. Table 2 tabulates the different variation in each category for a MEMS switch design.

Table 2: shows the difference variation in each category of a MEMS switch.

Actuation mechanism	Types of contact	Position of armature	Driving configuration	Circuit configuration
<ul style="list-style-type: none"> • Electrostatic • Electro-magnetic • Electro-thermal • Piezoelectric 	<ul style="list-style-type: none"> • Ohmic • Capacitive 	<ul style="list-style-type: none"> • Inline • Broadside 	<ul style="list-style-type: none"> • Switch • Relay 	<ul style="list-style-type: none"> • Series • Shunt

The majority of the MEMS switches under research uses electrostatic actuation [16-18, 24]. This actuation mechanism has negligible power consumption, as there is very little current flow during switching operation, and only requires a small area for the

actuation electrodes, compared to its electromagnetic [25, 26] and electrothermal [27-30] counterparts. For piezoelectric actuator [31-34], the development is hindered by the complexity and difficulty of the fabrication.

2.2.1 RF MEMS Series Contact Switch

Series contact MEMS switches comprise of a conductive beam which is suspended over two sections of a transmission line. The switch creates a closed circuit when the conductive beam is pulled down by an actuation force. The conductive beam connects the two sections of the transmission line. This allows the RF signal to pass through the circuit. The switch is in the OFF state when the actuation force is removed and the conductive beam returns to the original height. Figure 2.1 shows a schematic illustration of a series contact switch.

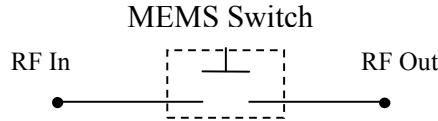


Figure 2.1: A schematic illustration of a series DC contact switch.

2.2.2 RF MEMS Shunt Capacitive Switch

The capacitive shunt RF MEMS switches as illustrated in Figure 2.2, comprises of a dielectric between the armature and transmission line. During the OFF state, the armature is suspended over the transmission line. The RF signals pass through the transmission line freely. The switch capacitance is usually around 10-100fF, which translates to a high impedance path to ground through the beam. In the ON state, a DC actuation voltage is exerted. The DC biased force pulls the armature towards the transmission line, resulting in a high switch capacitance. The high switch capacitance, usually around 1-10pF, causes a low impedance path from the transmission to the ground plane.

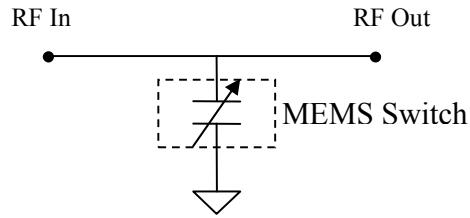


Figure 2.2: A schematic illustration of a capacitive shunt switch configuration.

2.3 Comparison of Semiconductor Switch and RF MEMS Switch

The commercial RF switches in use are usually p-i-n diodes or field effect transistors switches. MEMS switches, offering two distinct advantages in comparison with semiconductor switches, have an enhanced RF performance and almost zero-power consumption.

Despite of the abovementioned advantages, RF MEMS switches have not usurped their solid state counterparts. Two major weaknesses in MEMS switches are the slow switching time and the required high actuation voltage. In addition, the inability to handle high power has prompted considerable research effort in this area [18, 35-38]. Table 3 compares the different parameters of the switches.

Table 3: Comparison of the performance of FET, PIN Diode and RF MEMS switches [39].

Parameter	RF MEMS	PIN	FET
Voltage (V)	20-80	$\pm 3-5$	3-5
Current (mA)	0	3-20	0
Power Consumption (mW)	0.05-0.1	5-100	0.05-0.1
Switching Time	$1-300\mu\text{s}$	1-100ns	1-100ns
Cutoff Frequency (THz)	20-80	1-4	0.5-2
Capacitance Ratio	40-500	10	n/a
Isolation (1-10GHz)	Very High	High	Medium
Isolation (10-40GHz)	Very High	Medium	Low
Isolation (40-100GHz)	High	Medium	None
Power Handling (W)	<1	<10	<10
Loss (1-100GHz)(dB)	0.05-0.5	0.3-1.2	0.4-2.5

2.4 Literature Review

The first practical capacitive shunt switch was developed by Raytheon (formerly Texas Instrument) [40] in 1995, using a $0.3\mu\text{m}$ thick aluminium armature which is built onto a coplanar waveguide transmission line. At a RF frequency of 10GHz, the insertion loss and the isolation of the switch are approximately 0.5dB and 15dB respectively. An improved version of the MEMS switch, in term of RF losses, is reported in [41]. The required actuation voltage is 50V, with a switching on time of $6\mu\text{s}$ and a switching off time of $4\mu\text{s}$. The insertion loss is enhanced to 0.14dB at a RF frequency of 20GHz.

Since then, a large variation of MEMS switches are studied and developed by many different research groups [22, 42-44]. Apart from the summary in Table 2, the general actuation mechanism has evolved into hybrid systems, such as magneto-static [45], electro-piezo [46] and thermal-electrostatic [47]. MEMS switches are also reported using mercury as contact heads [48]. High dielectric constant materials, such as barium strontium titanate, hafnium oxide and lead zirconate titanate, have also been explored as alternatives to silicon nitride [49-51]. The details of these developments will be subsequently presented in this chapter. The following sections 2.4.1-3 will follow the development RF MEMS switches with electrostatic actuation, while the subsequent sections will concentrate on interesting research done on the other types of actuation mechanism, high RF power applications, as well as its reliability issues.

2.4.1 Development of MEMS Switch with Low Spring System

Despite of extensive researches over the past few years, the commercial market on RF MEMS switches is still in the pioneering stage. That is attributed to the developing technology of the RF MEMS, which results in the applications of the device being restricted significantly. One of the primary hurdles to commercialisation is high voltages required to actuate the switches. A typical MEMS switch requires 20V-80V for operations.

Several authors [16, 17, 34, 52-54] suggest decreasing the actuation voltage by means of using a complex mechanical suspension system. Huang *et al.* [55], studies the relationship between the effective spring constant and the residual stress of four different

armature structures on the actuation voltage of the capacitive shunt switch. The fixed-fixed suspension design yields the lowest actuation voltage of 6V as compared to the other designs, based on an assumption of zero residual stress.

Park *et al.* [56], investigate the minimum actuation voltage required for different suspension system designs. The RF MEMS switch with a meander-type suspension is reported an actuation voltage of 8V. The work, in addition, reported strontium titanate oxide (SrTiO_3) is used as the capacitive layer for the switch. This material has a high dielectric constant and the ON/OFF capacitive ratio is 600, with an ON capacitance of 50 pF.

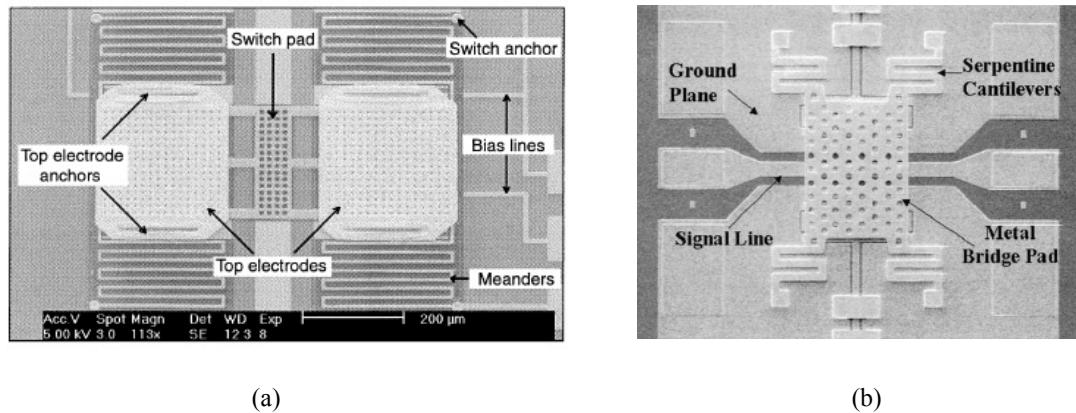


Figure 2.3: SEM photograph of the (a) capacitive shunt switch mentioned in [19] (b) series contact switch mentioned in [17], employing folded suspension beams.

Peroulis *et al.* [19], achieves a reduction of 80% in the actuation voltage of his switch by increasing the number of meanders in a serpentine folded configuration, of the mechanical spring from 1 to 5. The ideal actuation voltage and spring constant of the switch for 5 meanders are at 3V and 0.27Nm^{-1} respectively. However, the actuation voltage is 6V for a spring constant of 1.1Nm^{-1} . The difference between the predicted theoretical values and the experimental values of the actuation voltage is attributed to an intrinsic axial stress in the nickel armature during fabrication. The RF MEMS switch reported is illustrated in Figure 2.3(a)

While investigating the mechanical system, there are also some research groups that focus on reducing the mechanical spring constant with material studies. [57] reports that a MEMS switch with a low actuated voltage, uses an aluminium silicon alloy as the

armature material. The switch structure is optimized by calculating actuated voltages which depend on membrane materials and geometrical sizes of Young's modulus. The experimental results showed that the alloy has a lower actuation voltage of 5V, comparing to the gold counterpart with an actuation voltage of 45V. However, the transmission loss of the alloy membrane is twice in comparison to the gold membrane. The study demonstrated an improvement in the actuation voltage at the expense of the RF performance.

2.4.2 Development of Switch with Armature without Mechanical Spring

There are also other research groups working towards MEMS switches with ultra low actuating voltage of less than 5V. The approach is based on employing an unrestrained armature design in the RF MEMS switch

Shen *et al.* [58], propose using an anchorless armature that is hinged to the substrate by metal posts. This design is free from the mechanical spring constraints. Nevertheless, the switch must overcome the friction force when the armature contacts with the metal hinges during the switching. The actuation voltage is reported less than 10V.

Lee *et al.* [59] account a series contact RF MEMS switch using a pull-up structure without involving an elastic deformation during the switching operation. The armature, a 5 micron thick gold structure, is enclosed within a glass housing and a top silicon wafer where the transmission line and the pull up electrodes are fabricated. With the switch operating on a flat surface, the earth's gravity is acting perpendicularly to the armature, the actuation voltage of the switch is 4.5V and the time required to switch on is 120ns while the reverse operation required 130ns. The insertion loss and the isolation are 0.5dB and 55dB respectively at 50GHz. When the switch is operating in a tilted position, the actuation voltage of the switch is increased by the severity of the inclination.

An interesting DC-contact shunt switch design based on a flexible armature is presented by Segueni *et. al.* [60]. There are two sets of electrodes located on both sides of the supporting pillars. The switching operation is carried out by applying actuation voltage to either the inner set of electrodes or the outer set of electrodes as illustration in

Figure 2.4. The minimum actuation voltage to pull down the armature is 3.5V while the reverse action requires 1.5V. The S-Parameters of the switch is reported that the measured isolation is better than -30dB and an insertion loss less is than -0.45dB at 10GHz

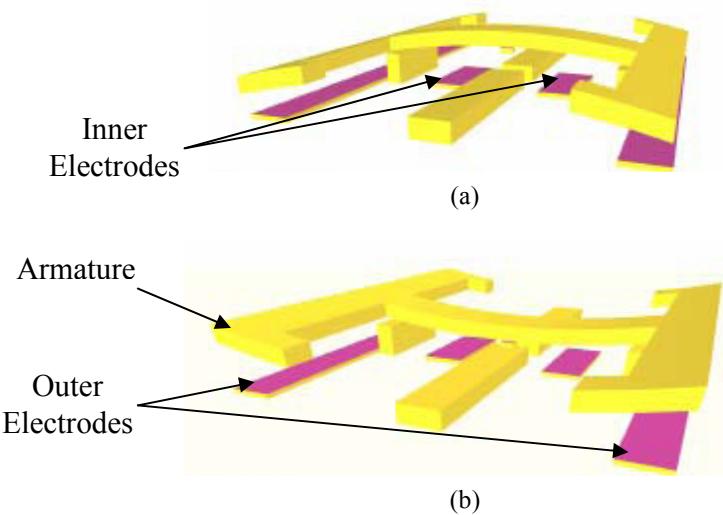


Figure 2.4: 3-D illustration of the switch proposed in [60] with an actuation voltage of 3.5V during (a) OFF state (b) ON state.

2.4.3 Development of Switch with Different Electrostatic Actuation Setup

Hah *et al.* [61] suggests another solution to reduce the actuation voltage. By changing the configuration of the actuation electrodes, the actuation voltage of the switch can be reduced. The design used a push-pull configuration to drive the electrostatic actuator, as shown in Figure 2.5(a). With the application of the DC biasing voltage at either the pull or the push electrode, the armature moves towards ('ON' position) or away ('OFF' position) the signal line accordingly. Since voltages are applied at both ON and OFF states, the switch is more robust to vibration or physical contact.

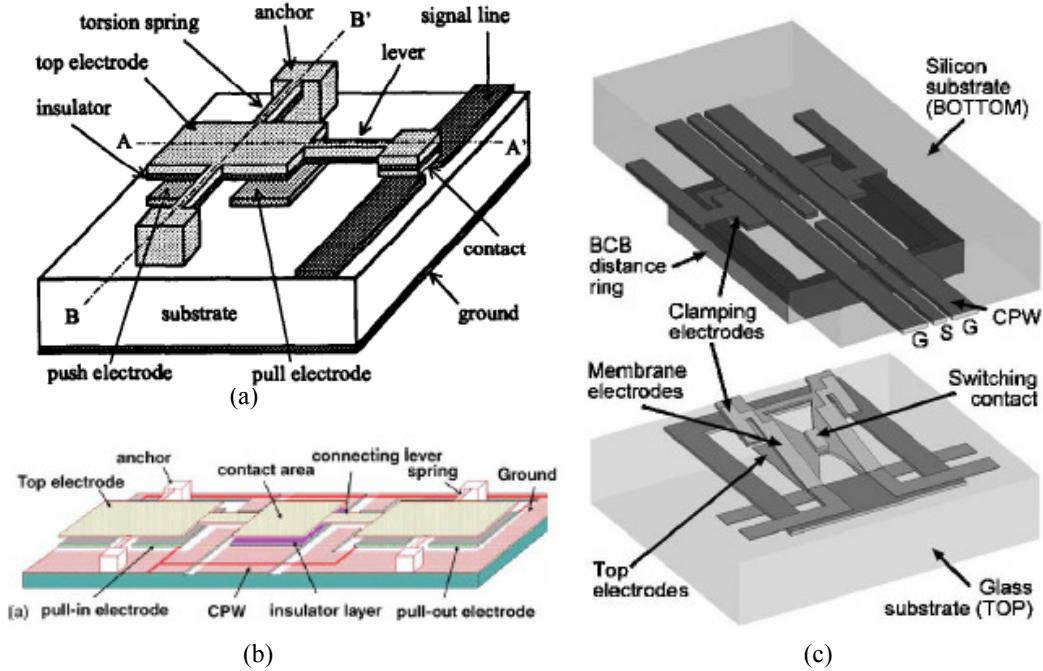


Figure 2.5: Illustration of (a) the single sided torsion spring designed by [61] (b) symmetric toggle switch design by [62] (c) the S-shaped film contact switch reported in [63].

Rangra *et al.* [62] presents a ‘Symmetric toggle switch’ (STS) concept as illustrated in Figure 2.5(b). The actuation mechanism is similar to the previously reported design. However, the torsion springs and the levers are placed on both sides of the transmission line. The experimental actuation voltages is 25V in comparison to the simulated actuation voltages which has a range of 8–10V. The difference is attributed to warping of the armature away from the substrate which increases the initial air gap.

Oberhammer *et al.* [63] presents a series contact switch using a S shaped-film actuator as illustrated in Figure 2.5(c). The film is designed with one end of the armature anchored to the substrate, while the other end is contacted to the surface of the clamping electrode after the switch is powered up. The film bends towards the transmission line. A voltage is then applied to the top electrode, pulling the middle section of the film away from the transmission line. Under these conditions, the film actuator is initialised for the switching operation. This operation occurs when a DC bias voltage is applied to the bottom electrode and the biasing voltage is removed at the top electrode concurrently. The film is pulled towards the transmission line to form a contact between the two sections. The switch exhibited an isolation of -45dB and an insertion loss of -2dB at

2GHz. The high insertion loss cannot be accounted as the gap is 14.2 μ m between the armature and the transmission line. The DC bias voltage for clamping the film is 19.2V while the switching on and off biasing voltage is 15.8V and 12V respectively.

2.4.4 Development of High-K Dielectric/Dielectric Manipulation Switches

Barium Strontium Titanate (BST) is used in [49] as a dielectric material of the proposed metal-insulator-metal (MIM) switch. The fabrication flow as detailed in [49], is based on a copper interconnect process, with the MEMS switch being integrated with a CMOS circuit. The utilization of BST improves the RF performance in comparison to the silicon nitride. An initial gap of 1.85 μ m yielded a capacitive ratio of more than 4500, with an actuation voltage of 18V. Reducing the gap to 0.85 μ m, the capacitive ratio is more than 2000 and the actuation voltage is 7V. These ratios could only be achieved if the initial gap is more than 44 μ m when silicon nitride is used as a dielectric layer.

Zhang *et al.*[50] reports a high RF performance π -type RF capacitive switch, using hafnium oxide as the dielectric layer in the MIM structure. The simulation shows that thinner layers of the dielectric produce a better isolation at RF frequencies of less than 20GHz. The dielectric constant of the material is 17 and could produce a capacitive ratio of 540. The experimental insertion loss and the isolation at a RF frequency of 50GHz are better than -0.8dB and -30dB respectively. The paper also describes some fabrication and reliability issues using the hafnium oxide. This material exhibits an increase in leakage current after the introduction of an annealing step, which has a negative impact on the quality of hafnium oxide. This effect can be attributed to the change in the crystalline structure after a high temperature treatment. Without the annealing process, the dielectric material had a leakage current with ranges of 10^{-6} Acm $^{-2}$ to 10^{-7} Acm $^{-2}$ at 15V. The material is able to withstand greater than 10^7 cycles of voltage changes without degradation.

A high-K dielectric organic spin on approach has been described in [64]. A photodefinable metal organic precursor, consisting of titanium(n-butoxide) $_2$ (2-ethylhexanoate) $_2$ and barium(2-ethylhexanoate) $_2$, is spun and exposed using a 248nm deep ultraviolet (DUV) exposure source. The exposed deposited layer acts like a

photoresist with the area reacting to the DUV source, turning into a metal oxide. This is followed by a development and bake step to form the structure on the wafer. The switch has a low insertion loss of -0.3dB and isolation of -24dB at 20GHz.

Herrmann et al. [65] introduces a dielectric material that consists of a mixture of alumina (Al_2O_3) and Zinc Oxide (ZnO) and is deposited using atomic layer deposition (ALD). Alumina provides the bulk of the material relative permittivity, the zinc oxide layer is employed as a charge dissipative layer which promotes the dissipation of trapped charges. This prevents dielectric charging, which is one of reliability issue of a capacitive MEMS switch. The experimental results shows that the dielectric constant of a 100% Al_2O_3 is similar to those of being mixed with ZnO when the materials is deposited using ALD. The dielectric constant of the mixture film is measured to be approximately at 6.8. The RF performance of the enhanced dielectric layer switch has an insertion loss and an isolation of -0.35dB and -55dB respectively at 14GHz. This material holds an advantage, i.e. a high dielectric constant and a low trap density, which is better than commonly used dielectric material, such as silicon dioxide and silicon nitride.

A DC contact capacitive shunt switch, designed and fabricated on a low-resistivity Si substrate, is described in [66]. This differs from the most capacitive shunt as the dielectric is deposited on the ground rather than on the transmission line of the coplanar waveguide. The switch would behave like a DC contact between the armature and the transmission line, with the RF signal being shunted through the dielectric layer over the ground lines. The design results in an ON state capacitance of 30pF as compared favourably to typical values of 4-5pF. The low-resistivity silicon wafer allows the coplanar waveguide to be fabricated with dimensions of $10\mu\text{m}/50\mu\text{m}/10\mu\text{m}$. This gives the switch an inductance of 2pH. A low inductance provides a better isolation during high RF frequency operations. At RF frequency of 26.5GHz, the insertion loss and the isolation are -0.4dB and -27dB respectively.

2.4.5 Development of Non Electrostatic Actuated Switch

Hartley *et al.* [25] describes the design, fabrication and testing of a magnetically actuated MEMS switch. The design of the magnetic actuator depicts the use of an

electromagnetic pot which redirects the magnetic flux generated from the current carrying coil to the armature. The air gap between the transmission line and the contact head is 100 μ m apart. A current of 1.4A, which corresponds to 80mW, is required to actuate the switch. The switching time is approximately 50ms. The RF switch has an insertion loss of 0.21dB and an isolation of 22dB when operating at a frequency of 10GHz. The switch is proven to be reliable as it completed 86000 cycle times without showing any form of degradation.

Cho *et al.* [45] reports the usage of a combination of the electromagnetic and the electrostatic actuation mechanism for a low-voltage (<5V) and a low-power operation in the MEMS switch. This design employs an electromagnetic actuation mechanism during the switching period and utilises an electrostatic actuator to hold the armature. The advantage in the design is the large actuation force ($\sim 20\mu$ N) produced by the electromagnetic actuation mechanism and improves the mechanical response of the switch. The hybrid system reduces the total power consumption required by the actuation systems of the switch. This actuation design reduces the operating voltage to 3.3V on a shunt type switch.

Saias *et al.* [47] develops a lateral RF MEMS switch by means of a thermal and an electrostatic actuator in the design. Similar to [45], the holding phase of the operation is carried out by electrostatic forces. The transition from OFF to ON state used a thermal actuation. The actuator requires a 20mA current and takes approximately 200 μ s to heat up the aluminium pads. It results in the armature bending and contacting with the transmission line. A driving circuit is also fabricated within the chip, producing 10V for both actuators when the switch turns on. The insertion loss and the isolation of the switch are 0.6dB and 40dB respectively with the operating RF frequency at 6GHz.

Wang *et al.* [28] reports an electrothermally actuated lateral-contact micro-relay for RF applications. This micro-relay used 6 V-shaped actuator beams, as shown in Figure 2.5, requires an actuation voltage of 2.5-3.5V to operate. The variation in the actuation voltage depends on a gap between the contact head and the transmission line, whereas the gap is dependent on the control of the fabrication process. Different from the electrostatic actuated switch with zero-power consumption, the electrothermally actuated switch consumes a power between 60mW to 100mW.

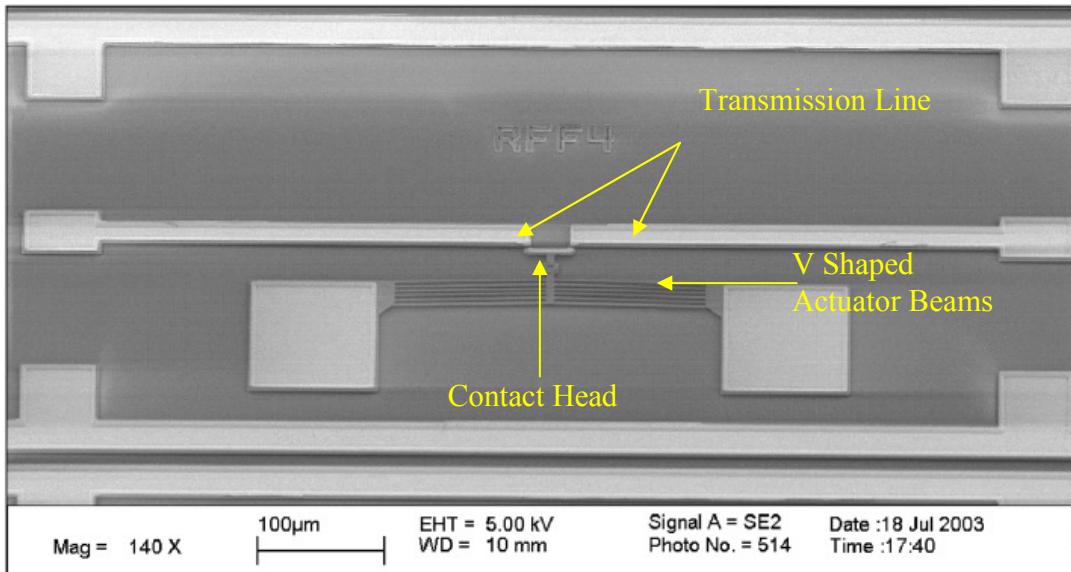


Figure 2.6: SEM photograph of the electro thermally actuated lateral contact relay reported in [3].

Lee *et al.* [32] proposes two Ohmic RF MEMS switches using a piezoelectric actuation. Lead zirconate titanate (PbZT) is used as a piezoelectric layer in the actuator design. When the actuation voltage is applied to the electrodes, the piezoelectric layer contracts towards the transmission line and changes the state of the circuit. The minimum achievable actuation voltage is 2.5V. The insertion loss and the isolation are -0.22dB and -42.5dB correspondingly at a RF frequency of 2GHz.

Apart from reducing the actuation voltage of the RF MEMS switch, some studies are based on improving reliability of the contact though a mercury contact head [48, 67, 68]. One of the research work reported in [48] demonstrates a gas expansion technique, where the position of liquid metal changes during switching and replacing the actuation mechanisms as depicted in Table 2. As shown in Figure 2.6(a), the thermal expansion engine consisted of a thin film heater made of TaN to heat up the gas. The expanded gas travels through the sub-channel and pushed the liquid metal away from the contact pad. The output port M is always in connection to either the contact L or the contact R. The switching time of this design is 0.1ms for OFF and 0.92ms for ON operation and requires an operating voltage of 22.5V. The insertion loss and the isolation of the switch are -1dB and -20dB respectively at a RF frequency of 18GHz. This switch is capable of handling

1A of DC current. The design has mitigated the problem of stiction during the switching operation and the micro-welding under high current applications.

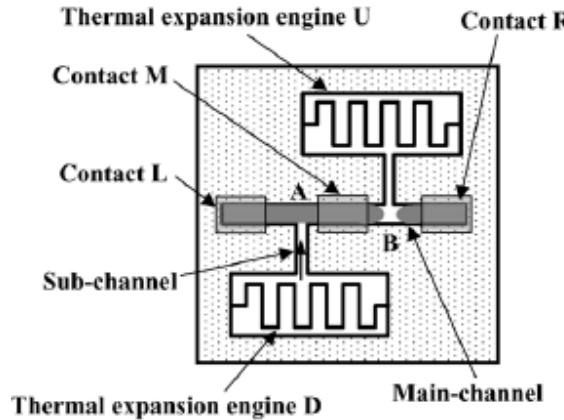


Figure 2.7: The liquid metal micro switch described in [48].

2.4.6 Development of High Power Application RF MEMS Switch

Poor power handling is one of the disadvantages of a RF MEMS switch. There are also works [18, 35-38] focusing on design of RF MEMS switches which is suitable for high RF power applications.

[35] reports on a RF MEMS switch design that is suitable for high power RF applications. The design is a 2 by 2 switching matrix, where the actuation mechanism is connected in series and the RF circuit elements are connected in parallel. The basic idea of the design is to share the RF power across a network of switches. Therefore, each switch is required to absorb a fraction of the total RF power transmitted with the transmission line. The series contact switch is a more suitable configuration in a high power application. However, large contact area and high planarity are required to achieve low contact resistance and reduce ohmic heating in a high current scenario. The power handling capability of the design is expected to handle up to 10W of RF power between 8GHz -12GHz.

Nishijima *et al.* [36] describes an electrostatically actuated series contact switch fabricated for the use in applications with a moderately high RF power (in the range of hundreds of mW's to 1W). There are two design goals achieved. The first goal is to design a switch with good metal contacts and reliability under actuation voltages of 50-

60V and the second goal is a reduction in RF current flowing through individual contact by networking several switching elements in parallel. The cantilever design has two contact pads. Due to the dimension of the design, the actuation pad is extended around the contact pads in aims of decreasing the required actuation voltage during the pull-down operation. Several arrangements of the contact pad and the cantilever switch are tested in [36]. In terms of configuration arrangement, a better isolation is observed using a parallel configuration, while the impact of the configuration on the insertion loss is less obvious. Increasing the number of contact pads improves the insertion loss, while the isolation suffers from degradation. The RF performance of the switch design, by placing the switching element in parallel and using 8 contact pads, yields an insertion loss and an isolation of -0.03dB and -22dB respectively at 2GHz.

Table 4 tabulates the performance of the low actuation voltage RF MEMS switch developed by the universities worldwide in recent years.

2.4.7 Fabrication Work on MEMS Devices with Mechanically Unrestrained Proof Mass

Most of the RF MEMS switches reported are fabricated using surface machining techniques. These switches usually employ sacrificial polyimide layers to form the capacitive gaps and subsequently use critical point drying (CPD) techniques to release the armature.

Shen et al. [58] describes a fabrication process of a hinged capacitive RF MEMS switch with seven masks. The switch is fabricated on a GaAs substrate with a 1mm thick gold layer to form the transmission line and electrodes. The dielectric layer is silicon nitride deposited using PECVD. A layer of polyimide is spun on the substrate followed by a micron of gold which is evaporated onto the polyimide to form the armature. A second layer of polyimide is spun on and patterned to create the supporting features for top electrodes. Silicon nitride is again used as the dielectric layer for top electrodes, while the electrodes are formed by gold deposition. The sacrificial polyimide layers are removed and the armature is released using critical point drying. The fabrication process requires two additional masks as compared to a similar cantilever switch design which is also reported by the research group [69].

There has also been some fabrication work on mechanically unconstrained devices conducted by the University of Southampton. These fabrication processes are approached using two methods, namely electroplating and DRIE. The advantages and disadvantages of these two methods are detailed as follows.

Electroplating

The first fabrication work carried out to form mechanically unconstrained devices in the University of Southampton combines a two substrate assembly technique and an electroplating technique which is used to form the middle layer. The electrodes are first patterned on the substrates, followed by electroplating of Nickel in a thick film mould from a chrome gold seed layer. The top wafer is then bonded onto the bottom wafer using a self aligning reflow process where conducting pillars act as electrical interconnect in between the two wafers. The device is completed with a final releasing step. This implementation allows the bond pads to be on one wafer, so as to enable the use of wire bonding. The full process is detailed in [70].

However, this process is complicated and required extensive process development time especially in the thick film mould and the electroplating of the nickel layer. This motivated the development of an alternative and simpler micromachining process, which is presented in the next section.

DRIE

A simpler alternative three wafer assembly process is introduced by Houlihan [71]. This process employs a double side polished highly doped silicon wafer anodically bonded between two Pyrex wafers. The electrodes are fabricated on Pyrex wafers which is subsequently covered with silicon dioxide and the mechanically unconstrained proof mass (in the form of a silicon disk) is made by means of deep reactive ion etching (DRIE). The silicon wafer is attached to a handle wafer with carbon adhesive tape prior to the through etch. The etched silicon is then released from the handle wafer by placing the stack in acetone. The assembly stage of the device requires the Pyrex wafer to be sawed into chips before the bonding step. The silicon disk and spacer are picked and placed manually onto the Pyrex chip, then anodically bonded to form the device. This process flow is illustrated in the Figure 2.8. There are several problems associated with this process.

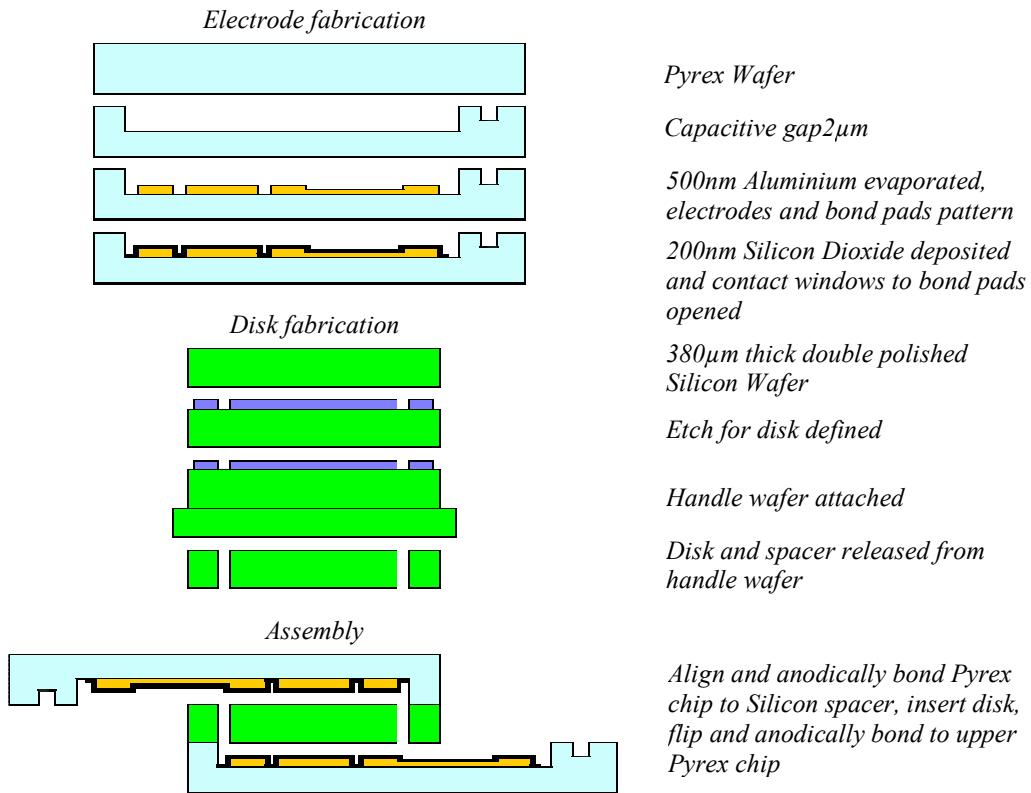


Figure 2.8: Process fabrication as described in [71].

- *Handling of the etched silicon disk:* As the disk is manually handled in the process; particle dusts can be a major failure cause. As the depth of Pyrex etch is $2\mu\text{m}$, if the surface was contaminated by any particle, it could cause the disk to be wedged. In addition after the acetone release step, any residuals from the carbon tape which remain on the silicon surface will also have a similar effect as particles in the capacitive gap.
- *Assembly of device:* The assembly of device is carried out by anodic bonding. Although this is a straightforward process, there are some complex issues for the work. It is found that most of the proof mass in the assembled devices are not free. A possible cause is due to the anodic bonding step for the top Pyrex chip. As anodic bonding requires the application of a high negative voltage ($\sim -1000\text{V}$) on the bonding Pyrex chip, the movable silicon proof mass is attracted towards the Pyrex chip via an electrostatic force, which is causing the proof mass to be bonded.

- *Multi-level Bond pads:* As the bond pads of the device are fabricated as part of the electrodes, the bond pads from both Pyrex chips will be facing each other. This makes normal wire-bonding very difficult.

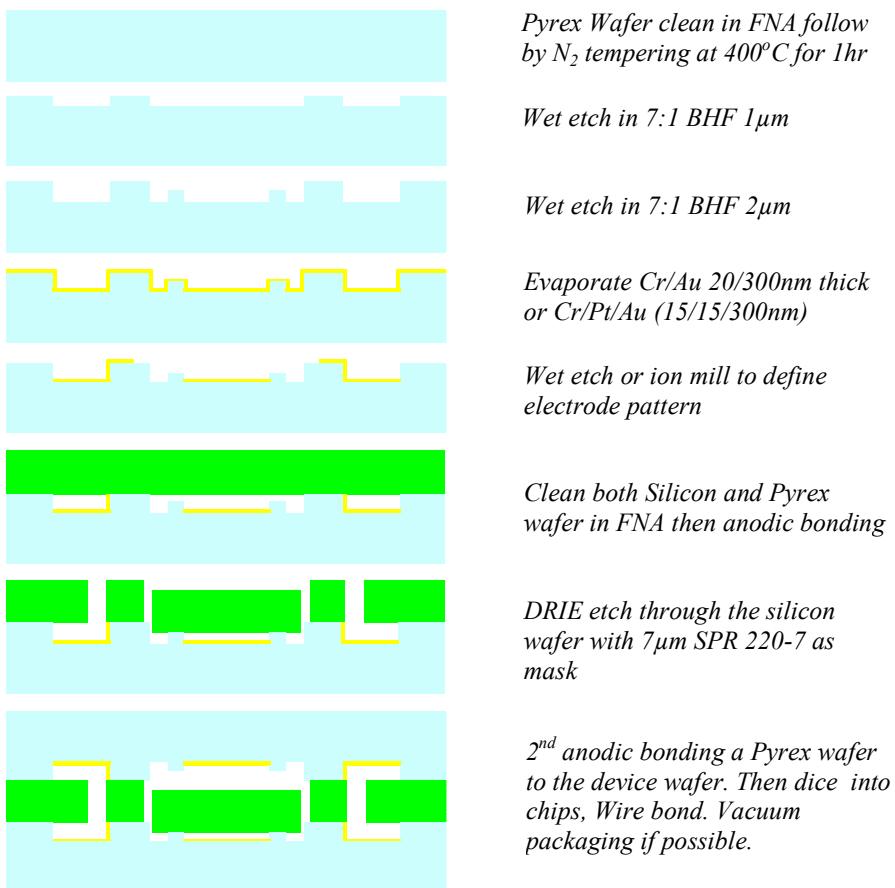


Figure 2.9: Process fabrication as described in [72].

A second DRIE approach is proposed Damrongsak [72], attempting to address many of design and fabrication problems arise in the previous approach. The Pyrex etch is split into two steps. The initial step is to create a general area for electrodes while the second step is to form stoppers in the cavity to prevent the silicon from shorting the electrodes when in contact. The electrodes are formed using a chromium/gold metal stack on the Pyrex wafers. The electrodes from the top wafer are electrically connected via the silicon wafer to the bottom wafer with all the bond pads located on the bottom Pyrex wafer. In order to reduce the particle contamination, the high conductivity ($\sim 0.001 - 0.02 \Omega \cdot \text{cm}$) silicon wafer is bonded onto the processed Pyrex wafer before the DRIE step to

form the spacer, electrical interconnects and silicon disk. This is followed by anodic bonding of the top Pyrex wafer to encapsulate the device prior to sawing the wafer into individual devices. The process flow is illustrated in Figure 2.9. However, there are still issues with this process.

- *Assembly of device*: The disk, after the second anodic bonding step, is not found to be movable. The stoppers are created to prevent electrical shorting as well as reducing the contact area between the Silicon disk and Pyrex wafer. The reduced contact area will, in turn, lower the possibility of Silicon disk bonded to the top Pyrex wafer. Therefore, the consideration of this design is insufficient as the silicon disk is still stuck after the process.

2.4.8 Reliabilities Issues

The reliability of RF MEMS switches is another problem which needs to be resolved for the applications in the consumer market. Depending on the application type and environment, a low end MEMS switch may require surviving at least 10 million operations. However, at the other end of the spectrum, such as channel-hopping filters or in space-based applications, the design needs to last for hundreds of billion switching operation in adverse condition. The reliability of RF MEMS switch can be studied from two areas:

- Design and material
- Packaging

If there are any contaminates or material imperfection, the actuation of the armature can easily be impeded and the life span of the device would be reduced.

Design and material

Reliability based on design, material, fabrication and packaging, is always a concern [73-75]. The main failure of the MEMS switch is not caused by structural failure of the armature or the switching membrane. In the case of an ohmic contact MEMS switch, the issue is on account of the hardening and pitting of the contact pad, which causes MEMS switches to fail. The failure tends to appear towards the last few thousand switching cycles of the MEMS switch lifespan [17]. The contact area between the

conductive beam and the transmission line becomes hard after prolonged usage. This increases the contact resistance and results in the degradation of the RF performance. Moreover, the contact becomes capacitive over time with the formation of thin dielectric layer on the surface of the conducting surface. The other issue for this type of the switch is arcing and micro-welding [76]. This phenomenon usually occurs under hot switching and high current application.

In the case of a capacitive MEMS switch, dielectric failure is a major reliability issue encountered. The capacitive shunt switch often fails due to charge up/breakdown of the dielectric [77]. With an establishment of electric fields between the electrodes and the armature during actuation, the surface charges of the materials change within the field. If the surface charges from the armature are transferred to the dielectric, the armature would return to the original position regardless of the existence of the DC actuation voltage. The reason is that the electric field, which is generated between the armature and the dielectric layer, is reduced after transferring charges to the dielectric. As the charges remain in the surface of the dielectric, the operating actuation voltage is required to increase subsequently in order to operate the switch [78].

Another possibility is if a charge is injected into the dielectric layer bulk, the dielectric layer would take up the polarity of the charge. This causes the armature to either remain in the ON-state position or non-actuating in the presence of an applied actuation voltage [78]. Solutions to the dielectric issues include choosing a dielectric material with a low trapping density or applying a dual polarity actuation voltage on the electrodes to mitigate the charging effect on the dielectric [79].

Packaging

Many MEMS packaging options are available. Nonetheless, suitable packaging techniques used for RF MEMS switches are limited due to the thin film armature and small capacitive gap, which is susceptible to process temperature, humidity and particles [80]. This has to be carried out under clean and hermetic conditions, using inert gases. Any outgassing of the sealant or leakages in the package will reduce the reliability of the switch greatly. There are several commonly used packaging for RF MEMS switch, including epoxy sealing [81], silicon-glass eutectic sealing with localised heating [82, 83]

and thin film encapsulation [84]. These package processes are often expensive to implement in large scale, as some of these process are performed on die level.

The outgassing and leakage usually lead to introducing moisture into the package. With the presence of moisture, stiction [85] will arise at the contact surface when the mechanical part touches the dielectric during actuation. Although passing a tight gross leak test is possible for most devices packages [80, 81], a fine leak test is sometimes not possible for a device package using epoxy sealing [86].

All these reliability and packaging issues made commercialisation of such devices challenging, thus one of reasons for the lack of commercial activities as reported in chapter 1.

2.5 Summary

Over the last 15 years, research work conducted in area of RF MEMS switch have span into many application areas, ranging from military to industrial equipment as well as personal telecommunication applications. Although a MEMS switch has the potential to fulfil the RF capabilities of these applications, the operating actuation voltage of such designs is typically higher than the voltage used for CMOS circuits. It is almost impossible to integrate a RF MEMS switch with existing circuits which are without a DC step up conversion.

A lot of effort is put into reducing the actuation voltage of the RF MEMS switch. The different methodologies suggested include using different actuation mechanism which are able to increase the pull in force with small actuation and to reduce the mechanical spring constant either through material studies or a complex spring design. There are also a small number of works on RF MEMS switch with an unrestrained armature.

In this thesis, a new approach in developing a RF MEMS switch with an unrestrained armature is explored. The proposed design will embark on a bulk micromachining technique, which is to fabricate a spring-less RF MEMS switch using a triple-stack wafer bonding method.

Research Institute	Actuation Mechanism	Actuation Voltage (V)	Insertion loss (dB)	Isolation (dB)	RF Frequency (GHz)	Switching Capacitance		Switching Time(μs)
						ON(fF)	OFF(pF)	
Dongguk University [59]	Electrostatic	4.5	0.5	55	50	Series Contact		0.12
Georgia Institute of Technology [16]	Electrostatic	15	0.9	25	40	50-70	4.5-5.0	-
Korea Advanced Institute of Science and Technology [45]	Magneto-static	3.3	0.85	20.7	19.5	-	-	230
Nanyang Technological University [87]	Electrostatic	20.4	0.1	16.5	10	137	4.26	-
Seoul National University [88]	Electrostatic	19	0.18-0.2	38-39	2	Series Contact		25
University of Illinois – Urbana-Champaign [58, 89]	Electrostatic	9-17	0.5	27	40	-	-	-
University of California [28]	Electro-thermal	2.5-3.5	0.1	20	40	Series Contact		282
University of Michigan [19]	Electrostatic	6	-	-	-	-	-	52
								213

Table 4: A compilation of low actuation voltage RF MEMS switches developed by different universities’ research group.

‘-’ denotes that the data is not presented in the paper.

Chapter 3

Design Considerations

This work presents a novel RF MEMS switch using electrostatic actuation without any mechanical suspension attaching the armature to substrate as depicted in Figure 3.1. The unrestrained armature is positioned over a coplanar waveguide which is used as a transmission line for the RF signal. A pair of actuation electrodes is located on either side of the armature to generate electrostatic forces. The actuation electrodes are energised with a DC voltage in order to allow movement of the armature depending on the switch state. As there is no mechanical spring connecting the switch armature to the substrate, it is electrically floating. The main objective of the work is to develop a spring-less MEMS switch suitable for RF applications. A couple of guidelines are set from the mechanical point of view when designing the switch. They are set in the order of importance as following:

1. Low actuation voltage, i.e. less than 3.5V,
2. Minimum switching time with respect to the dimensions of the armature.

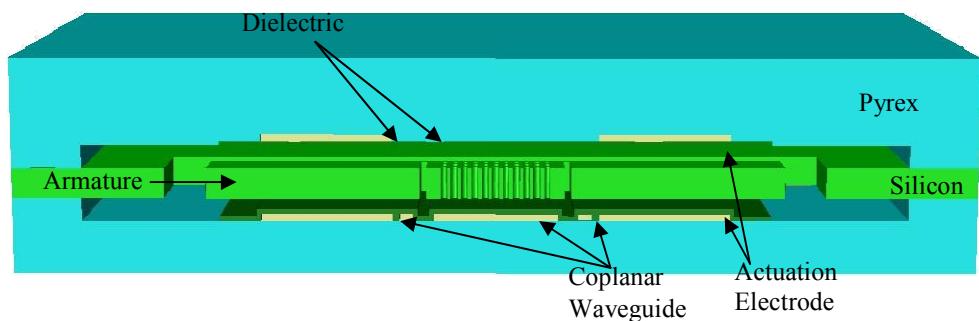


Figure 3.1: Conceptual illustration of the proposed MEMS switch.

Section 3.1 discusses about the principle of operation for the proposed RF MEMS switch. Section 3.2 derives the actuation voltage of the proposed design and explores the effects on the actuation voltage on different dimensions of the armature. Section 3.3 reports on the switching time of the proposed switch for a range of armature width based on the initial dimensions which are selected in section 3.2. Section 3.4 discusses on the effects of surface adhesion force on the minimum actuation voltage of the proposed design. A system level model representing the proposed MEMS switch is created using Matlab Simulink® which is detailed in section 3.5. Section 3.6 summarises the work performed in the chapter.

3.1 Principle of Operation

The following sections present the actuation mechanism to the free moving armature, in a configuration, that an electrostatic actuation force can be applied to the armature.

3.1.1 Electrostatic Actuation

The operation of the switch, i.e. lifting the armature, is achieved electrostatically to change the switching state of the device. In order to actuate the armature, the attractive electrostatic force generated must be greater than the other forces acting against it:

$$F_{electrostatic} \geq F_{mg} + F_{damp} + F_{ext} \quad (3.1)$$

where $F_{electrostatic}$ is the net electrostatic force, F_{mg} is the gravitational force acting on the armature, F_{damp} is the damping force acting on the armature and F_{ext} is the external applied inertial force acting on the armature. The $F_{electrostatic}$ can be written as:

$$F_{electrostatic} = \frac{\partial}{\partial x} \frac{1}{2} C V_{act}^2 \quad (3.2)$$

where x is the displacement, C is the capacitance and V_{act} is the applied actuation voltage,

By using a single top and bottom electrode configuration with the armature in between, the voltage of the armature, V_{arm} , can be formulated as:

$$V_{arm} = \frac{V_t(z_o + x) + V_b(z_o - x)}{2z_o} \quad (3.3)$$

where z_o represents the gap between the armature and the electrodes at nominal position, V_t is the top electrode voltage and V_b is the bottom electrode voltage. The nominal position is assumed to be in the middle of the capacitive gap in the analysis.

The forces acting on the armature can be calculated by substituting equation 3.3 into $F_{electrostatic}$ expression (equation 3.2):

$$F^+ = \frac{\partial}{\partial x} \left(\frac{1}{2} C (V_t - V_{arm})^2 \right) = \frac{\partial}{\partial x} \left(\frac{1}{2} \frac{\epsilon_o A_{ap}}{(z_o - x)} \left(V_t - \frac{V_t(z_o + x) + V_b(z_o - x)}{2z_o} \right)^2 \right) \quad (3.4)$$

$$F^- = \frac{\partial}{\partial x} \left(\frac{1}{2} C (V_{arm} - V_b)^2 \right) = \frac{\partial}{\partial x} \left(\frac{1}{2} \frac{\epsilon_o A_{ap}}{(z_o + x)} \left(\frac{V_t(z_o + x) + V_b(z_o - x)}{2z_o} - V_b \right)^2 \right) \quad (3.5)$$

where F^+ represents the electrostatic forces between the top electrode and the armature, F^- is the electrostatic forces between the bottom electrode and the armature, ϵ_o is the permittivity of free space and A_{ap} is the total area of the actuation electrode.,

Equations 3.4 and 3.5 can be further simplified to equation 3.6 and 3.7. By summing the simplified equations, the net resultant electrostatic force of zero in equation 3.8 is being derived.

$$F^+ = -\frac{\epsilon_o A_{ap}}{2} \frac{(V_t - V_b)^2}{4z_o^2} \quad (3.6)$$

$$F^- = \frac{\epsilon_o A_{ap}}{2} \frac{(V_t - V_b)^2}{4z_o^2} \quad (3.7)$$

$$F_{electrostatic} = F^- + F^+ = 0 \quad (3.8)$$

The derivation proves that a single top electrode and a bottom electrode configuration cannot achieve the actuation of the armature. The magnitude of the forces F^+ and F^- is equal but act in opposite direction. Therefore, it results in a net electrostatic force of zero on the armature. This cancels out the pull-up effect on the armature.

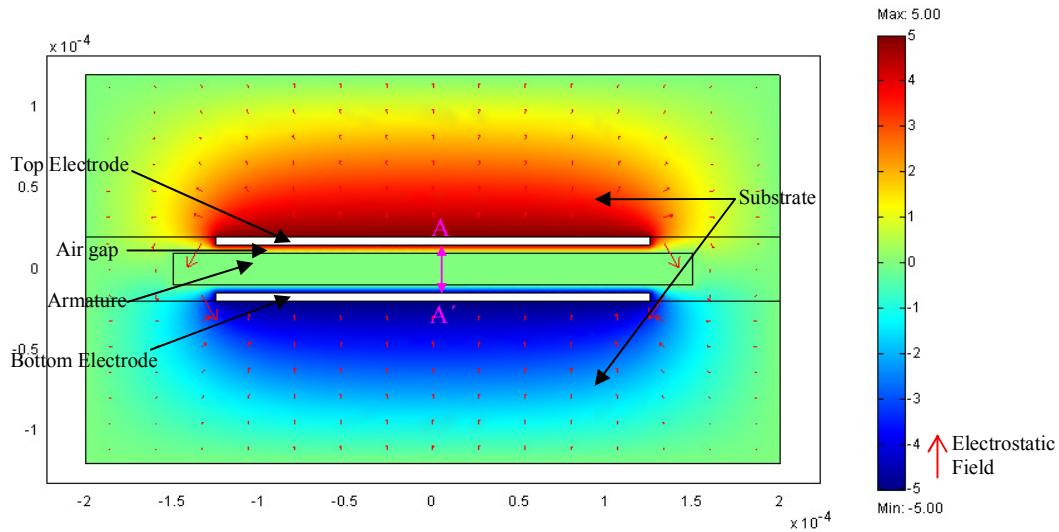


Figure 3.2: A COMSOL model showing the electrostatic field acting on the armature using $\pm 5V$ for a single top and bottom electrode configuration

The derivation is further verified using the electrostatic finite element model module within COMSOL. The model as shown in Figure 3.2 presents the electrostatic field between the two electrodes. The field lines travel from the top electrode to the bottom electrode. As a result, the electrical potential of the armature will vary linearly between the two electrodes (as shown in Figure 3.3(a)). This results in the electrostatic force acting on the armature between the top and bottom of the electrode is equal, hence the net resultant force becomes zero (as presented in Figure 3.3(b)).

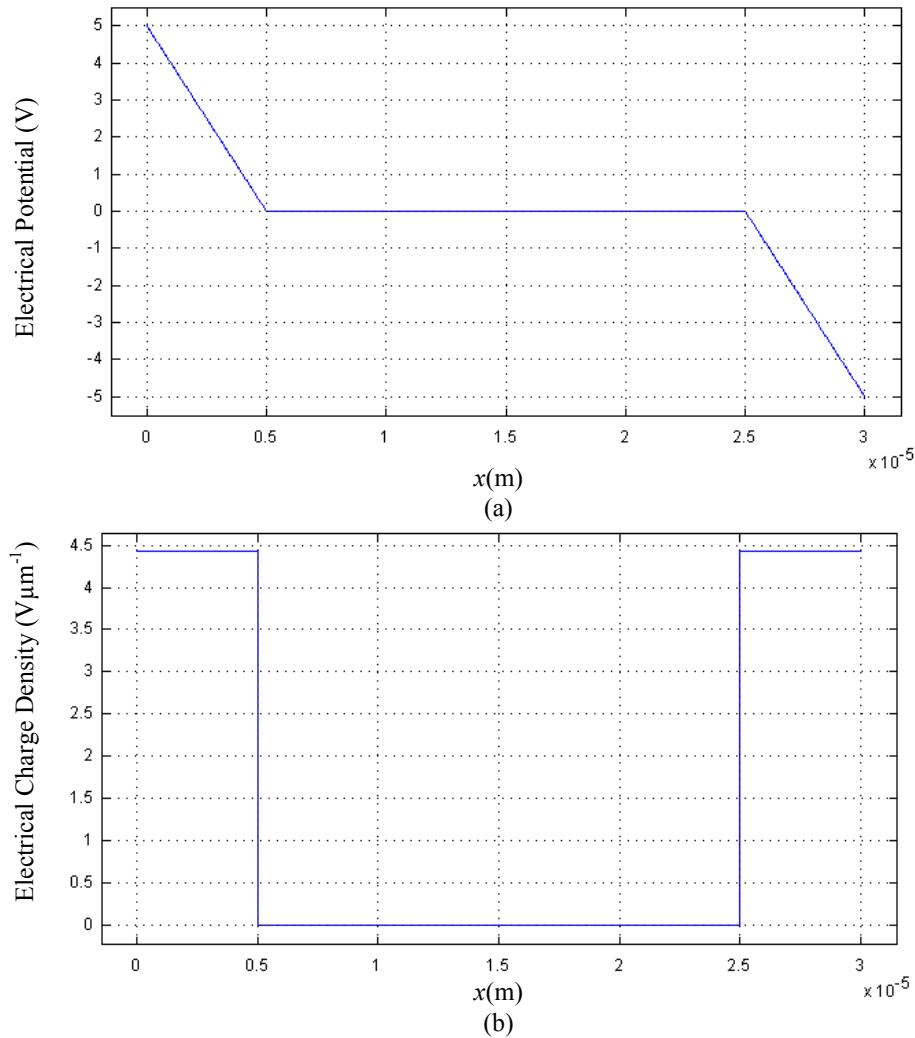


Figure 3.3: (a) Electrical potential distribution within cavity along A-A' marked out in Figure 3.2
 (b) Electrical charge density along A-A' marked out in Figure 3.2.

The problem can be resolved by at least a pair of top electrodes which is energised with opposite polarities as shown in Figure 3.4. Since the electrostatic force is proportional to the square of the voltage, both positive and negative charge electrodes produce an attracting effect on the armature. This configuration also causes the armature potential to be zero. By substituting this condition back into equation 3.2, the electrostatic force can be given as:

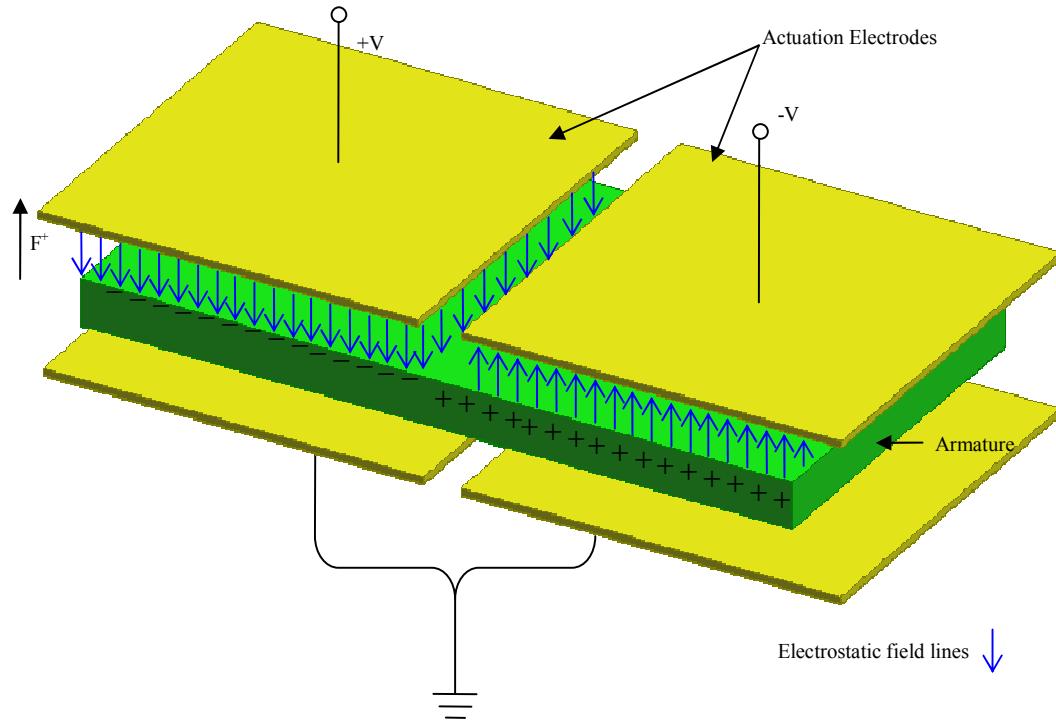


Figure 3.4: Charge distribution of the armature caused by induction of electrostatic field in attractive force between the armature and the pair of electrodes of different polarities.

$$F^+ = \frac{\partial}{\partial z} \left(\frac{1}{2} \frac{\epsilon_0 A_1}{(z_o - x)} (V_t - V_{arm})^2 + \frac{1}{2} \frac{\epsilon_0 A_2}{(z_o - x)} (-V_t - V_{arm})^2 \right) \quad (3.9)$$

$$F^+ = \frac{\epsilon_0 A_1}{2} \frac{(V_t)^2}{(z_o - x)^2} + \frac{\epsilon_0 A_2}{2} \frac{(-V_t)^2}{(z_o - x)^2} = \frac{\epsilon_0 (A_1 + A_2)}{2} \frac{(V_t)^2}{(z_o - x)^2} \quad (3.10)$$

where A_1 and A_2 are the area of the actuation electrode. Hence, the net resultant force acting on armature is:

$$F_{electrostatic} = F^+ \quad (3.11)$$

The calculated net resultant force acting on the armature is shown in Figure 3.5. An attractive force is observed on the armature. The force increases with an inverse quadratic relation to the displacement of the armature, with respect to the distance from the actuation electrode.

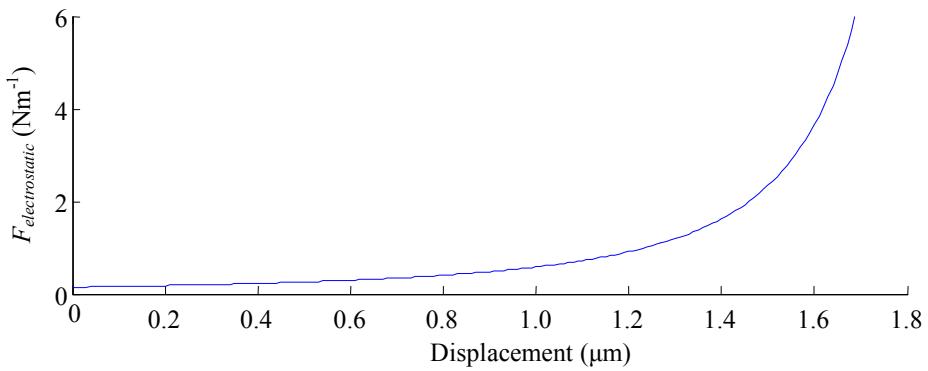


Figure 3.5: The resultant force F^+ acting on the armature for the case of a pair of actuation electrodes with different polarities.

The derivation was again verified using COMSOL. This model as shown in Figure 3.6 presents the electrostatic field between the two electrodes. Both electrodes were set at 5V but with different polarity. The field lines interacted between the positive electrode and the negative electrode and some of the field lines travel to/from the boundary. The latter effect was due to the assumption that all the boundaries are grounded.

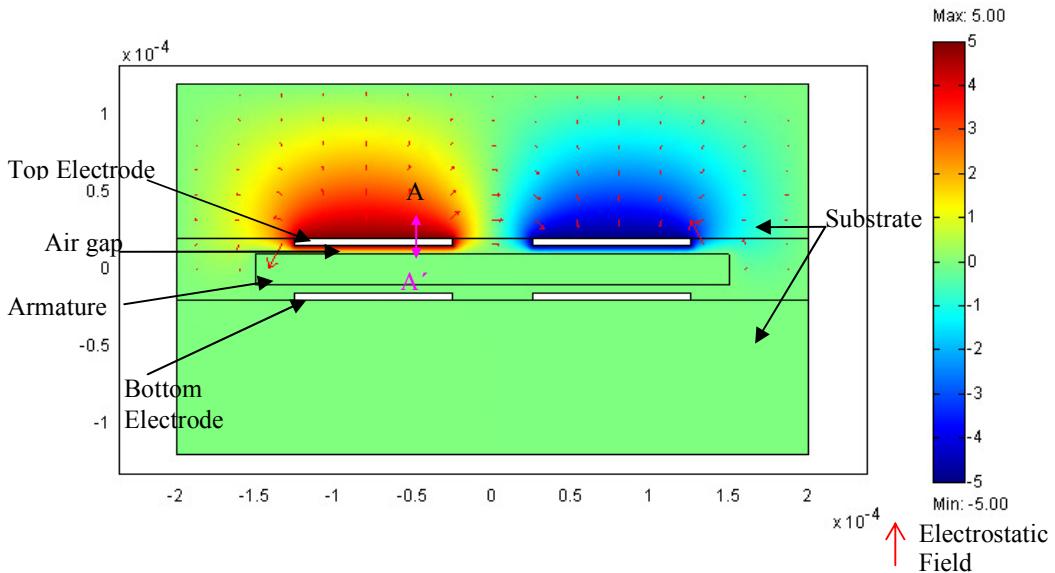


Figure 3.6: A COMSOL model showing the electrostatic field acting on the armature using a pair of actuation electrodes configuration with the two electrodes energised with 5V but of opposite polarities.

Figure 3.7(a) shows that the electrical potential of the armature will vary linearly from the top electrode to the armature with the electrical potential of armature 0V. As a result, there is an attractive electrostatic forces acting on the armature from the top electrode as shown in Figure 3.7(b). There is no potential difference between the armature and bottom electrodes, the armature therefore will be pulled towards the top electrode.

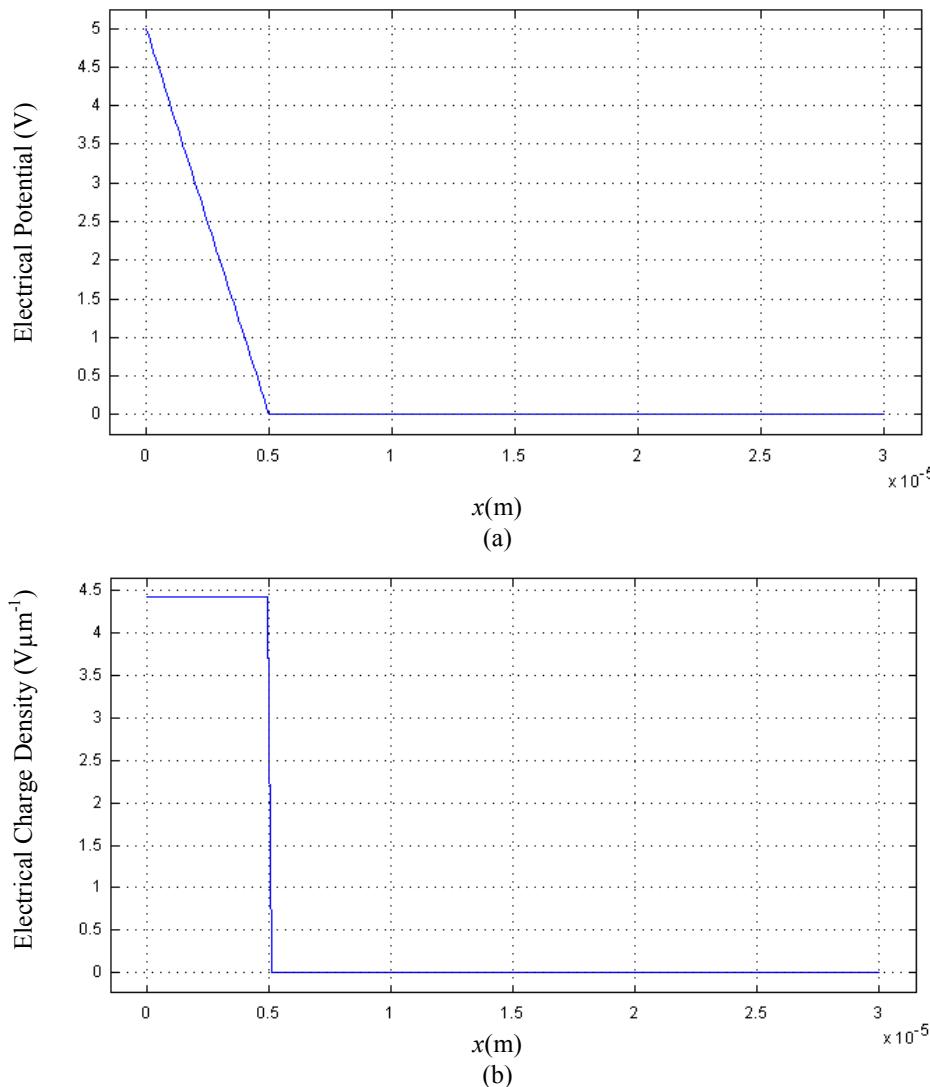


Figure 3.7: (a) Electrical potential distribution within cavity along A-A' indicated in Figure 3.6.
 (b) Electrical charge density along A-A' indicated in Figure 3.6.

3.2 Actuation Voltage

The previous section discussed the possibility of implementing an electrostatic actuation mechanism for the proposed switch as illustrated in Figure 3.1. Switching is achieved by generating a pulling electrostatic force to overcome the gravitational force which is acting upon the armature. With the dimensions being defined, Figure 3.8 depicts a top down view of the proposed switch without the top cover.

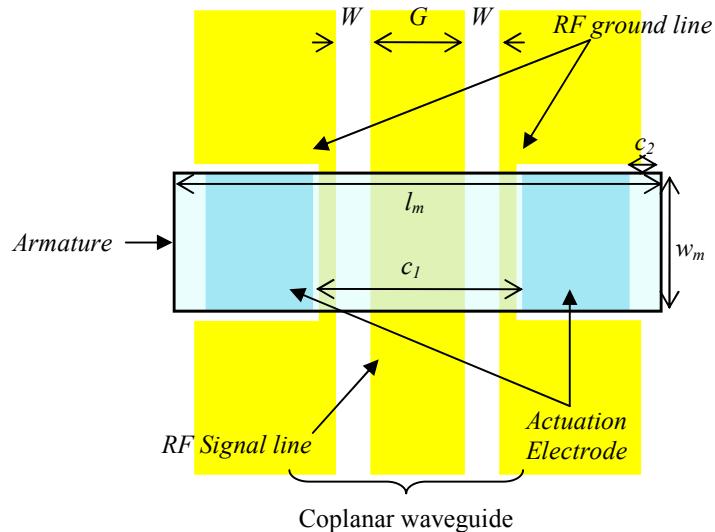


Figure 3.8: Simplified illustration of a proposed MEMS shunt switch shown in top down view.

As most RF systems are based on 50Ω or 75Ω load, a coplanar waveguide with matching impedance is designed. For a 75Ω coplanar waveguide fabricated on $500\mu\text{m}$ Pyrex substrate, the width of the signal line(G) and slot width(W) are $90\mu\text{m}$ and $60\mu\text{m}$ respectively. Similarly, the signal line width and slot width of a 50Ω coplanar waveguide are $90\mu\text{m}$ and $15\mu\text{m}$ respectively. The computation of the signal line width and slot width values is detailed in the next chapter. The study conducted in this chapter is based on a 75Ω coplanar waveguide. c_1 is the gap between the two actuation electrodes and c_2 is an extension of the armature required by the final release step during fabrication. There are several fabrication constraints which have to be considered in the design, i.e. the minimum thickness of the silicon armature is $50\mu\text{m}$ and minimum extension of c_2 is

30 μm . These are discussed further in chapter 5. As the surface interaction forces are material and process dependent, it will be consider separately in another section.

The pull-up electrostatic force is defined by equation 3.12 and is greater than the gravitational force acting on the armature:

$$F_{\text{electrostatic}} = \frac{1}{2} \frac{\varepsilon_o A_{ap} V_{act}^2}{g_o^2} \geq mG_f \quad (3.12)$$

where m is the mass of the armature and G_f is the earth's gravity. The theoretical minimum actuation voltage can therefore be calculated as:

$$V_{act(\min)} = \sqrt{\frac{2G_f m g_o^2}{\varepsilon_o A_{ap}}} \quad (3.13)$$

The formula can be reduced to:

$$V_{act(\min)} = \sqrt{\frac{2G_f \rho l_m t_m g_o^2}{\varepsilon_o (l_m - 2c_2 - c_1)}} \quad (3.14)$$

where ρ is the density of an armature material. It is observed that $V_{act(\min)}$ is independent of the width, w_m .

Figure 3.9 shows the relationship of minimum actuation voltage with respect to a range of armature length (l_m) and air gap (g_o). The minimum actuation voltage increases proportionally with the increasing gap height and decreases when the armature length increases. The slope of the minimum actuation voltage line is always getting flatter from left to right. The optimum range for l_m is in the region where the slope of the graph becomes shallow. This represents a good compromise between the switch length and a low actuation voltage. As the relationship between the gap height and $V_{act(\min)}$ is linear, this parameter will be further explored in the next section. Consequently, the armature length (l_m) of 680 μm is selected for the design.

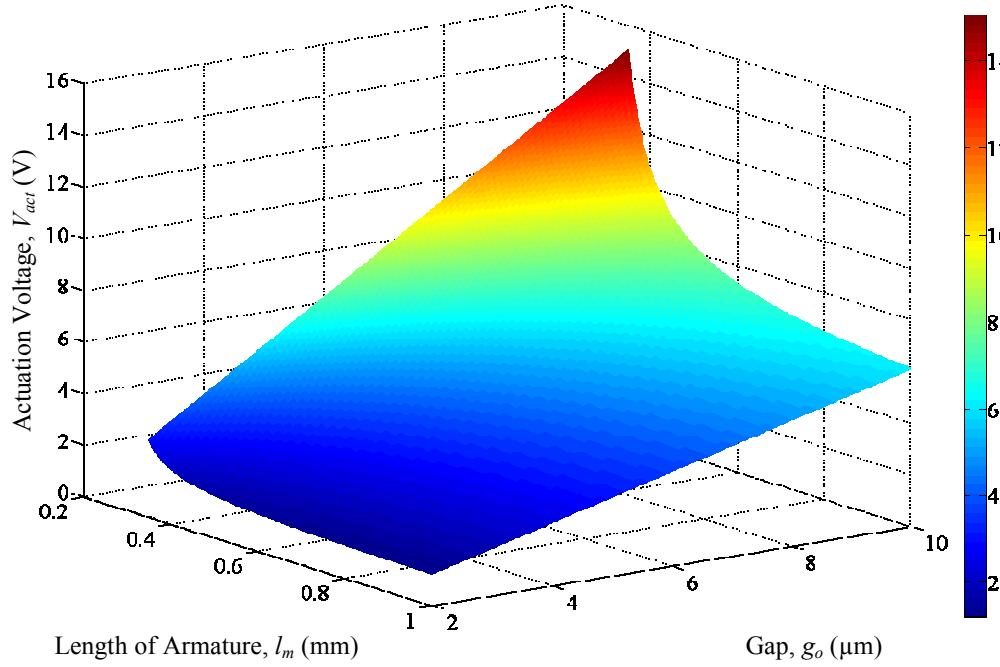


Figure 3.9: Minimum actuation voltage ($V_{act(min)}$) for different armature length varying from 400 μ m to 1mm with a variation of initial gap of the device from 2 μ m to 10 μ m.

3.3 Switching Speed

The other important characteristic of a RF switch is the switching speed. Gupta *et al* [90], approximated the switching time (T_{rise}) of MEMS switches using the dynamic equation of motion, with the following assumptions:

- Constant damping with gap height
- Damping dominated condition
- Applied actuation voltage \gg Minimum actuation voltage

$$T_{rise} = \frac{2bg_o^3}{3\epsilon_o A_{ap} V_{act}^2} \quad (3.15)$$

where b is the constant damping factor as stated in equation 3.29.

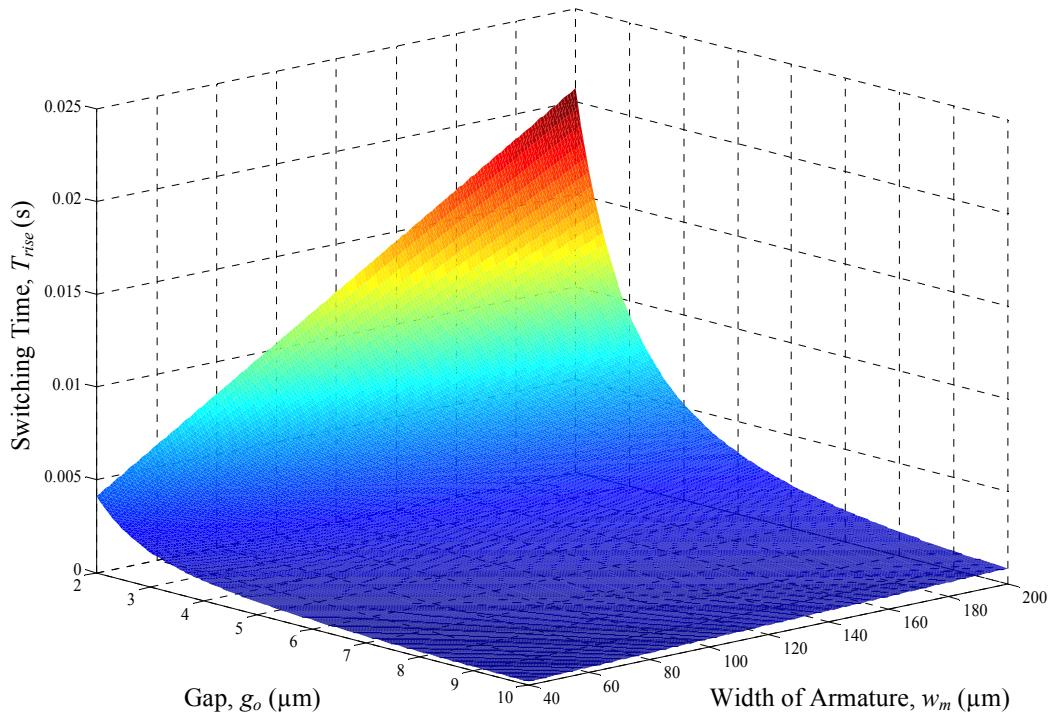


Figure 3.10: Simulated switching time of the MEMS switch as a function of the width of the armature varying from $40\mu\text{m}$ to $200\mu\text{m}$ and air gap from $2\mu\text{m}$ to $100\mu\text{m}$ with armature length = $680\mu\text{m}$.

The relationship among the width of the armature, the air gap of the switch and switching time is shown in Figure 3.10. The applied actuation voltage used in the analysis is twice of the minimum actuation voltage calculated using equation 3.13. The width of the armature increases proportionally with T_{rise} , while the T_{rise} decreases with larger air gaps. The trade-off of a large armature is a reduction in switching speed. This is due to the fact that the surface area is proportional to the damping force acting on the armature. The design value of $w_m=80\mu\text{m}$ is chosen. The dimension of the air gap is still undetermined at this stage.

Another design parameter considered is the air gap between the armature and the RF transmission line. This parameter affects not only the mechanical response of the MEMS switch but also its RF capabilities, as the RF losses are related to C_u , which is related to the initial gap height. The benefits of a large capacitive gap are:

- better capacitive ratio
- better switching time

Conversely, the drawback of an increasing initial gap results is an increase in the minimum actuation voltage (as given in equation 3.13). A cross analysis on the switching time and minimum actuation voltage is carried out to determine the gap of the switch.

Figure 3.11 shows the actuation time and the minimum actuation voltage of the MEMS switch as a function of the different capacitive gap with $l_m=680\mu\text{m}$ and $w_m=80\mu\text{m}$. The switching time line decreases with the gap increasing. The minimum actuation voltage rises proportionally, with respect to an increase in the initial gap. The initial gap was chosen at $5\mu\text{m}$, since the decrease in rate of change is less gradual in the switching time.

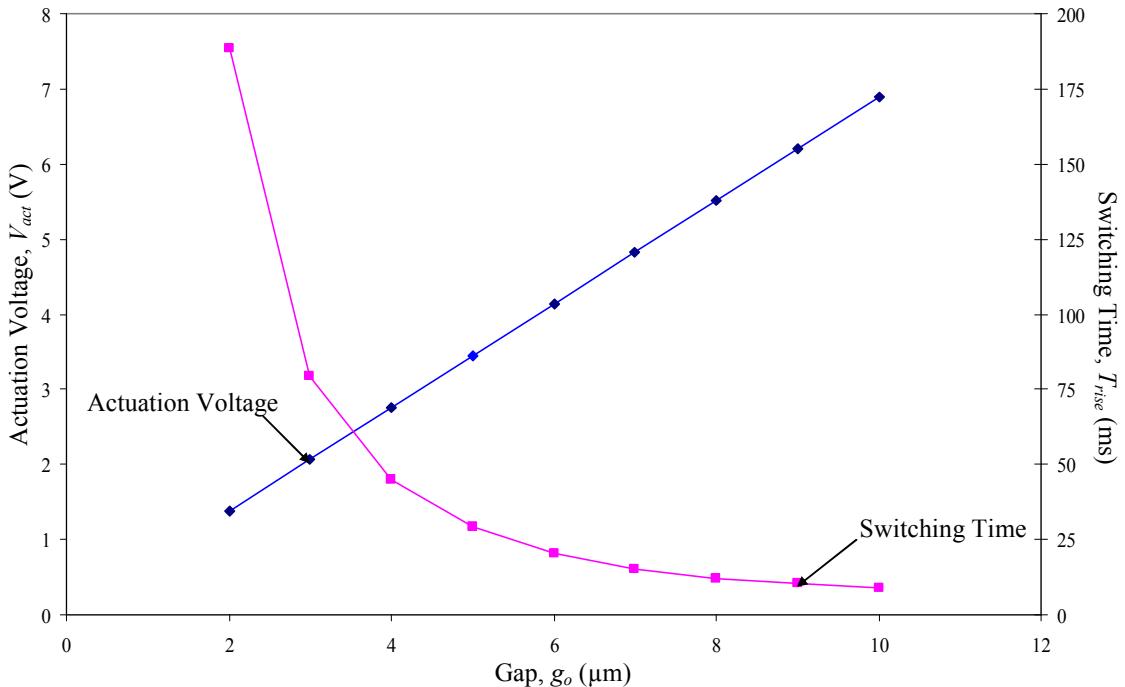


Figure 3.11: Simulated switching time and minimum actuation voltage of the MEMS switch as a function of the initial capacitive gap of the armature varying from $2\mu\text{m}$ to $10\mu\text{m}$.

The dimensions of the proposed RF MEMS switch summarized in Table 5 are based on the fabrication limitation and the analysis done in section 3.2 and 3.3. The minimum actuation voltage based on these dimensions is 3.4V without the consideration of surface adhesion forces.

Table 5: Proposed dimensions of the MEMS switch optimised based on the actuation voltage, switching speed and fabrication limitation, designed with a 75Ω coplanar waveguide.

<i>Armature Length, l_m</i>	680 μm	<i>Armature Thickness, t_m</i>	50 μm
<i>Armature Width, w_m</i>	80 μm	<i>Dielectric thickness, t_d</i>	0.2 μm
<i>Initial Gap, g_0</i>	5 μm	<i>Armature mass, m</i>	6.3e ⁻⁹ kg
<i>Transmission Line Width, G</i>	90 μm	<i>Slot width, W</i>	60 μm

3.4 Effects of Surface Adhesion Force on Actuation Voltage

Apart from the gravitational force acting on the armature, the surface adhesion force at the area of contact between the armature and dielectric layer is an interesting phenomenon observed in several works [19, 91, 92]. This section will look at the influence of such forces on the actuation voltage of the MEMS switch. Coupled with the surface adhesion model, the minimum electrostatic force required to pull up the armature can be re-written as:

$$F_{act} \geq F_{mg} + F_{contact} \quad (3.16)$$

where F_{act} is the electrostatic force, $F_{contact}$ is the surface adhesion force and F_{mg} is the force of gravity acting on the armature. As the electrostatic force is a function of the actuation voltage, the minimum actuation voltage can be re-expressed as:

$$V_{act(min)} = \sqrt{\frac{2(F_{mg} + F_{contact})g_o^2}{\epsilon_o A_{ap}}} \quad (3.17)$$

where $V_{act(min)}$ is the minimum actuation voltage, g_o is the capacitive air gap, ϵ_o is the permittivity of free space and A_{ap} is the total area of the actuation electrode.

The surface adhesion is considered to be Van De Waals forces between the contact surfaces of dielectric layer and armature [92]. It is given as:

$$F_{contact} = \frac{H_{vdW123} A_{contact}}{6\pi D^3} \quad (3.18)$$

where H_{vdW123} is the Hamaker constant, $A_{contact}$ is the total contact area between the armature and dielectric layer and D is considered as the distance between the contact surfaces of the two materials. The numerical subscript 1, 2 and 3 indicate the different materials under investigation. Under normal circumstances, D can also be considered as surface roughness of the contact surface. The Hamaker constant can be calculated using:

$$H_{vdW121} = \frac{3}{4} kT \left(\frac{\epsilon_1 - \epsilon_2}{\epsilon_1 + \epsilon_2} \right)^2 + \frac{3I}{16\sqrt{2}} \frac{(n_1^2 - n_2^2)^2}{(n_1^2 + n_2^2)^{3/2}} \quad (3.19)$$

where ϵ_1 and ϵ_2 are the dielectric constant of the materials, n_1 and n_2 are the refractive index of the two materials and I is the ionization potential that is approximately $2 \times 10^{-18} \text{ J}$ for most materials. The Hamaker constant for a silicon-air-silicon and a tantalum pentoxide-air-tantalum pentoxide material system are $8.15 \times 10^{-19} \text{ J}$ and $2.48 \times 10^{-19} \text{ J}$ respectively. Although there are many studies on the Hamaker constant, they have been revolved around two materials. The analytical formula of Hamaker constant for three materials is given as an approximation derived from the results of the two sets of two materials system and can be written as [93]:

$$H_{vdW123} = \sqrt{H_{vdW121} \times H_{vdW323}} \quad (3.20)$$

The Hamaker constant of silicon-air-tantalum pentoxide material system is approximately $4.49 \times 10^{-19} \text{ J}$.

Figure 3.12 shows the relationship of the surface roughness, the contact area and the calculated actuation voltage. Considering the overlapping of the armature and the area of the actuation electrodes and coplanar waveguide, the total contact area of the armature and dielectric layer is $3.5 \times 10^{-8} \text{ m}^2$. The actuation voltage ranges from 3.5V to 227V depending on the overlapping surface roughness and contact area of the armature and the structures on the bottom substrate. Actuation voltage, either in a rough surface and a smooth surface, is affected by the surface adhesion forces at the contact interface.

However, the computed actuation voltage is also dependent on the material used. There are also works [94, 95] which involves surface treatment so as to change the surface chemistry and lower the surface adhesion force. This can in turn decrease the actuation voltage of the switch.

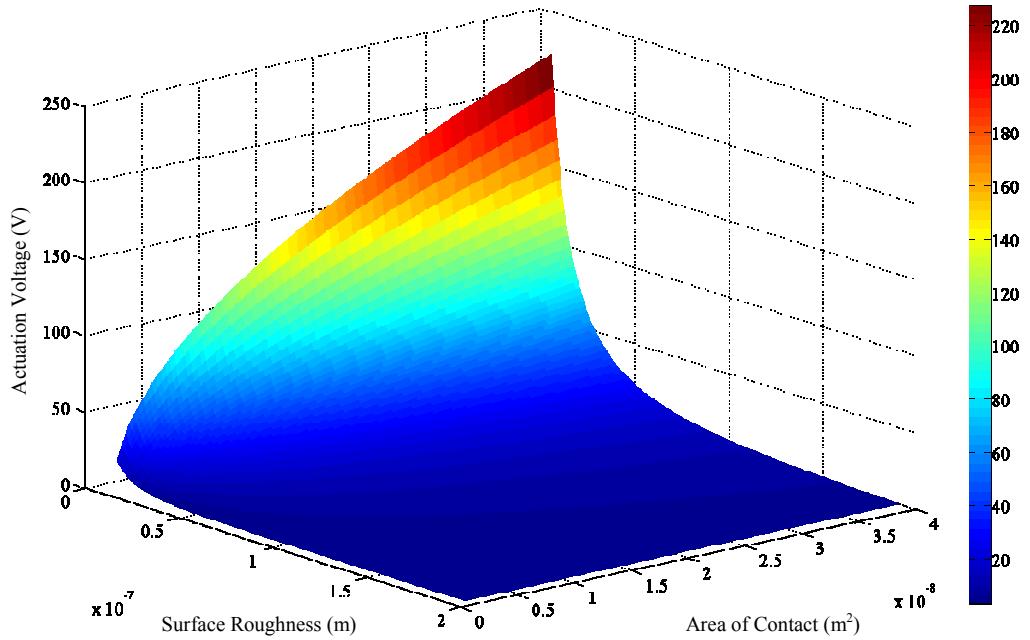


Figure 3.12: Calculated actuation voltage considering the effects of surface roughness and contact area for a silicon-air-tantalum pentoxide material system.

3.5 System Level Modelling

Most of the mechanical systems in MEMS are simplified and modelled as a spring-dashpot-mass system. The general equation of the dynamic motion to model the simplified system can be written as:

$$m\ddot{x} + b\dot{x} + kx = F_{electrostatic} \quad (3.21)$$

where m is the mass of the armature, b is the damping coefficient, k is the spring constant, x is the displacement of the armature, the superimposed dot is the $\frac{\partial}{\partial t}$ and $F_{electrostatic}$ is the electrostatic actuation force of the switch. Equation 3.22 gives the electrostatic actuation force with respect to the armature displacement:

$$F_{electrostatic} = \frac{\partial}{\partial x} \frac{1}{2} CV^2 = \frac{1}{2} \frac{\varepsilon_o A_{ap} V_{act}^2}{\left(g_o - x + \frac{t_d}{\varepsilon_r} \right)^2} \quad (3.22)$$

where ε_o is the permittivity of free space, A_{ap} is the total area of the actuation electrode, V_{act} is the applied actuation voltage, g_o is the initial capacitive gap, t_d is the thickness of

the dielectric material with dielectric constant, ε_r . The latter covers the metal electrode and prevents the armature from electrically shorting the electrodes.

The equation of the dynamic motion which governs the mechanical response of the proposed MEMS switch is rewritten as:

$$m\ddot{x} + b\dot{x} + kx = F_{electrostatic} + mG_f \quad (3.23)$$

As the armature is not suspended by a mechanical spring system, the earth gravity acting on the armature must be taken into consideration when computing the resultant force. The simulations in the following section are conducted with the switch dimensions tabulated in Table 5. The Simulink® model is attached in appendix A.

3.5.1 Squeeze Film Effects

An object, e.g. an armature, moves in the perpendicular direction of a surface, e.g. a substrate. The fluid between the armature and the substrate produces a force countering the action. This effect consists of an in phase damping force and out of phase spring force.

The respective magnitude of the forces is dependent on a dimensionless variable, which is called the Knudsen number, K_n . The Knudsen number is the ratio between the mean free path of the molecules of the fluid and the dimension of the flow conduit:

$$K_n = \frac{\lambda_o P_a}{g_0 p} \quad (3.24)$$

where λ_o is the mean free path of the air molecules at atmospheric pressure, P_a is the atmospheric pressure and p is the ambient pressure. There are four flow regimes identified by K_n number:

1. $K_n < 0.01$, it is considered to be in the continuum regime;
2. $0.01 < K_n < 0.1$, the flow is in the slip-flow regime;
3. $0.1 < K_n < 10$, the flow is in the regime which is called the transition-flow; and
4. $K_n > 10$, the flow is considered to be free molecular regime.

Figure 3.13 shows the Knudsen number varies at different ambient pressure with the corresponding flow regimes, and the capacitive gaps spacing used by MEMS switches in the range of $1\mu\text{m}$ to $5\mu\text{m}$.

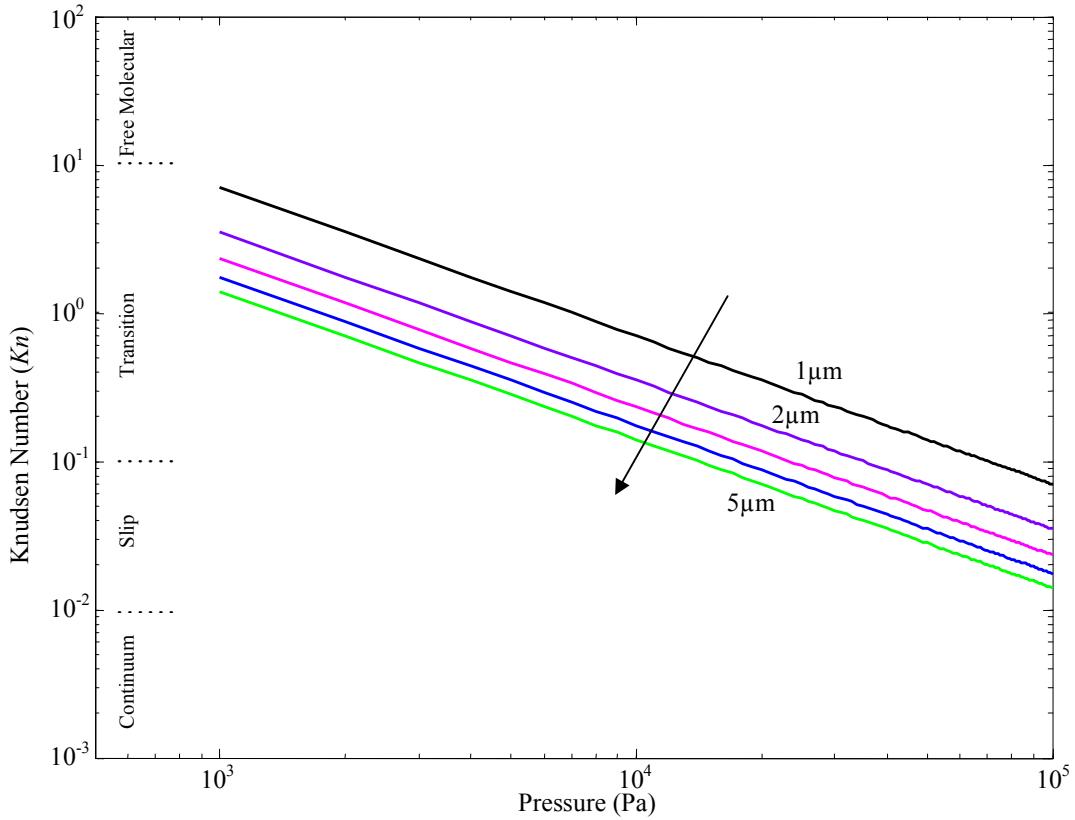


Figure 3.13: Variation of Knudsen number with pressure for gaps from 1 μm to 5 μm in 1 μm steps.

Blech [96] derives a solution to the linearised Reynolds equation for the squeeze film damping and the spring forces of rectangular plates, which are given by equations 3.25 and 3.26.

$$b = \frac{64\sigma P_a A_{arm}}{\pi^6 g_o} \sum_{n_1, n_2 = odd} \frac{n_1^2 + c^2 n_2^2}{(n_1 n_2)^2 \left[(n_1^2 + c^2 n_2^2)^2 + \frac{\sigma^2}{\pi^4} \right]} \quad (3.25)$$

$$k = \frac{64\sigma^2 P_a A_{arm}}{\pi^8 g_o} \sum_{n_1, n_2 = odd} \frac{1}{(n_1 n_2)^2 \left[(n_1^2 + c^2 n_2^2)^2 + \frac{\sigma^2}{\pi^4} \right]} \quad (3.26)$$

where n_1 and n_2 are odd integers, σ is the squeeze number, A_{arm} is the area of the armature, $c = w_m/l_m$. A key assumption made by the linearised Reynolds Equation is that the gap is small when compared to the dimension of the armature. The squeeze number, σ is given by:

$$\sigma = \frac{12\mu w_m^2 \omega}{P_a g_o^2} \quad (3.27)$$

where μ is the mean free path of the air molecules at atmospheric pressure and ω is the angular frequency which the armature switches at.

By replacing μ with μ_{eff} in equation 3.27, the equation is able to account for the gas rarefaction effect at low pressure or thin film [97]:

$$\mu_{eff} = \frac{\mu}{1 + 9.638Kn^{1.159}} \quad (3.28)$$

where μ_{eff} is the pressure dependent effective viscosity. This equation has a relative accuracy of $\pm 5\%$ and is valid for $0 < Kn < 880$.

Figure 3.14 illustrates the damping coefficient and the spring constant calculated by equation 3.25 and 3.26, with respect to the squeeze number and the operating frequency. The results indicate that the damping force dominates over the spring force for the range of operating frequencies investigated.

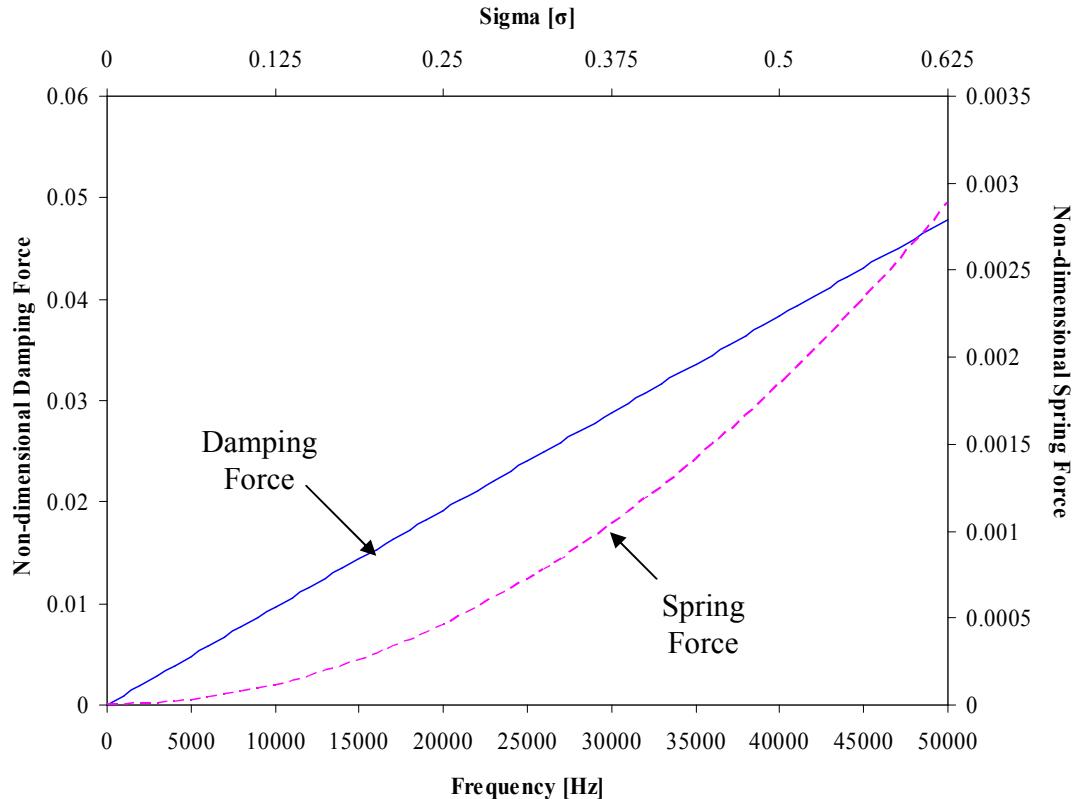


Figure 3.14: Calculation of damping coefficient and spring constant using linearised Reynolds equation from 0-50KHz. Atmospheric pressure was assumed in these simulations.

In the case of the spring-less MEMS switches, the spring force is almost negligible as the operating frequency is unlikely to be higher than 50 kHz. The numerical result for the given design shows that the spring force is negligible compared to the inertial and the damping forces.

Studies on mechanical dynamic respond have been using linearised Reynolds equation as a reference for the damping force in their design. Muldavin [19, 98, 99], introduces the damping coefficient for a pair of parallel plates for the dashpot spring model to be written as:

$$b = \frac{3}{2\pi} \frac{\mu_{eff} A_{arm}^2}{g_o^3} \quad (3.29)$$

As the damping force is dependent on the displacement of the armature, a constant damping is insufficient to provide the dynamic behaviour of the armature when it is switching. Muldavin incorporates a multiplicative displacement equation proposed by Sadd and Stiffler [100], to form a displacement compensating damping equation for modelling large displacement:

$$b = \frac{k}{\omega_o Q} \quad (3.30)$$

$$\omega_o = \sqrt{\frac{k}{m}} \quad Q = Q_o \left(1 - \left(\frac{g_o - x}{g_o} \right)^2 \right)^{\frac{3}{2}} \left(1 + 9.638 \left(\frac{\lambda}{x} \right)^{1.159} \right) \quad (3.31)$$

$$b = \frac{k}{\sqrt{\frac{k}{m}} Q_o \left(1 - \left(\frac{g_o - g}{g_o} \right)^2 \right)^{\frac{3}{2}} \left(1 + 9.638 \left(\frac{\lambda}{x} \right)^{1.159} \right)} \quad (3.32)$$

where Q_o is the nominal small displacement quality factor of the MEMS switch at $x=g_o$, ω_o is the resonating frequency of the armature at $x=g_o$ and k is the spring constant of the MEMS armature. The equation is based on an ambient pressure, which is equivalent to the atmospheric pressure. The last term in the denominator accounts for slip-flow effect. A constant of $k=5.9 \times 10^{-9} \text{ Nm}^{-1}$, which is equivalent to the squeeze film spring force calculated from equation 3.26, is used as a substitute to the mechanical spring constant since the proposed MEMS switch is a ‘spring-less’ design.

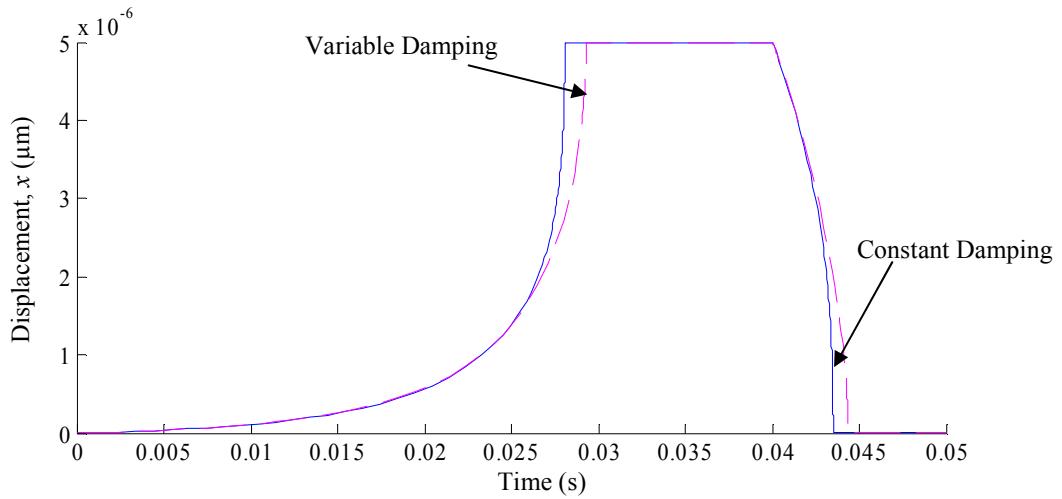


Figure 3.15: Mechanical response of the armature assuming variable damping (VD) and constant damping (CD) of the MEMS switch.

Figure 3.15 illustrates the simulated results of the switch using both the variable damping and the constant damping. The results show that the MEMS switch with variable damping requires a longer switching time than its constant damping counterpart. The difference between the two damping models used is at the last third of the switching. The switch model, using variable damping, encounters more damping force than that in the beginning two-thirds of the operation. The results show that the variable damping requires an additional 5% switching time compared to the constant damping.

The variable damping effect is able to generate more reliable result as the damping coefficient of the device is dependent on the displacement of the armature.

The simulation results using the variable damping model are compared with the calculated results using equation 3.14. When the actuation voltage is larger than the $V_{act(min)}$ shown in Figure 3.16, the two results are within 10% when V_{act} is approximately twice of $V_{act(min)}$. The equation is useful for estimation of T_{rise} during operation with a high V_{act} .

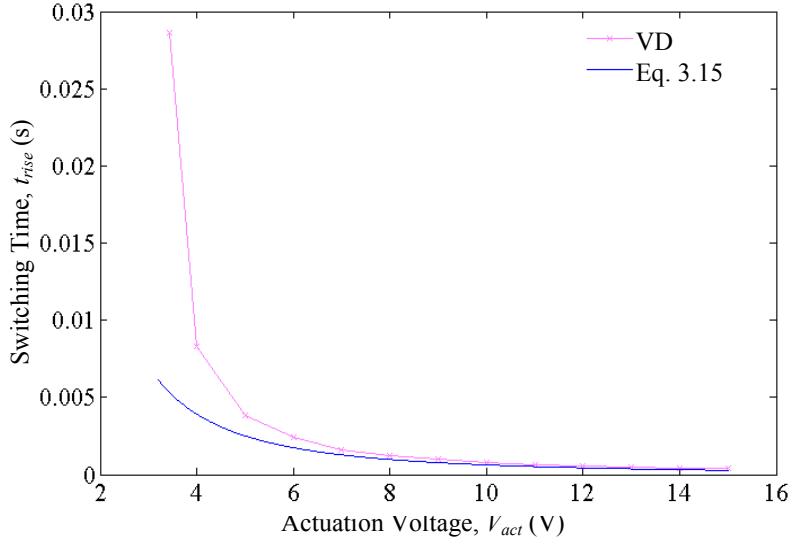


Figure 3.16: Comparison between the Simulink simulated switching time and equation 3.15 of the MEMS switch as a function of the actuation voltage varying from minimum actuation voltage, $V_{act(min)}$, to 15V.

3.5.2 Effects of Perforated Holes

Most armatures designed in RF MEMS switch have perforated holes. These holes are usually used to release the armature during the fabrication process and help to reduce the squeeze film effects which are acting on the device. Bao *et. al* [101] develops a modified Reynolds Equation, where the damping force considers the effects of perforated holes-plate.

$$b = \frac{48\mu}{g_o^3} l^2 (l_m - l)(w_m - l) \quad (3.32)$$

$$l = \sqrt{\frac{2(g_o - x)^3(t_a + 0.375\pi r_o^2)\eta}{3\beta^2 r_o^2}} \quad (3.33)$$

$$\eta = 1 + \frac{3r_o^4 K}{16t_a(g_o - x)^3} \quad (3.34)$$

where l is the characteristic length, η is a factor for the average damping pressure in a cell caused by air flow and $K = 4\beta^2 - \beta^4 - 4\ln\beta - 3$, where $\beta = r_o/r_c$. The radius of the perforated hole is given by r_o while r_c is the pitch between adjacent holes. In the

following simulation results, the diameter of the perforated hole and the pitch between adjacent holes are assumed to be 5 μm and 10 μm respectively.

If the perforated holes were considered, the simulated rise time (as shown in Figure 3.17) would be decreased to 9% of the original rise time when using a solid armature. This result indicates that the effect of the perforated holes cannot be ignored when modelling the MEMS switch. Furthermore, the inclusion of perforated holes helps to improve the switching time of the switch. The actuation time and the release time of the switch using a 50 μm thick silicon armature are tabulated in Table 6.

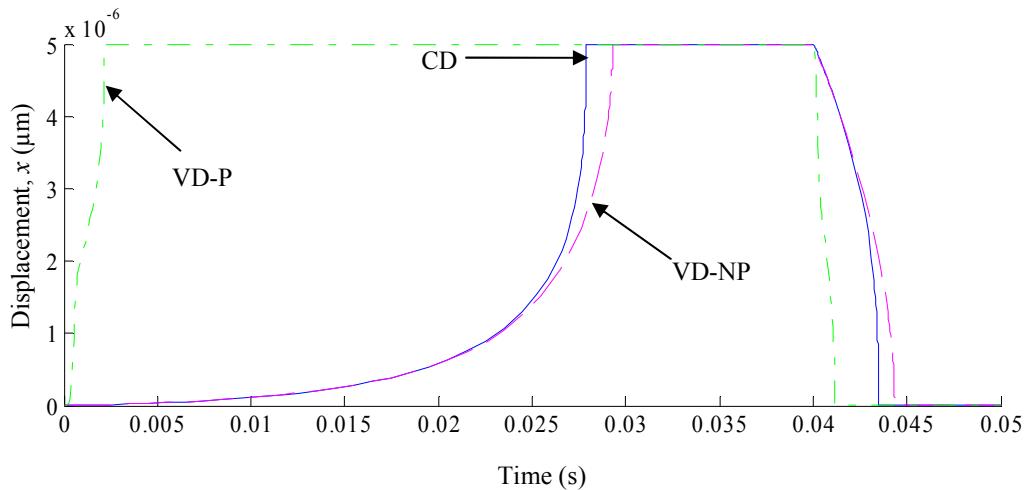


Figure 3.17: Comparison of actuation time and the release time of the MEMS switch, assuming the model using constant damping (CD), variable damping without considering perforated holes (VD-NP) and variable damping with perforated holes (VD-P).

Table 6: The simulated rise time (T_{rise}) and fall time (T_{fall}) of the proposed switch with the effect of constant damping, variable damping without perforated holes and variable damping based on the dimension tabulated in Table 5.

	CD (ms)	VD-NP (ms)	VD-P(ms)
T_{rise}	27.9	23.9	2.2
T_{fall}	3.5	4.4	1.2

The design using perforated holes in the armature shows a significant improvement in switching speed. Therefore, the perforated holes should be integrated in the design on the armature.

3.6 Summary

This chapter discusses the design considerations and electrostatic actuation mechanism of the proposed switch. The criteria for the design are established for the critical dimensions of the proposed MEMS switch based on the minimum actuation voltage and switching time.

The realisation of an electrostatic actuation mechanism for a RF MEMS switch with a mechanically unrestrained armature are examined in two configurations i) using a single top and bottom electrode and ii) using a pair of top and bottom electrodes. The latter configuration works for the actuation system yielding an attractive electrostatic force and that pull the armature towards the energised electrodes. This proves it is possible to implement an electrostatic actuation mechanism for a RF MEMS switch without mechanical suspension for the armature.

The dimensions of the switch are designed based on the minimum actuation voltage and switching time. Using the relationship between the minimum actuation voltage and the length of the armature, the length of the armature of $680\mu\text{m}$ was selected. The width and the initial gap based on the actuating time are further explored in the MEMS switch. The actuation time was simulated by various width dimensions and a positive linear relationship was observed between the width of the armature and the actuation time. Furthermore, by analysing various initial capacitive heights, the actuation time decreased with an increasing air gap, whereas a positive linear relationship appears between the minimum actuation voltage and the initial gap. In the compromised situation, the armature width of $80\mu\text{m}$ and initial gap of $5\mu\text{m}$ were selected. The minimum actuation voltage based on the 75Ω switch design is 3.4V without considering the surface adhesion forces. In contrast, when considering surface adhesion force, the minimum actuation voltage of the proposed switch ranges from 3.5V to 227V depending on the contact area and surface roughness of the contacting surfaces. Through the designing

phase, the aim of achieving a low actuation voltage switch of less than 3.5V has achieved. However the switching speed of the proposed switch is significantly slower than its counterparts due to the low actuation voltage.

A system level model, based on a lumped spring-dashpot model which was able to predict the mechanical response of the spring less RF MEMS switch, has also been described. The three damping models, namely constant damping, variable damping and variable damping with the considerations of perforation holes, have been explored based on the dimensions of the proposed switch. If the armature was designed without any perforation holes, the constant damping model would provide the best case response. However, a more realistic variable damping model describes the dynamic behaviour more accurately. For a perforated armature, the switch is able to respond faster as compared to its solid counterpart. The air spring constant for such a design has been determined.

Chapter 4

Electromagnetic Modelling

RF MEMS switches are of great interest to the commercial industry with applications in: wireless communication systems for frequencies from 0.8 to 6 GHz; instrumentation systems for frequencies from 0.01 to 50 GHz; satellite communication systems for frequencies from 12 to 35 GHz; military radar system for frequencies from 5 to 94 GHz and automotive radars for frequencies at 24, 60, and 77 GHz. For a capacitive shunt switch, typical insertion loss are at -0.1dB for frequencies up to 50 GHz, with isolation ranging from -20 to -40dB depending on the frequencies of operation.

This chapter discusses the electromagnetic aspect of the device based on the design dimensions derived in chapter 3, ensuring the initial aim of proposed switch being able to operate with insertion loss of less than -1dB and isolation better than -40dB at its electrical resonance. The electrical lumped model of the RF MEMS switch is presented in section 4.1. The scattering parameter (S-Parameter) of the proposed switch is explained in section 4.2. Section 4.3 draws a conclusion on the work performed in the chapter.

4.1 Electrical Model of the Capacitive Shunt MEMS Switch

A capacitive shunt RF MEMS switch comprises of a dielectric between the armature and transmission line. The variation in switching capacitance, depending on the UP or DOWN state of the switch's armature, determines the intensity of the RF signal passing through the transmission line. The armature in the conventional MEMS shunt

switch design illustrated in Figure 4.1(a) is grounded via its anchor to the substrate, whereas the proposed MEMS switch depicted Figure 4.1(b) is not physically grounded. The RF signal travels through the signal line of the transmission line during the UP state or through the armature of the switch into the ground planes via the dielectric layer during the DOWN (shunt) state. The lumped electrical model of the proposed RF MEMS switch can be modelled as shown in Figure 4.1(c). The model considers the characteristic impedance of the transmission line (Z_o), attenuation of the transmission line (α), as well as the impedance of the armature (Z_b). The impedance of the armature can be defined by the resistance of the armature, the inductance of the armature and the capacitance between the transmission line structure and the armature. It is given in equation 4.1.

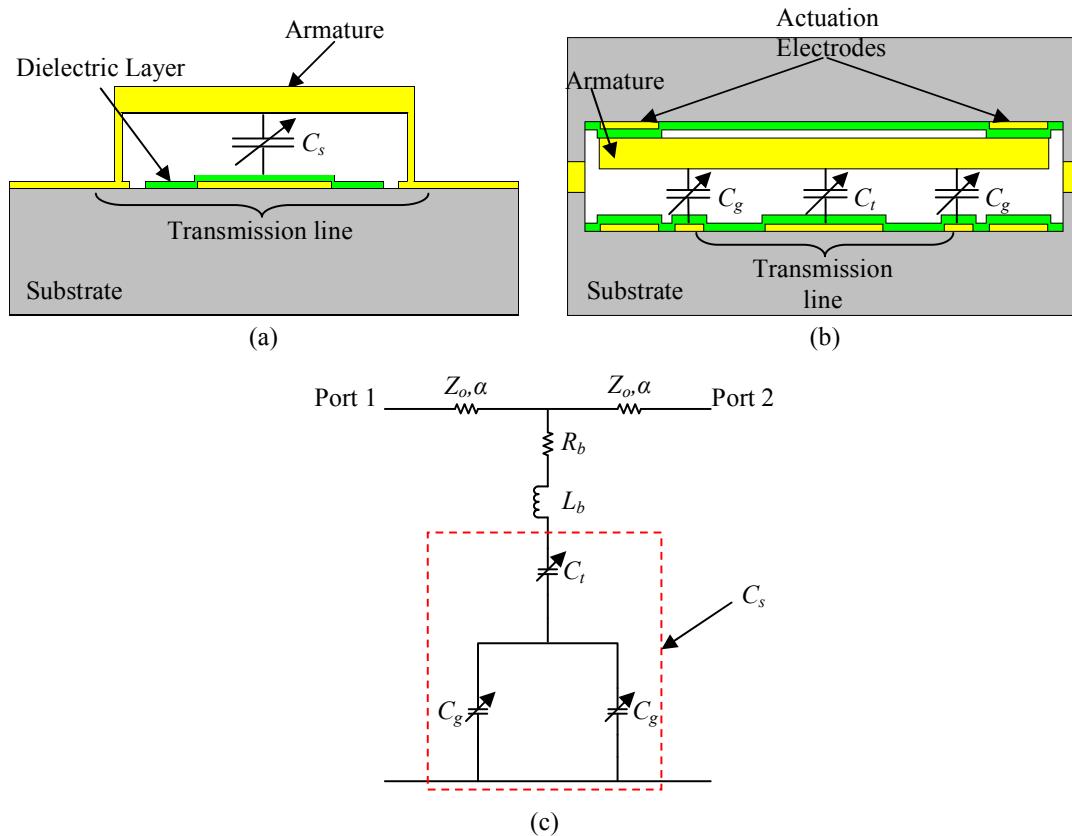


Figure 4.1: Cross section of (a) a conventional RF MEMS shunt switch (b) Proposed RF MEMS shunt switch. (c) Electrical equivalent circuit of the proposed RF MEMS shunt switch.

$$Z_b = R_b + j\omega L_b + \frac{1}{j\omega C_s} \quad (4.1)$$

where R_b is resistance of the armature, L_b is the inductance of the armature and C_s is the switching capacitance of the armature.

4.1.1 Designing of Coplanar Waveguide

There are many types of transmission line designs available for monolithic microwave integrated circuit. The most common types are strip line, microstrip, slot line, coplanar strips and coplanar waveguide. Each type has their advantages and disadvantages in terms of operating frequency, dimension, loss, ability to integrate with other technology. The coplanar waveguide design has excelled among the few common designs with its ability to incorporate CMOS circuitry as well as discrete components packaged directly onto the substrate [102].

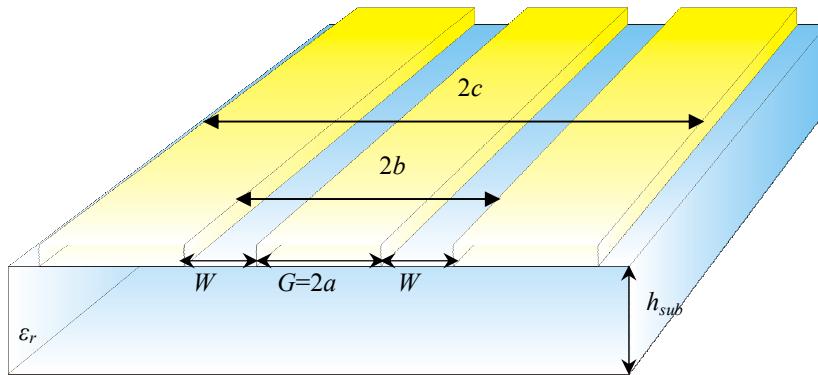


Figure 4.2: 3-D cross sectional illustration of a finite width coplanar waveguide.

C.P. Wen [103] proposed the coplanar waveguide (CPW) design (as shown in Figure 4.2), which fabricates a conducting layer on a substrate. The conducting layer consists of a centre signal strip flanked by two semi-infinite wide ground planes. With much interests and studies done on the topic, some other variant of the transmission line are tabulated in Table 7.

Table 7: Different types of coplanar waveguide design

Conventional CPW	Conductor back CPW	Micromachined CPW
<ul style="list-style-type: none"> • Coplanar waveguide with finite width ground plane (FW-CPW) 	<ul style="list-style-type: none"> • Conductor back coplanar waveguide (CB-CPW) • Conductor back coplanar waveguide with finite width ground plane (CBFW-CPW) 	<ul style="list-style-type: none"> • Coplanar waveguide suspended in a conducting enclosure

A general rule for determining the dimensions of the width of the signal line (G) and slot width (W) is $h_{sub} > G + 2W$, where h_{sub} is the thickness of the substrate [102]. This allows the characteristic impedance to be independent from variation of the substrate thickness. The dimensions of G and W are then established by the predetermined characteristic impedance of the transmission line and permittivity of the substrate.

Characteristic Impedance

The characteristic impedance (Z_o) is the ratio of the amplitudes of a single pair of voltage and current waves propagating along a uniform transmission line. Simple analytic equations can be approximated using the conformal mapping method with the CPW which is assumed to be propagating in a quasi-static TEM mode [104].

Under this assumption, the effective permittivity of the CPW structure is defined as [104]:

$$\varepsilon_{eff} = \frac{C_{cpw}}{C_{air}} \quad (4.2)$$

where C_{cpw} is the total capacitance of the transmission line per unit length and C_{air} is the capacitance in absence of the substrate per unit length. C_{air} can be calculated as [104]:

$$C_{air} = 4\varepsilon_o \frac{K(k)}{K(k')} \quad (4.3)$$

$$k = \frac{c}{b} \sqrt{\frac{b^2 - a^2}{c^2 - b^2}} \quad (4.4)$$

$$k' = \sqrt{1 - k^2} = \frac{a}{b} \sqrt{\frac{c^2 - b^2}{c^2 - a^2}} \quad (4.5)$$

where K is the complete elliptic integral of the first kind, k and k' are the variables depending on the geometry of the line. C_{cpw} can be computed as [104].:

$$C_{cpw} = 2\varepsilon_o (\varepsilon_r - 1) \frac{K(k_1)}{K(k_1)} \quad (4.6)$$

where

$$k_1 = \frac{\sinh(\pi c / 2h)}{\sinh(\pi b / 2h)} \sqrt{\frac{\sinh^2(\pi b / 2h) - \sinh^2(\pi a / 2h)}{\sinh^2(\pi c / 2h) - \sinh^2(\pi a / 2h)}} \quad (4.7)$$

$$k_1' = \sqrt{1 - k_1^2} = \frac{\sinh(\pi a / 2h)}{\sinh(\pi b / 2h)} \sqrt{\frac{\sinh^2(\pi c / 2h) - \sinh^2(\pi b / 2h)}{\sinh^2(\pi c / 2h) - \sinh^2(\pi a / 2h)}} \quad (4.8)$$

By substituting equation 4.3 and 4.6 into 4.9,

$$\epsilon_{eff} = 1 + \frac{1}{2} (\epsilon_r - 1) \frac{K(k)K(k_1')}{K(k')K(k_1)} \quad (4.9)$$

The characteristic impedance of a coplanar waveguide is given as [104]:

$$Z_o = \frac{1}{C_{cpw}v_{ph}} \quad (4.10)$$

$$v_{ph} = \frac{c}{\sqrt{\epsilon_{eff}}} \quad (4.11)$$

where v_{ph} is the phase velocity and c is the speed of light in vacuum, approximated at 3×10^8 m/s [104].

$$Z_o = \frac{30\pi}{\sqrt{\epsilon_{eff}}} \frac{K(k')}{K(k)} \quad (4.12)$$

Figure 4.3 shows a plot of the characteristic impedance of the FW-CPW based on equation 4.12 which is over a range of signal line width (G) and slot width (W). The analysis considers Pyrex as the substrate material with standard thickness of 500 μ m and a ground plane width of 250 μ m. The trend shows that the characteristic impedance of the CPW increases with the slot width increasing, while the characteristic impedance of the CPW decreases with an increase in signal line width. However, the changes will be less pronounced when the dimension of the signal line increases. To design a CPW with Z_o of 50 Ω and 75 Ω using a 90 μ m wide signal line, the slot width (W) will be approximately 15 μ m and 60 μ m respectively.

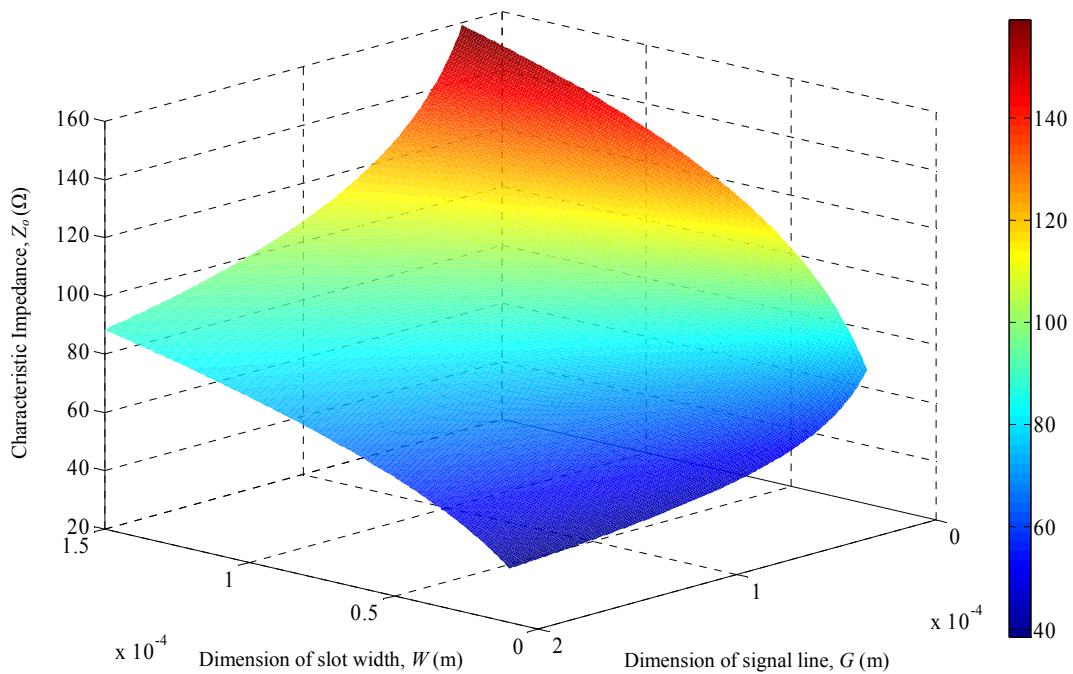


Figure 4.3: A three dimensional plot showing the characteristic impedance of a finite width conductor backed coplanar waveguide, with respect to the dimension of signal line and slot width using equation 4.12, for width of the ground plane = 250 μ m and $\epsilon_r = 4.82$.

Finite element modelling is also employed to verify the analytic formulae given in equation 4.9 and 4.12. The capacitance simulating model using COMSOL is shown in Figure 4.4(a). The signal line is applied with a 1V and the ground plane is set to 0V. The effective dielectric constant is calculated by taking the proportion of capacitance of the structure when all dielectrics are assumed to be air and the capacitance when substrate is filled with dielectric material property. The characteristic impedance is derived by implementing equation 4.10. Figure 4.4 shows the characteristic impedance and effective permittivity plotted over a range of slot width, given by a fixed signal line of 90 μ m fabricated on a 500 μ m Pyrex substrate. The plot illustrates that the characteristic impedance and effective permittivity increase with the slot width increasing. This finding is similar to those using the analytical formulae of equation 4.12.

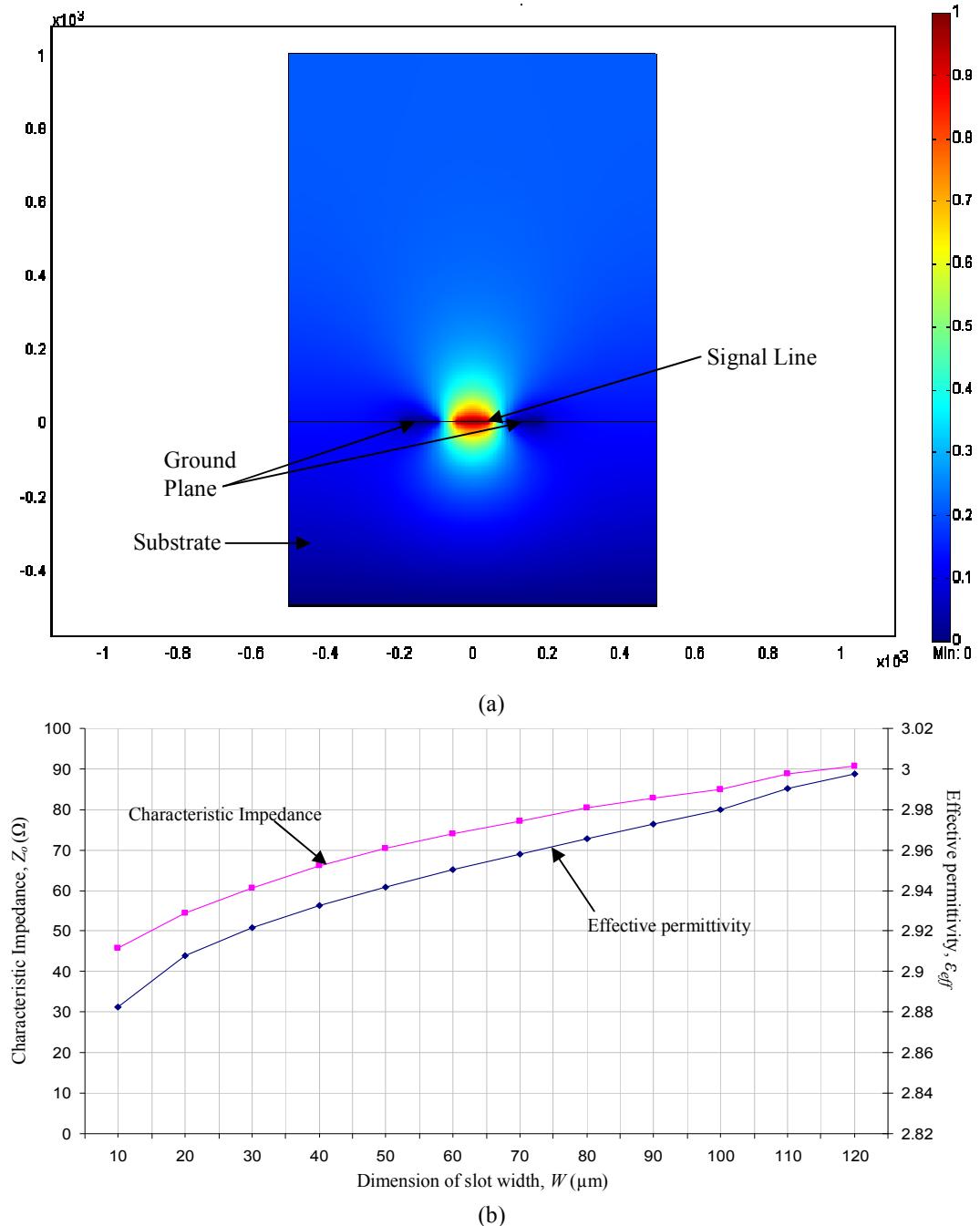


Figure 4.4 : (a) Electrical potential of a finite width coplanar waveguide using COMSOL when the signal line applied with 1V and the ground plane is set to 0V (b) Simulated characteristic impedance and effective dielectric constant of a finite width coplanar waveguide with $G= 90 \mu\text{m}$ over a range of slot width using COMSOL.

Losses in Transmission Line

Apart from the resistive losses in the armature, signal loss also occurs during the propagation due to the resistance of the transmission line and substrate material. This loss is known as attenuation. The total attenuation constant for the transmission line (α) can be written as [105]:

$$\alpha = \alpha_c + \alpha_d \quad (4.13)$$

where α_d is the attenuation constant due to substrate loss and α_c is the attenuation due to conductor loss. The equation for calculating α_d can be written as [105]:

$$\alpha_d = \frac{\pi}{2\lambda_o} \frac{\epsilon_r}{\sqrt{\epsilon_{eff}}} \frac{K(k)K(k'_1)}{K(k')K(k_1)} \tan \delta \quad (4.14)$$

where λ_o is the free space wavelength and $\tan \delta$ is the dielectric tangent loss of the substrate. The expression for α_c considering both signal line and ground plane is given as [105]:

$$\alpha_c = \frac{R_c + R_g}{2Z_o} \quad (4.15)$$

where R_c is the series resistance of the centre signal line and R_g is the distributed resistance of the ground plane. Both factors are in ohm per meter and are written as [105]:

$$R_c = \frac{R_s(\sigma\delta)^{-1}}{4G(1-k_o^2)K^2(k_o)} \left[\pi + \ln\left(\frac{4\pi G}{t}\right) - k_o \ln\left(\frac{1+k_o}{1-k_o}\right) \right] \quad (4.16)$$

$$R_g = \frac{k_o(\sigma\delta)^{-1}}{4G(1-k_o^2)K^2(k_o)} \left[\pi + \ln\left(\frac{4\pi(G+2W)}{t}\right) - \frac{1}{k_o} \ln\left(\frac{1+k_o}{1-k_o}\right) \right] \quad (4.17)$$

Figure 4.5(a) shows the attenuation of the coplanar waveguide with thickness of conductors of 500nm on a Pyrex substrate over a range of signal width (G) and slot width (W). The plot shows that a narrow signal line leads to high attenuation. This can be compensated by having a small slot width. The resistance of the coplanar waveguide conductors, R_{cpw} , based on the length of the transmission line of 2mm over a range of G and W , is illustrated in Figure 4.5(b). Similar observations to the attenuation plot are

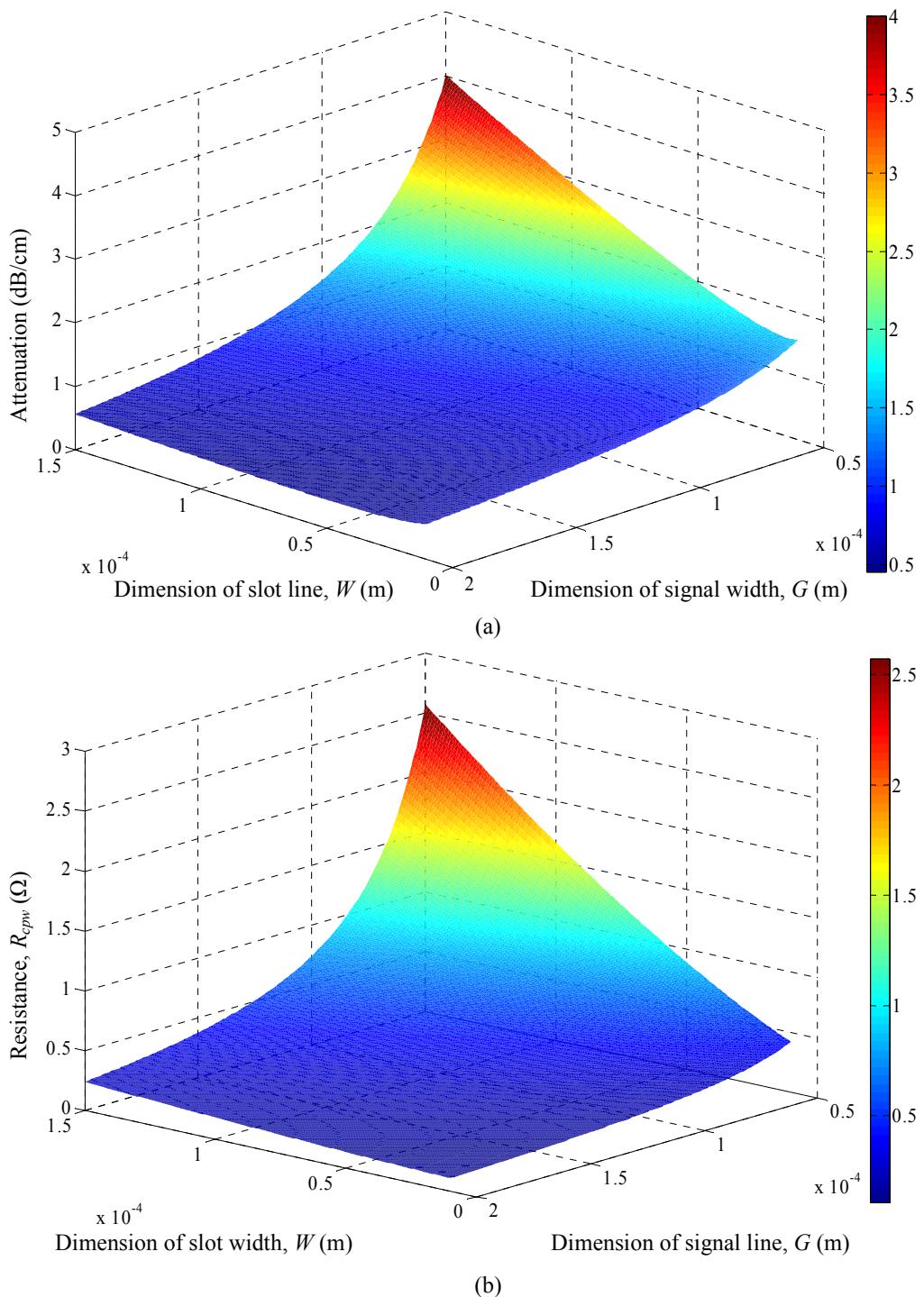


Figure 4.5: (a) Attenuation of the coplanar waveguide with thickness of conductors of 500nm on Pyrex substrate over a range of signal line width, G , and slot width, W based on equation 4.13. (b) Resistance of the coplanar waveguide conductors, R_{cpw} , based on the length of the transmission line of 2mm over a range of signal line width, G , and slot width, W .

made on the resistance of the coplanar waveguide conductors. The α and R_{cpw} of a 2mm 50Ω transmission line for the proposed design are approximately 1dB/cm and 0.25Ω for the proposed switch. The losses in transmission line must be kept to the minimum, as it is directly affecting the RF characteristic of the RF MEMS switch.

4.1.2 Switching Capacitance

For most of the RF MEMS shunt switch design [55, 56], the calculation of switch's capacitance can be simply considered as a parallel plate capacitor. The dielectric layer that is between the parallel plates is either an insulating layer only or an insulating layer with an air gap, depending on the operational state of the switch. This is due to the design of the device, where the armature is physically connected to the ground plane and creating a real ground reference to the transmission line. Their values can be calculated using equation 4.18 and 4.19.

$$C_d = \frac{\epsilon_0 \epsilon_r A_c}{t_d} \quad (4.18)$$

$$C_u = \frac{\epsilon_0 A_c}{g_o + t_d / \epsilon_r} \quad (4.19)$$

where ϵ_0 is the permittivity of free space, g_o is the initial capacitive gap, A_c is the area of the armature contacting the transmission line, t_d is the thickness of the dielectric material with dielectric constant, ϵ_r .

However, in the case of the spring-less RF MEMS switch, the armature is not physically attached to any structure. The shunt signal has to propagate from the transmission line to the ground plane through i) the air gap between the transmission line and armature ii) the air gap between the armature and the ground plane as shown in Figure 4.1(b). The formulae for the UP and DOWN state capacitance are modified based on equations 1.18 and 1.19 to account for the additional series capacitive path.

$$C_d = \frac{\epsilon_0 \epsilon_r A_c A_r}{t_d (A_r + A_c)} \quad (4.20)$$

$$C_u = \frac{\varepsilon_o A_c A_r}{\left(g_o + \frac{t_d}{\varepsilon_r}\right)(A_r + A_c)} \quad (4.21)$$

where A_c and A_r are the areas in which the armature contacts the transmission line and the ground line, respectively.

When the armature is in the UP state position, a fringe capacitance (C_f) is presented in the RF MEMS switch. There are designs with the fringing capacitance up to 20-50% of the C_u [106]. Table 8 shows the simulated and calculated C_u of the proposed RF MEMS switch design for different armature width and capacitive gap, using COMSOL and equation 4.21. The design parameters used for the analysis are armature length of 680 μm , width of the CPW's signal line and ground plane is 90 μm and 10 μm respectively. The area of the armature overlapping the ground plane is $2 \times 10\mu\text{m} \times w_m$, area of the armature overlapping the signal line is $90\mu\text{m} \times w_m$. The dielectric layer used is silicon nitride with a permittivity of 7.6 and a thickness of 200nm. From the tabulated results, the simulated C_u is approximately 15% more than the calculated C_u for a capacitive gap of 2 μm while the fringing capacitance accounts for an additional 29% of UP state capacitance for a 5 μm gap. These values are similar to those reported in [106]. Hence it can be deduced that fringing capacitance increases with gap height increasing.

Table 8: Simulated and calculated UP state capacitance for different armature width and gap height with dimensions of armature length, $l_m=680\ \mu\text{m}$, CPW's signal line width=90 μm , CPW's ground plane width=10 μm $\varepsilon_r=7.6$ and $t_d=200\text{nm}$.

Armature Width, w_m	Gap Height, g_o	Simulated C_u	Calculated C_u	Fringing Capacitance, $C_f = (\text{Simulated } C_u - \text{Calculated } C_u)$
40 μm	2 μm	4.5fF	3.9fF	0.6fF
80 μm	2 μm	9.2fF	7.9fF	1.3fF
120 μm	2 μm	13.8fF	11.8fF	2fF
40 μm	5 μm	2.1fF	1.6fF	0.5fF
80 μm	5 μm	4.2fF	3.2fF	1.0fF
120 μm	5 μm	6.2fF	4.8fF	1.4fF

In the design of a RF MEMS switch, a large capacitance ratio is beneficial as a large DOWN state capacitance decreases the impedance of the armature, which

encourages the shunting of RF signal. The capacitance ratio is the ratio between DOWN state capacitance and UP state capacitance and is given as:

$$\frac{C_d}{C_u} = C_{ratio} = 1 + \frac{g_o \epsilon_r}{t_d} \quad (4.22)$$

Three parameters determine the ratio, i.e. air gap, permittivity of dielectric material and thickness of dielectric layer. It is not effective that the capacitance ratio is manipulated by the air gap or the thickness of the dielectric material. This is due to the fact that a larger air gap compromises the actuation voltage of the switch. Thin dielectric layers of approximately 100nm often provide insufficient coverage on the bottom layer and leads to the formation of pinhole. As mentioned in Chapter 2, researches on using high-K dielectrics to improve the capacitance ratio are carried out. If a 200nm of Silicon Nitride (Si_3N_4) was used with a capacitive gap of $5\mu m$, the capacitive ratio would be 191. However if a high k-dielectric, e.g. Tantalum Pentoxide (Ta_2O_5) was used, the capacitive ratio would increase to 625. The fabricated switch is not able to achieve such high ratio due to imperfect surface contacts between the armature and dielectric layer. Such imperfection is usually caused by surface roughness, d_r . An equation is derived from [106] to consider surface roughness of the proposed design.

$$C_{down_rou} = \frac{\epsilon_o A_r A_c}{2(A_r + A_c)} \left(\frac{1}{d_r + \frac{t_d}{\epsilon_r}} + \frac{\epsilon_r}{t_d} \right) \quad (4.23)$$

The surface roughness only affects the DOWN state capacitance, while the air gap capacitance is the dominating factor in the setup during the UP state operation. If the dielectric surface is approximately $5nm$ [107-109], the DOWN state capacitance for a Si_3N_4 or Ta_2O_5 based switch would be $0.41pF$ and $1.2pF$ respectively based on the dimensions of the proposed switch. The realistic capacitive ratios are approximately 176 and 505 respectively.

4.1.3 Resistance of the Armature

The resistance of the armature can be simply calculated using:

$$R_b = \frac{\rho L}{A} \quad (4.24)$$

where ρ is the resistivity of the material, L is the length of the conducting path and A is the cross sectional area of the armature. However, equation 4.24 is not sufficient for electromagnetic analysis for RF devices, as the parameter is affected by the high frequency skin effect.

When an alternating current (AC) source is applied to the conductor, a skin effect is established where the current density tends to distribute near the surface rather than the core of the conductor. The skin effect is due to a magnetic field established by the alternating current. The magnetic field creates an opposing electric field to the original electric field, cancelling the flowing of current in the core of the conductor.

The skin effect [110] is illustrated in Figure 4.6, which shows a signal applied to the top surface of a $1\mu\text{m}$ thick Gold conductor. The signal is a direct current (DC) source in Figure 4.6(a); an AC source with a frequency of 1GHz in Figure 4.6 (b); an AC source with a frequency of 10GHz in Figure 4.6(c); an AC source with a frequency of 100GHz in Figure 4.6(d). The current flows uniformly through the structure when the DC source is applied. From Figure 4.6(b)-(d), the distance of the current flow from the surface of the conductor decreases with respect to an increasing frequency. When an alternating source is used and the frequency increases, the current density concentrates near the surface of the conductor. The distance where the current density is reduced to approximate 37% of the current density at the surface is known as skin depth (δ) and can be calculated using [111]:

$$\delta = \frac{1}{\sqrt{f\mu\sigma}} \quad (4.25)$$

where μ is the absolute magnetic permeability of armature material, σ is the electrical conductivity of the material of propagation and f is the frequency of the RF signal. By substituting the skin depth formula into equation 4.24, the impedance of the armature encompassing the skin effect is derived.

$$R_b = \frac{\rho L}{w\delta} \quad (4.26)$$

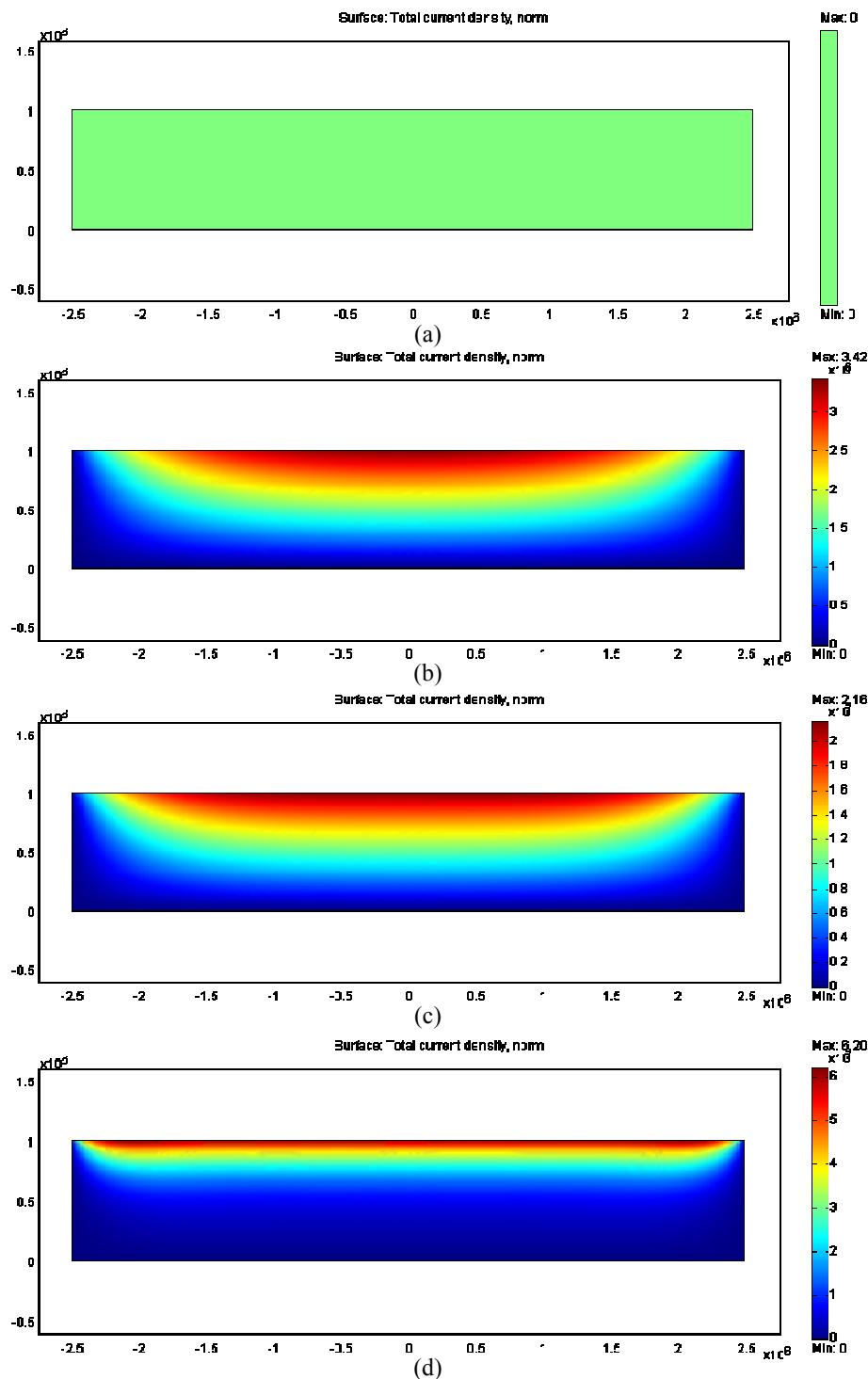


Figure 4.6: FEMLAB simulation of skin effect of a current transmitting through a $1 \mu\text{m}$ thick Gold conductor at (a) DC, (b) 1GHz, (c) 10GHz and (d) 100GHz.

Figure 4.7 shows the skin depth measurement of the four different materials, i.e. copper, gold, aluminium and highly conductive silicon (10000S/m), over a range of frequencies up to 100GHz. The skin depth values of the 3 metallic materials are relatively similar and that of the highly doped silicon is larger by an order of magnitude. This is because the electrical conductivity of the highly doped silicon is two orders of magnitude lower than the metal counterparts. The skin effect is more prominent for materials with lower conductivity. The absolute value of R_b is not significant, as it varies with the frequency of the RF signal. The reported R_b values in literatures are usually related to the magnitude of isolation when the switch is at its DOWN state electrical resonating frequency. Nominal R_b value of a RF MEMS switches are in the range of 0.1-2.0Ω [39].

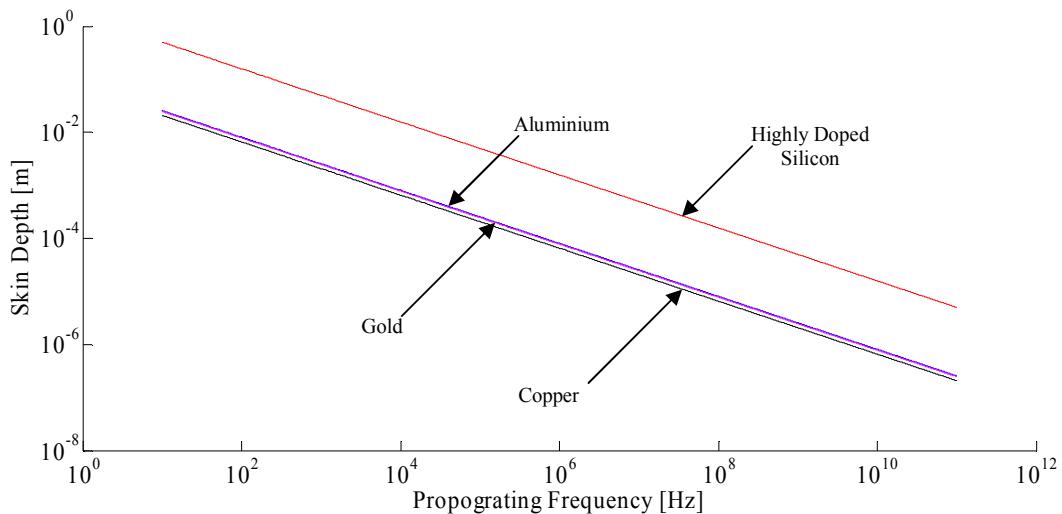


Figure 4.7: Skin depth of various materials that can be used as armature with respective to propagating frequency from 10Hz to 100GHz based on equation 4.25.

4.1.4 Inductance

Inductance is formed when an electric current travels the circuit. For the case of a RF MEMS switch, inductance is formed when the armature is in the DOWN state position. The RF signal is shunted from the signal line to the ground plane via the armature. The armature inductance is very difficult to derive mathematically [111], however it can be approximated with some degree of accuracy using equation 4.27 [112]:

$$L_b = \frac{\mu_0 L}{2\pi} [\ln(2L) - \ln(p) - 1] \quad (4.27)$$

$$\ln\left(\frac{p}{c}\right) = -\frac{25}{12} - \frac{1}{6} \left\{ \left(\frac{w_m}{t_m} \right)^2 \ln \sqrt{1 + \left(\frac{t_m}{w_m} \right)^2} + \left(\frac{t_m}{w_m} \right)^2 \ln \sqrt{1 + \left(\frac{w_m}{t_m} \right)^2} \right\} + \frac{2}{3} \left\{ \frac{w_m}{t_m} \arctan\left(\frac{t_m}{w_m}\right) + \frac{t_m}{w_m} \arctan\left(\frac{w_m}{t_m}\right) \right\} \quad (4.28)$$

where $c = \sqrt{w_m^2 + t_m^2}$, w_m is the width of the armature, t_m is the thickness of the armature and $L = 2W$. Figure 4.8 shows the inductance values of a 50μm thick armature with respect to a range of slot width and armature width. The plot shows that the switch inductance is less than 20pH in most designs with the armature kept as a solid rectangular slab. The inductance of the armature based on the dimensions of the proposed switch with a 60μm slot width and 80μm armature width is 6.5pH.

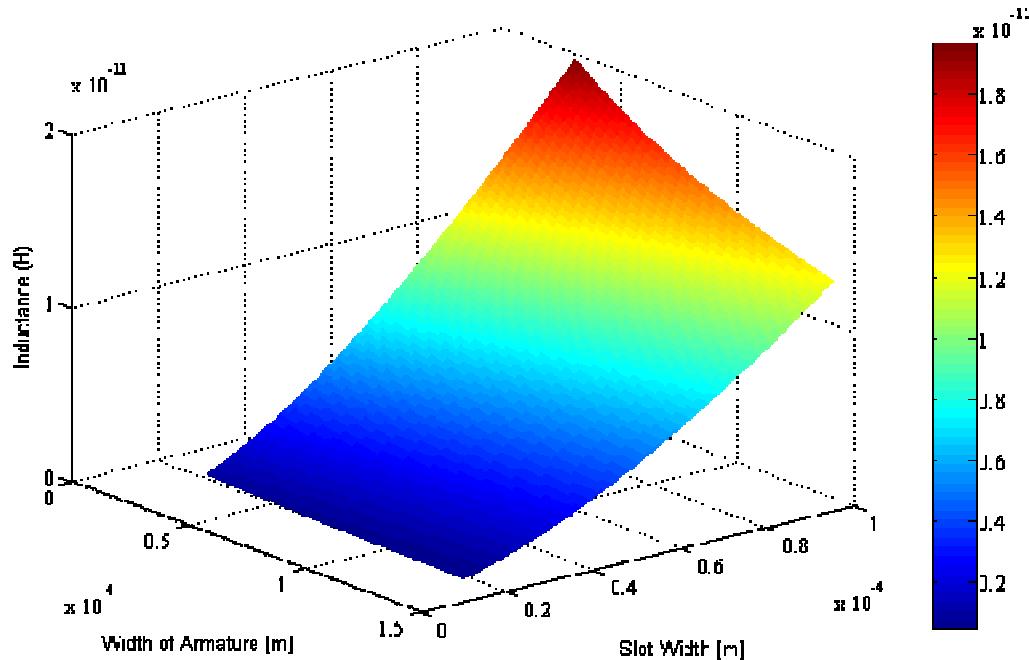


Figure 4.8: Calculated switch inductance for a 50μm thick armature over a range of possible slot width and armature width based on equation 4.27.

The electrical lumped model of the proposed RF MEMS switch has been defined by the values of the individual components calculated. For the proposed switch with a 75Ω coplanar waveguide using Ta_2O_5 as the dielectric material, the UP state capacitance is $2.3fF$, the DOWN state capacitance is $1.44pF$, the armature inductance is approximately $6.5pH$ and the armature resistance is 0.66Ω at $77GHz$

4.2 RF Characteristic of the Proposed Switch

The scattering parameters (S-parameters) determine the RF characteristic of the switch. The switch can be modelled as a two port network with a shunt network. The S_{11} parameter denotes the return loss of the switch in both operating states, while the S_{21} parameter represents the insertion loss at UP state position and isolation at DOWN state position of the armature. The subscript 11 or 21 refers to the port number as shown Figure 4.9. S_{11} and S_{21} are defined as [113]:

$$S_{11} = -20 \log \left| \frac{-Z_o}{2Z_b + Z_o} \right| \quad (4.29)$$

$$S_{21} = -20 \log \left| \frac{2Z_b}{2Z_b + Z_o} \right| \quad (4.30)$$

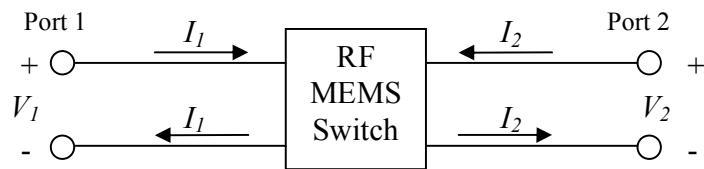


Figure 4.9: Two-Port network for the RF MEMS Switch.

The return loss is defined as the reflected power over the incident power in a transmission line. In the case of a RF MEMS switch, Z_b is the impedance of the armature. When the armature is not actuated, the resistance and inductance are negligible as the armature does not have any physical contact with the dielectric layer. Therefore, no

current passes through the armature. The UP state return loss of a capacitive shunt switch with the impedance of the armature substituted into equation 4.29, can be written as [113]:

$$S_{11} = -20 \log \left| \frac{-j\omega C_u Z_o}{2 + j\omega C_u Z_o} \right| \quad (4.31)$$

where S_{11} is the magnitude of the return loss, ω is the angular frequency of the RF signal, Z_o is the characteristic impedance of the transmission line and C_u is the UP state capacitance of the MEMS switch.

The isolation and insertion loss are defined as the transmitted power over the incident power in a transmission line. By substituting the armature impedance into the equation 4.30 depending on DOWN or UP state, the isolation or insertion loss can be calculated respectively. Equations 4.32-4.34 calculate the isolation of the capacitive shunt MEMS switch depending on the frequency of the RF signal [113].

$$S_{21} = \begin{cases} -20 \log \left| \frac{2}{2 + j\omega C_d Z_o} \right| & \text{for } f \ll f_o \\ -20 \log \left| \frac{2R_s}{R_s + Z_o} \right| & \text{for } f = f_o \\ -20 \log \left| \frac{2j\omega L_b}{Z_o + 2j\omega L_b} \right| & \text{for } f \gg f_o \end{cases} \quad (4.32)$$

$$(4.33)$$

$$(4.34)$$

where S_{21} is the magnitude of the isolation and C_d is the DOWN state capacitance. f_o is the LC series resonating frequency of the switch given by:

$$f_o = \frac{1}{2\pi\sqrt{L_b C_s}} \quad (4.35)$$

The capacitance value C_s is dependent on the actuation state of the MEMS switch. Unlike the UP state resonance frequency, the DOWN state resonating frequency is usually within the possible operating range of the transmission line. Hence, the DOWN state S_{21} must consider all possible operating range of the transmission line.

The return loss, insertion loss and isolation of the proposed MEMS switch on a 50Ω and a 75Ω coplanar waveguide are presented in the following simulation. S-

Parameter simulation for the 50Ω switch based on dimensions tabulated in Table 5 are presented, with the exception of the slot width (W) being $15\mu\text{m}$.

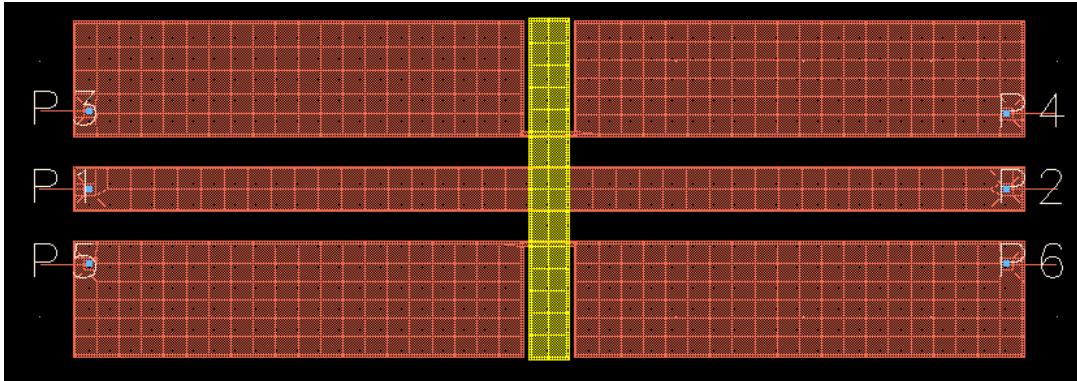


Figure 4.10: ADS Momentum model of the proposed RF MEMS switch with a 50Ω coplanar waveguide.

Figure 4.10 depicts the ADS Momentum model of the proposed switch with a 75Ω coplanar waveguide. The orange structure represents the coplanar waveguide while the yellow strip is the silicon armature. P1 represents the port 1 with corresponding P3 and P5 are the ground reference to P1. P2 represents the port 2 with corresponding P4 and P6 are the ground reference to P2.

Figure 4.11 shows the S-Parameters of a 75Ω RF MEMS switch. The RF simulation is carried out from 0.1GHz to 100 GHz. During the UP state operation, the return loss peaks at -5.9dB when the frequency is at 72GHz. The switch insertion loss is $<-1.96\text{dB}$ at 75GHz. During DOWN state operation, the return loss is less than -0.3 dB and isolation is -46dB at a resonant frequency of 77GHz.

Figure 4.12 depicts the ADS Momentum model of the proposed switch with a 50Ω coplanar waveguide. The difference between the two models is the dimension of the slot width, where the dimensions of 75Ω switch design is $60\mu\text{m}$ and that for 50Ω is $15\mu\text{m}$. The 50Ω variation, not optimised though, is able to switch with a lower actuation voltage as the area of the actuation electrode will be greater the 75Ω counterpart.

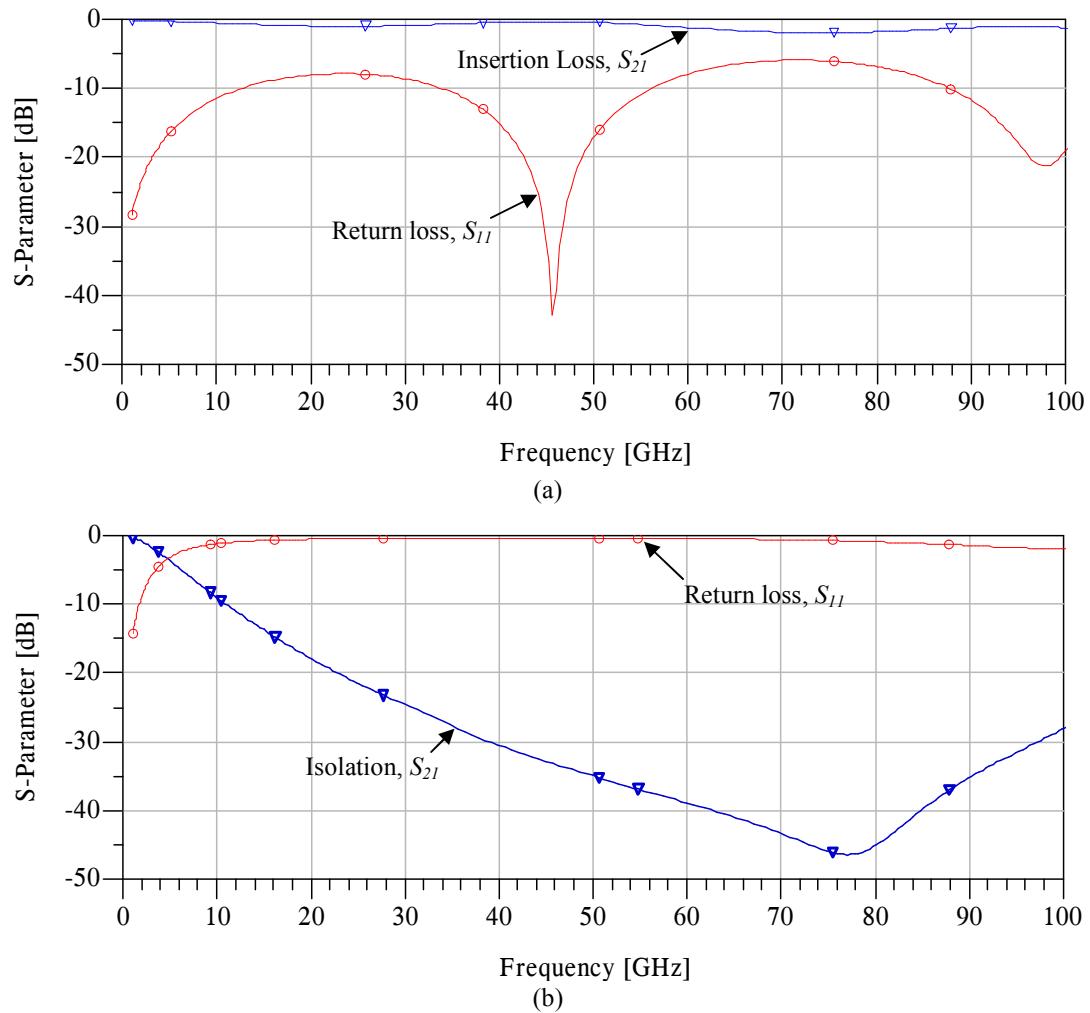


Figure 4.11: Simulated (a) UP state (b) DOWN state S-Parameter for a 75Ω RF MEMS switch.

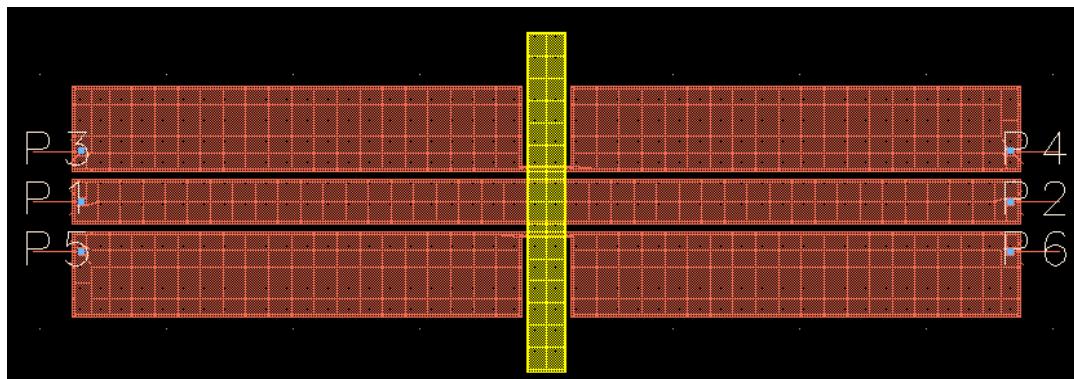


Figure 4.12: ADS Momentum model of the proposed RF MEMS switch with a 50Ω coplanar waveguide.

Figure 4.13 shows the simulated S-Parameter of the 50Ω RF MEMS switch design from 0.1GHz to 120GHz. This range is higher than those of the 75Ω switch as the switch's resonant frequency is higher. This is due to the design of the coplanar waveguide, where the slot width is decreased to $15\mu\text{m}$ with the width of signal line unchanged. The decrease in slot gap gives rise to lower inductance and impedance in the armature of the switch. During the UP state operation, the return loss increases up to the frequency of 60GHz whereby the maximum loss is -10dB . The switch insertion loss is $<-1.7\text{dB}$ at 120GHz. During DOWN state operation, the isolation is -39dB at a resonant frequency of 115GHz. The isolation is relatively broadband of approximately -24dB , for a frequency range between 55GHz and 85GHz.

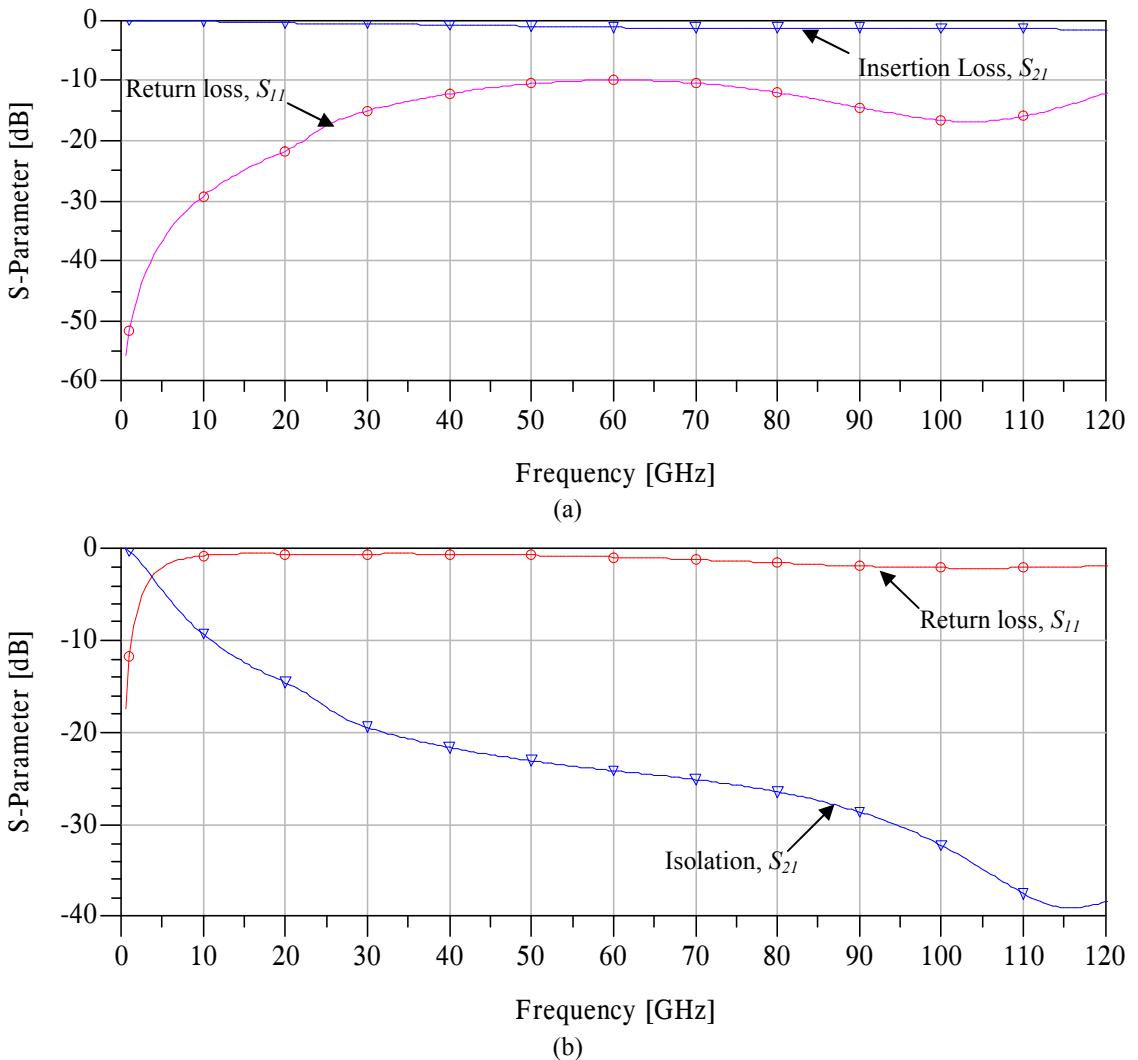


Figure 4.13: Simulated (a) UP state (b) DOWN state S-Parameter for a 50Ω RF MEMS switch.

Figure 4.14 illustrates the current density of the coplanar waveguide for the frequency of a) 1GHz and b) 75 GHz when the switch is in the UP state, where the armature is raised 5 μ m above the transmission line. At low operating frequency of 1GHz, the current density is distributed equally throughout the signal line of the coplanar waveguide. When the RF frequency increased to 75GHz, the current was observed to be transmitting along the signal line as the density plot showed intense current distribution after the position of the armature towards port 2.

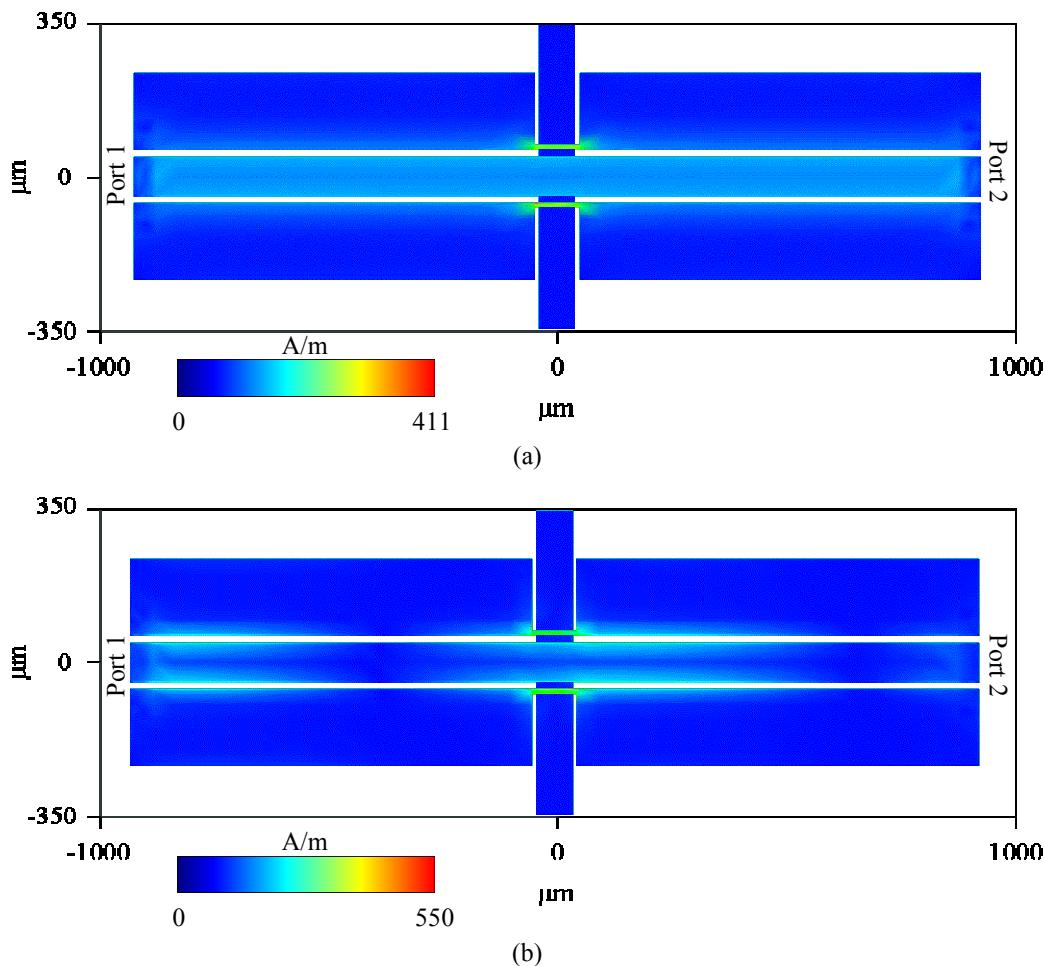


Figure 4.14: Simulated current flow of the 50Ω RF MEMS switch in the UP state at (a) 1GHz and (b) 75GHz.

Figure 4.15 shows the current density of the coplanar waveguide when the switch is at the DOWN state, i.e. the RF signal is being shunted to the ground planes through the armature. It is noted that the shunting effect is not obvious when the switch is operating

in the low GHz region as shown in Figure 4.15(a). The current is distributed throughout the signal line of the coplanar waveguide. As the frequency increases to 75GHz, current is being diverted to the ground planes via the armature as illustrated in Figure 4.15(b). The current flowing in the signal line after the armature is approximately zero and the isolation of the switch is at the best.

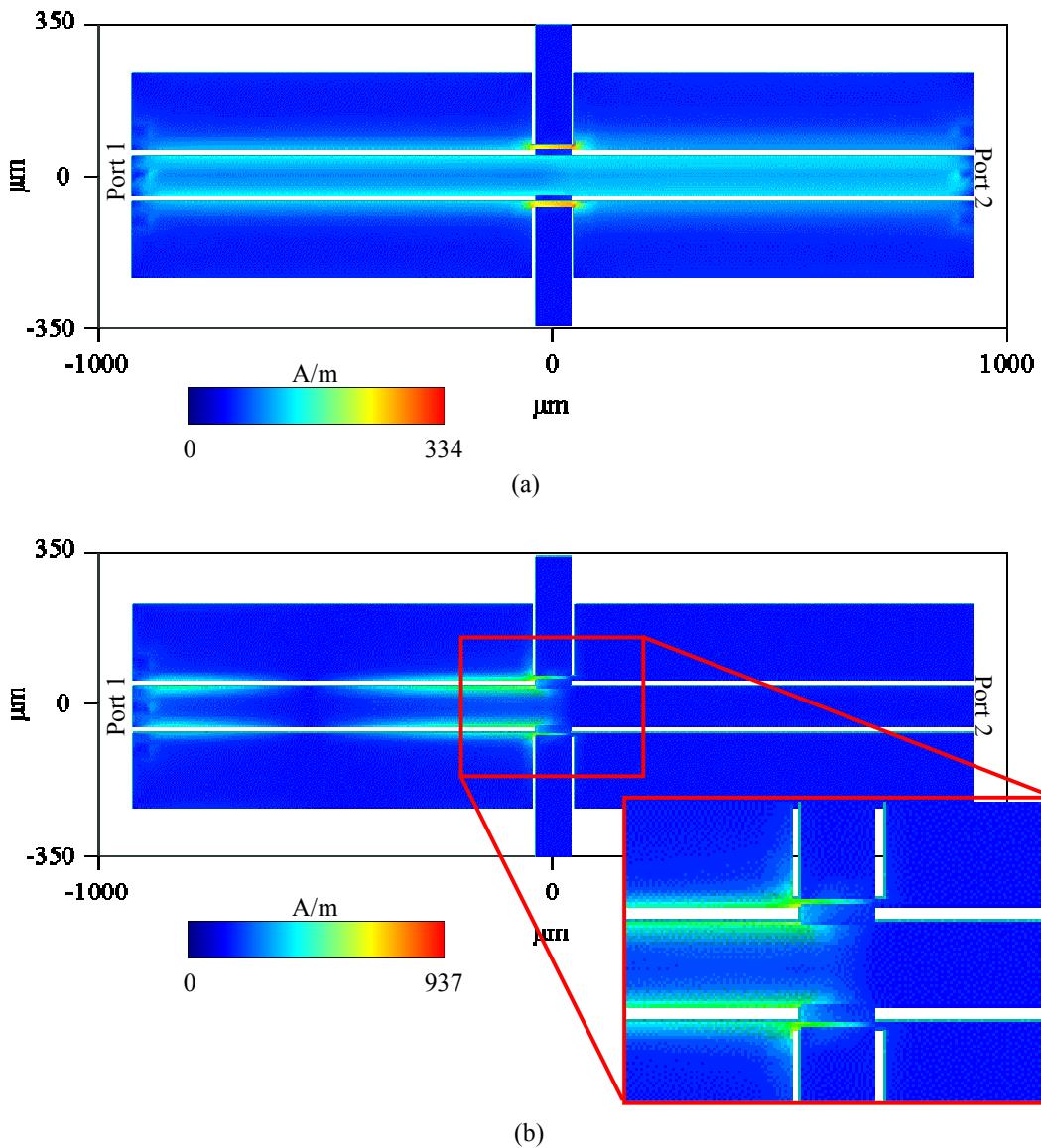


Figure 4.15: Simulated current density plot of the 50Ω RF MEMS switch in the DOWN state for (a) 1GHz and (b) 75GHz.

The current density plot of the 75Ω RF MEMS switch is similar to those of the 50Ω , hence it is not reported in this work.

4.2.1 Effect of Different Dielectric Material on Isolation Plot

This section discusses the effect of different DOWN state capacitance, C_d , on the isolation of the MEMS switch by employing different dielectric materials. The simulations based on the proposed dimensions of the RF MEMS switch with a 75Ω coplanar waveguide. As mentioned in the previous section, the high K dielectric is sometimes preferred in the design of a RF MEMS switch. The following isolation simulation employed silicon nitride (Si_3N_4), aluminium oxide (Al_2O_3) and tantalum pentoxide (Ta_2O_5) as the dielectric material for the capacitive switch design illustrated in Figure 4.1(b). The simulation was based on the proposed switch design with a 75Ω CPW ($W/G/W = 60\mu\text{m}/90\mu\text{m}/60\mu\text{m}$) on a $500\mu\text{m}$ Pyrex wafer. As the proposed switch has a small DOWN state capacitance due to the inherent design, the contact area over the ground plane is increased to the same of the signal line. This ensures the resonant frequency to appear within 100GHz, in order to allow easy illustration of the isolation plot.

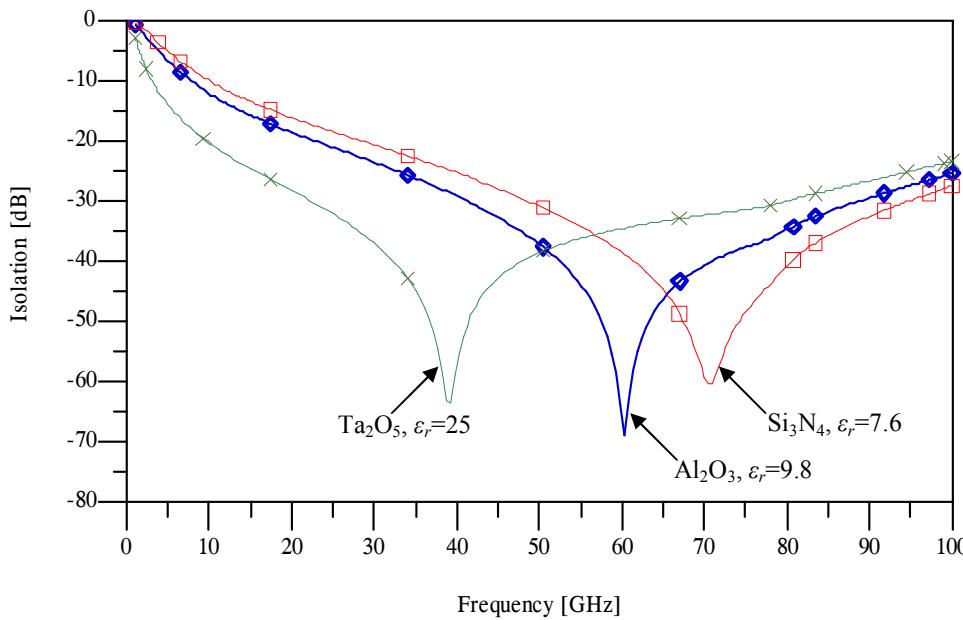


Figure 4.16: Simulated isolation with based on silicon nitride (Si_3N_4), aluminium oxide (Al_2O_3) and tantalum pentoxide (Ta_2O_5) with a switch design of $l_m=680\mu\text{m}$, $w_m=80\mu\text{m}$, $G=90\mu\text{m}$ and $W=60\mu\text{m}$, $A_r=A_c=7.2\times 10^{-9}\text{m}^2$ and $t_d=200\text{nm}$.

Figure 4.16 shows the simulated isolation of the three different dielectric materials. The resonant frequency of the switch design with Ta_2O_5 , Al_2O_3 and Si_3N_4 is 39GHz, 60GHz and 72GHz respectively. The isolation plots with a higher dielectric constant which translates to higher DOWN state capacitance attained better results over those with smaller capacitance. The isolation for Ta_2O_5 and Si_3N_4 at 20GHz are -28.3dB and -16.2dB respectively. Hence, using a dielectric material with higher permittivity results in better isolation when $f < f_o$ as compared to the Si_3N_4 .

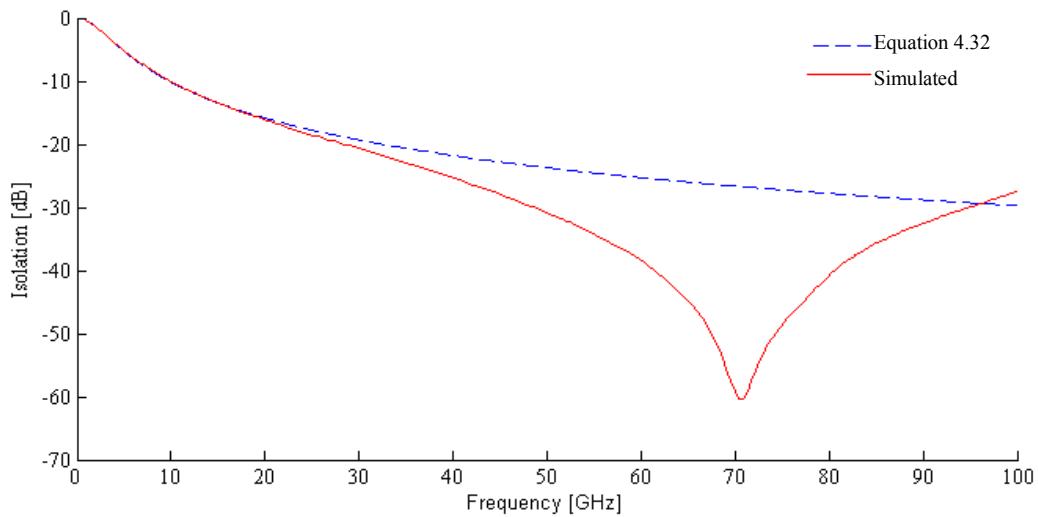


Figure 4.17: Comparison between simulated isolation and analytical isolation solution using equation 4.32 based on silicon nitride (Si_3N_4) with a switch design of $l_m=680\mu\text{m}$, $w_m=80\mu\text{m}$, $G=90\mu\text{m}$ and $W=60\mu\text{m}$, $A_r=A_c=3.6\times 10^{-9}\text{m}^2$ and $t_d=200\text{nm}$.

As the capacitance of the switch is the dominating factor in the isolation plot when $f \ll f_o$, it is possible to extract the capacitance (C_d) of the switch from the simulated isolation plot. Using the isolation plot of silicon nitride as the dielectric layer, the isolation at 1GHz is approximately -0.36dB. The extracted C_d from the simulation based on equation 4.32 is approximately 1.25pF, which is very close to the calculated C_d of 1.21pF. By plotting the equation 4.32 against the simulated plot illustrated in Figure 4.17, it shows that capacitance approximation is valid till $f_o/5$. This is because the impedance effects from the inductance and resistance of the armature, which are not considered in the approximation, kick in after $f_o/5$.

From this section, it is understood that large C_d produces better isolation.

4.2.2 Effect of Different Armature Material on Isolation Plot

The following simulation is done based on the proposed switch design with different armature material and thickness. Figure 4.18 shows the isolation behaviour of a RF MEMS switch with different armature material. The materials involved in the simulation are 2 μ m thick copper, 2 μ m thick gold and 50 μ m thick high conductivity silicon. The conductivity of the two metallic materials is about 2 orders of magnitude higher than the silicon counterpart. The isolation when $f \ll f_o$ and $f \gg f_o$ is similar for the two metallic materials. The effect, i.e. the magnitude of the isolation for the silicon armature is lesser than the other materials, is more obvious when $f \sim f_o$. This observation reflects the effect of equation 4.22.

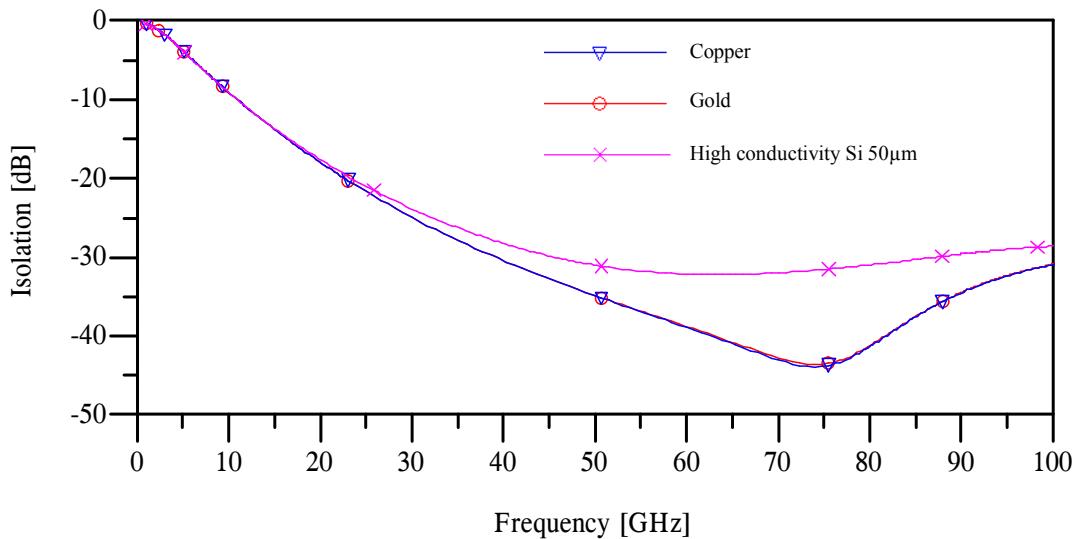


Figure 4.18: Effect of different armature material on the isolation of the RF MEMS switch with a finite width conductor backed coplanar waveguide $W/G/W=60\mu\text{m}/90\mu\text{m}/60\mu\text{m}$ and on a Pyrex substrate of $\epsilon_r = 4.82$.

4.2.3 Effect of Different Armature Geometries on Isolation Plot

This section examines the isolation behaviour of a RF MEMS switch with different armature geometries over the slot width. The variation in design produces different inductance values for the switch. There are two methodologies to vary the inductance of the switch i.e. i) by increasing the slot width and ii) changing the geometry of the armature above the slot width. The first option is not suitable for this study as any change in slot width will vary the switching capacitance and characteristic impedance of the transmission line. The second choice enables the study to be carried out with minimum impact on other parameters that affect the end result of the analysis. This alternative can also be used in actual implementation to tune the RF characteristic of a switch design.

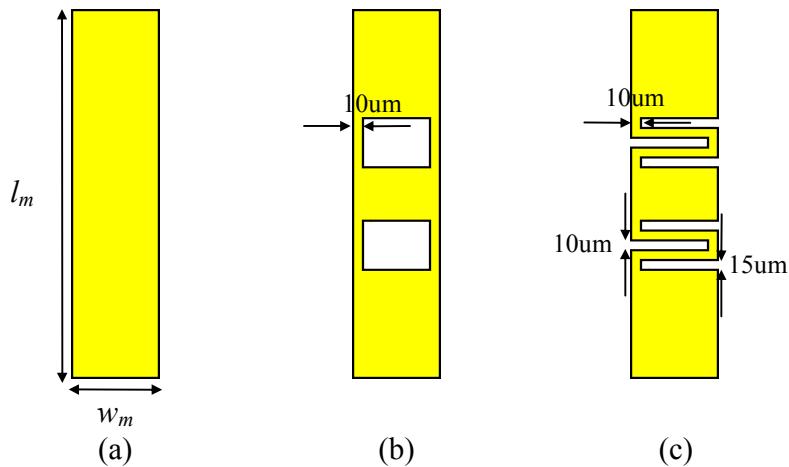


Figure 4.19: (a) A simple rectangle shape armature, (b) a rectangle armature with rectangle hole over the slot width area and (c) a rectangle armature with a serpentine like design over the slot width area.

Figure 4.19 shows the different geometries and dimensions of the $2\mu\text{m}$ thick gold armature that are used in the analysis. The inductance of the armature is in ascending order from design (a) to (c). The inductance value for the simple rectangle armature can be calculated using equation 4.34, whereas inductance calculation of other designs is

more complex. However, an effective and accurate method to calculate the inductance of the switch is through extraction from the S-Parameter simulation. The following simulation was performed with the proposed switch dimension tabulated in Table 5 with a 200nm thick Ta_2O_5 dielectric layer.

Figure 4.20 shows the different isolation trends based on the geometries shown in Figure 4.19. Two observations can be made based on the inductance value related to the isolation of the MEMS switch. Firstly, the electrical resonance of the switch shifted towards lower operating frequencies with the increment of the inductance value. The resonant frequency of the geometry a, b and c are 24GHz, 63GHz and 71GHz respectively. Secondly, the inductance of the armature begins to have a significant effect on the RF behaviour after $f_o/5$. Extraction of the inductance of the switch can be done using the isolation plot with equation 4.34. Using the geometry (c) as an example, isolation of the switch at 100GHz is -7.54dB, the inductance computed by the equation is approximately 26pH. The inductance of geometry (a) and (b) derived using the extraction method are 5.9pH and 7.6pH respectively.

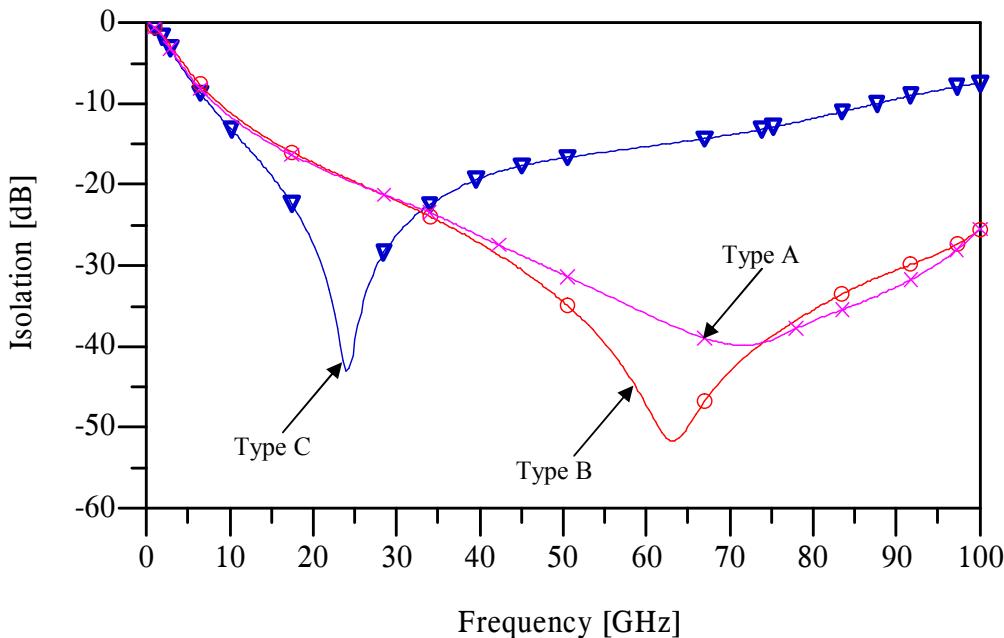


Figure 4.20: Isolation of actuated RF MEMS switch with armature geometries from Figure 4.19(a-c) over a finite width conductor backed coplanar waveguide $W/G/W=60\mu m/90\mu m/60\mu m$ and on a Pyrex substrate of $\epsilon_r = 4.82$, of different inductance value.

From this work, it is shown that the proposed switch can be employed into different applications by manipulating the geometry of the armature as well as using different dielectric material presented in 4.2.1.

4.3 Summary

This chapter discusses the electromagnetic modelling of a RF MEMS switch as a lumped RLC model, which focused on a proposed design detailed in chapter 3. The four main components of the lumped model are the characteristic impedance of the transmission line, the armature resistance, the armature inductance and the state dependent switch capacitance. The design of the coplanar waveguide is reported with the signal line width and slot width being determined for both 50Ω and 75Ω on a $500\mu\text{m}$ Pyrex substrate. The components representing the armature are also examined and the analytical values of each component based on the proposed switch are presented.

S-Parameter simulations were conducted on the designed dimensions for both 50Ω and 75Ω switch design. The 50Ω switch had an insertion loss of $<-1.7\text{dB}$ at 120GHz . The return loss during the UP state operation increases with the frequency increasing. The maximum loss was -10dB at a frequency of 60GHz . During DOWN state operation, the isolation was -39dB at resonant frequency of 115GHz . The isolation was relatively broadband of approximately -24dB for a frequency range between 55GHz and 85GHz . For the 75Ω switch design, the UP state return loss was at its maximum of -5.9dB at a frequency of 72GHz . The switch insertion loss was $<-1.96\text{dB}$ at 75GHz . At the resonant frequency of 77GHz , the UP state return loss was -6.3dB which an insertion loss was -1.9dB . During DOWN state operation, the return loss was less than -0.3dB and isolation was -46dB . Both switch designs are suitable for the application in W-Band, i.e. collision avoidance in automotive industry or in Doppler radar. The simulations have shown that the initial goal of having an insertion loss of less than -1dB is not met, however, the isolation results have performed better than required. The main reason of the shortfall is due to the low dielectric constant of the substrate, which makes the design lossy at higher frequencies.

Finally, the values of three armature components are varied to examine its effects on the S-Parameter. The results show that the RF characteristics of a MEMS switch can be tuned according to different armature design, material as well as the dielectric material.

Chapter 5

Fabrication

There are two main fabricating techniques for MEMS devices, namely surface micromachining and bulk micromachining. In general terms, surface micromachining is a process that different structural layers are deposited and etched on top of the substrate, while bulk micromachining is a process that structures are defined by selective etching into regions of a substrate. Many of the RF MEMS switches reported are fabricated using surface micromachining techniques [16, 18, 58, 114, 115]. These fabrication processes usually require 4-6 photolithography masks. Apart from the mainstream fabrication processes, there are also a number of works on Printed Circuit Board (PCB) RF MEMS [116-119].

This chapter will explore the feasibility of realising a RF MEMS with a mechanically unrestrained armature via two routes. The first route is using bulk micromachining techniques to fabricate the device as shown in Figure 5.1, while a second method is a novel fabrication process based on PCB RF MEMS [116-119] and techniques using dry film resist in microfluidic devices [120].

This chapter firstly details the fabrication process of the designed micron-scale MEMS switch in section 5.1. Section 5.2 summarises the fabrication process of the rapid prototype design. The last section draws a conclusion of the work carried out in the chapter.

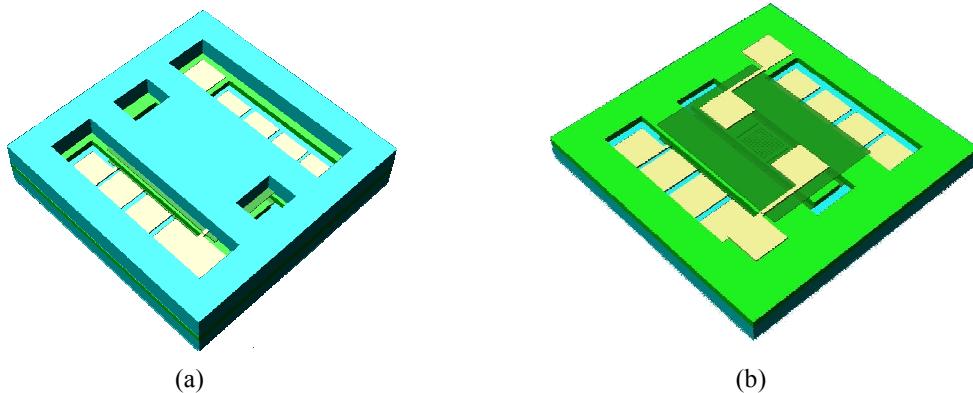


Figure 5.1: 3-D view of the (a) with top Pyrex wafer (b) without top Pyrex wafer of proposed MEMS switch (not drawn to scale).

5.1 Fabrication Process of a Micron-Scale Prototype

This process requires using a Silicon on Insulator (SOI) wafer and two Pyrex wafers. The SOI wafer is bonded between the two Pyrex wafers. The entire process consists of 18 major fabrication steps, which comprises deposition, patterning, etching, bonding of the wafers; it is illustrated in Figure 5.2. The process is explained in three different stages: the Pyrex wafer fabrication, the SOI wafer fabrication and the assembly of the device. The more complex process steps are further explored and discussed.

5.1.1 Pyrex Wafer Fabrication

The Pyrex wafers were initially prepared using fuming nitric acid for 15 minutes. The top and the bottom Pyrex wafer had a $3\mu\text{m}$ cavity trench etched using 7:1 buffered hydrofluoric acid (BHF), which is to make the operating region for the armature and provide the space for the bond pads. A chromium gold (CrAu) stack with the thickness of 40nm and 500nm respectively was deposited using e-beam evaporation. The metal stack was then etched to form the coplanar waveguide, the actuation electrodes and the bond pads of the device. A 200nm thick sputtered tantalum pentoxide (Ta_2O_5) layer was selected as the material for the dielectric which covered the coplanar waveguide and the actuation electrodes. The top and bottom wafers are shown after these processing steps in Figure 5.3.

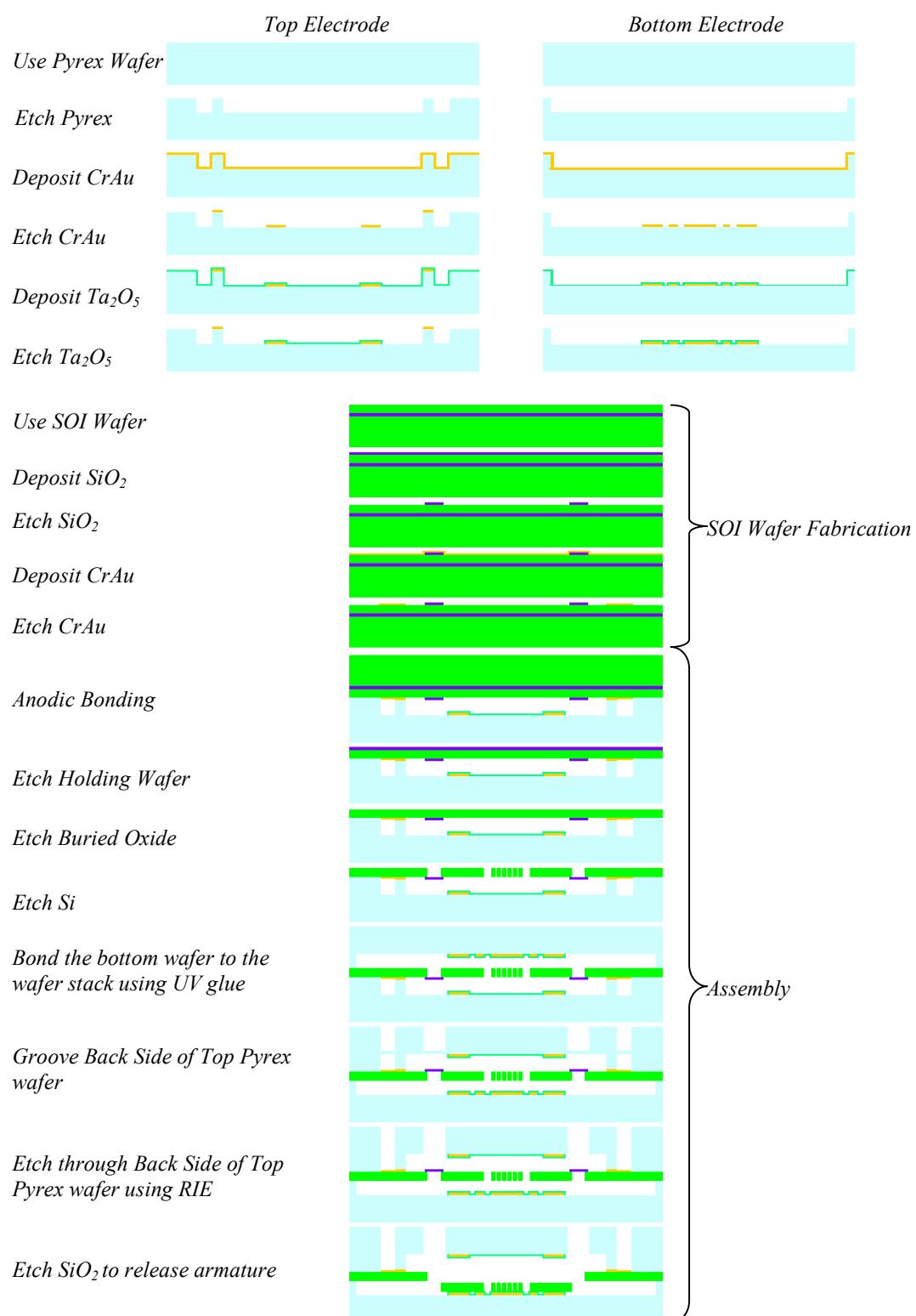


Figure 5.2: Fabrication flow for 3 wafer stack process for the micron-scale prototype described in section 5.1.

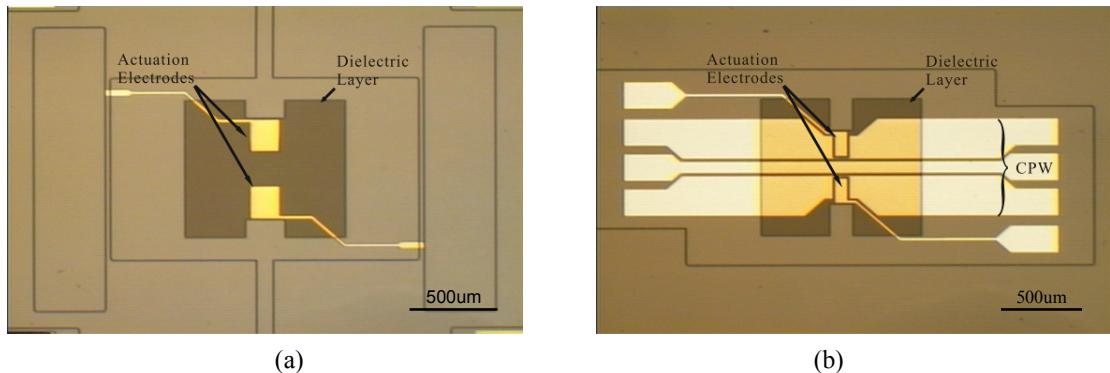


Figure 5.3: Microscopic picture of structures of a processed (a) top Pyrex wafer (b) bottom Pyrex wafer.

5.1.2 SOI Wafer Fabrication

The armature is fabricated on a SOI wafer (50 μ m/2 μ m/500 μ m). Firstly, a 2 μ m layer of the sacrificial silicon oxide is deposited using E-beam evaporation. The primary function of the oxide is to hold the armature to the wafer during the pumping and venting cycles of the different processes after the armature is formed. Since the mass of armature is relatively small ($\sim 10^{-9}$ kg), the armature is displaced easily during such equipment operation. This feature is proposed as a precautionary measure to prevent removing of armature from the bonded substrate. It is noted that the mechanical properties of the evaporated silicon oxide are inferior compared to the chemical vapour deposition (CVD) or the thermal oxidation form. However, this option is chosen due to equipment limitation within the fabrication facility. A 40nm/500nm layer of CrAu was deposited on the surface of the active layer. The metal layer was patterned to form the bond pads for the top Pyrex wafer. The processed SOI wafer is shown in Figure 5.4.

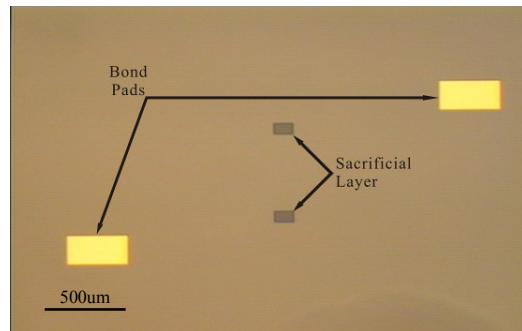


Figure 5.4: Microscopic picture of structures of a processed SOI wafer.

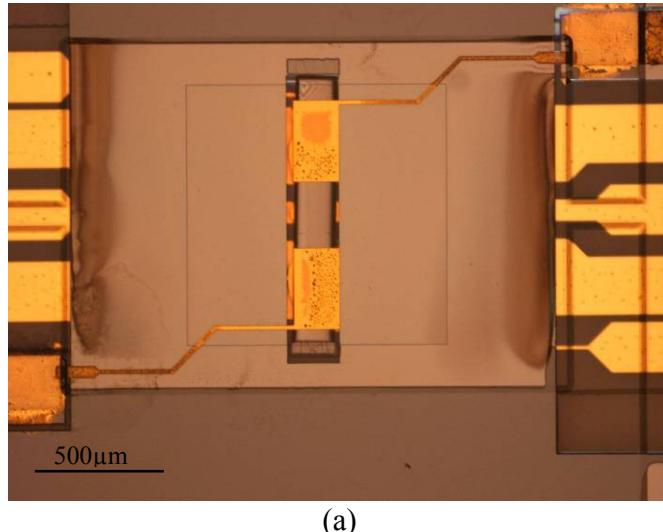
5.1.3 Assembly of Device

The assembly of the device required the SOI wafer to be bonded twice. Initially, the processed SOI wafer was anodically bonded to the top Pyrex wafer. This bonding process was also used to electrically connect the metal tracks of the top Pyrex wafer to the bond pads on the SOI wafer. The handle wafer and the buried oxide were subsequently removed using Surface Technology Systems (STS) Pegasus deep reactive ion etching (DRIE) module with a non-Bosch process [121] and 7:1 BHF etching respectively, which was exposing the back of the active layer of the SOI wafer.

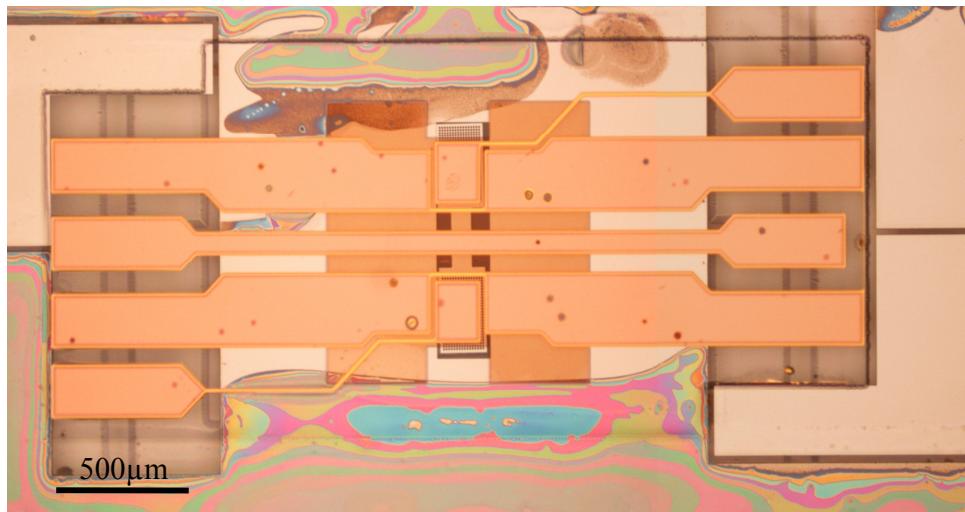
The armature was subsequently etched from the active layer using the Bosch process [121] of the DRIE machine. A layer of ultraviolet (UV) glue Norland NOA 61 was manually applied to the bonding surface of the bottom Pyrex® wafer. The bottom Pyrex wafer was then aligned to the Silicon/Pyrex stack with the aid of a microscope and subsequently pressed onto the stack to achieve proper contact. The bonded Pyrex/Silicon/Pyrex wafer stack was then flood exposed by UV light using a EVG 620 aligner for 60s to cure the adhesive layer. The top and bottom side of the bonded wafer stack are as shown in Figure 5.5.

Contact windows had to be opened for probe contact as well as sacrificial etch on the back of the top Pyrex wafer. It is widely known that creating through holes in Pyrex wafer is often slow and complex [122-124]. A simple and efficient way to create the contact windows was to split the process step into two parts, i.e. groove and etch. The grooving step required using a dicing saw with a blade wider than the required dimension

of the contact window to saw 470 μm into the top Pyrex wafer of the wafer stack. The remaining Pyrex was removed using a ICP-RIE process [125].



(a)



(b)

Figure 5.5: Microscopic picture of a Pyrex-Silicon-Pyrex bonded wafer stack from the (a) top Pyrex wafer of RF MEMS switch design and (b) bottom Pyrex wafer of a RF MEMS switch with a different armature design.

With the opened contact windows, the sacrificial layer can be removed using hydrofluoric (HF) vapour phase etch and the armature can be released through the windows. The wafer can then be diced into devices using the Mitsubishi Diamond MS300A-CE scribe. The process was carried out by pushing a scribing wheel along the

scribe line on both the top and bottom surfaces of the Pyrex/Silicon/Pyrex wafer stack. By applying a small amount of force on the scribed surface, the wafer breaks into individual devices.

The next section will discuss the difficulties faced during the fabrication run and propose some solutions.

5.1.4 Discussion

The following subsections discuss the most complex process steps involved in the fabrication:

- Glass etch
- Bonding of processed SOI wafer to Pyrex wafer
- Forming the armature using the DRIE process
- UV glue bonding

The fabrication work was hampered by the recent clean room fire. Process development work on the glass etching and part of the SOI-Pyrex wafer anodic bonding were done by an American company called Nanoshift LLC. Data and results received from them were collated, analysed and later adapted into processes which were suitable for the temporary clean room setup in the University of Southampton.

Glass etch

Glass etching is usually a very straightforward and well documented process, where a patterned wafer can be dipped into HF or HF based etchant, e.g. buffered oxide etchant, which results in a well characterized etch rate. As the fabrication process requires using anodic bonding, Pyrex wafers have to be used for the work. The details of the anodic bonding were explained in the next section. However, the level of challenge is increased by etching of Pyrex wafer, due to its chemical composition. A Pyrex wafer is made up of SiO_2 81%, B_2O_3 13%, Na_2O 4%, Al_2O_3 2% [126]. The etch rate differs for individual materials. This also affects the overall surface roughness of the wafer after etching [127].

An etch test conducted by Nanoshift LLC was to find out on the etch rate and profile of the Pyrex patterned with a $2\mu\text{m}$ thick OCG 835 35CS photoresist mask for a

targeted depth of $3\mu\text{m}$ in Buffered Oxide Etch (BOE) 5:1 solution. The etch test was based on the chemicals used in the company's foundry. Figure 5.6(a) shows a $55\mu\text{m}$ wide ridge-like structure was the narrowest feature on a dark field mask, which was required to be transferred onto the Pyrex wafer for the RF switch design. It can be seen that the feature is properly transferred onto the photoresist mask as shown in Figure 5.6(b).

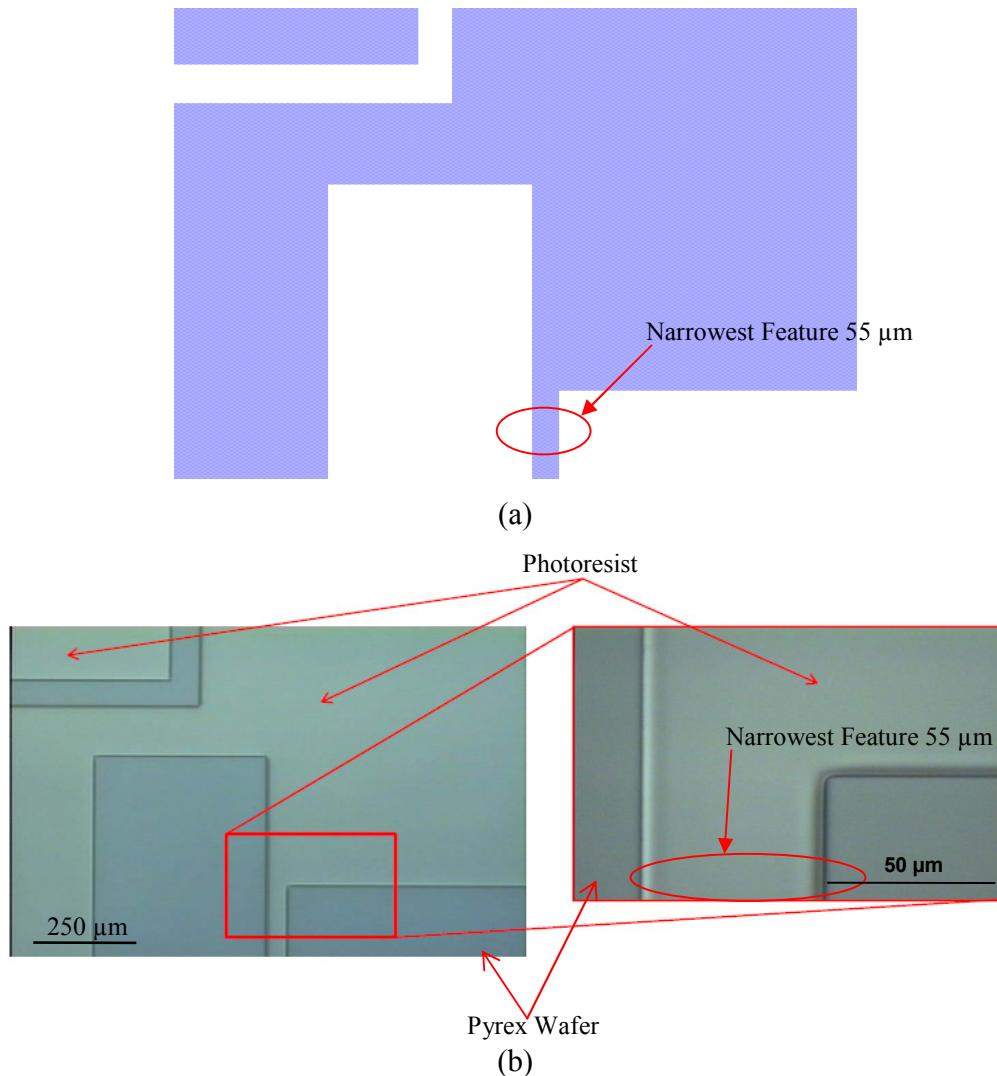


Figure 5.6: (a) Narrowest device feature to be transferred onto the Pyrex wafer on the dark field mask design (b) Photoresist structure on Pyrex wafer after development.

However, considerable undercuts were observed after the $3\mu\text{m}$ etch at all features on the Pyrex wafer as shown in Figure 5.7. The foot of the etched structure seemed smooth and straight compared to the top surface of the wafer, whereas the edge was

rough and the top surface of the narrowest structure had been completely etched. Although undercutting is a common problem for an isotropic wet etch process, it is not expected to be that severe. The process tolerance factored between this mask and the following metal circuit mask is $20\mu\text{m}$, i.e. the undercutting for the wet etch process must be less than the process tolerance. This shows that the mask material for this process was not adequate and the photoresist probably was delaminated during the etching process.

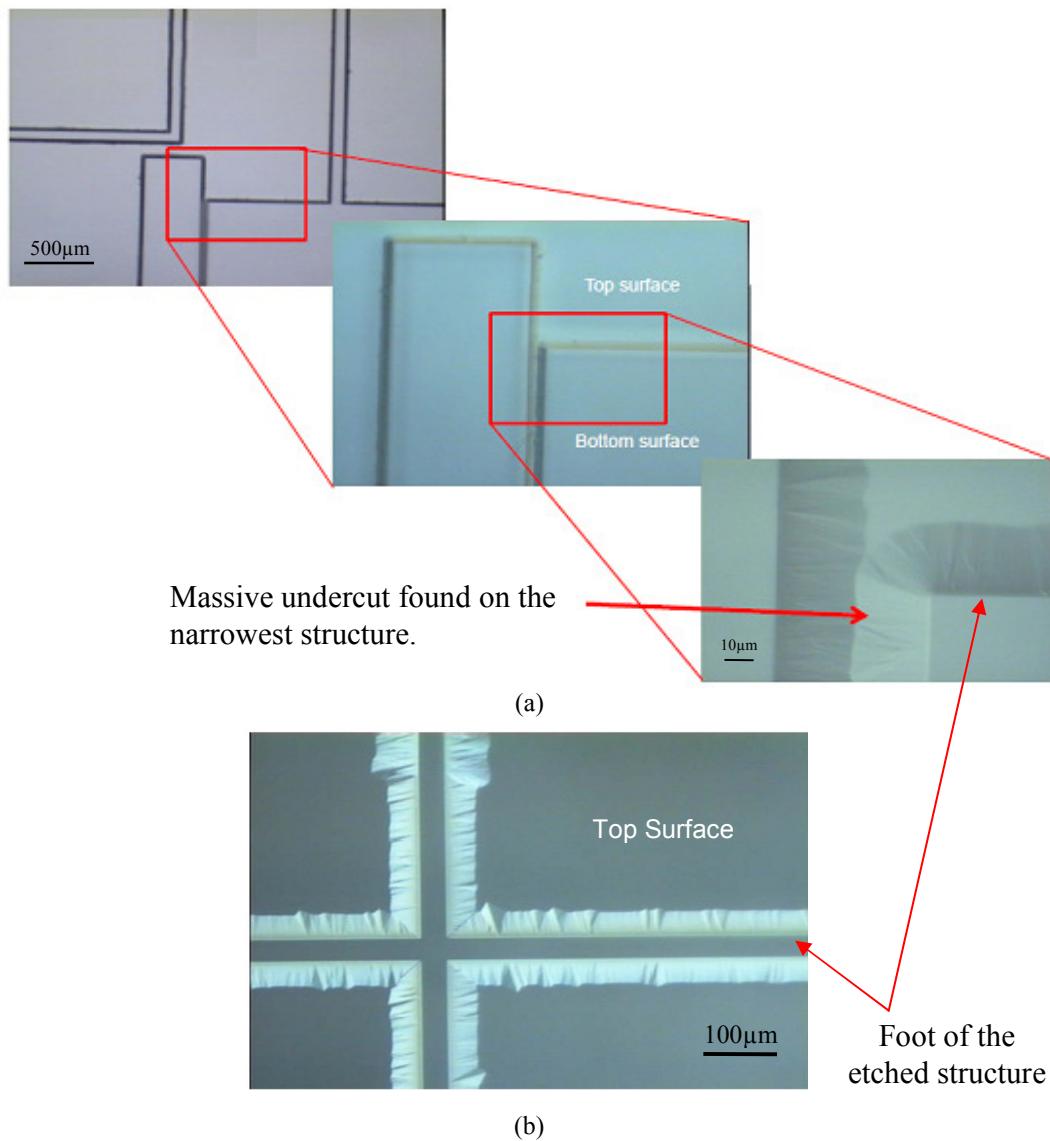


Figure 5.7: Microscope images of the etch profile on the severity of the undercut at (a) the $55\mu\text{m}$ wide ridge like structure on the Pyrex wafer using a photoresist mask (b) alignment mark on the Pyrex wafer using a photoresist mask.

A second test was conducted to confirm the initial hypothesis. Two Pyrex wafers were etched in this test. The first wafer was coated with a photoresist mask but was etched to a shallower depth of $1.5\mu\text{m}$, while the second wafer is coated with a hardmask mask and then etched for $3\mu\text{m}$. The hardmask was a chromium-gold metal stack. This type of metal mask is usually used for deep glass etching [128-130]. However, it has a disadvantage that the wafer requires metallisation and then patterning, which increases the fabrication cost. The outcome of the test is illustrated in Figure 5.8.

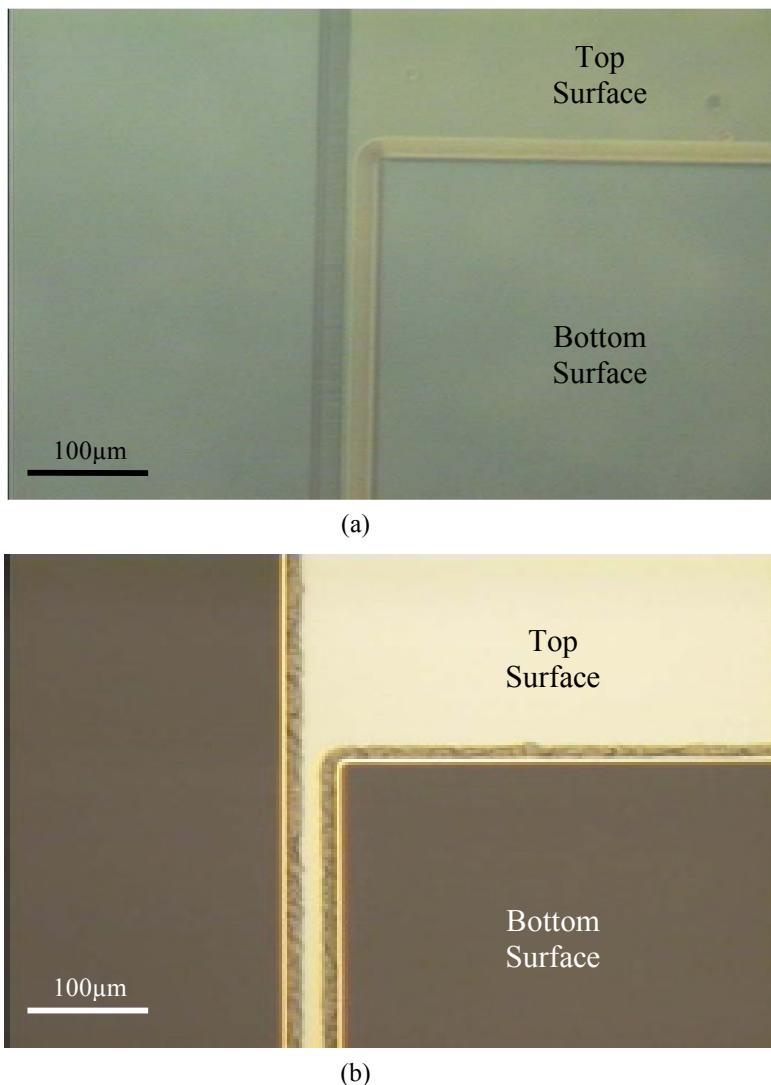


Figure 5.8: (a) $55\mu\text{m}$ wide ridge-like structure on Pyrex wafer after $1.5\mu\text{m}$ of etching using a photoresist mask. (b) $55\mu\text{m}$ wide ridge like structure on Pyrex wafer after $3\mu\text{m}$ of etching using a metal mask.

The wafer with the photoresist mask was still suffering from considerable undercut, though the etch depth was reduced by half. In contrast, the wafer with the metal mask has shown a ridge forming after the etch. Through surface profiling of the wafer with the metal mask, the dimension of the ridge's top surface was 22 μm . The undercut measured with the metal mask was 16.5 μm . This value was within the process tolerance set between the glass etch mask and the metal circuit mask layout. Hence, the metal tracks, which are located on the top surface of the wafer and used to connect the bond pads on the silicon layer and actuation electrodes, can be used.

The results from the mask material test were used and then developed into a wet etch process, which is compatible with chemicals available in the temporary clean room setup in the University of Southampton. In the developed process, the etch mask material used consisted of a 1.3 μm thick Microposit® S1813 photoresist and a layer chromium-gold. BHF 7:1 etchant was used to etch the Pyrex wafer. In the etch trial, the Pyrex wafer was patterned with both the photoresist and the metal mask and was dipped into the etchant for 110mins. In order to have a good understanding of the etch profile and uniformity across the wafer, the surface profiling was taken using KLA Tencor P16 stylus profiler at five different sites of the wafer as shown in Figure 5.9. The step profile was measured twice. The first measurement was taken with the mask stack and the second was carried after stripping the mask layers. The average etch rate derived from the trial was 30nm/min with a uniformity of 2%. The measured data for the etch trial are tabulated in Table 9. With this information, the etch time required for a depth of 3 μm using the BHF 7:1 etchant was 100 minutes.

Table 9: Etch rate information of a 6 inch Pyrex wafer using BHF7:1 for 110 minutes.

Site	After Etch (μm)	Actual Etch Depth (μm)	Height of Photoresist + CrAu Mask (μm)	Etch Time (min)	
Centre	4.782	3.303	1.479		110
Left	4.639	3.262	1.377	Average(μm)	3.302
Right	4.689	3.337	1.352	Etch Rate ($\mu\text{m}/\text{min}$)	0.03
Top	4.642	3.280	1.362	Etch Uniformity	2%
Flat	4.662	3.328	1.334		

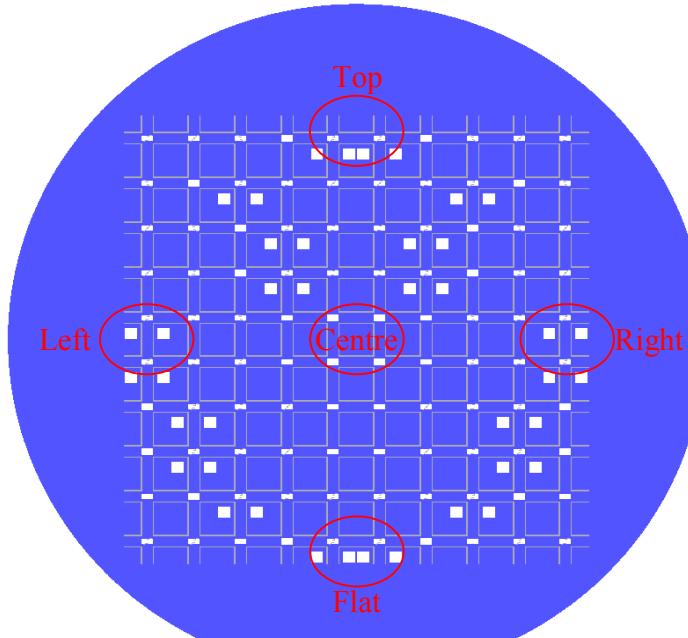


Figure 5.9: The different sites on the 6 inch Pyrex wafer where the step profiles are measured.

Anodic Bonding

There are many methods for wafer bonding, namely eutectic [82, 131], fusion [82, 132] and anodic bonding [133, 134]. The prior two techniques require a high bonding temperature (more than 800°C) as compared to the anodic bonding, which can be carried out at a temperature below 400°C . This low operating temperature is beneficial for device fabrication with a low thermal budget, especially when a metallisation step is involved, as a high temperature can cause the metal to melt or diffuse into the substrate.

The basic concept of anodic bonding is to apply at high voltage across the silicon and Pyrex wafer (as shown in Figure 5.10(a)). With an appropriate bonding temperature, the sodium ion within the Pyrex wafer are attracted towards the electrode, leaving the oxygen ions to interact with Si at the wafer interface to create a physical bond between the two wafers. Additionally, an O_2 plasma surface conditioning can be done to improve the bond strength before the bonding step [135].

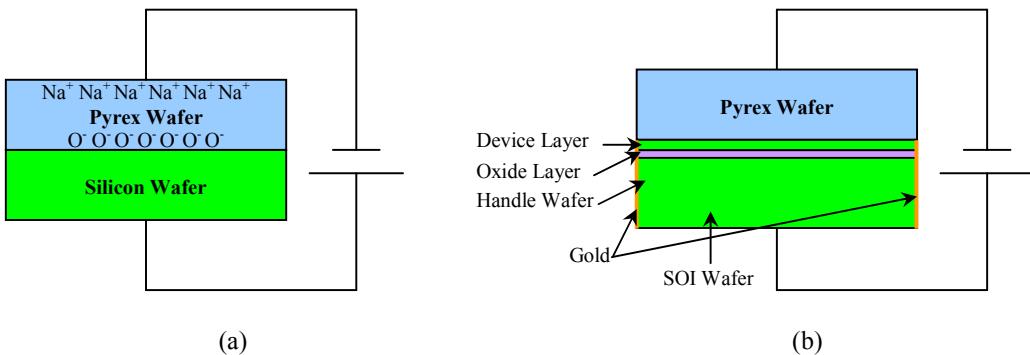


Figure 5.10: Schematic representation of the layer sequence for (a) Silicon-Pyrex (b) SOI-Pyrex anodic bonding.

However, in this work, the situation was a rather complex as a SOI wafer was used instead of a standard silicon wafer. The current is unable to flow through the wafer as there is an insulating silicon dioxide layer between the device and the handle wafer. Studies on anodic bonding of SOI and Pyrex wafers were reported in [136-138]. The buried oxide thickness used in the studies varies from two hundred nanometres to one micron and there are no structures on the bonding surfaces. The insulating property of the oxide layer is overcome by applying voltages ranging from -700V to -1000V across the wafer stack as well as increasing the bonding temperature, which improves the conducting path.

Several attempts to bond wafers at -1500V and 400 degrees Centigrade were carried out by Nanoshift LLC. In most cases, it results in limited bonding between the interface of the Silicon and Pyrex. Nevertheless, complete bonding was achieved for a pair of SOI and Pyrex wafers. A typical outcome of the bonding process was that some areas of the Silicon and Pyrex wafers are bonded as shown in Figure 5.11(a). The only successfully bonded wafer pair undergo a simple bond strength test, where a razor blade was used to ply open the wafer stack at the bonded interface. The bonded wafer split during the test due to the weak bond strength. Hence, the conventional bonding methodology is deemed as unsuitable for this fabrication work.

The main problem for successful anodic bonding was lack of a conducting path through the SOI wafer. This can be overcome by depositing a layer of a conducting material [138], e.g. Gold, on the edge of the SOI wafer. This creates conducting path

from the device layer to the handle wafer across the buried oxide layer (as illustrated in Figure 5.10(b)). An e-beam evaporated chromium gold metallisation layer was selected as the conducting material due to the limitation of the equipment and material in the University of Southampton temporary clean room.

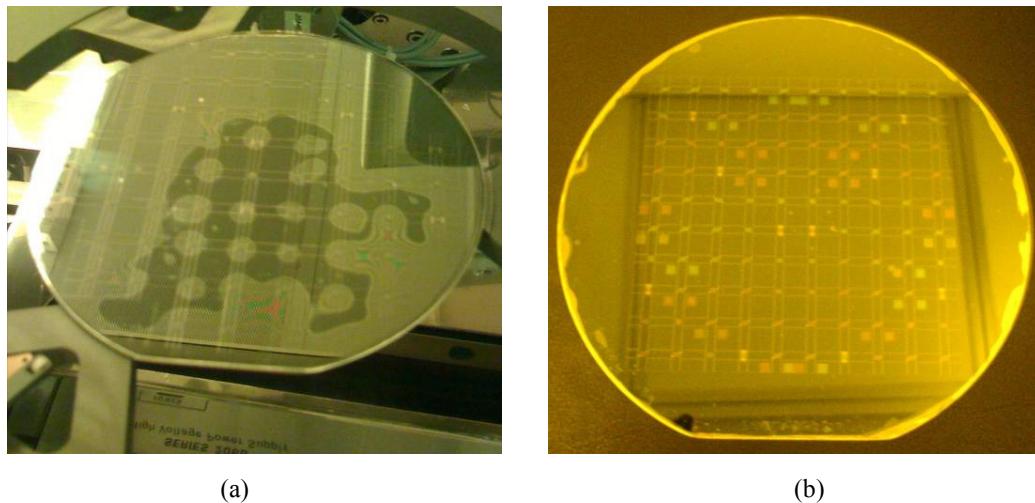


Figure 5.11: (a) A poorly anodically bonded Pyrex SOI wafer stack using -1200V at 400°C without metal interconnect at the rim of the SOI wafer. (b) A successfully bonded Pyrex SOI wafer stack using -1000V at 385°C with metal interconnect at the rim of the SOI wafer.

The process parameters used in the anodic bonding experiment are presented in Table 10. The first set of parameters used was based on an anodic bonding recipe which was used for bonding a standard silicon wafer and Pyrex wafer. The outcome of the first bonding recipe is as shown in Figure 5.11(b). The bond was a success with only a few small air pockets formed in areas where there were some surface contamination.

Table 10: Process parameters for the two anodic bonding trial involving fully processed SOI and Pyrex wafers.

	Recipe 1	Recipe 2
Temperature	385°C	355°C
Piston Force	400N	400N
Voltage	-800V	-800V
Time	15 minutes	15 minutes

However, there were two problems with the bonded wafer under close inspection. Firstly, it can be observed that there was some chromium-gold diffusion in the metallisation stack as shown in Figure 5.12(a). This leads to degradation in the conductivity of the gold tracks, which affects the time constant of the electrostatic actuation mechanism. Therefore, it aggravates the switching time of the armature during actuation. A similar issue is also observed in work reported by [72]. The problem can be resolved by either changing the chrome-gold metallisation to a chromium-platinum-gold stack or decreasing the process temperature of the bonding process. The intermediate platinum layer in the chrome-platinum-gold stack acts as a barrier layer. It stops the chromium and gold layers from diffusing into each other during the bonding process.

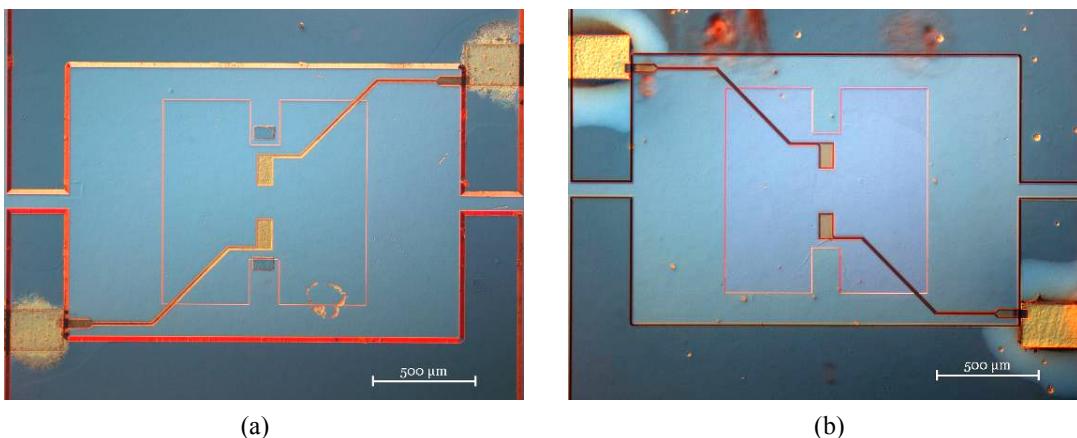


Figure 5.12: Microscopic picture of structures of an anodically bonded Pyrex-Silicon wafer stack using -800V at (a) 375°C (b) 355°C.

The second problem observed was the amount of the gold melting and spreading around the predefined features. The spread of gold increased the risk of shorting the whole silicon layer even after the DRIE process step, which physically isolated the bond pads from the rest of the silicon structure. This issue can be resolved by either reducing the bonding temperature or reducing the piston force exerting on the wafer stack during the bonding process. So reducing the processing temperature has the potential to mitigate both problems.

In the second trial, the bonding temperature was therefore reduced by 20°C to 355°C with the remaining parameters unchanged. The issues observed in the first trial had

reduced considerably. As shown in Figure 5.12(b), the chrome gold diffusion was localised to the bond pads. From the micrograph, it also can be seen that the amount of diffusion has reduced. The smoother the metallised surface is, the higher intensity of the reflected light is derived by compared to the previous result. The spread of gold around the predefined area was also reduced considerably.

As the recipe fit the purpose of the work, no further development work was undertaken. The second recipe is deemed to be suitable for this work.

Deep Reactive Ion Etch

Etching of Silicon is considered to be one of the critical processes in bulk micromachining of MEMS devices. The most common methodology is via wet etch, i.e. etching of silicon using KOH solution [139-141] while other ways include the RIE. These techniques are relatively straightforward. However they are unable to attain deep silicon etch with good aspect ratio. To attain such profiles, deep reactive ion etching (DRIE) based on the Bosch process [142] and Cryogenic-RIE process [143] are required. The prior is used as the primary technology. The Bosch process, also known as pulsed or time-multiplexed etching, uses two phases, i.e. etch and passivation, in each cycle. The substrate is firstly etched followed by a passivation step. The passivation step is used to protect the sidewall profile during the etch step.

The following trial work was carried out on a STS Pegasus machine using standard process recipes on a silicon wafer [121]. This was intended to be used as the etch recipe to form the armature on the Pyrex-Silicon wafer stack. The wafer was patterned with a $6\mu\text{m}$ thick AZ9260[®] photoresist. The first problem encountered was grassing. Grassing is undesirable roughness in the etching base which is usually caused by inadequate etching at the base of the trench. With platen power set at 50W, grassing was observed at the etch base of the substrate, as shown in Figure 5.13(a). Etching at the base of the trench seemed to be inadequate. Similar observations are made by Park et. al [144]. The platen power of the etch process was increased to 60W, with the etch profile shown in Figure 5.13(b). The base of the etch profile was smooth compared to the Figure 5.13(a), while the grassing issue was being resolved. It proved the hypothesis that the initial platen power of 50W was insufficient for the etch process.

With this tuned recipe, etching the armature on the device layer of the SOI-Pyrex wafer stack was carried out. The STS Pegasus is installed with an electrostatic chuck, the wafer stack cannot be loaded directly into the process chamber as the chuck would not be able to hold down the wafer stack due to the insulating nature of the Pyrex wafer. This problem can be solved by either attaching the wafer stack to a silicon carrier wafer or depositing a layer of conductive material on the back of the Pyrex wafer. The former method was chosen as any deposition on the Pyrex side of the wafer stack at this stage of the fabrication can damage the silicon surface when mounting on the wafer stack onto chuck.

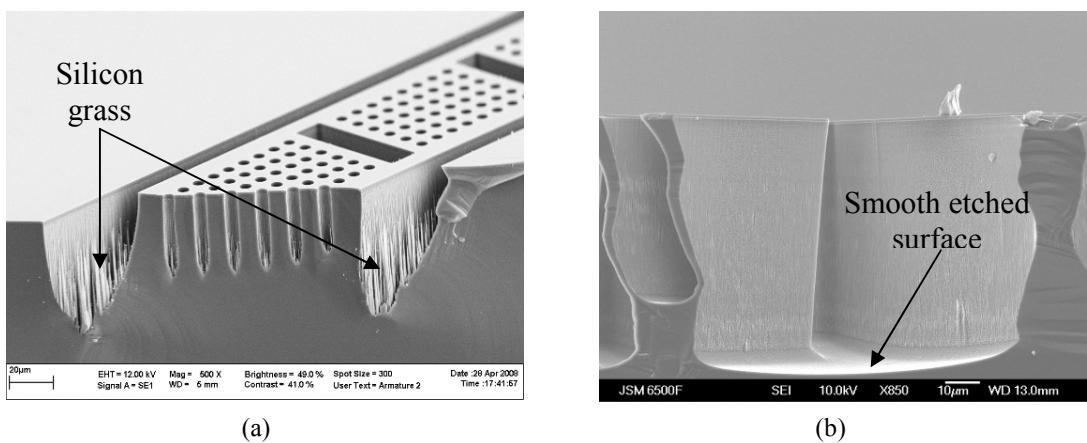


Figure 5.13: SEM picture of the DRIE trial for grassing issue using platen power at (a) 50W (b) 60W.

The wafer stack was attached to the handle wafer using CrystalbondTM 555, which is a temporary wafer mounting adhesive used in research laboratories and industries [145, 146]. The etching recipe (as given Appendix B), with an etch rate of $4.17\mu\text{m}/\text{min}$, was set to run for approximately 12minutes in order to achieve through etching for all the features predefined by the photolithography mask. The result of the etch is shown in Figure 5.14. As seen from the micrographs, the armature was missing and the surface of the silicon suffered from grassing. Measurements are taken using the surface profiler and revealed that only $10\mu\text{m}$ of the silicon layer remained on the bonded substrate. This result was not anticipated as the expected measurement should be approximately $50\mu\text{m}$ (thickness of the silicon layer) plus the photoresist remaining from the etch process. Most likely the wafer stack suffered from a heat dissipation problem, as both the

CrystalbondTM and the Pyrex wafer sandwiched in the wafer stack were not thermally conductive. The heat generated during etching was not conducted via the backside cooling helium at the platen, which caused the etch selectivity of the photoresist mask and silicon to be decreased from 1:100 to less than 1:5. The photoresist mask was heated up to a temperatures higher than its specified range, which caused the material to be either soften or burn-off during the etching process.



Figure 5.14: Micrograph of silicon Pyrex stack after DRIE of (a) a view of the fail etch through the Pyrex wafer with the armature missing (b) a view of the fail etch from the silicon side, showing that the photoresist layer and part of the silicon layer has been etched.

The main problem was the inability of dissipating heat which was built up from the wafer surface during the etch process. A simple solution was to include a cool down period at regular intervals during the process. Based on the results of the fail etch and the etch rate of recipe used, the layer of photoresist was assumed to be completely removed from the wafer surface after 2.5minutes of etching. Thus, it exposed the underlying silicon for etch in the remaining etch process. For the worst possible scenario, in order to ensure that photoresist remains on the surface of the wafer, the duration of etch should not be more than 2.5minutes, otherwise the surface of the wafer would be overheated. A 5minutes cooling interval was added to the recipe for every 2minutes of etching. This solution was not optimal as the temperature at the etching surface was not consistent throughout the process. This ensures that the heat built up during the etching process would be relieved regularly without affecting the end result of the process. Figure 5.15 illustrates the improved DRIE etch and shows that the silicon armature remained in place

after the etch process. The silicon layer under the photoresist mask was not etched on the Silicon/Pyrex stack.



Figure 5.15: Micrograph of success DRIE etch showing that the silicon layer under the photoresist mask was not etched on the Silicon/Pyrex stack for the (a) RF MEMS switch design (b) a RF MEMS switch with a different armature design.

UV Glue Bonding

As mentioned in the previous section, the bottom Pyrex wafer was bonded to the silicon-Pyrex wafer stack using Norlands NOA 61 UV adhesive glue. As the equipment tooling for process was not available at the point of fabrication, the UV glue was manually applied onto the bonding surface of bottom Pyrex wafer with a brush.

The armature was found to be stuck in the gap between the silicon and the bottom Pyrex as illustrated in Figure 5.16 during an optical inspection of the grooving step. This problem was attributed to the thickness of the UV glue. As the UV glue was manually spread onto the bonding surface of the bottom Pyrex wafer, the thickness of the glue was uncontrollable. The gap between the bottom Pyrex and the silicon wafer with the UV glue was greater than the thickness of the armature, thus it allowed the dislodged armature to be stuck in the cavity. The armature was suspected to be dislodged by the mechanical vibration of the dicing during the grooving step. This problem can be overcome by rerunning of the existing fabrication plan with a proper UV glue application method [147-149].

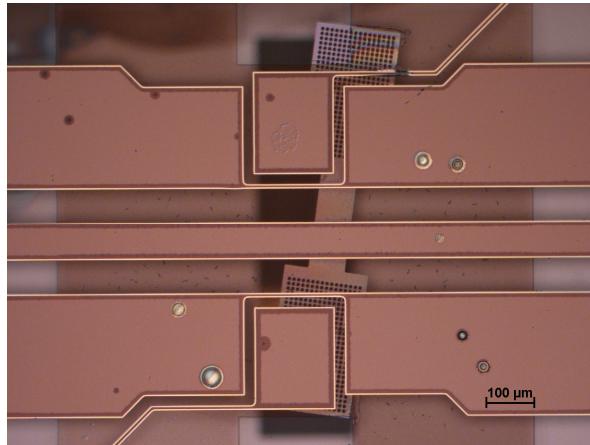


Figure 5.16: Microscopic view of a bonded wafer stack from bottom Pyrex wafer showing the armature is stuck between the bottom Pyrex wafer and silicon wafer.

Due to the shortage of processed wafer pairs and equipment, the fabrication work was terminated after the grooving step. Although improvement was observed from this work as compared to the predecessors described in section 2.4.7, i.e. the armature was successfully freed after the second bond, no working devices were achieved.

5.2 Fabrication Plan for a Rapid Prototyping MEMS switch

A full clean room fabrication process is usually costly and time consuming. In the case of the RF MEMS switch, numerous problems are encountered. Therefore, a cheap and quick prototyping process flow was developed to overcome these limitations. This process allowed the fabrication of a large scale RF MEMS switch with an unconstrained armature (as shown in Figure 5.17), thus it proved the viability of the concept. The dimensions of the switch are in the range of millimetres.

This work required using a PCB for high frequency application and microscope glass slide as a substrate. The glass slide acted as the top cover where the actuation electrodes were fabricated. The PCB operated as the bottom substrate where a 50Ω coplanar waveguide was patterned. The spacer stack, which defined the gap between the microscope slide and the PCB, consisted of a layer of Ordyl SY320 epoxy dry film resist, a piece of silicon slab and a layer of adhesive which was applied between the silicon and PCB for bonding. The unconstrained armature and the silicon spacer were fabricated on a

low resistivity silicon wafer. As the main goal of this work was to achieve a working device, the dimensions of the prototype switch were chosen to aid manual manipulation of the different parts during fabrication. The dimensions of the prototype switch are tabulated in Table 11.

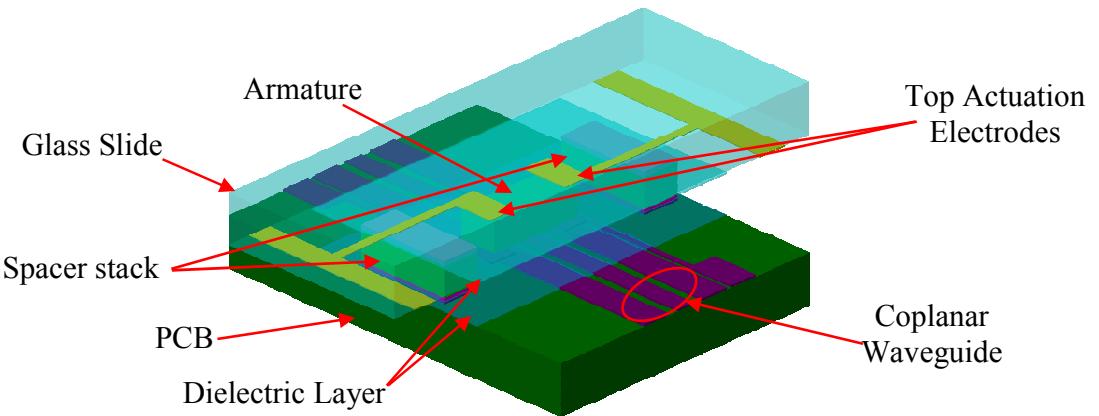


Figure 5.17: Conceptual drawing of the rapid prototype RF MEMS switch.

Table 11: Dimensions of the RF MEMS prototype switch

<i>Armature Length</i>	8mm	<i>CPW Slot Width</i>	0.3mm
<i>Armature Width</i>	4mm	<i>CPW Signal Line Width</i>	1.8mm
<i>Armature Thickness</i>	525 μ m	<i>Capacitive Gap, g_o</i>	40 μ m
<i>Dielectric Thickness</i>	200nm	<i>Substrate Thickness</i>	1.52mm

The fabrication process of the prototype switch is shown in Figure 5.18. The different fabrication steps for the fabrication of the electrodes on a standard microscope glass slide are described in section 5.2.1. Section 5.2.2 describes the PCB processing while section 5.2.3 describes the assembly of the device. Section 5.2.4 discusses about the selection of the dielectric material that was used in the work.

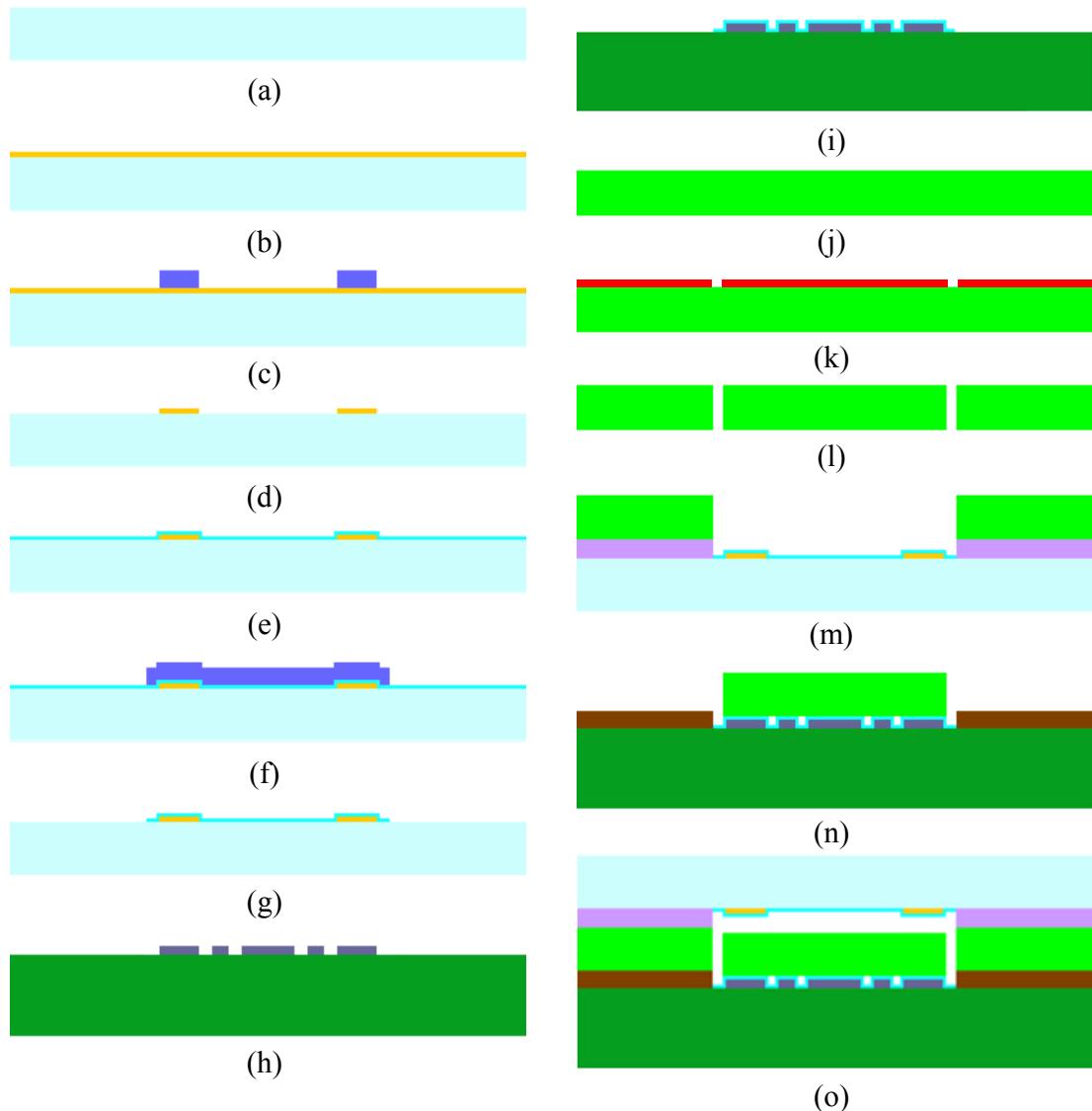


Figure 5.18: Fabrication flow for an RF MEMS switch based on low cost rapid prototyping process described in section 5.2 (a) Microscope glass slide (b) Deposit chromium-gold layer (c) Laminate, expose and develop a layer of Ordyl AM130 dry film resist (d) Etch chromium-gold layer/Strip dry film resist (e) Deposit Ta_2O_5 as dielectric layer (f) Laminate, expose and develop a layer of Ordyl AM130 dry film resist (g) Etch dielectric layer/Strip dry film resist (h) Roger's RO4003 with pre-fabricated CPW (i) Deposit Ta_2O_5 on PCB (j) Low resistivity silicon wafer (k) Spin, expose and develop 10 μm of AZ9260 photoresist (l) DRIE silicon wafer to form armature and spacer (m) Insert and bond spacer stack (n) Insert Si armature into the bonded stack (o) Apply adhesive to PCB then bond the glass slide and PCB together

5.2.1 Glass Slide Fabrication

A standard microscope glass slide (Agar Scientific, UK) measuring 76mm x 26mm x 1.2mm was rinsed in acetone and isopropanol (IPA) to remove any organic residues. This was followed by a dehydration bake at 200°C for 30 minutes using a convectional oven [120]. Next, a 10nm layer of chrome and a 200nm layer of gold were deposited using Edwards A306 e-beam evaporator. Acrylic dry film resist, Ordyl AM 130, was used to pattern the actuation electrodes. The resist was laminated onto the chrome-gold layer using a Mega Electronics A4 laminator (Cambridge, UK) heated to 110°C, with a speed of 0.15 m min⁻¹. A 3600dpi positive film acetate foil was used as a mask for patterning the resist. The resist was exposed for 20 seconds, using a Mega Electronics vacuum ultraviolet (UV) exposure unit that was equipped with 6×15 W bulbs. The resist was then developed for 40 seconds using a 0.8% sodium carbonate solution in an ultrasonic bath. The metal layers were then etched using Rockwood Gold etchant and Rockwood Chrome etchant. The dry photo resist was then removed using acetone and IPA, followed by a 10 minutes fuming nitric acid clean. As the dielectric layer for RF MEMS switch is typically about 100nm-200nm thick [106], a 200nm thick layer of sputtered tantalum pentoxide (Ta₂O₅) was deposited on the metal structure using an Oxford Instrument RF sputtering machine as a layer of dielectric material. The contact pads were opened using RIE etch of Ta₂O₅. Figure 5.19 illustrates a processed microscope glass slide with the spacer stack bonded to it.

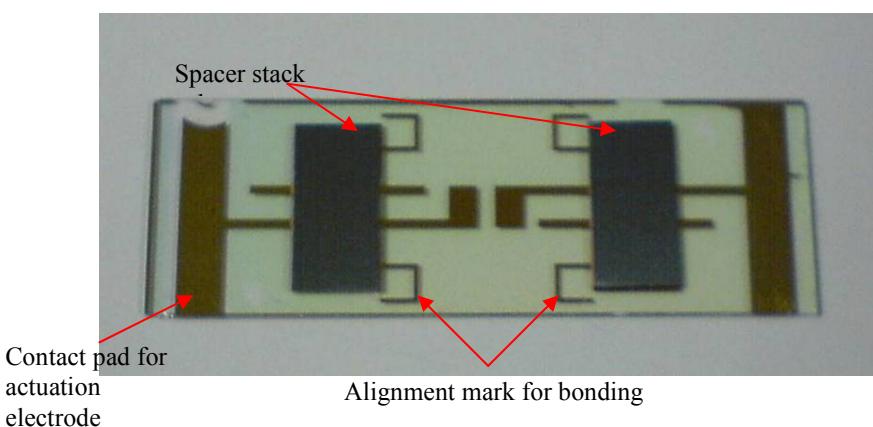


Figure 5.19: A fully processed glass slide electrode with the bonded spacer stack.

5.2.2 PCB Fabrication

A high frequency application PCB (Roger's RO4003[®]) was used as material for the second substrate. The material was selected due to its RF stability at frequencies from 1-18GHz. A coplanar waveguide, with the slot width of 0.3mm and the width of signal line of 1.8mm, was fabricated by a PCB manufacturer (Printed Wiring Technologies Ltd) on a 1.52mm board clad with a 35 μ m copper layer. A layer of photoresist was manually brushed onto the PCB, covering the contact pads of the PCB. This will act as a lift off mask for patterning the dielectric layer on the PCB. A 200nm thick layer of tantalum pentoxide (Ta_2O_5) was then deposited on the metal structure using an Oxford Instrument RF sputtering machine as a layer of dielectric material.

As typical pitch size of commercially available Ground-Signal-Ground (GSG) RF probes is less than 250 μ m, it is therefore not useable for this work. Sub Miniature version A (SMA) connectors were selected as the interface instead between the CPW and network analyzer. These connectors were soldered onto the PCB at the end the PCB fabrication stage.

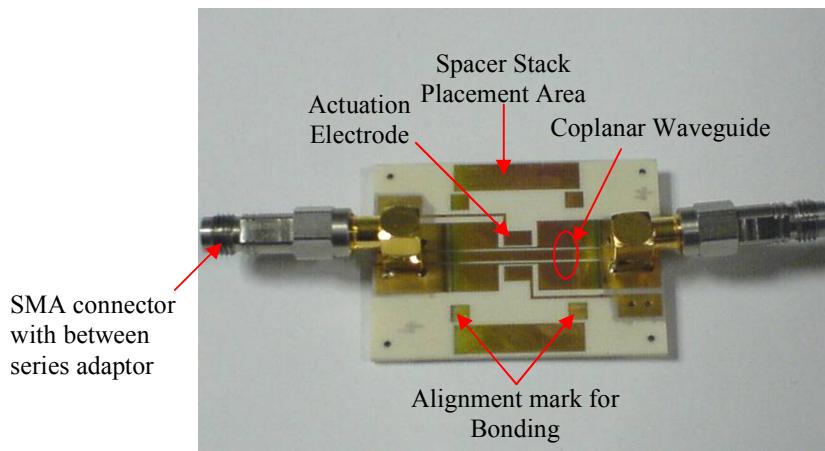


Figure 5.20: An image of the processed Roger's RO4003[®] PCB with the SMA connector and between series adaptors mounted to the substrate.

5.2.3 Fabrication of Armature, Spacer and Prototype Assembly

The armature and spacer of the prototype were formed by etching through a 500 μ m low resistivity silicon wafer. Firstly, the wafer was spun with a 10 μ m layer of

AZ9260. It was then patterned with the design of the armature (8mm by 4mm, rectangle silicon slab) and spacer (20mm by 10mm, rectangle silicon slab). The patterned wafer was mounted onto a carrier wafer using crystal bond before the through etch process, which utilises the STS Pegasus DRIE machine. Finally, the spacer and armature were ready to be manually picked up from the carrier wafer.

A layer of 20 μ m thick Ordyl SY320 epoxy dry film resist was laminated on the silicon spacers. This layer of resist acted as the bonding adhesive between the spacer and the glass slide. The lamination was done using a Mega Electronics A4 laminator at a speed of 0.15 m min⁻¹. The laminated spacers were then manually aligned onto the glass slide without any optical aid. The aligned stack was then sandwiched and clamped by two other glass slides and bulldog clips. They were then cured in a 150°C oven for 4 hours with a ramping rate of approximately 5°C/min [120].

A layer of adhesive was manually applied using a brush to the surface of the PCB where the spacer was placed. The silicon armature was then manually placed across the CPW of the PCB. The glass slide was subsequently visually aligned by eye to the PCB via the pre-defined alignment marks as indicated in Figure 5.19 and Figure 5.20. They were then bonded together by applying force on the PCB and glass slide. Figure 5.21 is the image of a fully fabricated rapid prototype RF MEMS switch.

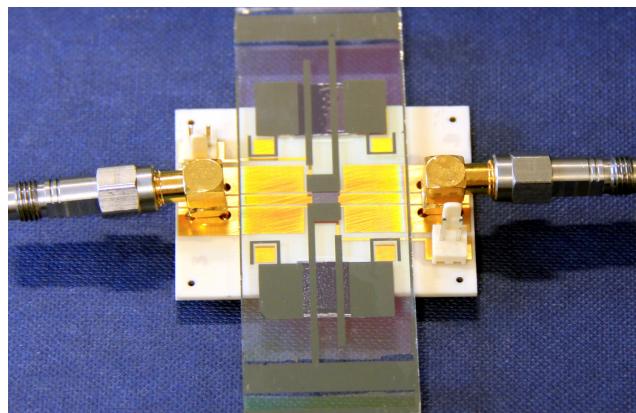


Figure 5.21: An image of the fully fabricated rapid prototype RF MEMS switch.

5.2.4 Discussion

The purpose of this process is to realise an inexpensive and fast method to prototype a RF MEMS switch. Hence, all process steps are relatively straight forward with the exception of the dielectric deposition step.

Silicon dioxide was initially selected as the dielectric material for this process step. The dielectric layer was deposited on to the electrode structure using an ion beam deposition System, Ionfab 300 Plus (Oxford Plasma Technology, UK). This was the only oxide deposition technique available at this time. The deposited layer had adhesion problem at the gold interface, causing the oxide layer to delaminate as illustrated in Figure 5.22. The adhesion problem can be attributed to the material properties of gold. Annealing of the gold layer could improve adhesion, but this was not feasible as the oxide layer was already damaged when the deposition chamber was vented to atmospheric pressure after the deposition process. Consequently, an alternative dielectric material was explored to resolve this issue.

As the temporary clean room was newly setup at the point of evaluation, there were limited number of dielectric materials that were available for deposition. They are TeflonTM and tantalum pentoxide (Ta_2O_5). Both of them have excellent dielectric properties [150-152] e.g. stable dielectric constant over a wide range of frequencies.

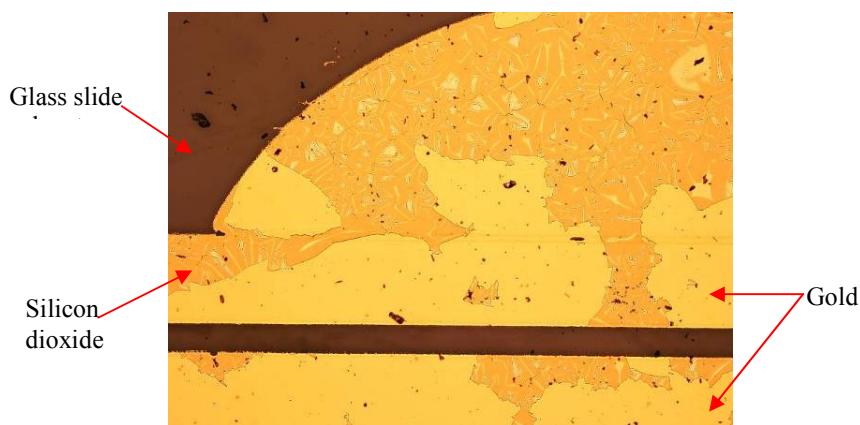


Figure 5.22: A microscope image of a ion beam deposited silicon dioxide layer poorly adheres to the chrome gold structure on a microscope glass slide.

TeflonTm was deposited using an Edwards A306 thermal evaporator. The deposition rate ranged from 0.3nm/s to 3.0nm/s at a current of 0.6A. The large variation in deposition rate made the repeatability of depositing a thin film rather challenging. This was due to the fact that the source was evaporated through resistive heating of the crucible. The time lag from the current being terminated to the complete halt of evaporation is usually sufficient to overshoot the deposition target thickness. Furthermore, the deposited layer was relatively soft and was easily damaged during post-process handling and testing.

Tantalum pentoxide (Ta_2O_5) was deposited using the Ionfab RF Sputtering system. The sputtering takes place in an argon and oxygen environment at a temperature of 200°C, with a deposition rate at approximately 1.5nm/s. This dielectric material is well known for both its chemical and physical robustness [153], which makes it difficult to etch. A well documented method for removing the oxide layer employs a dry etch system with carbon tetrafluoride (CF_4) as one of the etch gases [154]. However, this as not available in the cleanroom, sulfur hexafluoride (SF_6) was used as a substitute. The recipe with SF_6 as a processing gas works well but produces a slower etch rate of 30nm/min as compared to the CF_4 version.

After consideration of all issues about the selection of the dielectric materials, tantalum pentoxide was chosen to be the most suitable material.

5.3 Summary

A suitable fabrication process was described in this chapter for the micron-scale prototype, building on previous work done on similar mechanically unrestrained devices within the research group. The fabrication, which was reported in three sections, utilised nine photolithography masks and required 19 major process steps to realise the final device. Processing of all individual wafers as well as the wafer bonding was successful. Work on the bonded stack had reached the stage of Pyrex grooving where the armature was found to be stuck between the silicon layer and bottom Pyrex wafer. The reason for the failure was the uncontrolled application of UV glue on the bottom Pyrex, which caused the thickness of the adhesive layer to be thicker than that of the armature.

There were other challenging issues encountered during the fabrication process, especially the glass etch, bonding of the SOI wafer to the Pyrex wafer and the DRIE process, which were discussed in detail and solved successfully.

The process flow for a rapid prototype device was introduced, requiring two positive film masks and six major fabrication steps. The fabrication of the rapid prototype switch has been successful. During the course of fabrication, opportunities were available to evaluate the feasibility of depositing the different dielectric materials for the wafer level fabrication. The rapid prototyping process has proven to be simple and cost effective in proofing of concept, where the cost and the turnover time were kept to a minimum.

Chapter 6

Measurement

The characterisation of an RF MEMS switch is performed to ascertain its RF losses, electromechanical responses and the operation lifetime of the switch [155-157]. The switching capacitance and its mechanical response can be measured using the setup shown in Figure 6.1(a). When a range of DC voltages below the minimum pull-in voltage is applied to the RF MEMS switch, the switching capacitance at different air gap can be measured. Increasing the DC actuation voltage above the minimum pull-in voltage will determine the switching time of the device. With the setup illustrated in Figure 6.1(b), the switch lifetime can be characterised. When a fixed RF frequency is applied on the coplanar waveguide (CPW) coupled with a DC pulsed actuation voltage, the switch actuates between the UP and DOWN states. Degradation in actuation voltage can be used as a factor in determining the lifetime of switch. If the RF signal is applied in the sweeping mode, e.g. 0.1-40GHz, the RF losses of the RF MEMS switch can be measured during the two states of the pulse signal.

Although the fabrication did not harvest any working micron-scale prototype at the end of the process, some tests were conducted on fabricated wafers with transmission line to verify the RF characteristic of proposed design. Section 6.1 details the S-Parameters of the fabrication CPW design. Section 6.2 discusses the RF characteristics of the shunted CPW, utilising a silicon slab as the armature of the RF MEMS switch. Section 6.3 reports on the RF characteristics and mechanical response of the rapid prototype switch. Finally, a conclusion of the work is drawn in section 6.4.

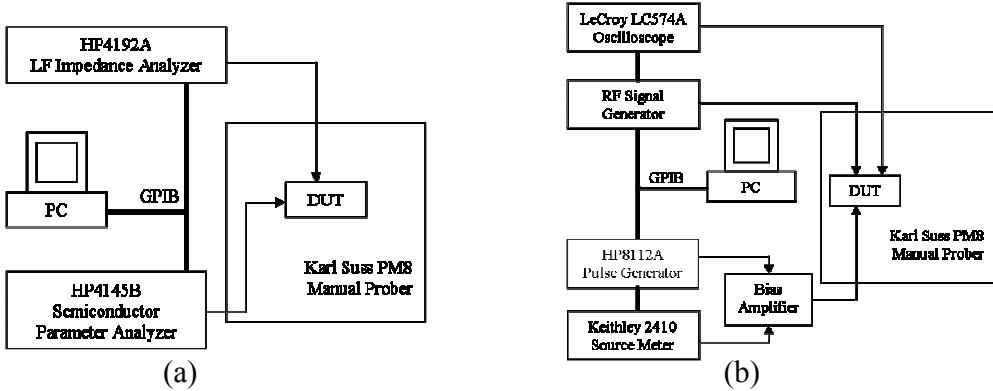


Figure 6.1: RF MEMS switch testing setup for (a) quasi-static CV measurement (b) life time measurement [158].

6.1 RF Characterisation of the Transmission Line

The RF characterisation of the transmission line was carried out in both University of Glasgow and University of Southampton. The difference of the measurement laboratories was the network analyser utilised. In the University of Glasgow, it uses the Agilent N5250C PNA Millimeter-Wave Network Analyzer together with Cascade Air Coplanar Probes, which was capable of sweeping frequencies from 10MHz to 110GHz. Due to the inherent design and substrate material, the micron-scale prototype was expected to operate optimally in W-band frequency between 67GHz – 110GHz. This measurement setup will be able to realise the actual potential of the switch. The experimental setup in University of Glasgow is as shown in Figure 6.2(a). On the other hand, the laboratory in Southampton is equipped with Agilent E8361A PNA Network Analyzer and Cascade Infinity probes, which is capable of measuring up to 67GHz.

The return and insertion losses as shown in Figure 6.2(b) are measured from the two transmission lines of different parts of the wafer for a frequency of 0.1GHz to 110GHz. The return loss of the fabricated transmission line is more than -10dB for frequencies above 22GHz. The measured insertion loss presented is more than -4dB for frequencies above 30GHz. There is a resonance at 75GHz which is measured about -

48dB. A true transmission line should have relatively low and constant insertion loss. The fabricated transmission line was considered to be lossy in the measured frequency range.

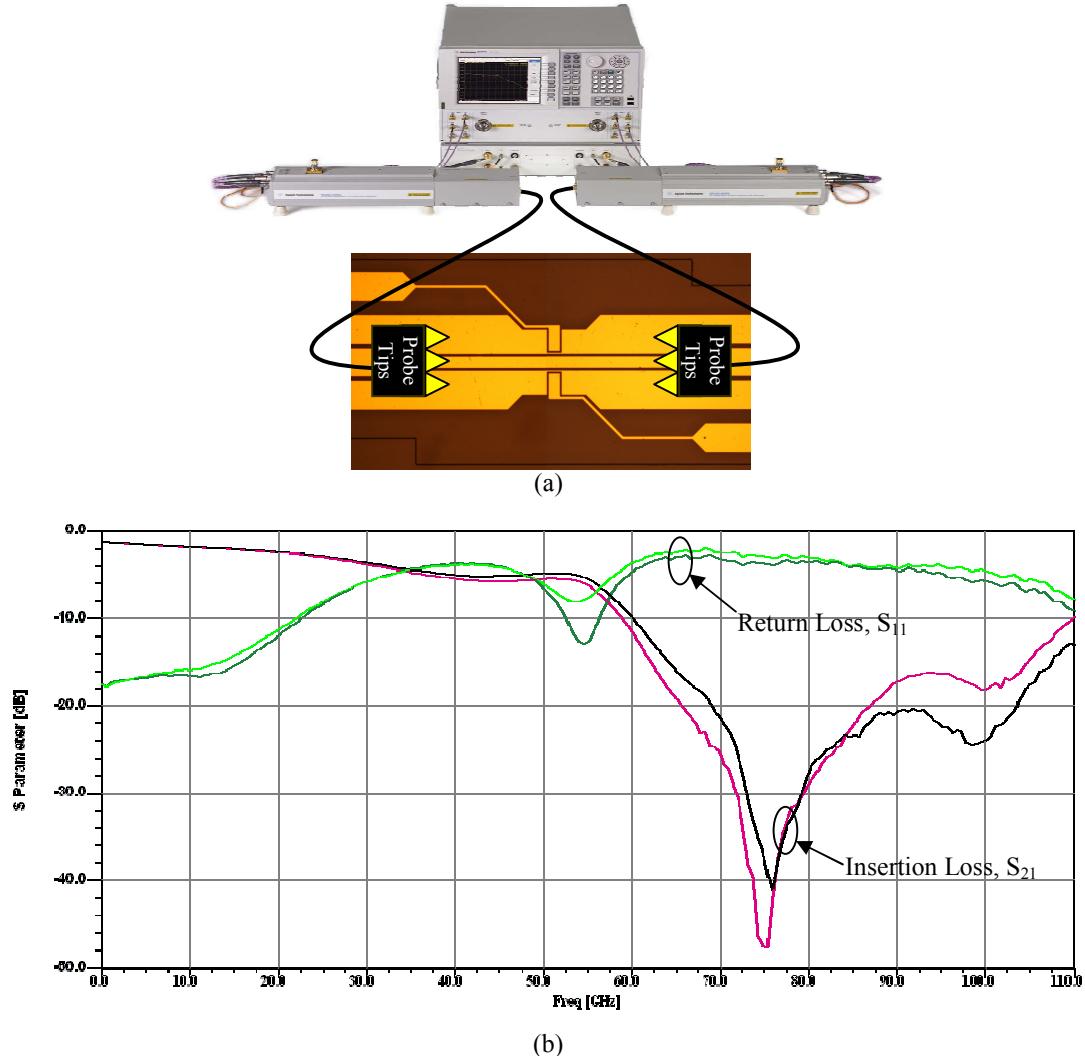


Figure 6.2: (a) Setup for S-Parameter measurement using Agilent N5250C PNA Millimeter-Wave Network Analyzer with Cascade air coplanar probes on the fabricated CPW. (b) Measured S-Parameter of two 50Ω CPW from 0.1-110GHz.

The CPW together with the probe pads were modelled using Agilent Advanced Design System (ADS) as lumped model of the test structure shown in Figure 6.3(a). Components CPW1 and CPW2 represent the full length of the 50Ω transmission line while component CPW3 and CPW4 correspond to the probe pads terminating at both ends as defined in Figure 6.3(b). Term1 and Term2 were equivalent of the two probes connected to the network analyser. However, the grey area as shaded in Figure 6.3(b)

cannot be modelled as it had a tapper feature which could not be easily represented in the simulation package.

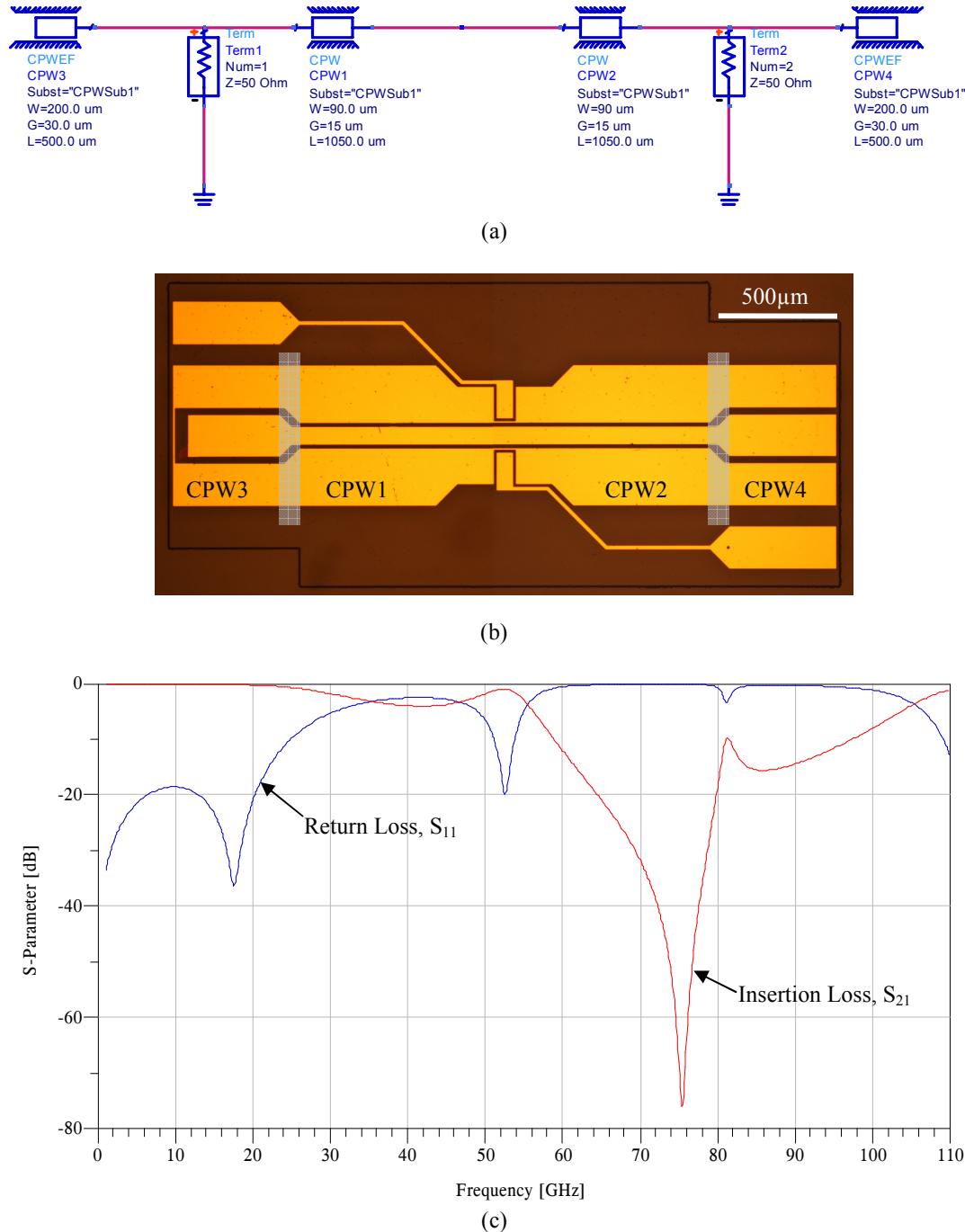


Figure 6.3: (a) Micrograph of the transmission line under test (b) Lumped model of the transmission line using Agilent ADS (c) Simulation results of the fabricated CPW using Agilent ADS.

The simulated results (as shown in Figure 6.3(c)) for both return and insertion losses of the RF MEMS switch were similar to measured values presented in Figure 6.2(b). The simulated return loss is more than -10dB for frequencies above 25GHz. The simulated insertion loss starts to roll off frequencies above 52GHz. There is a resonance at 75GHz which is measured about -76dB. Based on the insertion loss at the resonant frequency, it can be deduced that the resistivity of the fabricated transmission line was much higher than the ideal case. The resonance dip at 75GHz in both simulation and measurement results indicated the presence of high reflectance structure in the CPW.

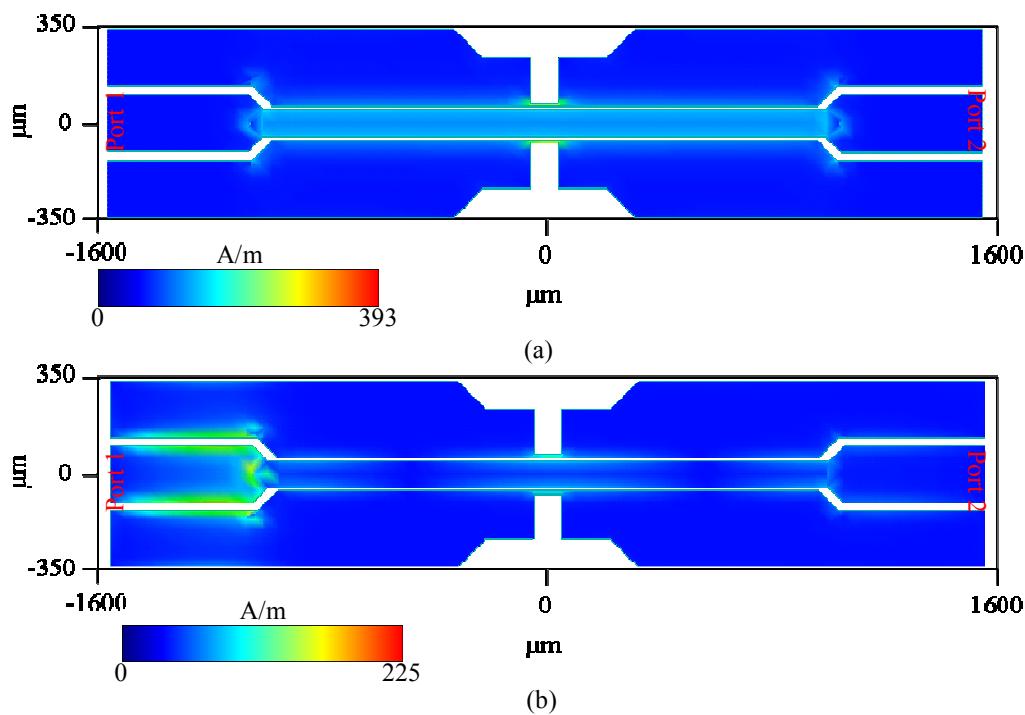


Figure 6.4: Simulated current density plot of the CPW at (a) 1GHz (b) 79GHz using Agilent Momentum.

The current density plot of the CPW transmission line was modelled using the Momentum module from Agilent Advanced Design System (ADS) simulation package. The simulation was to identify the electromagnetic characteristic of the resonance dip. The current density plot of the transmission line which was driven by a 50Ω port is depicted in Figure 6.4. The results revealed that the electromagnetic wave was able to flow through the signal strip without much problem at frequencies below 50GHz. However, at higher frequencies, it was concentrated at the probe pad region. The

mismatch in probe pad design of the CPW have caused degradation in the RF performance of the transmission line design.

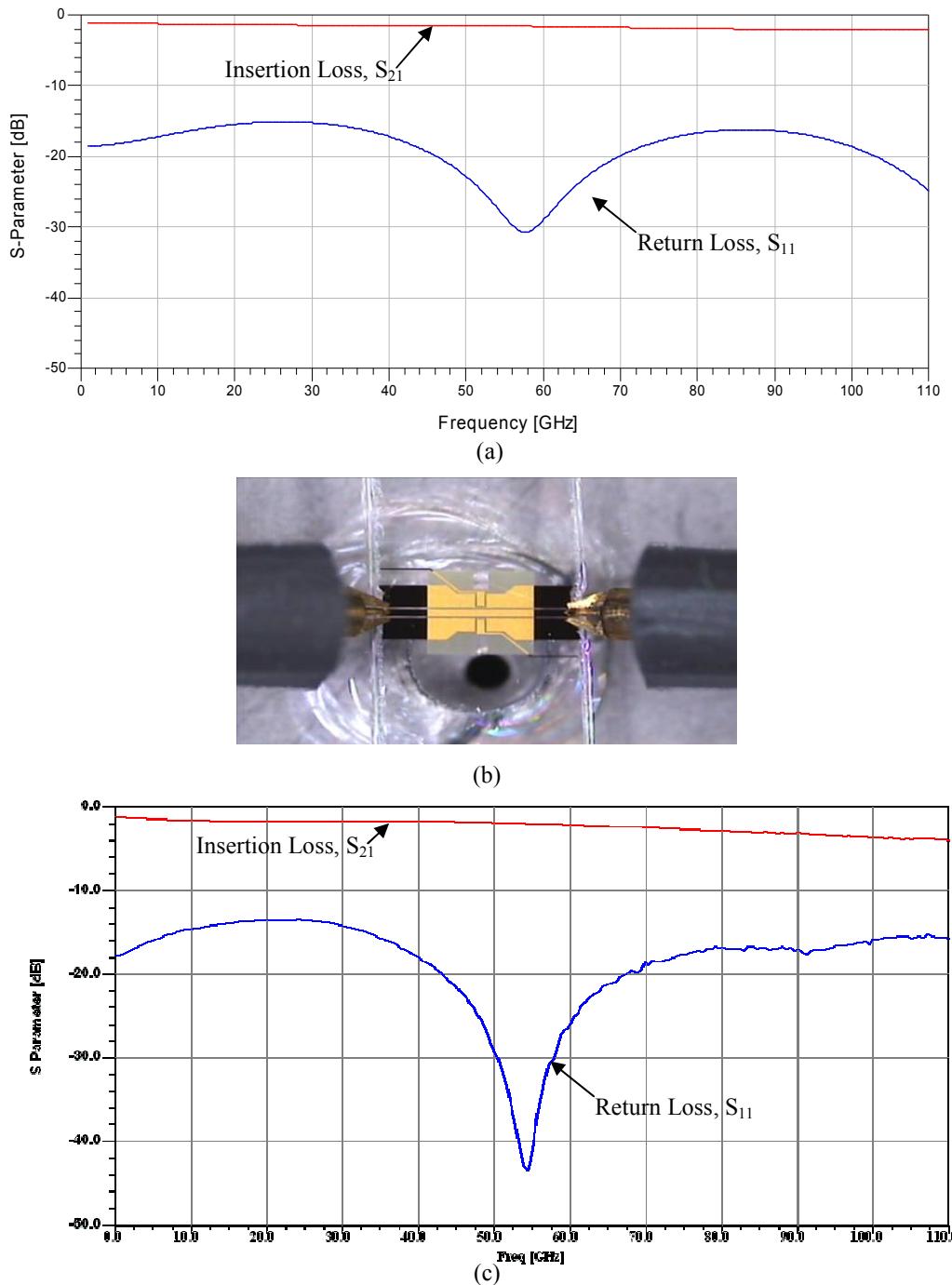


Figure 6.5 : (a) Simulated S-Parameters of the CPW without probe pads using Agilent ADS. (b) Fabricated transmission line structure with the probe pads being physically removed for the measurement (c) Measured S-Parameters of the transmission line as shown in Figure 6.5(b).

By removing CPW3 and CPW4, the simulated S-Parameters are shown in Figure 6.5(a). The insertion loss is less than -2dB for frequencies up to 110GHz. In addition, the return loss of the CPW is no more than -15dB for frequencies up to 110GHz. After removing the probe pads from the fabricated 50Ω transmission line as illustrated in Figure 6.5(b), the S-Parameter was measured again. Figure 6.5(c) presents the return and insertion losses of the transmission line from 0.1-110GHz. These results show the true features of a properly designed transmission. The insertion loss shows a gradual increase between port 1 and port 2 as the sweep frequency increases. In addition, the return loss shown in Figure 6.5(c) has similar trends as that observed in simulations shown in Figure 6.5(a). The return loss is less than 13.5dB for frequencies up to 110GHz. This experiment has also proven the lossy S-Parameters shown in Figure 6.2(b) and Figure 6.3(c) are related to the tapered feed design which is deemed to be too steep. This shows the importance of integrating the probe pad design into the CPW.

6.2 RF Characterisation of a Shunted Transmission Line

The main goal was to measure the S-Parameter of the switch in the UP and DOWN state, with the armature away or in contact with the dielectric layer on the transmission line. During the UP state with a large capacitive gap, the RF MEMS switch was assumed to be a transmission line without an armature. The armature was manipulated manually by placing or removing across the transmission line, so that the S-Parameters of RF MEMS switch can be measured. It was a challenge to manually manipulate an armature with the size of $680\mu\text{m} \times 80\mu\text{m} \times 50\mu\text{m}$, hence a piece of silicon measuring $800\mu\text{m} \times 800\mu\text{m} \times 500\mu\text{m}$ was employed as the armature. The transmission line characteristic measurement repeated in University of Southampton was to confirm the measurement results taken from University of Glasgow and to further measure the effects of having a shunting armature on the CPW. Figure 6.6 shows the CPW with an armature during measurement.

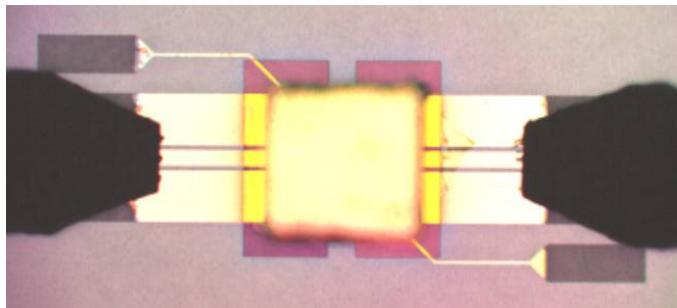


Figure 6.6: Micrograph of the S-Parameter measurement using Agilent E8361A PNA Millimeter-Wave Network Analyzer with Cascade infinity probes on the fabricated CPW with a $800\mu\text{m}$ by $800\mu\text{m}$ silicon slab acting as armature.

Figure 6.7(a) illustrates the measured S-Parameters of the transmission line from 0.1-67GHz. The measured S-Parameter results are similar to those of Figure 6.5(c) with the exception of a shorter RF range, i.e. up to 67GHz. The insertion loss is approximately -1dB at 67GHz. The modelled current flow plot of the transmission line as depicted in Figure 6.7(b) has also shown the electromagnetic field was propagating in the transmission line structure. These results also confirmed the initial findings of the measurements done at the University of Glasgow.

The switch was assumed to be in DOWN position when the silicon armature was placed over the CPW. The measurements taken were overlay with simulation results as shown in Figure 6.8(b). The DOWN state S_{21} is approximately -13dB at a frequency of 67GHz. This showed that the silicon armature was shunting signal to the ground plane of the CPW. The measured results were fitted into the lumped RLC model using Agilent ADS depicted in Figure 6.8(a). The fitted model showed a high inductance, at approximately 20pH, while the switch's DOWN state capacitance was approximately 0.15pF. The accuracy of the switch resistance is unable to be determined as the sweep frequency range is lower than the DOWN state resonant frequency of the switch. The fitted results were very different from the analytical parallel plate capacitance which was expected to be approximately 64pF. However, when the armature was bowed, the calculated DOWN state capacitance was reduced to 0.58pF. There is a possibility that the silicon armature is not in proper contact with dielectric layer as the S-Parameter changes when a force was exert on the top surface of the armature.

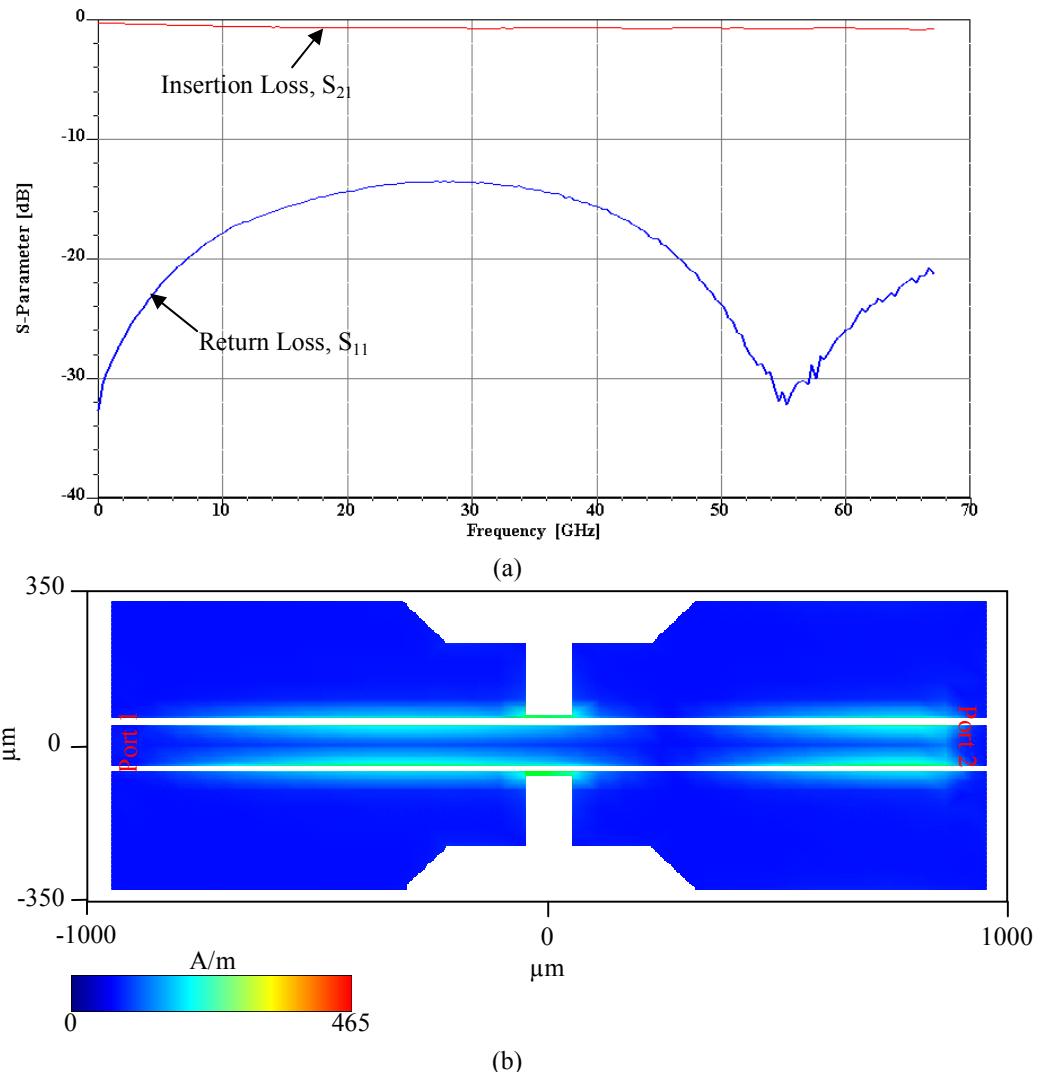


Figure 6.7 : (a) Measured S-Parameters of the CPW from 0.1-67GHz (b) Simulated current plot of the CPW at 70GHz using Agilent Momentum.

To verify the armature structure, a FEM model using ADS Momentum was created to investigate the effects of improper contact between the armature and transmission line. As ADS Momentum is unable to model a bowed armature, the armature was assumed to be position above the transmission line with an air gap. The S-Parameter of such model is depicted in Figure 6.8(b). These simulated results matched well to the measured results. Hence, the initial hypothesis of the analysis was verified. The current plot of the model shown in Figure 6.9 verified that even though the armature

was not in proper contact to the transmission line, the silicon armature demonstrated good electromagnetic coupling

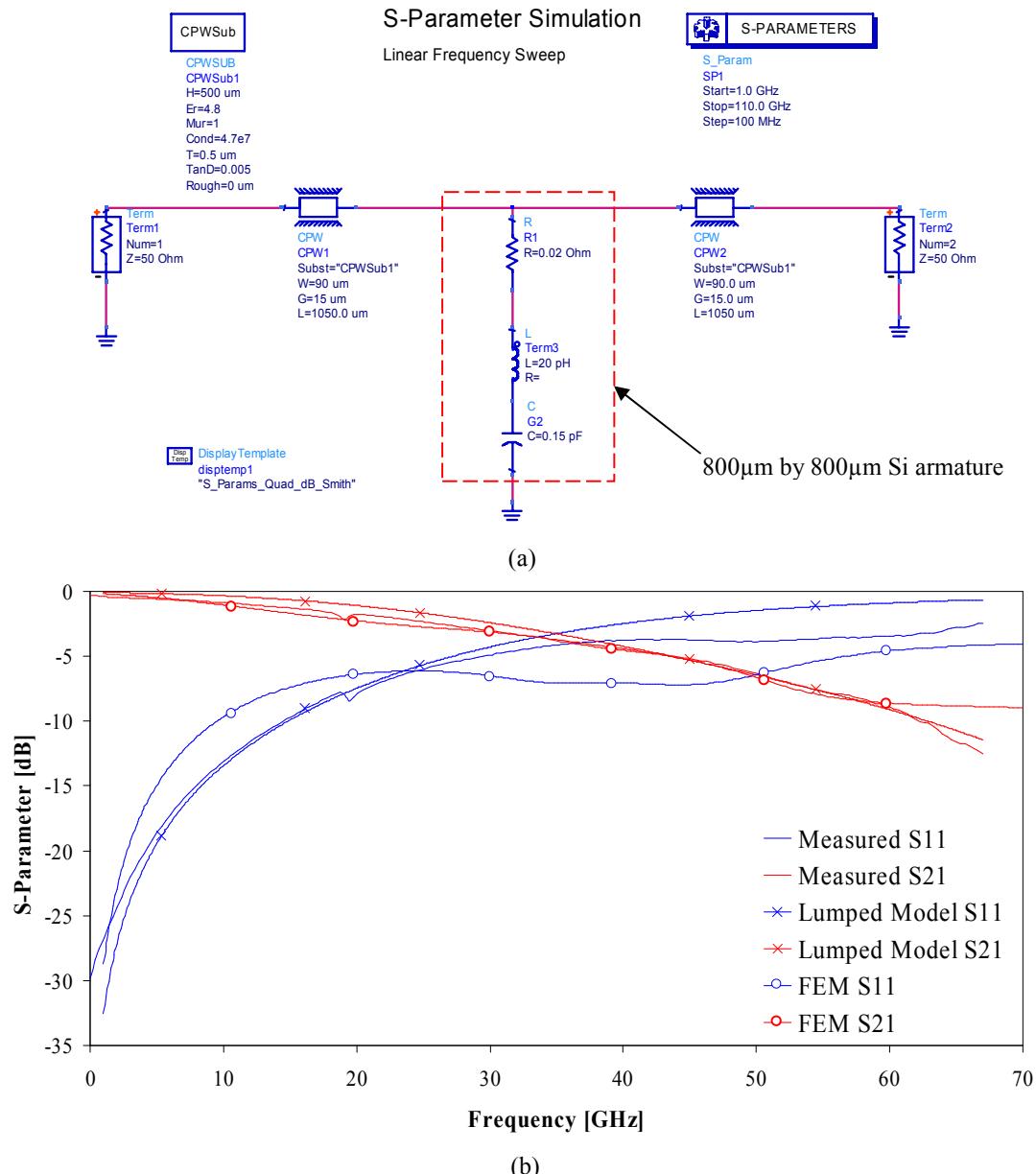


Figure 6.8 : (a) Agilent ADS lumped model of the RF MEMS switch with with a 800μm by 800μm silicon slab acting as armature. (b) Measured, ADS lumped model simulated and FEM simulated S-Parameters of the RF MEMS switch from 0.1-67GHz.

In comparison to the isolation and insertion loss of the RF MEMS switch from Figure 6.7 and Figure 6.8, the insertion loss is relatively flat as compared to the isolation.

The RF switching function can be realised by employing a low resistivity silicon armature, where the conductivity of the armature material is 2 orders of magnitude lower than any conventional armature.

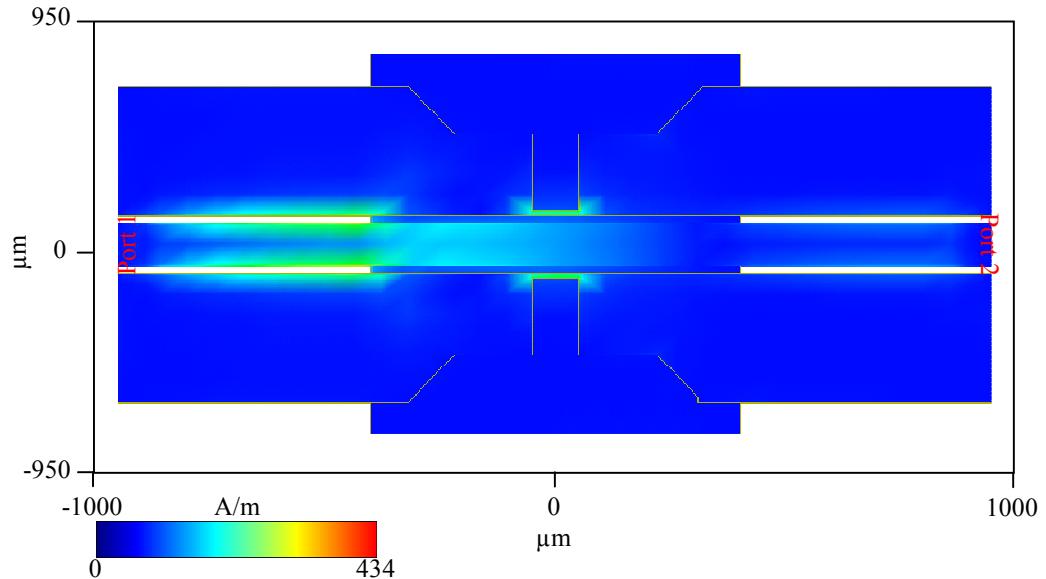


Figure 6.9 : Simulated current density plot of the CPW with armature shunting the RF signal at 70GHz using Agilent Momentum.

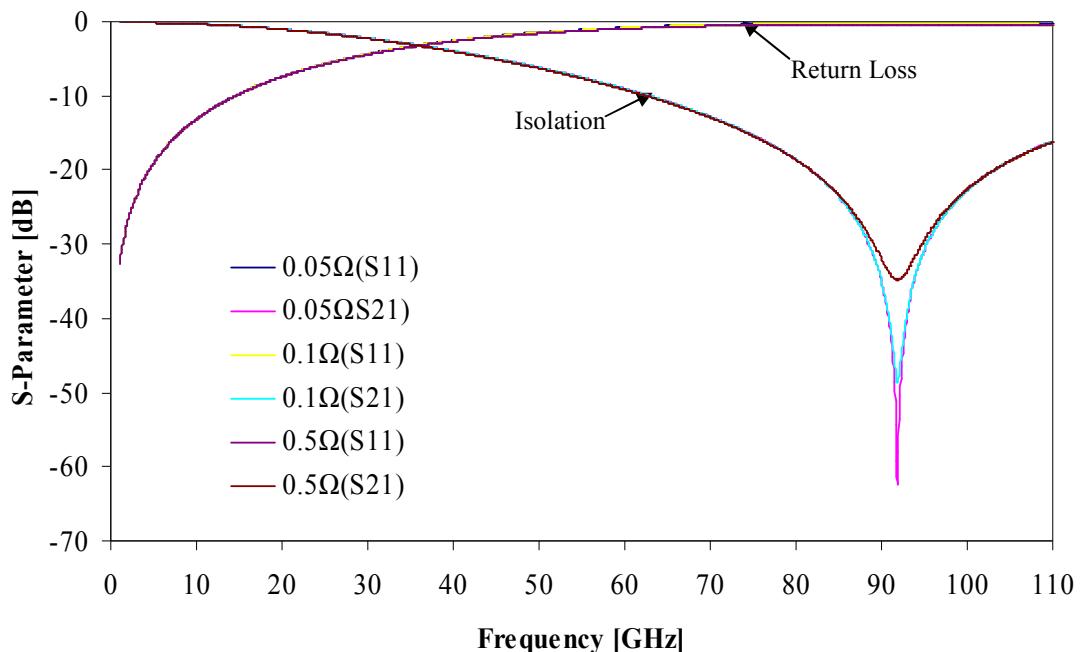


Figure 6.10 : Simulated Insertion loss and Isolation of proposed RF MEMS switch from 1 – 110GHz for switch resistance value of 0.02Ω , 0.1Ω and 0.5Ω .

When the fitted model was extended further to 110GHz, the switch resonant frequency appeared at 92GHz. Three isolation curves as shown in Figure 6.10 are simulated from the model by using three different armature resistances, i.e. 0.02Ω , 0.1Ω and 0.5Ω . The general trend of these curves does not change except that the lower switch resistance give better isolation performance at the isolation minima.

6.3 Measurement of the Rapid Prototype Switch

As the main goal of this work was to prove the feasibility of the concept, most of the device dimensions, e.g. the capacitive gap, size of the armature, were selected based on the ease of handling during measurement. The rapid prototype switch was fabricated with a 50Ω conductor backed coplanar waveguide. This section is subdivided into 2 parts. Section 6.3.1 reports on the RF characteristics of the rapid prototype switch while section 6.3.2 details the mechanical response of the rapid prototype switch.

6.3.1 RF Measurement of the Rapid Prototype Switch

The measurement setup used in this section is similar to the one described in the previous section. However, the measurements were taken with a pair of SMA connectors which were soldered to the two ends of the CPW. The rapid prototype device was mounted with a 0-18 GHz SMA connector which was used to interface between the transmission line and network analyzer. The RF cable of the network analyzer employed a 1.85mm connector which was not compatible with the SMA connector. In order to match the SMA connector and 1.85mm connector of the PNA cable, a between series adapter was required during measurement. The calibration of the PNA was done with Agilent N4694A Electronic Calibration Module. Figure 6.11 shows the setup for measuring the S-Parameters of the transmission line of the rapid prototype switch. The setup consisted of an Agilent E8631A network analyzer which was connected to the device under test (DUT) via a pair of between series connectors.

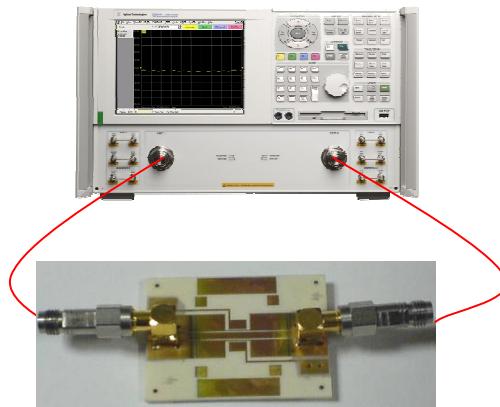


Figure 6.11: Measurement setup for initial testing of the transmission characteristics of the rapid prototype device using an Agilent E8361A network analyzer.

Figure 6.13 (a) shows the simulated lumped model of the test structure using Agilent ADS software. The lumped model used in the simulation consists of a CPW transmission line [159], a capacitor, an inductor and a phase shift element, where the latter three components represent the SMA connector [160]. The simulation was driven by a pair of 50Ω ports, which represent the two port connectors of the network analyzer.

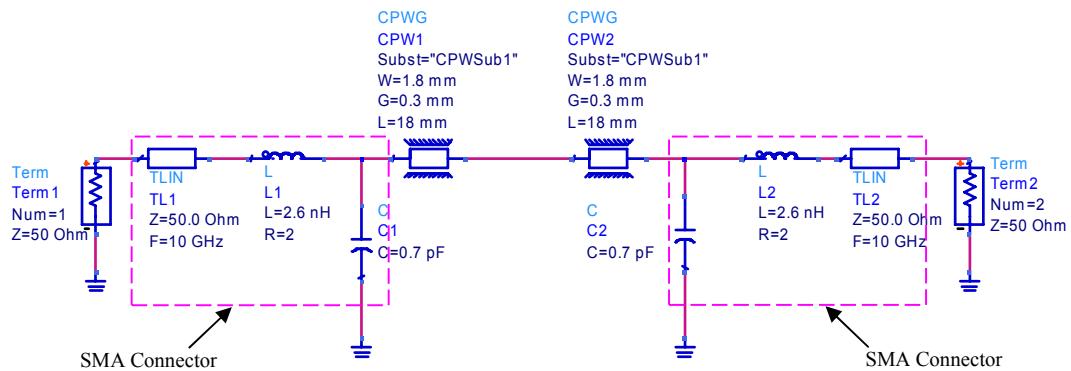


Figure 6.12: (a) Agilent ADS lumped model of the rapid prototype switch's CPW embedded with SMA connectors.

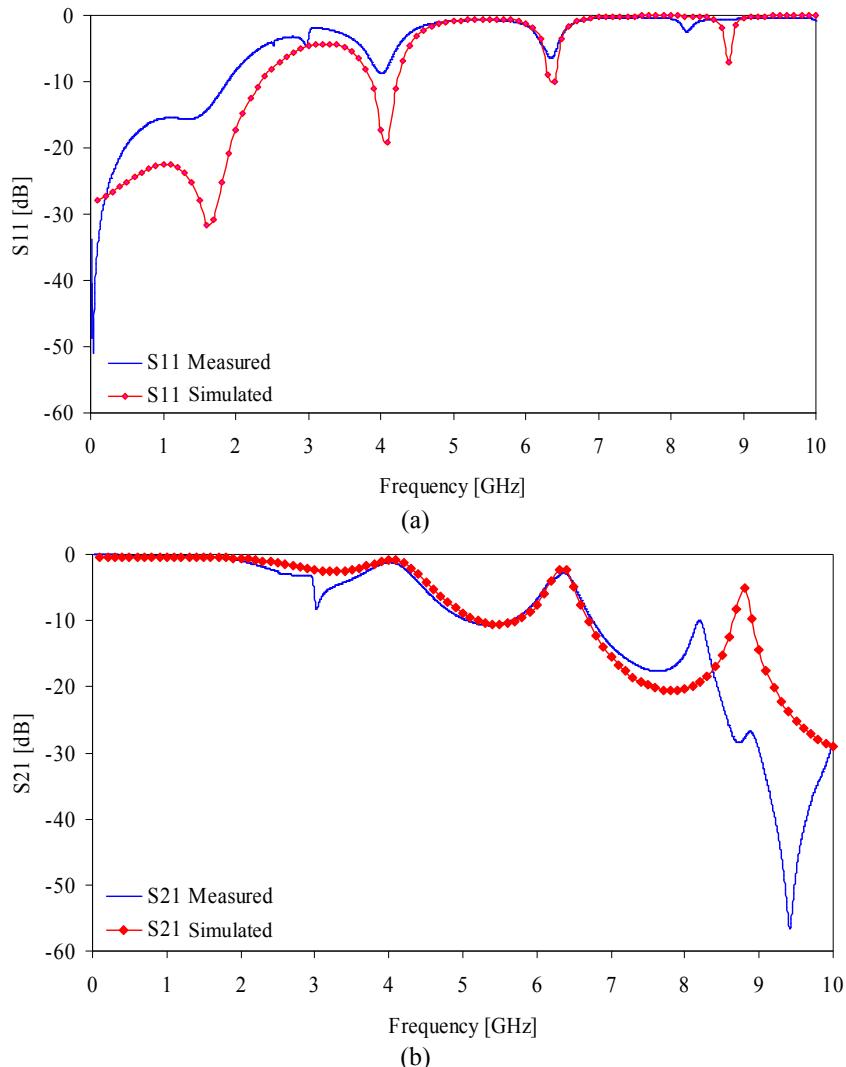


Figure 6.13: Measured and simulated (a) S₁₁ and (b) S₂₁ of the rapid prototype switch's CPW from 0.1-10GHz.

Figure 6.13 (a) and (b) illustrate the simulated and measured S₁₁ and S₂₁ parameters of the rapid prototype switch's CPW. As the parameters of SMA lumped model were unknown, the simulation was performed to find the best fitted results as compared to the measured data. The simulated values of the series resistance of the inductor, the inductance and the capacitor of the SMA model were 2Ω, 0.7pF and 2.6nH respectively. The simulated return and insertion loss of the CPW were -0.5dB and -29dB for frequency at 10GHz respectively. Both simulated and measured S-Parameters exhibited some form of electromagnetic modes occurring at periodic intervals. The

measured results were compared with the simulated results of the DUT modelled with the Agilent ADS software. The difference between the simulated and measured S_{11} is about 7dB at 1GHz. But the results converge as RF frequency increases. The measured S_{21} results deviated from the simulation for frequencies above 7GHz. The difference is approximately 30dB at 9.5GHz. These differences can be attributed to the unavailability of a lumped model which represents the between series adaptors used in the measurement. The simulated results of lumped modelling are less accurate, as the compared to full 3D electromagnetic modelling, higher electromagnetic order mode of the device structure are ignored. The modelled SMA connector from the measurement results was used at a later stage to de-embed the S-Parameter of the rapid prototype switch from the simulated model of the measured results.

By removing the SMA related elements from the ADS, the S-Parameters of the CPW can be simulated. These simulations are shown in Figure 6.14 (a) and (b). The simulated return loss and insertion loss of the rapid prototype switch's CPW are -37dB and less than 0.24dB for frequencies under 10GHz respectively.

So far only the CPW is measured and measurements on the RF MEMS are presented in the next section. Figure 6.15 shows the measurement setup of the rapid prototype switch. The setup consists of an Agilent E8631A network analyzer and Agilent 66101A power supply. The network analyzer was used to measure the S-Parameters of the rapid prototype switch, while the power supply generated an actuation voltage to the electrode, which actuated the armature of the rapid prototype switch.

For the unpowered switch, the armature of the rapid prototype switch is always in the DOWN state. The S-Parameters can be measured by simply connecting the network analyser to the SMA connectors of the rapid prototype switch. When the actuation voltage is applied to the top actuation electrodes, a pull-up force is generated to attract the armature to the top electrode. With the armature in the UP state, the S-Parameters are measured by the network analyzer when operating in a single trigger mode function. When the DC voltage is removed from the top electrode, the armature falls down due to the earth's gravity.

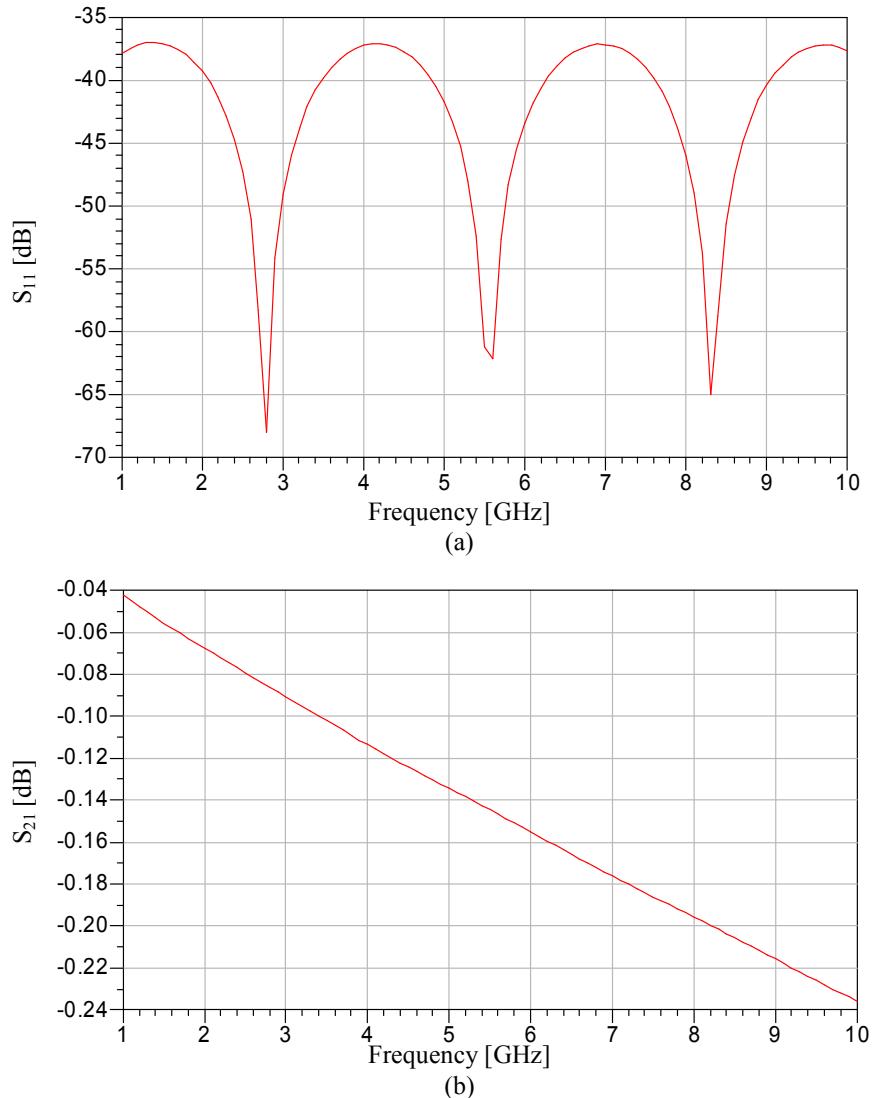


Figure 6.14: Simulated (a) S_{11} and (b) S_{21} of the CPW from 0.1-10GHz using ADS.

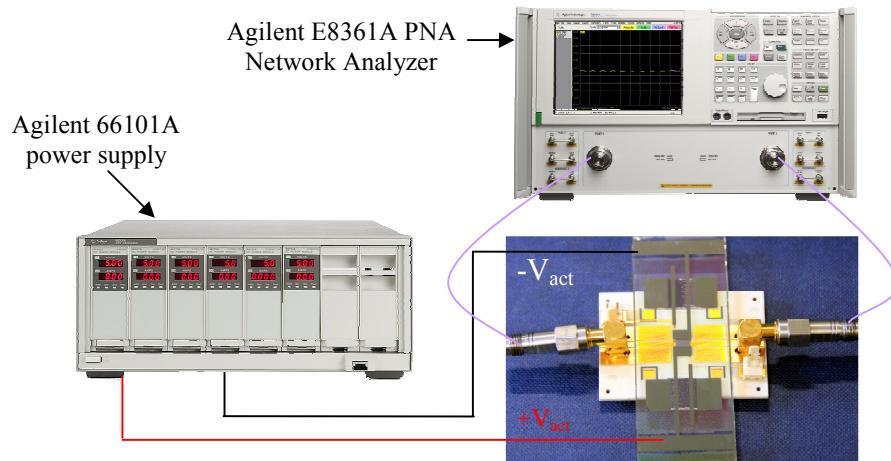


Figure 6.15: Measurement setup for mechanical response of the rapid prototype device using an Agilent E8361A network analyzer and an Agilent 66101A DC power supply.

The measured return losses for the RF MEMS switch in both states (as shown in Figure 6.16 (a)) exhibits similar losses of <-0.5 dB for frequencies above 4GHz. Figure 6.16 (b) illustrates the measured S_{21} of the rapid prototype switch for both actuation states. The general trends look comparable. The rapid prototype switch was very lossy as the measured insertion loss was higher than -10dB for frequencies greater than 2GHz. There is a resonance like double dip at frequencies between 5.4GHz and 6.3GHz, which is due to higher order substrate mode. However, it is noted that the switch cannot be operated at frequencies around 1.6-2.7GHz and 5.5-6.6GHz. The signal shunted over those frequencies is much higher when the armature is in the UP state as compared to the DOWN state. The best narrow band operating frequencies is at 3.3GHz and 6.9GHz. The difference between the insertion loss and isolation is about 15dB at both frequencies. This was modelled using Agilent ADS tool to determine the SMA influence.

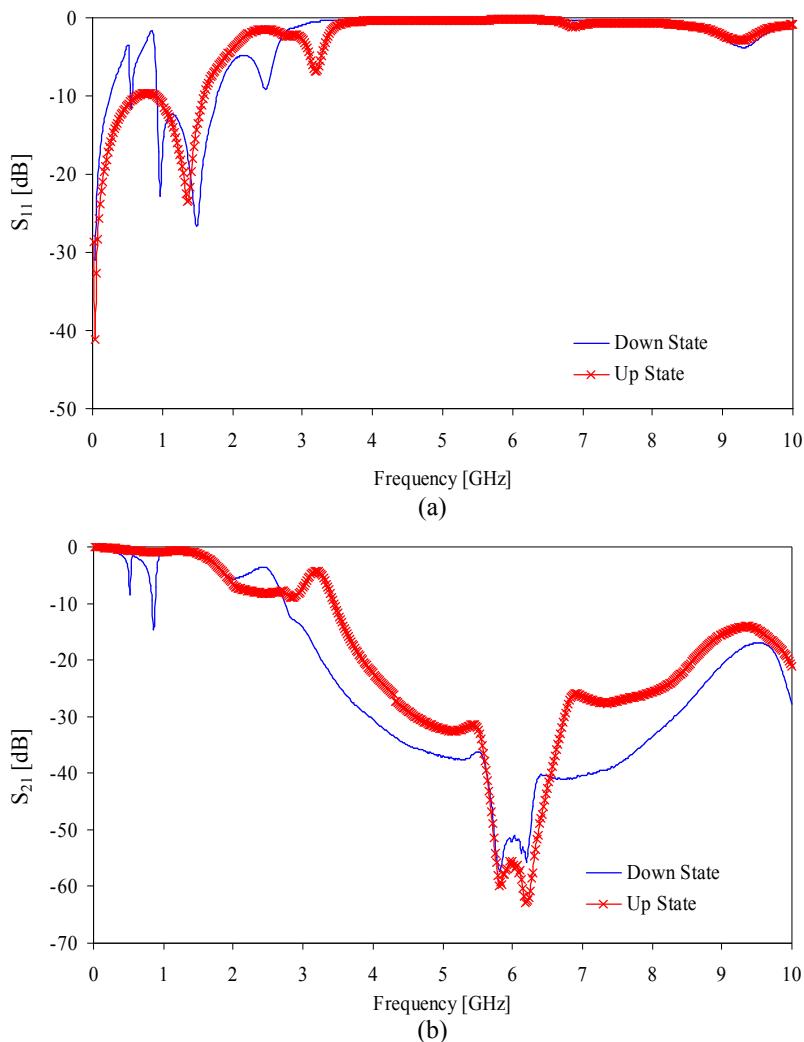


Figure 6.16: Measured (a) S_{11} (b) S_{21} parameter of the rapid prototype switch when the aramture is at the DOWN and UP state from 0.1-10GHz.

Figure 6.17 (a) illustrates the Agilent ADS lumped model of the rapid prototype switch. This model encompassed the SMA model (denoted in the pink box) and the lumped RLC model of the rapid prototype switch (denoted in the red box). The simulation was driven by a pair of 50Ω ports, which represent the two port connectors of the network analyzer.

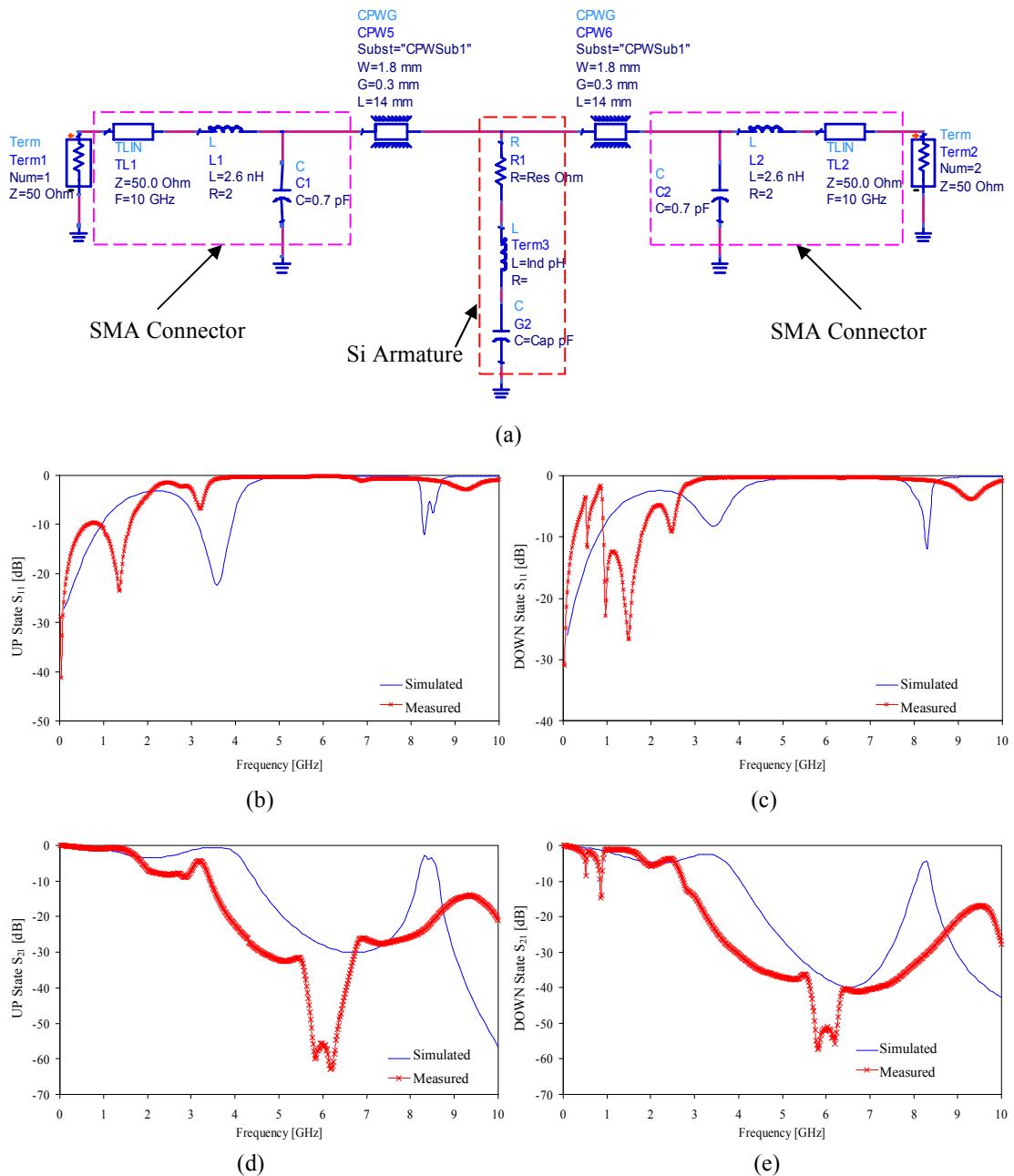


Figure 6.17: (a) Agilent ADS model for the rapid prototype switch embedded with the SMA connectors. (b) Measured and simulated UP state S_{11} (c) Measured and simulated DOWN state S_{11} (d) Measured and simulated UP state S_{21} (e) Measured and simulated DOWN state S_{21} parameter of the rapid prototype switch from 0.1-10GHz.

Figure 6.17 (b-e) depicts the simulated S-Parameter overlaid with the measured results of the rapid prototype switch for both UP and DOWN state. The simulated results show some correlation with the measurement results. The simulated RLC value of the UP state model are 0.1Ω , 110pH and 2pF respectively, while the simulated RLC value of the DOWN state model were 2Ω , 205pH and 2.7pF respectively. The discrepancy between the two results can be attributed to several factors. Firstly, the DOWN state armature was considered as a fixed resistance value. The skin effect of the RF signal propagating in the silicon armature was not taken into consideration. The skin depth of the RF signal is $50\mu\text{m}$ at 1GHz and decreased to $18\mu\text{m}$ at 10GHz . The actual resistance of the armature at 10GHz is three times than that at 1GHz . Secondly, the error in modelling observed in Figure 6.13 was also coupled into the new model presented here.

By removing the lumped model of the SMA connectors from the simulation, the simulated S_{11} and S_{21} parameters of the rapid prototype switch are shown in Figure 6.18. The insertion loss of the rapid prototype switch was very high, i.e. more than -1dB . The DOWN state resonant frequency is at 6.8GHz with an isolation of -23dB . The capacitance ratio is 1: 1.35. The poor capacitance ratio is mainly attributed to the poor DOWN state contact between the dielectric layer and the armature. The roughness of the contact area surfaces and the bowing/warping of the silicon armature are the main reasons for such poor contact. The simulated DOWN state capacitance was 2.7pF as compared to the theoretical value of 32.4pF (based on equation 4.20). This phenomenon was also observed in the measurement described in section 6.2.

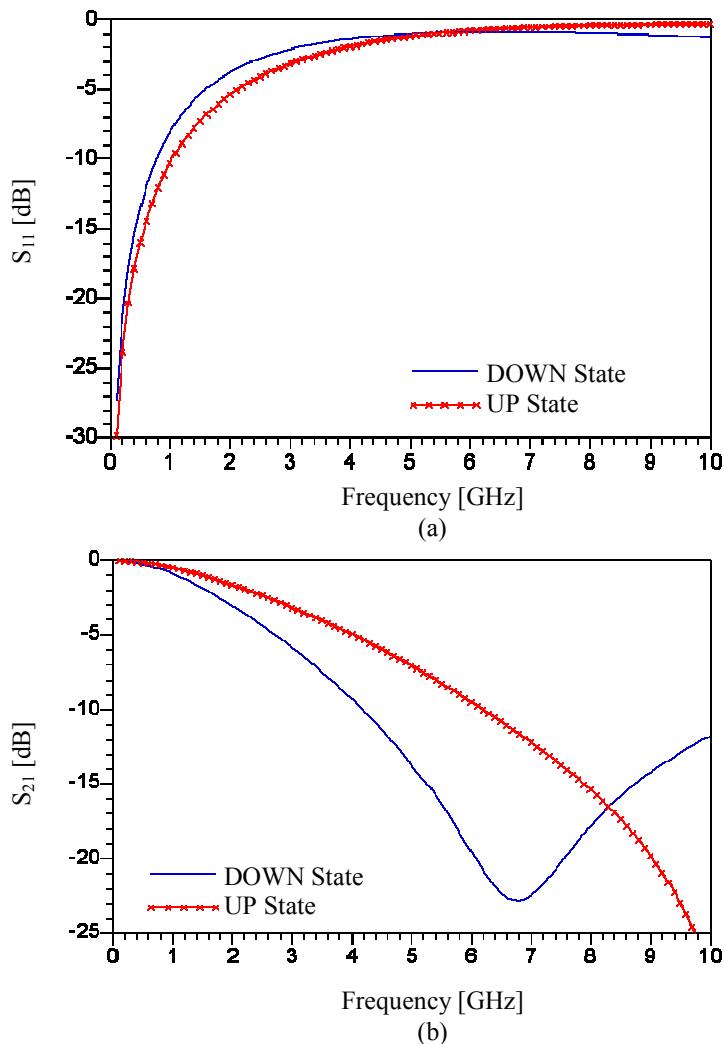


Figure 6.18: Simulated (a) S_{11} and (b) S_{21} of the rapid prototype switch de-embedded from the SMA connectors using Agilent ADS model from 0.1-10GHz.

6.3.2 Mechanical Response Measurement of the Rapid Prototype Switch

In order to measure the mechanical response of the armature during actuation, an actuation voltage has to be applied to the actuation electrodes. As mentioned in chapter 3, the surface interaction force between the dielectric layer and the armature could influence on the minimum actuation voltage of the proposed RF MEMS switch. The minimum actuation voltage can be calculated using equation 3.17.

The surface roughness in the contact region of the armature and the transmission line were examined using white light interferometer on a MSA-400 Micro System Analyser [161]. As the silicon wafer was mirror polished and the surface was protected by a layer of photoresist during processing, the roughness is expected to be dominated by the transmission line topography. The roughness of the transmission line topography is shown in Figure 6.19. The average roughness of contact surface on the PCB substrate is around 280nm.

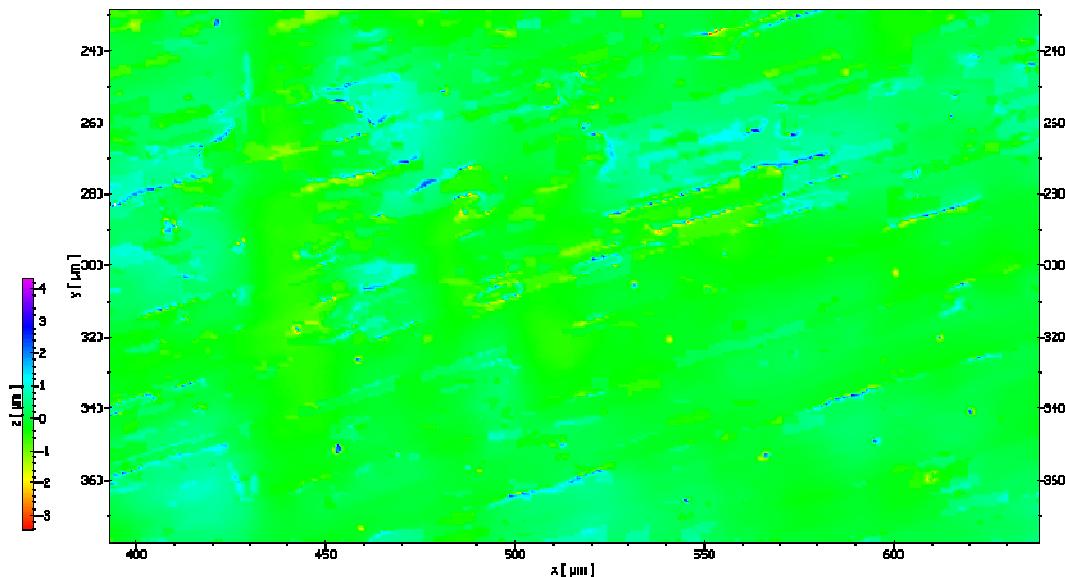


Figure 6.19: Measured surface roughness over a section of the transmission line where the armature is positioned using a MSA 400 Micro System Analyser.

Figure 6.20 shows that the computed minimum actuation voltages for the rapid prototype switch based on equation 3.17, for a range of surface roughness and contact areas with a gap height, g_o , of 40 μm . The minimum actuation voltage of the switch is approximately 92V regardless the contact area between the armature and transmission line.

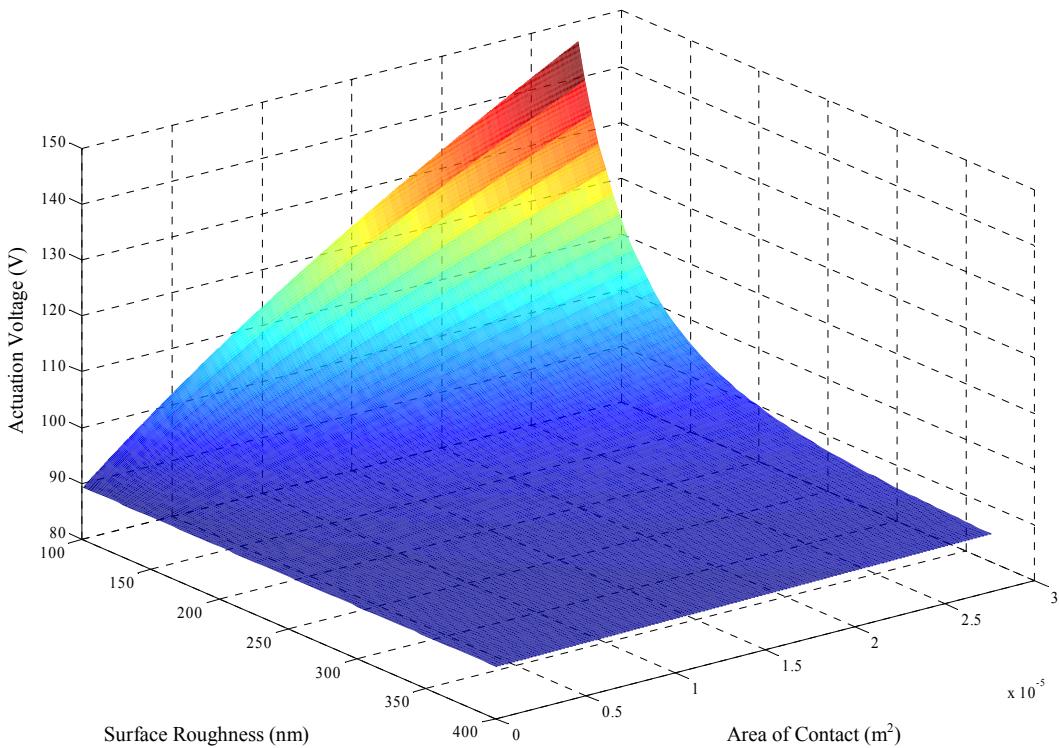


Figure 6.20: Calculated minimum actuation voltage considering the effects of surface roughness and contact area for a Tantalum Pentoxide–air–silicon material system for a gap height of $40\mu\text{m}$.

The mechanical response measurement setup of the rapid prototype switch is depicted in Figure 6.21. Using the time sweep mode [162], the network analyzer is set to measure losses between port 1 and port 2 of the device under test (DUT) at a fixed RF signal. The losses were measured with respect to time. The pulse signal of the function generator was used as the actuation control of the switch. The voltage amplifier magnified the signal from the function generator to actuate the armature of the rapid prototype switch. The amplified signal was applied to the top actuation electrodes. A pull up force is generated when the pulse is high, attracting the armature to the top electrode. During the low state of the pulse, the armature falls down due to the earth's gravity.

The difference between the setup in this measurement and the setup illustrated in Figure 6.15, is the voltage source used for supplying the actuation voltage. An Agilent 33220A 20MHz function/arbitrary waveform generator and an Elbatech T-100D voltage amplifier replaced the power supply used in the previous section, as the transient time for

generating a 100V square pulse is rather slow in the range of milliseconds. If the expected response time of the rapid prototype switch was in a similar range, the measurement of the network analyser would be affected. The transient time for a 100V pulse using a function generator and voltage amplifier is in the range of microseconds.

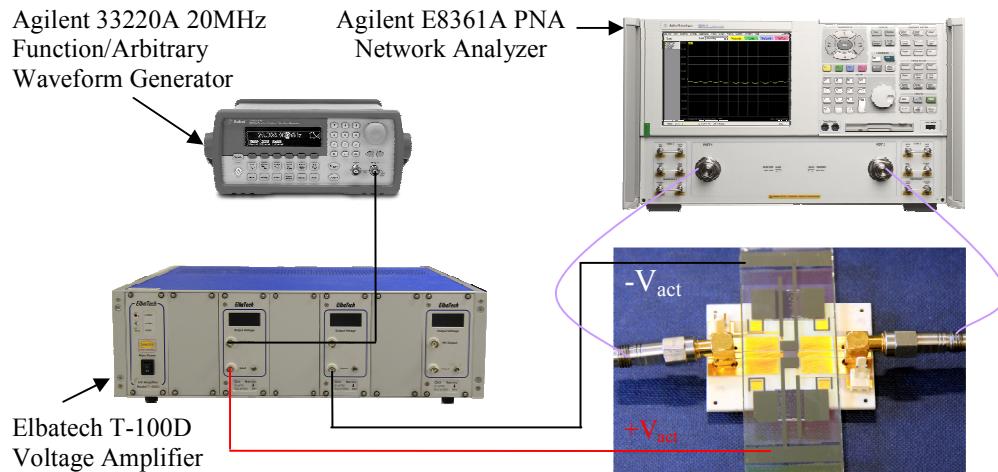


Figure 6.21: Measurement setup for rapid prototype device using an Agilent E8361A network analyzer, Agilent 33220A 20MHz function/arbitrary waveform generator and Elbatech T-100D voltage amplifier.

Figure 6.22 illustrates S_{21} is the signal of the rapid prototype switch when the armature was actuated with an actuation voltage in form of a 1Hz DC pulse of $\pm 93V$ applied at the top electrodes. The network analyzer was set to measure the losses at the frequency of 7.5GHz and the data was displayed versus time. When the actuation voltage was applied, the S_{21} changes from $\sim -26.5dB$ to $-38.5dB$. The time taken from DOWN state to UP state represented the rise time (T_{rise}) while that from UP state to DOWN state was the fall time (T_{fall}) of the switch actuation operation. The T_{rise} and T_{fall} are 165ms and 180ms respectively.

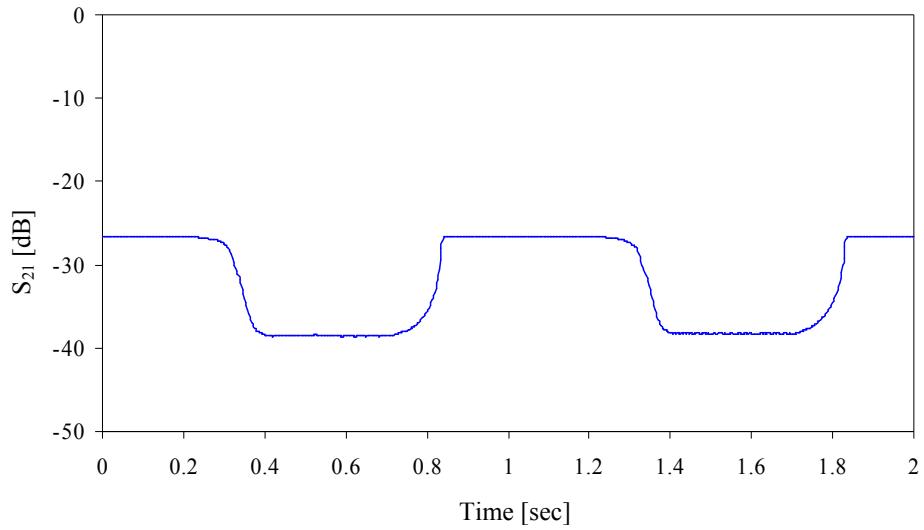


Figure 6.22: S_{21} signal of the rapid prototype switch using an actuation voltage of $\pm 93V$ at a RF frequency of 7.5GHz.

Figure 6.23 shows the measured and the simulated T_{rise} values of the rapid prototype switch for different actuation voltages ($\pm 97.5V$ to $\pm 142.5V$). The simulation model used in this case was based on the variable damping without perforated hole which is described in section 3.5.1. Although the measured T_{rise} was slower than the simulated value by a factor of 10, the trends for both simulated and measured data show T_{rise} decreases when actuation voltage increases. The minimum actuation voltage for the rapid prototype switch is 93V. The discrepancy in the two sets of data is attributed to the fact that current model cannot predict the damping dynamic of the actual armature movement accurately, as these published models [19, 98, 99, 163] for variable damping coefficient are generally derived from the linearised Reynolds Equation. The current damping coefficient model consists of an experimental factor in the displacement compensating equation, Q (as denoted in Equation 3.31). The choice of this factor has an effect on the response time of the simulated result [39].

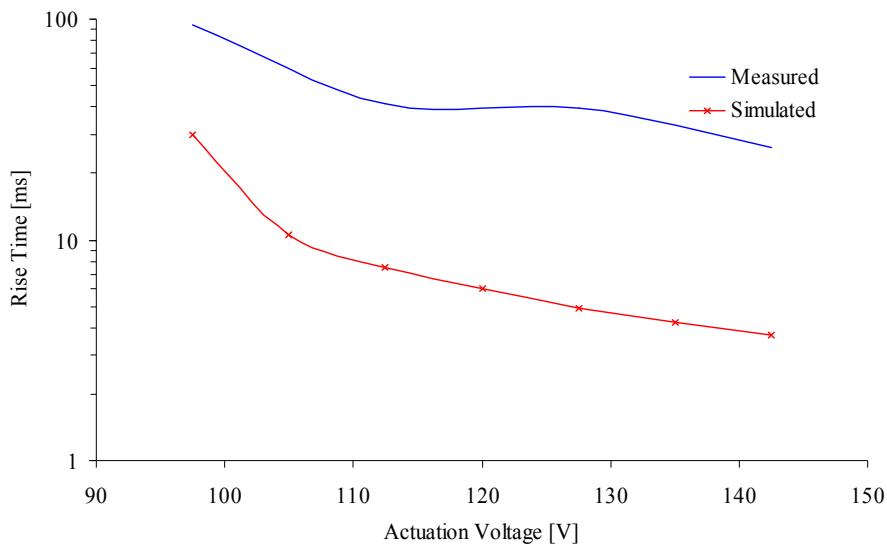


Figure 6.23 : Simulated and measured rise time of the rapid prototype device as a function of the actuation voltage.

6.4 Summary

This chapter has detailed the test setup and the initial S-Parameter measurements of the transmission line of the micron-scale RF MEMS switch. The measured return loss and insertion loss of the fabricated transmission line are more than -10dB for frequencies above 22GHz and more than -4dB for frequencies above 30GHz respectively. The probe pads of the design are observed to be interfering with actual RF characteristics of the design of the transmission line. The probe pads are removed to improve the characteristic.

As a working device is unavailable from the fabrication run, a $800\mu\text{m} \times 800\mu\text{m}$ low-resistivity silicon is used as the armature of the original design. The S-Parameter of the shunted transmission line is measured and the DOWN state S_{21} is approximately -13dB at a frequency of 67GHz. Although the armature was not in proper contact with the transmission line, there was significant shunting of the RF signal through the armature. This work has proven that a low-resistivity silicon is able to fulfil the role of shunting an RF signal even though its conductivity is 2 orders of magnitude lower than the conventional material. The actual micron-scale prototype could work if the fabrication was successful.

Both measured and simulated RF characteristics of the transmission line and the rapid prototype switch are presented. The effect of the SMA connector was verified using the Agilent ADS model and the simulated RF characteristic of the switch is detailed. The rapid prototype switch has a very high insertion loss of <-2 dB for frequencies above 2GHz. The DOWN state resonant frequency of the rapid prototype is at 7GHz with an isolation of -23dB.

The mechanical response of the rapid prototype switch was also examined. The effects of the surface adhesion forces acting on the armature of the switch are discussed in relation to the overall contact area and the roughness of the contact area surface. The computed minimum actuation voltage was approximately ± 92 V for a set range of the surface roughness and contact area. The experimental minimum actuation voltage was ± 93 V. The dynamic response of the switch was also characterised and compared with simulated results of the Simulink model presented in Chapter 3. The measured results were 10 times slower than the simulated ones. The difference is attributed to the experimental value used in the modelling equation.

Chapter 7

Conclusion and Future Works

This thesis reports on a selection of the state of the art RF MEMS switches, with the main focus on the development of electrostatically actuated and high K-dielectric switches. A number of RF MEMS switches based on other actuation mechanisms, as well as designs for high RF power applications are also detailed. Through the review, there is a strong drive towards development of RF MEMS switches with low actuation voltage, which is suitable for the integration with existing CMOS circuits. In this work, a new approach is developed to realise a RF MEMS switch with an unrestrained armature which has a potential of operating at a low actuation voltage.

The main goals of having the proposed switch to operate at less than 3.5V and with an isolation of better than -40dB is met, with the 75Ω design achieving an actuation voltage of 3.4V and isolation of -46dB at 77Ghz. The higher than expected insertion loss is attributed the substrate material used for the transmission line. The slower than expected switching time is due to the damping force acting on the armature during operation.

The basic electrostatic theory of actuating a mechanically unrestrained armature was explored. It was proven by FEM simulation that electrostatic actuation for conducting armature in a single top and bottom electrode configuration will not work. However, by employing a pair of top and bottom electrodes and applying a voltage of opposite polarity on the two electrodes, it yielded an attractive electrostatic force which pulled the armature towards the energised electrode. This proved the feasibility of

implementing an electrostatic actuation mechanism for a RF MEMS switch with a mechanically unrestrained armature.

The criteria as well as the fabrication limitations are established for designing the proposed MEMS switch. The dimensions in the form of armature length, width and initial gap of the proposed MEMS switch were set to be explored within the criteria and the formulation of the minimum actuation voltage was derived. Based on the relationship between the minimum actuation voltage, the length of the armature and the initial capacitive gap, an armature length of $680\mu\text{m}$ was selected for the design. The initial gap was undetermined as the actuation voltage increased linearly with the gap. The width and the initial capacitive gap were further explored based on the switching time for the MEMS switch. The switching time was simulated by various width dimensions and a positive linear relationship was observed between the width of the armature and the switching time. Furthermore, by analysing various initial capacitive heights, the switching time decreased with the increased of initial gap, whereas a positive linear relationship appeared between the minimum actuation voltage and the initial gap. As a compromise for the two parameters, the armature width was set as $80\mu\text{m}$ and the initial gap was determined to be $5\mu\text{m}$. The surface interaction forces between the silicon armature and dielectric layer, affecting the minimum actuation voltage have been explored.

A Simulink® system level model is created to predict the mechanical response of the spring less RF MEMS switch and the results shows that the perforated armature switch is the fastest. Through the simulations, the air spring constant of the spring-less switch is also determined. Although the constant damping model was not sufficient to model the mechanical response of the armature over a large displacement, it can be used to demonstrate the best scenario when switching.

The electromagnetic model of the proposed RF MEMS switch is introduced with a lumped RLC model. The four main components of the model are the impedance from the transmission line, resistance, inductance and switching capacitance from the armature. The effects of the individual RLC component on the S-Parameters were explored using the Agilent Advanced Design System electronic design automation software as well as from an analytical approximation approach. The S-Parameters of the designed RF MEMS

switch is also discussed. This work shows that the RF characteristics and electrical resonant frequency of a RF MEMS switch can be tuned according to different armature materials and designs.

A fabrication flow for the micron-scale prototype, employing two Pyrex wafers which is sandwiching a SOI wafer, is introduced. The Pyrex wafers were initially etched to define the capacitive gap of the switch. Metallisation in the form of a chromium and gold stack was deposited and etched to form the transmission line and actuation electrodes. A layer of dielectric was then deposited to form the capacitive nature of the RF MEMS switch. Metal bond pads as well as sacrificial layer in the form of silicon dioxide were deposited and defined on the SOI wafer. Some parts of the fabrication process were carried out with the assistance of Nanoshift Inc, USA, when the facilities were not available due to a fire which destroyed the University's cleanroom. The end results were later converted and introduced when the University's cleanroom was operational. Although no working device was achieved at the end of the fabrication flow, improvements were made as compared to the previous work. The cleanroom fabrication has been discussed with the challenging issues encountered during the fabrication. A scaled up version of the proposed switch fabricated using the rapid prototype concept is also introduced. The main materials used in the process are relatively cheap and require less clean room equipment as compared to the micron-scale prototype. The turnover time is also comparatively shorter. The rapid prototype switch has produced both RF and mechanical measurement results.

Although no working micron-scale prototype is achieved, RF characterisation of the CPW fabricated on the Pyrex wafer is conducted. A silicon armature, which measures $800\mu\text{m}$ by $800\mu\text{m}$ by $500\mu\text{m}$, was placed across the CPW to mimic the different actuation states of the switch by manual manipulation. The measured RF characteristic of the coplanar waveguide showed a large amount of reflection loss at frequencies above 50GHz due to the tapered interface between the probe pads and the coplanar waveguide being too steep. With the removal of the probe pad and its tapered interface, the measured results are close to the simulated results. The DOWN state of the proposed switch was simulated by placing the armature across the coplanar waveguide. The measured results show improper contact between the two interfaces.

The measured results of rapid prototype switch demonstrate that RF shunting is feasible when low resistivity silicon is used as the armature material. The measured switching time of the rapid prototype device is slower than the simulated time in the same order of magnitude. The actual minimum actuation voltage is within 5% of predicted results.

The proposed rapid prototype methodology has proven the concept of this research work.

7.1 Future Work

This section provides some ideas and thoughts to improve the subject of implementing a RF MEMS switch with an unrestrained armature. These ideas can be split into two aspects, i.e. design and modelling as well as fabrication.

7.1.1 Design and Modelling

The current probe pad design as discussed in chapter 6 is too wide and suffers from high reflection loss at frequencies above 50GHz. To facilitate measurement within the University's facility, the probe pad dimensions should be made similar to that of the transmission line.

To improve the accessibility of the probe pads [164], it is recommended to move them to the outer surface of the bottom substrate. This will allow the device to be easily integrated onto other circuitry.

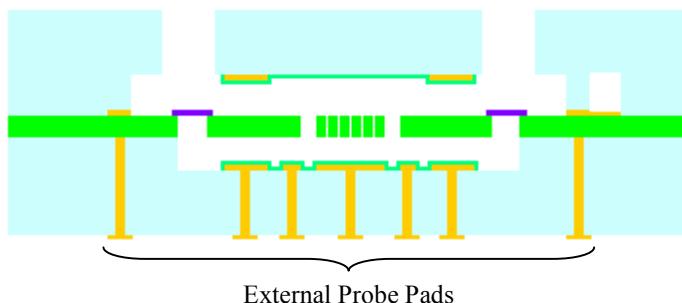


Figure 7.1: Cross section illustration of the proposed switch with probe pads located on the exterior of the substrate.

As mentioned in chapter 4, the RF characteristic of the MEMS switch can be tuned. For a mid term goal or second generation spring-less switch, the armature of the switch can be redesigned by incorporating more inductance or capacitance in order to make the resonant frequency of the switch lower. This will allow the proposed design to be applicable to telecommunication or test equipment.

In the aspect of modelling, the damping equations of the system level model have been based on linearised Reynolds equation [19, 96, 101]. These equations demonstrate the simulation result within reasonable limits for fixed-fixed structures. However, the proposed MEMS switch design is a free-free structure, the accuracy for the measured simulated results is within an order of magnitude. The model could be more accurate if a damping model based on this situation was derived.

The surface adhesion force model is based on the works reported in [92, 93]. The measured minimum actuation voltage is within 5% of the simulated results. However, the effects of such forces are not mentioned in similar designs reported in [58, 59]. The result needs to be verified further using atomic force microscopy technology mentioned in [165, 166]. This will provide a better understanding on the effects of the adhesion forces on the actuation voltage of the proposed MEMS switch.

7.1.2 Fabrication

The root cause for the failure identified in Chapter 5 is related to the thickness of the UV glue. According to works reported in [147-149], the application of UV glue can be properly defined using a stamping method. The UV glue is initially spun on a carrier wafer. The bottom wafer is ‘stamped’ onto the adhesive carrying wafer, to transfer the UV glue across the top surface of wafer. The bottom wafer is then aligned and bonded to the Pyrex/Silicon wafer stack.

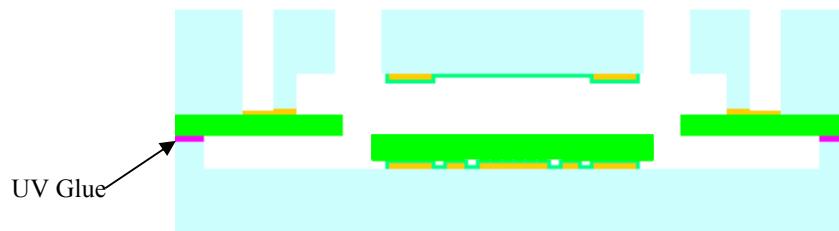


Figure 7.2: Cross section illustration of the proposed switch with well defined UV glue interface.

Appendix A: Simulink Model

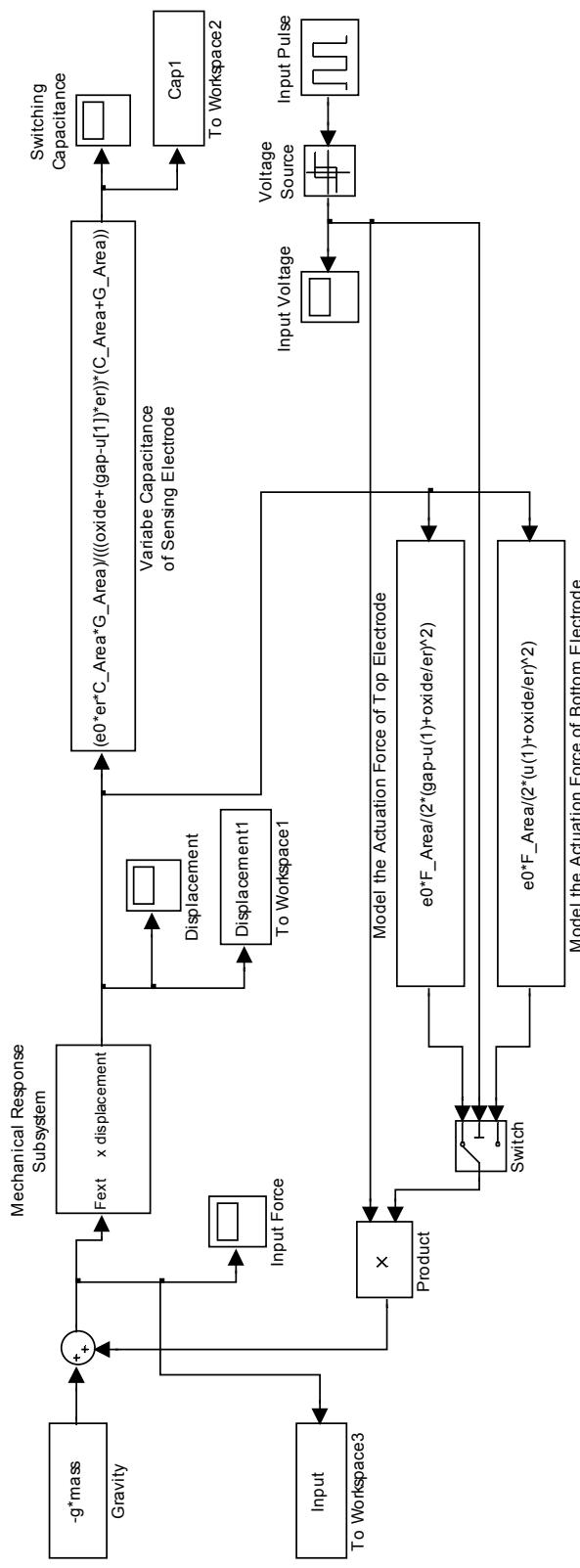


Figure A-1: System level model of proposed RF MEMS switch which was created in Matlab/Simulink.

Appendix B: Fabrication Process

Flow for Micron-Scale Prototype

STEP	PROCESS	DESCRIPTION	REMARKS
1	Materials	<p>Sensor Prep Services, Inc. 7740 Pyrex Wafers, 150mm\pm0.5, DSP, Thickness 0.50mm\pm0.025mm, Surface Finish: SI 15–20 Å</p> <p>Ultrasil Corporation SOI Wafers, 150\pm.2 diameter, $<100>\pm 0.5^\circ$, Double Sides Polished (DSP) Device Layer N-type, 0.001 – 0.0015Ω cm, Thickness 50μm\pm0.5μm BOX Layer Thickness 2μm\pm5% Device Layer P-type, 1-20Ω cm, Thickness 500μm\pm5μm</p>	
PYREX WAFERS			
2	Wafer clean	Fuming Nitric Acid: 15min	
3	Evaporate	Cr/Au: 200Å /1500Å	
4	Photolithography Mask 1: TE and BE (front side)	<p>Dehydration: 15min @140°C in an oven</p> <p>TI Prime : 30sec @4krpm</p> <p>Bake the substrate: 2mins@120°C on a hotplate</p> <p>S1813: spread 5sec @500rpm, spin 30sec @4krpm</p> <p>Soft bake: 60sec @120°C on a hotplate</p> <p>Expose: EVG620 20mW/cm² 6sec</p> <p>Hard contact</p> <p>Hard bake : 2min @120°C on a hotplate</p> <p>Develop: MIF 319 60sec+10sec</p>	<p>TE: for top glass wafers BE: for bottom glass wafers Measure the thickness of S1813</p>

5	Wet etch Cr/Au	Etch Au: Rockwood Gold etchant 1min or 'til clear Etch Cr: Rockwood Chrome etchant 10sec or 'til clear	Measure the thickness of Cr/Au layer
6	Etch glass 3µm	Rockwell 7:1 BHF with surfactant Inspect etch depth using step profilometer	
7	Strip photoresist (PR)	Fuming Nitric Acid: 15min	
8	Wet etch Cr/Au	Etch Au: KI-based etchant 1min or 'til clear Etch Cr: CR-14 etchant 15sec or 'til clear	Measure the thickness of Cr/Au layer
9	Wafer clean	Fuming Nitric Acid: 15min	
10	Evaporate	Cr/Au: 200A°/5000A°	
11	Photolithography Mask 2: TC and BC (front side)	Dehydration: 15min @140°C in an oven TI Prime : 30sec @4krpm Bake the substrate: 2mins@120°C on a hotplate S1813: spread 4sec @500rpm, spin 30sec @4krpm Soft bake: 60sec @120°C on a hotplate Expose: EVG620 20mW/cm ² 4.5sec Hard contact Develop: MIF 319 60sec+10sec Hard bake : 2min @120°C on a hotplate	FB: for bottom glass wafers FT: for top glass wafers Measure the thickness of S1813
12	Wet etch Cr/Au	Etch Au: KI-based etchant 1min or 'til clear Etch Cr: CR-14 etchant 15sec or 'til clear SRD	Measure the thickness of Cr/Au layer
13	Strip photoresist (PR)	Fuming Nitric Acid: 15min	
14	Wafer clean	Fuming Nitric Acid: 15min	
15	Dielectric deposition	RF Sputtering Ta ₂ O ₅ Recipe : Platen temperature : 200°C Chamber pressure : 1×10 ⁻⁴ Torr Magnetron Power : 300W Gas: Argon @ 20sccm Oxygen @ 5sccm Rate: 0.17nm/min	

16	Photolithography Mask 3: CL (front side)	TI Prime : 30sec @4krpm Bake the substrate: 2mins@120°C on a hotplate S1813: spread 4sec @500rpm, spin 30sec @4krpm Soft bake: 60sec @120°C on a hotplate Expose: EVG620 20mW/cm ² 4.5sec Hard contact Develop: MIF 319 60sec+10sec SRD Hard bake : 2min @120°C on a hotplate	Mask design Compatible for both top and bottom wafer Measure the thickness of S1813
17	Etch Ta ₂ O ₅	RIE Ta ₂ O ₅ Platen temperature : 40°C Chamber pressure : 30mTorr Magnetron Power : 400W Gas: Argon @ 25sccm CHF ₃ @ 25sccm SF ₆ @ 25sccm	
18	Strip photoresist (PR)	Fuming Nitric Acid: 15min	
SOI Wafer			
19	Wafer clean	Fuming Nitric Acid: 15min	
20	Evaporate	SiO: 2um	
21	Photolithography Mask 4: OL (front side)	Dehydration: 15min @140°C in an oven Vapour HMDS or HMDS: 30sec @4krpm S1813: spread 4sec @500rpm, spin 30sec @4krpm Soft bake: 60sec @115°C on a hotplate Expose: EVG520 20mW/cm ² 4.5sec Hard contact Develop: MIF 319 50sec+10sec Hard bake : 15min @115°C in an oven	Measure the thickness of S1813
22	Etch SiO	Transene 7:1 BOE with surfactant Inspect etch depth using step profilometer	Measure the thickness of Sacrificial layer
23	Strip photoresist (PR)	Fuming Nitric Acid: 15min	
24	Wafer clean	Fuming Nitric Acid: 15min	
25	Evaporate	Cr/Au: 200 Å /5000 Å	

26	Photolithography Mask 5: EP (front side)	<p>Dehydration: 15min @140°C in an oven</p> <p>Vapour HMDS or HMDS: 30sec @4krpm</p> <p>S1813: spread 4sec @500rpm, spin 30sec @4krpm</p> <p>Soft bake: 60sec @115°C on a hotplate</p> <p>Expose: MA6 20mW/cm² 4.5sec</p> <p>Hard contact</p> <p>Develop: MIF 319 60sec+10sec</p> <p>Hard bake : 15min @115°C in an oven</p>	Measure the thickness of S1813
27	Wet etch Cr/Au	<p>Etch Au: Rockwood Gold etchant 1min or 'til clear</p> <p>Etch Cr: Rockwood Chrome etchant 10sec or 'til clear</p>	Measure the thickness of Cr/Au layer
28	Strip photoresist (PR)	Fuming Nitric Acid: 15min	
29	Wafer clean	Fuming Nitric Acid: 15min	
Top Pyrex + SOI Wafer			
30	Wafer clean	Fuming Nitric Acid: 15min	Both Top Pyrex Wafer and SOI Wafer
31	Anodic bonding	<p>Recipe :</p> <p>Top/Bottom temperature : 355°C</p> <p>Chamber pressure : 1×10^{-6} Torr</p> <p>Contact force : ~400 N</p> <p>Voltage: 15min @ -800V</p> <p>Cool down: 100°C</p>	EVG 520
32	Solvent clean	Acetone + IPA + DI Rinse	
33	Attach a Carrier wafer	<p>Attached Wafer stack to Carrier Wafer:</p> <p>Place Carrier Wafer on 70oC Hotplate</p> <p>Apply a thin layer of Crystal Bond Wax to Carrier Wafer</p> <p>Place Pyrex Side of Wafer stack on the wax</p> <p>Remove heat and wait for wafer stack to cool down</p>	
34	Etch Silicon	<p>STS Recipe:</p> <p>Target depth: 500μm</p> <p>Recipe :</p> <p>Etch Passivation</p> <p>SF6 130 sccm -</p> <p>O2 13 sccm -</p> <p>Coil Power 2000 W -</p> <p>Platen Power 60 W -</p> <p>Time 12 sec -</p>	Remove Handling Wafer

35	Remove a Carrier wafer	Place Wafer stack on 70°C Hotplate Slide Wafer stack off Carrier wafer Remove heat and wait for wafer stack to cool down Wipe clean Pyrex Surface with methanol + clean room wipe	
36	Etch SiO	Rockwood 7:1 BOE with surfactant	
37	Photolithography Mask 6: AM (Back side)	Dehydration: 15min @200°C in an oven AZ9260: spread 4sec @500rpm, spin 30sec @4krpm Soft bake: 60sec @115°C on a hotplate Expose: EVG620 20mW/cm ² 16sec Hard contact Develop: AK400Z:DI 3:1 90sec	Measure the thickness of AZ9260
38	Attach a Carrier wafer	Attached Wafer stack to Carrier Wafer: Place Carrier Wafer on 70°C Hotplate Apply a thin layer of Crystal Bond Wax to Carrier Wafer Place Pyrex Side of Wafer stack on the wax Remove heat and wait for wafer stack to cool down	
39	DRIE (ST TM)	Target depth: Thru wafer 50µm Recipe : Etch Passivation C4F8 - 85 sccm SF6 130 sccm - O2 13 sccm - Coil Power 2000 W 600 W Platen Power 60 W - Time 3 sec 3 sec	
40	Remove a handle wafer	Place Wafer stack on 70°C Hotplate Slide Wafer stack off Carrier wafer Remove heat and wait for wafer stack to cool down Wipe clean Pyrex Surface with methanol + clean room wipe	
41	Strip photoresist (PR)	O2 Ashing RIE 80+	
PYREX/SILICON + Bottom PYREX			
42	Wafer clean	Fuming Nitric Acid: 15min	Bottom Pyrex Wafer
43	UV Glue Bonding	Expose: EVG620 20mW/cm ² 60sec	Optical Inspection

		Flood Expose	
44	Grooving	Loadpoint Microace Series 3 Dicing Saw 600micron disc blade for 450um depth 25KRPM @ 3m feeding rate	
45	Photolithography Mask 6: PB (Back side)	Dehydration: 15min @140°C in an oven Vapour HMDS or HMDS: 30sec @4krpm AZ9260: spread 4sec @500rpm, spin 30sec @4krpm Soft bake: 60sec @115°C on a hotplate Expose: EVG620 20mW/cm ² 16sec Hard contact Develop: AK400Z:DI 3:1 90sec	Measure the thickness of AZ9260
46	Etch SiO	RIE SiO ₂	
47	Strip photoresist (PR)	O ₂ Ashing RIE 80+	
48	Sacrificial Etch	HF Vapour phase etch	
49	Dicing	Mitsuboshi Diamond MS300A-CE	

Appendix C: Fabrication Process

Flow for Rapid Prototype Device

STEP	PROCESS	DESCRIPTION	REMARKS
1	Materials	Agar Scientific PLAIN SLIDES 0.8mm - 1.0mm THICK Printed Wiring Technologies Rogers 4003 TM PCB, 1.52mm thick Copper Foil Cladding: 35um. Si-Mat High Conductive Silicon Wafers, 150mm±0.5, DSP, Thickness 0.50mm±0.025mm, Surface Finish: SI 15–20Å	
GLASS SLIDE			
2	Solvent clean	Acetone + IPA + DI Rinse	
3	Evaporate	Cr/Au: 10nm/200nm	
4	Photolithography Mask 1: GE acetate mask	Ordyl AM 130: laminate @ 110°C, with a speed of 0.15 m/min Expose: Mega Electronics lightbox 20 seconds, vacuum contact Develop: 40s in 0.8% sodium carbonate solution + ultrasonic bath	
5	Wet etch Cr/Au	Etch Au: Rockwood Gold etchant 1min or 'til clear Etch Cr: Rockwood Chrome etchant 10sec or 'til clear	Measure the thickness of Cr/Au layer
6	Strip photoresist (PR)	Acetone + IPA + DI Rinse	
7	Substrate clean	Fuming Nitric Acid: 15min	
8	Dielectric deposition	RF Sputtering Ta ₂ O ₅ Recipe : Platen temperature : 200°C Chamber pressure : 1×10 ⁻⁴ Torr Magnetron Power : 300W Gas: Argon @ 20sccm Oxygen @ 5sccm Rate: 0.17nm/min	

9	Photolithography Mask 2: CL acetate mask	Ordyl AM 130: laminate @ 110°C, with a speed of 0.15 m/min Expose: Mega Electronics lightbox 20 seconds, vacuum contact Develop: 40s in 0.8% sodium carbonate solution + ultrasonic bath	
10	Etch Ta ₂ O ₅	RIE Ta ₂ O ₅ Rate: 0.17nm/min	Measure the thickness of Cr/Au layer
11	Strip photoresist (PR)	Acetone + IPA + DI Rinse	
12	Substrate clean	Fuming Nitric Acid: 15min	
PCB			
14	Apply photoresist	Manually brush a layer of PR at bond pad areas	
15	Dielectric deposition	RF Sputtering Ta ₂ O ₅ Recipe : Platen temperature : 200°C Chamber pressure : 1×10 ⁻⁴ Torr Magnetron Power : 300W Gas: Argon @ 20sccm Oxygen @ 5sccm Rate: 0.17nm/min	
16	Strip photoresist (PR)	Acetone + IPA + DI Rinse	
SILICON WAFER			
17	Wafer clean	Fuming Nitric Acid: 15min	Both Top Pyrex Wafer and SOI Wafer
18	Photolithography	Dehydration: 15min @200°C in an oven AZ9260: spread 4sec @500rpm, spin 30sec @4krpm Soft bake: 60sec @115°C on a hotplate Expose: EVG520 20mW/cm ² 16sec Hard contact Develop: AK400Z:DI 3:1 90sec	Measure the thickness of AZ9260
19	Attach a Carrier wafer	Attached Wafer stack to Carrier Wafer: Place Carrier Wafer on 70°C Hotplate Apply a thin layer of Crystal Bond Wax to Carrier Wafer Place Silicon wafer on the wax Remove heat and wait for wafer stack to cool down	

20	DRIE (STSTM)	<p>Target depth: Thru wafer 525µm</p> <p>Recipe :</p> <p>Etch Passivation</p> <p>C4F8 - 85 sccm</p> <p>SF6 130 sccm -</p> <p>O2 13 sccm -</p> <p>Coil Power 2000 W 600 W</p> <p>Platen Power 60 W -</p> <p>Time 3 sec 3 sec</p>	
21	Remove a handle wafer	<p>Place Wafer stack on 70°C Hotplate</p> <p>Slide Wafer off Carrier wafer</p> <p>Remove heat and wait for wafer stack</p> <p>Pick and clean armature and spacer</p>	
22	Solvent clean	Acetone + IPA + DI Rinse	
BONDING			
23	Apply adhesive to spacer	Ordyl SY320: laminate @ 110°C, with a speed of 0.15 m/min	
24	Bonding	<p>Bond Spacer to glass slide</p> <p>Optically align spacer to glass slide</p> <p>Clamped between 2 other glass slides via bulldog clips</p> <p>150°C for 4hours with ramp rate 5°C/min</p>	
25	Apply adhesive to PCB	Manually brush a layer of sliver paint to the bonding surface of the PCB	
26	Bonding	<p>Manually place the armature across the CPW</p> <p>Optically align glass slide to PCB using alignment marks</p> <p>Apply force to bond the two substrate</p>	

Appendix D: L-EDIT Layout of the Micron-Scale Prototype

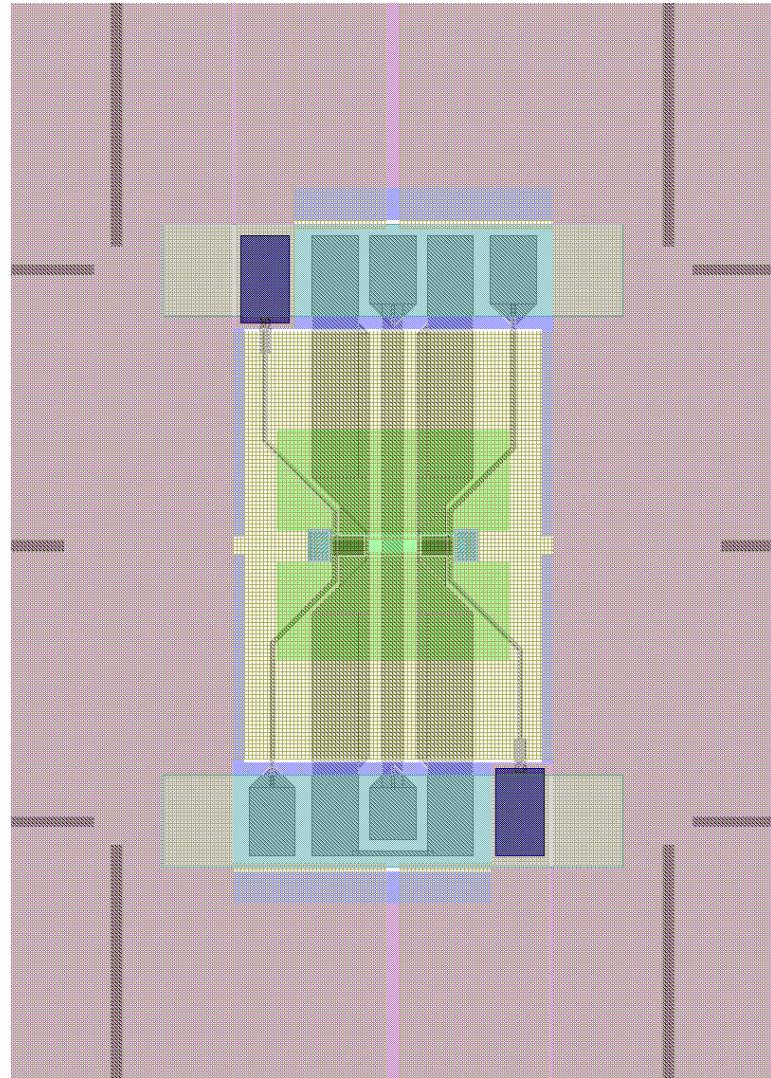


Figure A-2: L-Edit layout of the proposed RF MEMS switch.

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