University of Southampton
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Low Cost Si Nanowire Biosensors by Recrystallisation Technologies

by

Kai Sun

A thesis submitted for the degree of
Doctor of Philosophy

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Supervisor: *Professor Peter Ashburn*

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF PHYSICAL AND APPLIED SCIENCE
SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

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Recently, silicon nanowires are gaining much attention for applications in biosensing for medical diagnosis, drug discovery and national security. Silicon nanowires offer the prospect of real-time, label-free, high selectivity and high sensitivity sensing. Currently silicon nanowires are generally fabricated using CMOS technology and require the use of expensive SOI substrates and electron beam lithography, which seriously limit their uses in low cost applications. In this work, polysilicon nanowire biosensors are fabricated using thin film transistor technology. This approach offers the prospect of much lower fabrication costs and hence is suitable for products such as disposable diagnostic kits. The polysilicon nanowires are fabricated by crystallising amorphous silicon and techniques are investigated for producing polysilicon at temperatures below 450°C for compatibility with cheap glass substrates.

Metal-induced lateral crystallisation is achieved for the first time at temperatures down to 428°C and a crystallisation length of 1.2 μm is measured after a MILC anneal at 428°C for 20 hours. The effect of fluorine on metal-induced lateral crystallisation is investigated at different temperatures. At temperatures in the range 525°C to 550°C, an optimum fluorine implantation dose of 2.5×10^{15} cm^{-2} is found at which significantly increased crystallisation lengths are achieved. Raman spectroscopy is used to analyse the Si film crystallinity and the results show that fluorine suppresses random crystallisation up to a dose of 2.5×10^{15} cm^{-2}, but that damage from the fluorine implant (amorphisation) counteracts this effect at a higher dose. At temperatures below 500°C, a fluorine implant reduces the crystallisation length and hence no benefit is obtained from the fluorine implant.

Then metal-induced lateral crystallisation of amorphous silicon (α-Si) ribbons and nanowires is also investigated. The crystallisation decreases with decreasing ribbon width and the crystallisation lengths for nanowires lie below the trend line for ribbons. Metal

induced lateral crystallisation is therefore more difficult in nanowires than ribbons, which is tentatively explained by surface roughness. The metal-induced lateral crystallisation of α-Si ribbons deposited by PECVD and LPCVD on different substrate materials is also investigated. The crystallinity of the as deposited α-Si is shown to have a big effect on the crystallisation length. LPCVD α-Si ribbons on oxide give significantly longer lateral crystallisation lengths than PECVD α-Si ribbons on oxide and slightly longer lateral crystallisation lengths than LPCVD α-Si ribbons on nitride. Raman spectroscopy reveals that amorphous silicon deposited by PECVD is more amorphous than by LPCVD, because of the lower deposition temperature.

A top-down nanowire fabrication process has been developed using a Bosch etch process, which is shown to provide rectangular nanowires with a well-controlled width of about 100 nm. Electrical measurements show that the resistance can be varied by the application of a back-gate bias. The fabricated nanowires have reproducible characteristics in about 10% variation in resistance at the central part of the wafer. Nanowires with and without a thermal oxide layer are studied and oxidised nanowires give less conductance variation and less dependence on back-gate bias. Polysilicon nanowire biosensors have been successfully fabricated using this technology and experiments in liquid show that the nanowire biosensor can be used to detect changes in pH.

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Declaration of Authorship

I, Kai Sun, declare that the thesis entitled:

”Low Cost Si Nanowire Biosensors by Recrystallisation Technologies”

and the work presented in it are my own. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
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- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
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- parts of this work have been published in research journals. A list of publications is provided with this manuscript.

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List of Publications

Conference Presentations

Metal-induced Lateral Crystallization of Amorphous Silicon Nanoribbons for Application in Biosensors

K. Sun, M. M. A. Hakim, P. Ashburn, E-MRS09, Strasbourg, France (Jun 2009).

Fluorine Dose Effect on the Nickel-induced Lateral Crystallisation of Amorphous Silicon

K. Sun, M. M. A. Hakim, P. Ashburn, The 39th European Solid-State Device Research Conference (ESSDERC 2009), Athens, Greece (Sep 2009).

Recrystallised Si Nanofingers and Nanowires for Low Cost Biosensor Applications

K. Sun, M. M. A. Hakim, J. Kong, M. R. R. d. Planque, H. Morgan, P. L. Roach, D. E. Davis, P. Howarth, P. Ashburn, Symposium on Atom-scale Si Hybrid Nanotechnologies, Southampton, UK (Mar 2010).

Low Cost Nanowire Biosensor Fabrication using Thin Film Amorphous Silicon Crystallisation Technologies

K. Sun, M. M. A. Hakim, J. Kong, M. R. R. d. Planque, H. Morgan, P. L. Roach, D. E. Davis, P. Howarth, P. Ashburn, Infectious Disease Research Network, Leceister, UK (May 2010).

Low Cost Nanowires Defined by Spacer Etch using Bosch Process for Biosensor Applications

K. Sun, M. M. A. Hakim, J. Kong, M. R. R. d. Planque, H. Morgan, P. L. Roach, D. E. Davis, P. Howarth, P. Ashburn, International Conference on Micro and Nano Engineering, Genoa, Italy (Sep 2010).

Sensors Chemical Detection Based on Top-down Fabrication Nanowires

K. Sun, M. M. A. Hakim, M. Lombardini, M. R. R. d. Planque, H. Morgan, P. L. Roach, D. E. Davis, P. Howarth, P. Ashburn, NanoBioTech, Montreux, Switzerland (Nov 2010).

High Quality Location Controlled Polycrystalline Silicon Nanowires for Bio-sensors using Low Cost Process

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Journal

Rectangular Polycrystalline Silicon Nanowires by Dry Etching for Biosensor Applications

M. M. A. Hakim, K. Sun, M. R. R. d. Planque, H. Morgan, P. L. Roach, D. E. Davis, P. Howarth, P. Ashburn, Nano Letter (in preparation).

List of Symbols

A_0	Lateral crystallisation growth coefficient
C_{IT}	Effective net interface charge
C_{ox}	Gate oxide capacitance
C_d	Depletion capacitance
E_a	Activation energy for lateral crystallisation
E_C	Conduction band energy
E_F	Fermi level
E_{Fn}	Electron quasi-Fermi level
E_{Fp}	Hole quasi-Fermi level
E_g	Energy band gap
E_i	Intrinsic Fermi level
E_v	Valence band energy
h	Plank constant
I_a	Area of Raman contribution of amorphous silicon
I_{ds}	Drain current
$I_{ds,sat}$	Drain current in the saturation mode
I_p	Area of Raman contribution of polysilicon
J_n	Electron current density
k	Boltzmann constant
L_g	Grain length
m	Body-effect coefficient
n_i	Intrinsic carrier density
N	Dopant concentration
N_A	p-type dopant concentration
N_D	n-type dopant concentration
N_t	Trapping state density
N_T	Effective trap state density per unit area per eV
q	Charge on an electron
Q_d	Depletion charge
Q_f	Fixed oxide charge
Q_m	Mobile ionic charge
Q_{ot}	Oxide trapped charge
Q_i	Inversion charge
Q_{it}	Interface trapped charge
Q_{IT}	Effective net interface charge

Q_s	Surface charge
R_{ch}	Nanowire channel resistance
R_{ds}	Source/Drain and contact resistance
R_{total}	Total measured resistance of nanowire transistor
SS	Sub-threshold slope
T	Temperature
t_{Si}	Silicon channel thickness
t_{ox}	Gate oxide thickness
V	Bias along the channel due to drain bias
V_b	Barrier height
V_{bg}	Back-gate bias
V_{ds}	Drain bias referred to Source
V_{fb}	Flat band voltage
V_g	Gate bias
V_t	Threshold voltage
v	Emitted light frequency
v_0	Incident light frequency
W_d	Depletion layer width
W_i	Inversion layer width
β	The term of $C_{ox}\mu_{eff}\,(W/L)$
χ	Crystalline fraction
ϵ_{Si}	Silicon permittivity
ϵ_{ox}	Silicon dioxide permittivity
ψ_b	The difference between the E_F and E_i in bulk silicon
ψ_m	Gate work function
ψ_s	Surface potential
ψ_{Si}	Si channel work function
λ_d	Debye length
μ_n	Electron mobility
$\mu_{n,eff}$	Effective electron mobility
$\mu_{ps,n,eff}$	Effective electron mobility in polysilicon film

Chapter 1

Introduction

The detection of a small amount of ions, molecules, proteins, antigens and DNA is of great importance for clinical diagnosis, drug discovery and screening and for applications in security and defence against terrorism [1]. The critical part of the detection, referred as a biosensor, is the transduction of signals associated with the recognition of the species of interest. Many approaches have been researched for biosensors, including surface plasmon resonance [2], nanoparticles [3] and chemically sensitive field effect transistors [4][5]. However, none of the above approaches provides the combination of features required for rapid and highly sensitive detection. Recently, a series of Si nanowire biosensors have been reported for sensing pH [6], ions [7] and DNA [8][9]. Promising results have been obtained, for example real-time, high selectivity, label-free sensing with a high sensitivity up to 10 femtomolar (fmtomol/L or fM) [10]. The high sensitivity is attributed to the nanoscale diameter of nanowires, which gives a high ratio of surface area to volume and hence a high sensitivity to surface charge [11]. Additionally, biosensors with Si nanoribbons were found to give 10 nanomolar sensitivity [12]. Therefore, Si biosensors using nanowires or nanoribbons are very promising for Point-of-Care diagnosis, particularly when used with 'Lab-on-a-Chip' technology.

Si nanowire biosensors have been fabricated by both 'bottom up' (about 10 %) and 'top down' (about 90 %) methods (Table 2.2). The 'bottom up' method mainly uses vapour-liquid-solid chemical vapour deposition to grow self-assembled single crystal Si nanowires on insulator substrate [13]. Although the grown Si nanowires are excellent in electrical characteristics for biosensor applications [14], the poor location controllability and incompatibility with current CMOS technology make the 'bottom up' method undesirable for industry. For the 'top down' method, which is compatible with CMOS technology, silicon nanowires have generally been fabricated using expensive

silicon-on-insulator (SOI) substrates [8][15], high-cost ion implantation and advanced lithography, such as electron-beam lithography [15][16] or deep ultraviolet lithography [7][17]. However, these fabrication methods are high-cost and cannot satisfy the requirements for low cost disposable biosensors for point of care applications. For these reasons, new low-cost fabrication processes need to be investigated.

In the past decades, Si thin film transistors (TFTs) have been well researched and widely applied in Liquid Crystal Displays (LCDs). Compared with the complex and high-tech fabrication processes used in CMOS technology, the relative simple and low-tech fabrication processes used in TFT technology [18] should lead to a significant cost reduction. Therefore, TFT technology could be a good candidate for low-cost Si nanowire biosensor fabrication. Compared with the single crystal Si used in CMOS technology, amorphous silicon (α-Si) and polysilicon (poly-Si) used in TFT technology have inferior electrical properties. For example, state-of-the-art single-crystal Si MOSFETs have an electron mobility of about 650 cm^2/V.s compared with 1 cm^2/V.s for α-Si transistors [19] and 580 cm^2/V.s for state of the art poly-Si transistors [20]. From point of view of series resistance, poly-Si would be preferred to α-Si for nanowire biosensor fabrication because of its dramatically higher mobility. In the TFT industry, high mobility polysilicon is produced by recrystallising α-Si deposited on a low-cost glass substrate. However, a glass substrate limits the process temperature to temperatures below 450°C to avoid glass substrate shrinkage and warpage (Corning Eagle 2000 glass) [21][22][23]. For biosensor applications, it is unclear whether low cost crystallisation techniques can be developed consistent with this process temperature constraint. Furthermore, poly-Si nanowire biosensors patterned by e-beam lithography were recently reported and showed a good performance with detection limit of about 30 nM [16][24]. Thus these issues provide a suitable subject for further study with the aim of producing a Si nanowire biosensor using a simple, low cost, low temperature process, but with a reasonable performance.

The simplest recrystallisation technique, solid-phase crystallisation (SPC) [25][26], requires a high temperature anneal for a long duration, typically above 600°C for 24 hours. However, this high process temperature limits the use of low-cost glass substrates and hence several advanced crystallisation technologies have been proposed and researched to reduce the crystallisation temperature, such as laser-based crystallisation (ELC) [27][28] and metal-induced lateral crystallisation (MILC) [29][30]. Although ELC technologies have been widely used in LCD displays for high-end applications, e.g. mobile phones and digital cameras, the high cost of laser equipment and the non-uniformity in device performance make it unsuitable for low cost Si nanowire biosensor

fabrication. Compared with ELC, MILC provides α-Si recrystallisation at a lower temperature, typically about 550°C, without using high cost equipment. MILC could be suitable for low cost glass substrates if the process temperature could be further reduced, for example, by using fluorine implantation [31]. Recently, single crystal Si nanowires were produced using metal induced lateral crystallisation [32][33] and this makes MILC a very promising technique for the fabrication of low cost Si nanowire biosenors. Therefore, an intensive study of α-Si MILC is needed for biosensor applications. Additionally, Si nanowires have been fabricated using a 'spacer' method [29][30][34], which eliminates the need for high cost advanced lithography. As Si ribbons can be used as an alternative to nanowires for biosensor applications, it is also of interest to study the crystallisation of Si ribbons. The primary goal of this PhD project is to develop a low-cost fabrication process for Si nanowire biosensors.

The structure of this thesis is organised as follows. Chapter 2 gives an extensive literature review of research done on amorphous silicon crystallisation and Si nanowire biosensors. Then, chapter 3 introduces conduction models of MOSFETs and poly-Si TFTs and a model for Si crystallinity analysis using Raman spectroscopy. In chapter 4, metal-induced lateral crystallisation at lower temperatures below 550°C is investigated and the effect of various fluorine doses on MILC growth is presented for different anneal temperatures with aim of identifying the optimum fluorine dose. In chapter 5, results are presented on the metal-induced lateral crystallisation of amorphous silicon ribbons and nanowires deposited by LPCVD and PECVD on different substrate materials. In addition, the effect of Si ribbon width on MILC growth is also presented and compared with the preliminary MILC results of MILC on α-Si nanowires. In chapter 6, results are presented on Si nanowire biosensors using TFT technology. The nanowires are fabricated by depositing α-Si over a sharp step and then etching using a Bosch process. The electrical characteristics of the fabricated devices in dry ambient and liquid environments are also presented. Conclusions and Future Work are given in Chapter 7.

Chapter 2

Literature Review

2.1 Crystallisation Technologies

Silicon thin film transistors (TFTs), made from amorphous silicon and polysilicon, are commonly used as channel materials for display applications. Amorphous silicon has a low mobility around 1 cm^2/V.s [19], whilst polysilicon has a higher mobility around 580 cm^2/V.s [20] and thus polysilicon offers an improved device performance. For TFTs, poly-Si is normally obtained by recrystallising the α-Si layer on a glass substrate and its carrier mobility strongly depends on the crystallisation technology and the crystallisation conditions. Therefore, crystallisation technologies need to be optimised to give a high quality polysilicon layer at a low process temperature. In this section, the α-Si recrystallisation technologies of solid phase crystallisation and metal-induced lateral crystallisation are reviewed to inform the further investigations in this thesis.

2.1.1 Solid phase crystallisation

Solid phase crystallisation (SPC) is the conversion of amorphous silicon into polycrystalline silicon by annealing for a long time at a temperature, typically 600°C for 24 hours [35]. The SPC process consists of two stages: (1) nucleation and (2) crystallisation. Initially, the atoms are rearranged due to surface energy lowering and then form a nucleation site for cluster growth. Then the nucleated clusters subsequently enlarge to grow into grains and the amorphous silicon becomes polysilicon. During crystallisation, grains grow from random locations and compete with each other. Therefore, the grains can be enlarged by an increase of nucleation/grain growth ratio by suppressing

grain nucleation sites. In the classical nucleation theory, grain growth at sizes below the critical size, R_T, is very slow, but grain growth increases by orders due to a twin-defect assisted crystal growth mechanism [35]. The growth of grains by SPC is strongly dependent on anneal temperature [35] and follows an Arrhenius-like behaviour, as shown in Fig. 2.1.

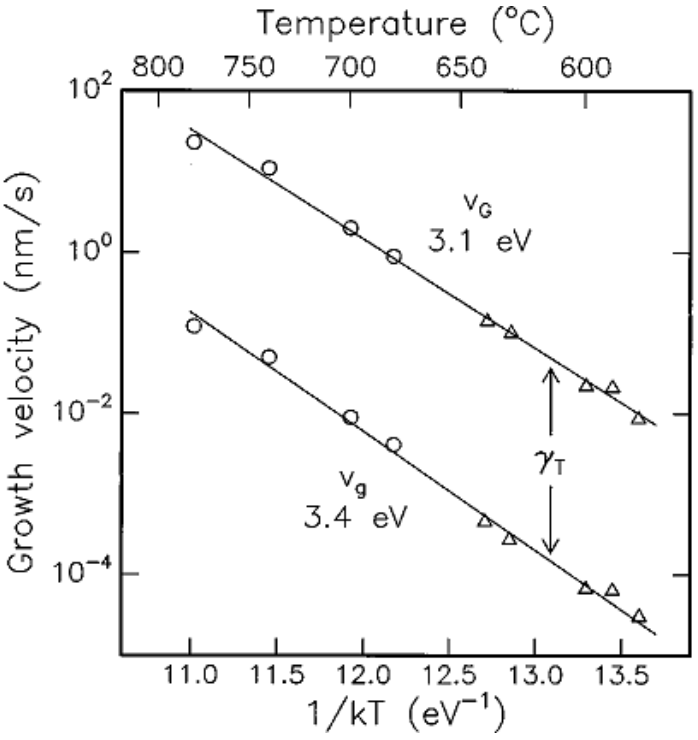
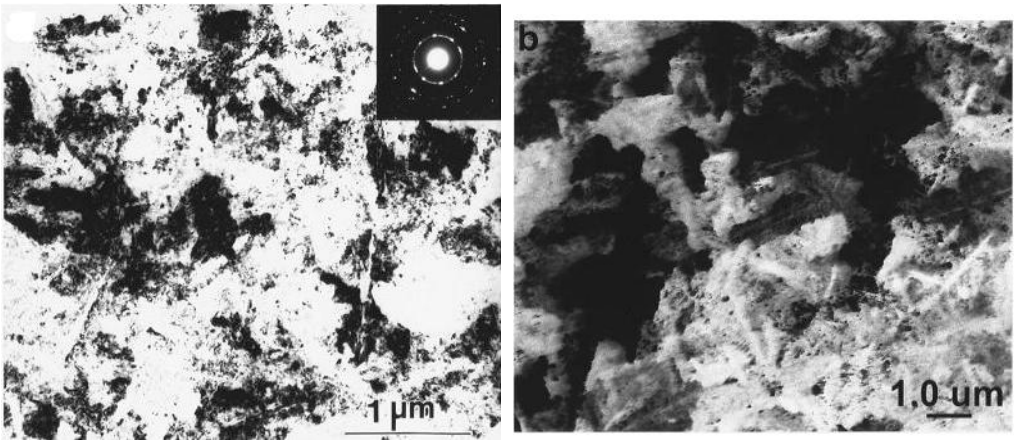


FIGURE 2.1: Grain growth velocities, v_g and v_G, for grain sizes $R<R_T$ and $R>R_T$, respectively, as a function of reciprocal temperature. The parameter γ_T is the ratio between v_G and v_g and is equal to 200-300 and R_T is about 1 nm. After Spinella *et al* [35], copyright AIP.

Usually, the α-Si film is deposited on silicon dioxide (referred as the underlying oxide) [36] and nucleation starts preferentially at the interface between the α-Si and the underlying oxide [37]. This preferred nucleation location is attributed to the strain influence in the Si film. Tensile stress increases the crystallisation rate, whilst compressive stress decreases the crystallisation rate [38]. Due to the different thermal expansion coefficients of α-Si and the underlying oxide [39], the tensile stress is located at the Si/SiO_2 interface and thus the interface becomes a preferential site for nucleation. A secondary nucleation location has been identified at the top Si surface and the surface nucleation rate was measured to be much slower than that at the Si/SiO_2 interface [40].

Several approaches have been studied to suppress grain nucleation at the interface by giving a treatment to the interface. In Chang's work [26], an argon implantation was

found to give an improved poly-Si film quality and grain size by suppressing interfacial grain nucleation. By removing the underlying oxide before the crystallisation, a Si-on-Air structure was fabricated and investigated in [40] and [41]. For the Si-on-Air samples, shown in Fig. 2.2(a), the grain size was increased to 3.0 μm from 0.6 μm and intragranular defects decreased by one order of magnitude after a 600°C anneal for 24 hours, compared with control Si-on-Oxide samples, as shown in Fig. 2.2(b) [40]. The increase in grain size and decrease in defects for Si-on-Air samples were explained by: (a) reduced grain nucleation due to the elimination of preferred grain nucleation sites at the Si/SiO_2 interface and (b) the free volume contraction for the Si-on-Air structure. Strong bonds exist at the Si/SiO_2 interface for the Si-on-Oxide structure and hence free volume contraction is constrained. SPC is advantageous as a simple process, with no requirement for complicated equipment, like laser annealing equipment. However, the annealing temperature for SPC (typically 600°C) is not compatible with low-cost glass substrates. For example, Corning glass requires the process temperature to be below 450°C [21][22][23].



(a) (b)

FIGURE 2.2: Planar TEM micrographs of polysilicon films after a 24 hour 600°C anneal for (a) a sample with an underlying oxide layer (grain size $\approx$ 0.6 μm) and (b) a sample without an underlying oxide layer (grain size $\approx$ 3 μm). After Bo *et al* [40], copyright AIP.

2.1.2 Metal-induced lateral crystallisation

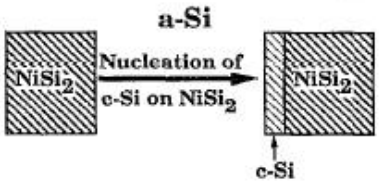
Compared with SPC normally requiring an anneal at 600°C, crystallisation temperatures were found to be lowered when certain metals were deposited on top of the amorphous silicon, for example, Ni [42], Pd [43] and Au [44]. This phenomenon is known as

metal-induced crystallisation (MIC) and can be used for α-Si crystallisation on glass substrates, providing a cheaper method for poly-Si TFT fabrication. However, considerable metal contamination is also introduced into the polysilicon, which significantly affects the device performance and in particular gives high values of leakage current [45]. For this reason, polysilicon by MIC is unsuitable for high performance poly-Si TFTs and likely to be unsuitable for biosensors as well though this has not been well studied.

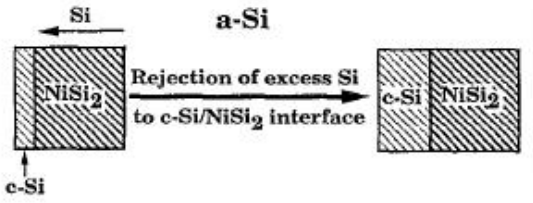
The MIC metals, Ni and Pd, which are silicide forming metals, can also crystallise α-Si in the adjacent region unexposed to metals [46]. This is called metal-induced lateral crystallisation (MILC). A lateral distance of 100 μm can be obtained by Pd MILC with a poly-Si grain size between 10 μm and 20 μm after a 10 hour 500°C anneal [43]. This crystallisation rate is much higher than that achieved in SPC. However, Pd-MILC is not applicable for transistor fabrication because the crystallised silicon contains large numbers of microtwin defects [47]. For the above reasons, Ni [46], as the most promising candidate for MILC technology, is chosen for study in this project.

2.1.2.1 MILC mechanism

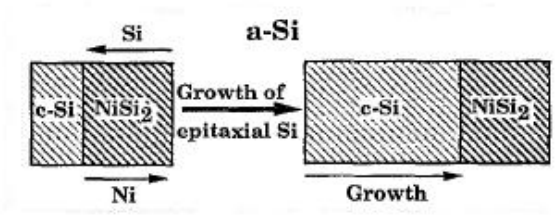
Hayzelden *et al* [46][48] proposed the mechanism of metal-induced lateral crystallisation for Ni. As illustrated in Fig. 2.3, the Ni-MILC process has three stages [48]. First, Ni forms crystalline $NiSi_2$ with α-Si after an anneal above a threshold temperature (found to be 450°C [49]) and this is called $NiSi_2$ nucleation. After the formation of $NiSi_2$, the Ni diffuses into the α-Si region to form new $NiSi_2$. Because the lattice mismatch between $NiSi_2$ and crystalline Si (c-Si) is only about 0.4% [50], an epitaxial crystalline Si layer is formed. The diffusion driving force is widely believed to be that Ni atoms have a lower chemical potential at the $NiSi_2$/α-Si interface than at the $NiSi_2$/c-Si. Then the crystallisation process repeats again and again, leaving a long trail of c-Si. In the MILC region, the Ni concentration is much lower than that in the MIC region as shown in Fig. 2.4. Similar results were also reported in [51] using micro-Auger electron spectroscopy. This leads to a lower leakage current in devices fabricated using MILC than MIC. It should also be noted that there is another high nickel concentration region at the crystallisation front. In the MILC region, the grains are mainly (110)-oriented [51] and grow along the $\{111\}$ plane for its lowest surface energy [52].



(a) $NiSi_2$ nucleation



(b) Ni diffusion



(c) c-Si formation

FIGURE 2.3: Schematic diagram of Ni-MILC process including (a) $NiSi_2$ nucleation, (b) Ni diffusion towards α-Si/$NiSi_2$ interface and (3) growth of epitaxial c-Si. After Hayzelden *et al* [46], copyright AIP.

2.1.2.2 Process parameters and structures for MILC improvements

Many issues including process parameters and structures have been investigated for Ni-MILC growth and a summary of these results is given in Table 2.1. The MILC rate was found to decrease with a decrease of α-Si film thickness [56]. Moreover, the crystallinity was found to be influenced by the α-Si film thickness. For the 40 nm thick Si film in Fig. 2.5(a), a single grain layer was formed, whilst a double grain layer structure was observed for a 100 nm film in Fig. 2.5(b) [62]. As the Si thickness is reduced to 16 nm, the lateral crystallisation is suppressed and replaced by MIC and the orientation was found to change from (110) to (100) [66]. Thus, an α-Si thickness of $>$ 16 nm is needed for MILC.

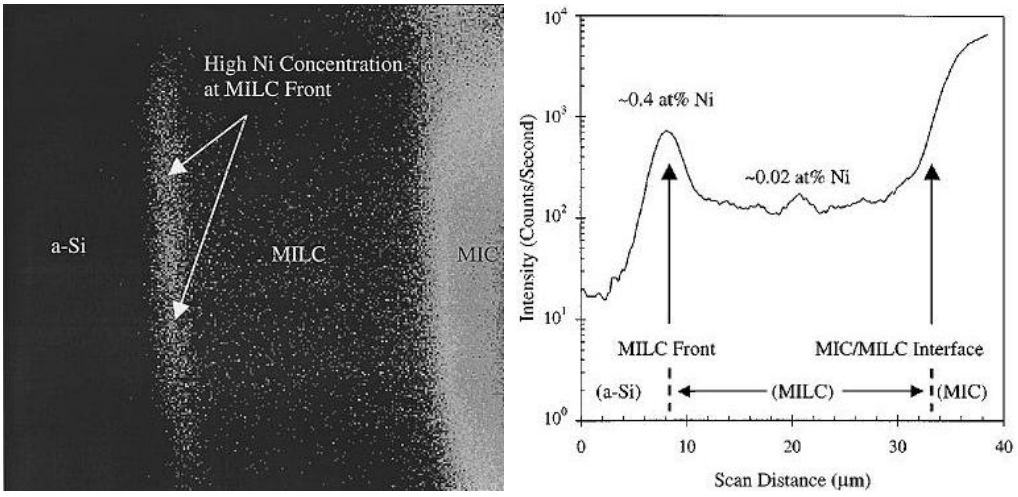
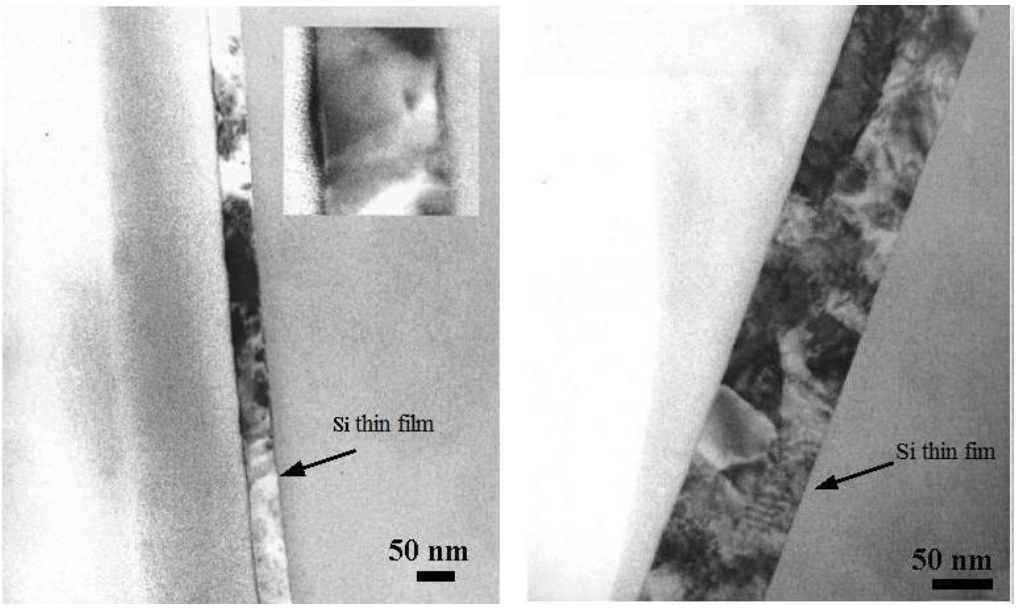


FIGURE 2.4: (a) Scanning SIMS analysis of Ni distribution in a crystallised α-Si film in the MIC, MILC and α-Si regions and (b) Ni distribution cutline in the Si film by SIMS. After Hayzelden *et al* [46], copyright AIP.

TABLE 2.1: Survey of parameter influence on MILC

Experiment	Results	α-Si deposition	Ref.
Ni threshold	Ni threshold concentration for MILC is 5E18 cm^{-3}	-	[42]
Ni shape	Device performance: Oval-shaped Ni > Line-shaped Ni	LPCVD	[53]
Annealing	Film quality: MILC by FA[a] > MILC by RTA[b]	LPCVD	[54]
Preannealing	MILC rate is reduced in preannealed silicon film	LPCVD	[55]
Dopants	MILC rate: P and As implanted < undoped	LPCVD	[56]
	MILC rate: B implanted > undoped	LPCVD	[57]
	MILC rate: B-doped > undoped > P-doped (*in situ*)	LPCVD	[58]
	MILC rate: B-doped > undoped > P-, As-doped (*in situ*)	LPCVD	[59]
	MILC rate: undoped > P-doped or B-doped (*in situ*)	PECVD	[60]
Stress	MILC rate: Tensile stress > unstressed > compressive stress	LPCVD	[47]
	MILC rate: Tensile stress > unstressed	LPCVD	[61]
Fluorine	MILC rate and quality is improved for F-implanted Si film	LPCVD	[31]
α-Si thickness	Poly-Si crystallinity: 30 nm > 100 nm	LPCVD	[62]
	Device performance: 30 nm > 100 nm	LPCVD	[55]
	MILC length, device performance: 100 nm > 300 nm	LPCVD	[63]
Ni thickness	Thin Ni film leads to improved poly-Si quality	PECVD	[64]
Grain filter	Poly-Si quality: MILC is improved through a grain filter	PECVD	[65]

a: FA-furnace annealing *b*: RTA-rapid thermal annealing

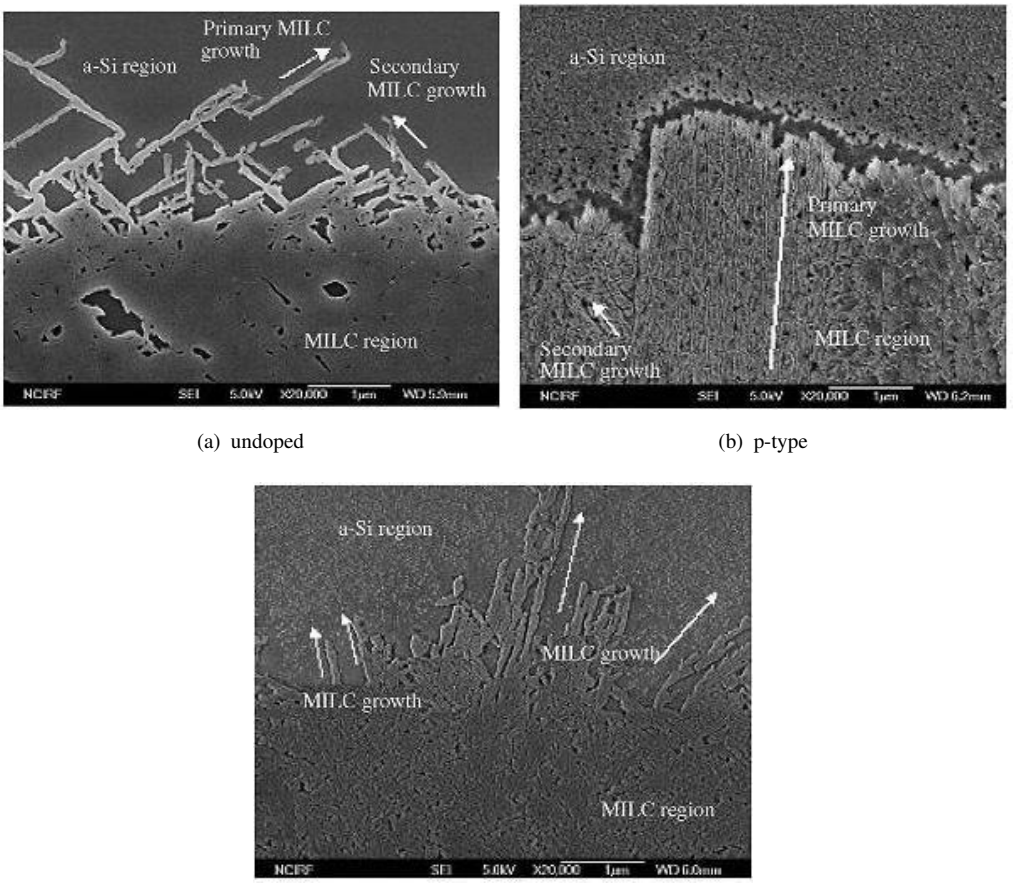


(a) (b)

FIGURE 2.5: Cross-section TEM images of Ni-MILC poly-Si films of (a) 40 nm and (b) 100 nm. Both samples were annealed for 20 hours at 500°C. After Chang *et al* [62], copyright ECS.

Dopants in α-Si also have an influence on Ni-MILC. Phosphorus and arsenic implanted into α-Si reduce the MILC rate and degrade the film morphology [56], whilst boron implanted into α-Si gives an improved MILC rate [67]. Similar doping influences were also found for *in situ* doped α-Si [58], with the MILC rate of n-type $<$undoped $<$p-type. As illustrated in Fig. 2.6, the needle-like grains in n-type doped samples are randomly-oriented, whilst the needle-like grains in p-type samples are parallel and narrower than those in undoped samples. Therefore, Si nanowires doped by n- or p-type may be preferred from nanowire MILC considerations for Si nanowire biosensor fabrication.

The influence of fluorine in MILC was investigated in [31]. In this work, fluorine was implanted into either the amorphous silicon or the underlying buffer oxide layer before the α-Si deposition. In both cases, the Ni-MILC rate increased by 65% compared with that of samples without a fluorine implantation after a 500°C 20 hour anneal (Fig. 2.7). This improvement was explained by F chemical effects that suppressed random crystallisation at the Si/SiO_2 interface [31]. For higher temperatures, e.g. 550°C and 600°C, however, the MILC growth rate and length were degraded compared with samples without fluorine.



(a) undoped (b) p-type

(c) n-type

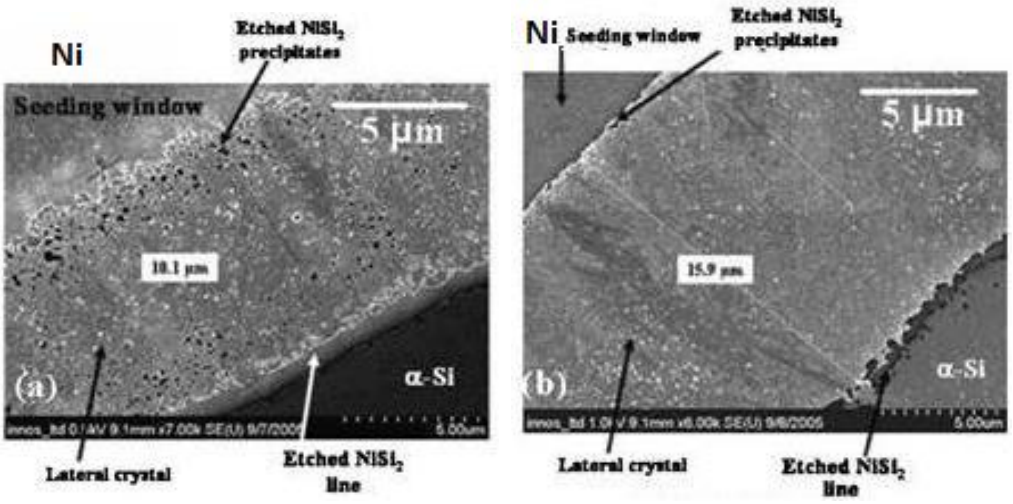
FIGURE 2.6: Plan SEM micrographs after a MILC annealing of 5 hours at 550°C for (a) undoped (b) boron *in situ* doped and (c) phosphorus *in situ* doped samples. After Ahn *et al* [58], copyright Elsevier.

2.1.3 Single-crystal Si nanowires and pillars by MILC

In this section, some advanced crystallisation technologies are briefly reviewed, which aims to achieve single crystalline silicon nanowires at low temperature. These same technologies could be used for Si nanowire biosensor fabrication.

2.1.3.1 Single-crystal Si nanowires

As discussed above, a single grain layer of polysilicon can be obtained when the thickness of the α-Si is decreased [62]. Single crystal nanowires 2.2 μm in length were obtained using Ni-induced lateral crystallisation of sub 100 nm α-Si nanowires [32]. TEM images for the crystallised nanowires after annealing at 500°C for 20 hours are shown in Fig. 2.8. In this work, the width of the nanowires was found to be critical for



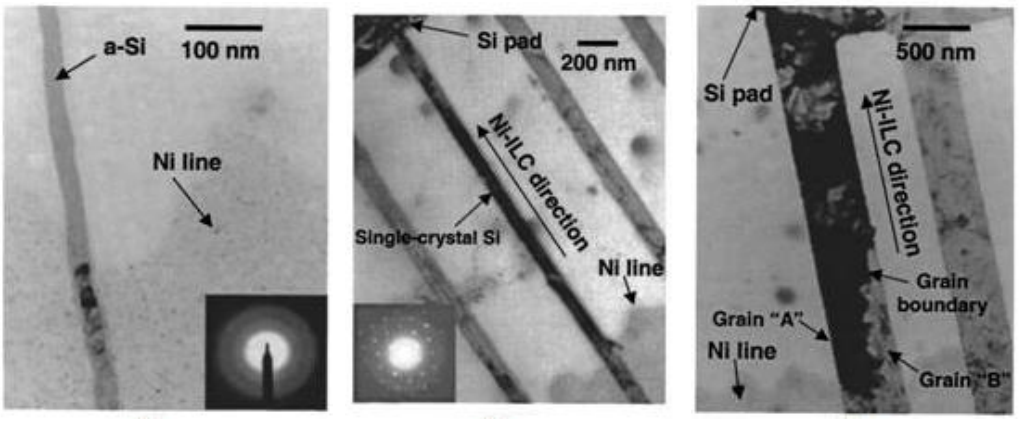
(a) without Fluorine (b) with Fluorine

FIGURE 2.7: Plan SEM micrographs of laterally crystallised samples (a) with a fluorine implant and (b) without a fluorine implant after an anneal at 500°C for 20 hours. After Hakim and Ashburn [31], copyright ECS.

the crystalline quality. Fig. 2.8(a) shows that $NiSi_2$ precipitates were found after the anneal for 20 nm wide α-Si nanowires but no obvious lateral crystallisation was found. This suggests that there is a minimum width for MILC and hence the crystallinity cannot be continuously improved by reducing the α-Si nanowire width. Fig. 2.8(b) shows the MILC region for 70 nm Si nanowires after the anneal. Clear evidence of crystallisation is seen, with a crystallisation length of 2.2 μm and a single grain in the crystallised region. For 450 nm Si nanowires after the anneal, multi-grains can be clearly identified in Fig. 2.8(c), which indicates that competitive grains occur in Si nanowires beyond a given width. By taking α-Si thickness and width influences into consideration, the dimension of Si nanowires needs to be carefully optimised if single crystal nanowires are to be produced by MILC.

2.1.3.2 Single crystal Si pillars

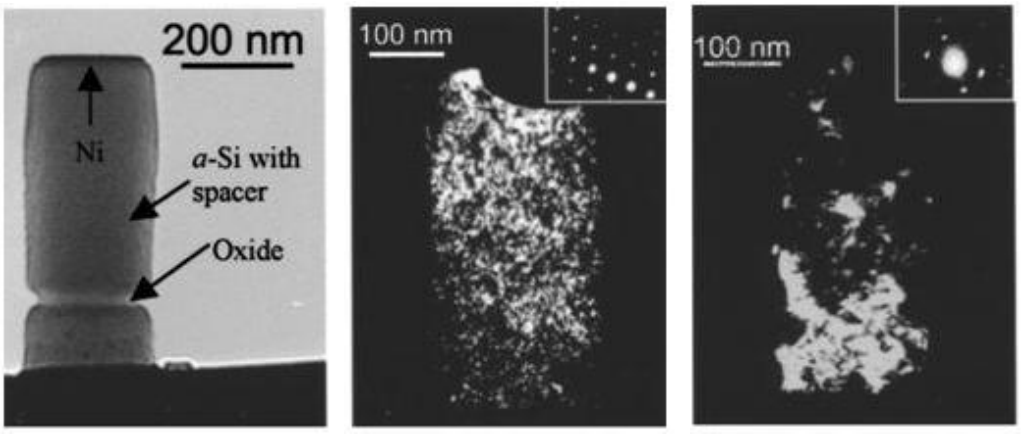
Single crystal Si pillars were reported using a two-step MILC anneal [33]. After a Ni layer was deposited on the top of the α-Si pillars in Fig. 2.9(a), the samples were annealed at 400°C for 15 hours, during which $NiSi_2$ precipitates were nucleated. It should be noted that this anneal temperature for $NiSi_2$ is slightly lower than the threshold temperature reported in [49]. After a second annealing step at 550°C for 2 hours, pillars with widths of 180 nm were found to be single crystal, as shown in Fig. 2.9(b). The percentage of single-crystal pillars achieved using the two-step anneal was also found to



(a) 20 nm wide (b) 70 nm wide (c) 450 nm wide

FIGURE 2.8: TEM micrographs of crystallised Si nanowires achieved after a 10 hour crystallisation anneal at 500°C: (a) 20 nm wide, (b) 70 nm wide and (c) 450 nm wide. After Gu *et al* [32], copyright AIP

be much higher than that using a one-step anneal at 550°C for 6 hours, as shown in Fig. 2.9(c). This phenomenon can be explained by the suppression of random crystallisation by the low temperature anneal in the first step. The width influence was also investigated and the percentage of single crystal pillars decreased from 95% to around 50% as the width increased from 180 nm to 400 nm [33]. This work gives a promising method to get high quality Si nano pillars by suppressing random crystallisations during MILC and also indicates that the crystallinity of the crystallised Si nanowires can be improved by suppressing random crystallisation during MILC.



(a) (b) (c)

FIGURE 2.9: Cross-section TEM micrographs of pillar samples (a) before anneal (bright-field image), (b) after a 400°C 15 hour anneal followed by a 550°C 2 hour anneal (dark-field image) and (c) after a 550°C 6 hour anneal (dark-field image). After Liu *et al* [33], copyright AIP

2.2 Nanowire Biosensors

The structure of a typical Si nanowire biosensor is illustrated in Fig. 2.10. A single nanowire or an array of nanowires is laid on an insulator between a highly doped source and drain. Below the insulator, the doped Si substrate works as a back gate. The source and drain electrodes are isolated from the sensing liquids by a protection layer, e.g. silicon nitride. The nanowire surface is exposed and target receptors with specific functional groups are attached to the Si nanowire surface by molecular linkers.

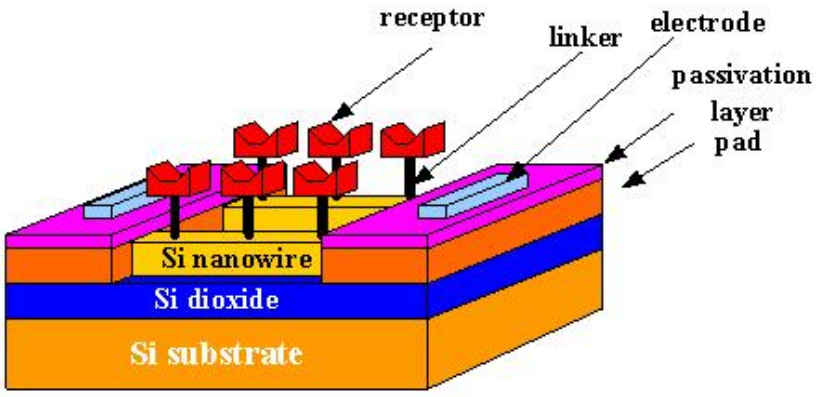


FIGURE 2.10: Schematic diagram of the structure of a Si nanowire biosensor.

2.2.1 The mechanism of Si nanowire biosensing

The sensing mechanism of a Si nanowire biosensor is described as follows and shown in Fig. 2.11. When the nanowire surface is exposed to the sensing targets, receptors on the nanowire surface have the capability of immobilising the targets, e.g. ions, DNA, or proteins. For DNA biosensors, only single-stranded(ss) DNA, which is complementary to receptors carrying negatively charges, is immobilised on the nanowire surface by a hybridisation with receptors. The accumulated charges carried by the captured DNA chain give an electrostatic gating effect to the nanowire channel, which in turn depletes or accumulates for n-type and p-type, respectively. Therefore, the capture of the target molecule is seen as a change in channel conductance.

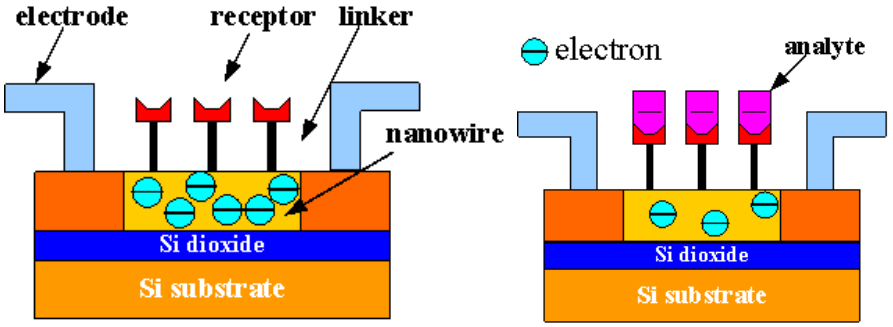


FIGURE 2.11: Schematic diagrams showing the sensing principle of a Si nanowire biosensor (a) without a complementary DNA and (b) with a complementary DNA

2.2.2 Literature review of Si nanowire biosensors

Silicon nanowire biosensors can provide a real-time, high selectivity, label-free sensing tool for sensing pH [6], ions [7] and DNA [8][9]. A number of papers have been published on Si nanowire biosensors and a summary of the main results is provided in Table 2.2. A paper has also been published on a Si nanoribbon biosensor, which uses a wider Si ribbon defined by photolithography to achieve biosensing. The electrical detection of DNA has been achieved at concentrations as low as 10 fM (femtomolar) [11]. This high sensitivity was attributed to the nanoscale dimension of the nanowires, which is comparable to the size of the proteins and DNA. The high sensitivity was achieved as a result of the high surface-to-volume ratio of the nanowires [9]. It was found that the sensitivity increases linearly with reducing nanowire diameter from 800 nm to 100 nm. An even stronger enhancement of sensitivity was found on reducing the nanowire diameter from 100 nm to 50 nm. Since the diameter of single crystal Si nanowires achieved by MILC is also of the order of several deca-nanometers [32], crystallised α-Si nanowires are likely to be quite suitable for nanowire biosensor fabrication. As Si nanoribbons were also reported to achieve good performance [12], this gives the potential that a reasonable performance can be achieved on larger geometry wires or ribbons.

The sensitivity of biosensors is affected by several factors, especially, the ion strength of the buffer solution. This influence is expressed in terms of the Debye length, λ_d, which is defined as the typical distance required to screen the surplus charge by the mobile charges present in the solution [77]. In other words, the negative charges on proteins and DNA show no net charge on the nanowire as the negative charges are surrounded by positive charges in the solution [71]. Several experimental works [17][71][73][74] have shown the effect of the buffer ion concentration on the sensitivity. In Chua's work

TABLE 2.2: Survey of Si nanowire/nanoribbon biosensors

Year	Nanowires	Lithography[a]	Linkers	Receptors	Detection limit	Ref.
2001	VLS[b], p-type	-	APTES[c]	biotin	10 pM	[6]
2004	gold-catalyzed CVD[d]	-	avidin	ssPNA[e]	10 fM	[10]
2005	SOI[f], p-type	e-beam[g]	MPTMS[h]	ssDNA, ssPNA	10 pM	[53]
2005	gold-catalyzed CVD	e-beam	APTMS[i]	abl tyrosire	100 pM	[13]
2006	SOI, n-&p-type, pass[k]: Si_3N_4	e-beam -	APDMES[j] tert-BAC	- -	1 nM 10 pM	[8]
2007	SOI, n-&p-type	DUV[l]	AEAPS[m]	biotin	10 pM	[68]
2007	SOI, pass: Si_3N_4	self-oxidation	APTMS	PNA	10 fM	[69]
2007	SOI, n-type	e-beam	APTES	anti-PSA	30 nM	[70]
2007	SOI, n-&p-type	e-beam	APTES	biotin	-	[71]
2008	SOI, nanoribbons	optical lith.	APTES	biotin	1 nM	[12]
2008	SOI, p-type	e-beam	HUPA[n]	PNA	1 μM	[72]
2008	Si, p-type	wet etch	APTES	anti-CRP	10 nM	[73]
2008	poly-Si, n-type	self-oxidation	t-BOC[o]	PNA	1 nM	[74]
2009	SOI, n-type	DUV	APTES	anti-cTnT	1 fg/mL	[17]
2009	poly-Si	spacer etch	APTES	anti-IgG	17 pM	[24]
2009	poly-Si, n-type	e-beam	APTES	GOD[p]	10 nM	[75]
2009	poly-Si, n-type	spacer etch	APTES	PNA	1 fM	[76]
2010	poly-Si, n-type	e-beam	APTES	PNA	30 nM	[16]

a: lithography only refers to the lithography techniques for nanowires patterning, whilst optical photolithography might be used throughout other processes.
b: VLS - vapor-liquid-solid growth, bottom-up technology
c: APTES - 3-aminopropyltriethoxysilane
d: CVD - chemical vapor deposition
e: ssPNA - single-stranded Peptide nucleic acid
f: SOI - silicon-on-insulator
g: e-beam - electron-beam lithography
h: MPTMS - 3-mercaptopropyltrimethoxysilane
i: APTMS - 3-(trimethoxysilyl)propyl aldehyde
j: passivation layer to isolate device from analyte
k: APDMES - 3-aminopropyldimethylethoxysilane
l: DUV - deep-ultraviolet lithography
m: AEAPS - N-(2-aminoethyl)-3-aminopropyl-trimethoxysilane
n: HUPA - 11-hydroxyundecylphosphonate
o: t-BOC - 10-N-Boc-Amino-dec-1-ene
p: GOD - glucose oxidase

[17], the Debye length was found to increase with the decrease of solution ionic strength and hence the sensitivity increases with the increase of the Debye length. Therefore, a diluted buffer with low ion concentration is preferred for a longer Debye length, however, this concentration is normally limited by the biological activity of proteins [17]. In Zhang's work [74], the effect of the charge layer on sensitivity was studied and the sensitivity was found to reduce with the increasing charge layer distance from the nanowire surface. Thus, a shorter linker chain is preferred but this is also limited by the functionalisation chemistry. Finally, biosensor sensitivity is also affected by nanowire carrier concentration and a lower carrier concentration gives a larger conductance change and hence an improved sensitivity [78].

To date nanowires have been fabricated by both 'top-down' [8][53][68] and 'bottom-up' [6][10][53] methods. The 'top-down' method, which is compatible with CMOS technology, has generally used advanced lithography technologies, such as e-beam lithography [53] or deep ultra-violet lithography [68] to pattern nanowires on SOI wafers. E-beam lithography, which uses direct pattern-writing with an electron beam, can define patterns with widths down to 10 nm. However, it has a slow writing speed, which makes it impractical for large-scale manufacturing. Deep ultra-violet lithography is also an expensive process because it requires advanced photoresists and an advanced light source. In addition, other reported Si nanowire biosensors using feature reduction processes, such wet etch [73] and self-oxidation [74] also suffer from poor device repeatability and uniformity issues for large substrate fabrication. The 'bottom-up' method fabricates nanowires uses a self-assembly process, e.g. metal-catalyst CVD [10][13] or vapor-liquid-solid (VLS) growth [6]. The main advantage of a self-assembly process is its low-cost. However, self-assembly provides little control over nanowire location and hence is difficult to integrate with CMOS technology for signal processing. Therefore, current technologies do not provide a viable route to the manufacture of low-cost Si nanowire biosensors, which is essential if disposable biosensor systems are to be produced for point of care healthcare applications. Hence new approaches to Si nanowire fabrication are required which use the top-down approach, but do not use expensive advanced lithography technologies or expensive SOI substrates.

Recently, some polycrystalline silicon nanowire biosensors have been reported using e-beam lithography [16][75] and spacer etch [24][76][79]. These research demonstrates that polysilicon nanowires using TFT technology are a promising solution for the fabrication of nanowires, but the reported spacer nanowires are triangular in shape and this makes it difficult to control the width and height. Therefore, a method for producing nanowires with better control of width and height is needed.

2.2.3 Si surface functionalisation for Si nanowire biosensors

After Si nanowires are fabricated, the nanowire surface needs to be functionalised with receptors that act as sensing probes. Fig. 2.12 shows the functionallisation process of Si nanowires including surface silanisation and surface modification with receptors. The Si nanowires are treated in an oxygen plasma [6] or water-vapor plasma [53] with the purpose of cleaning contaminants and generating hydroxyl (OH) groups on the nanowire surface. Then the Si nanowires are exposed to a linker solvent, shown in Fig. 2.13(a). The most commonly used linker (Table 2.2) is , (3-aminopropyl)-triethoxysilane (APTES), which leaves amino (NH_2) groups on the nanowire surface. After a rinse in an organic solvent and a blow dry with nitrogen gas, the surface is modified with chemicals containing aldehyde groups, like the very popular Glutaraldehyde [70], as shown in Fig. 2.13(b). Then the modified surface has a capability of immobilising biomolecules, like antibodies, PNA or DNA, as shown in Fig. 2.11.

Fig. 2.13 shows schematics of an example of DNA captures by peptide nucleic acid (PNA) receptors [69]. After PNA strands are immobilised on the surface of the nanowires (Fig. 2.12(a)), the PNA strands can hybridise fully complementary DNA strands and hence DNA strands with negative charges are captured on the nanowire surface, as shown in Fig. 2.12(b).

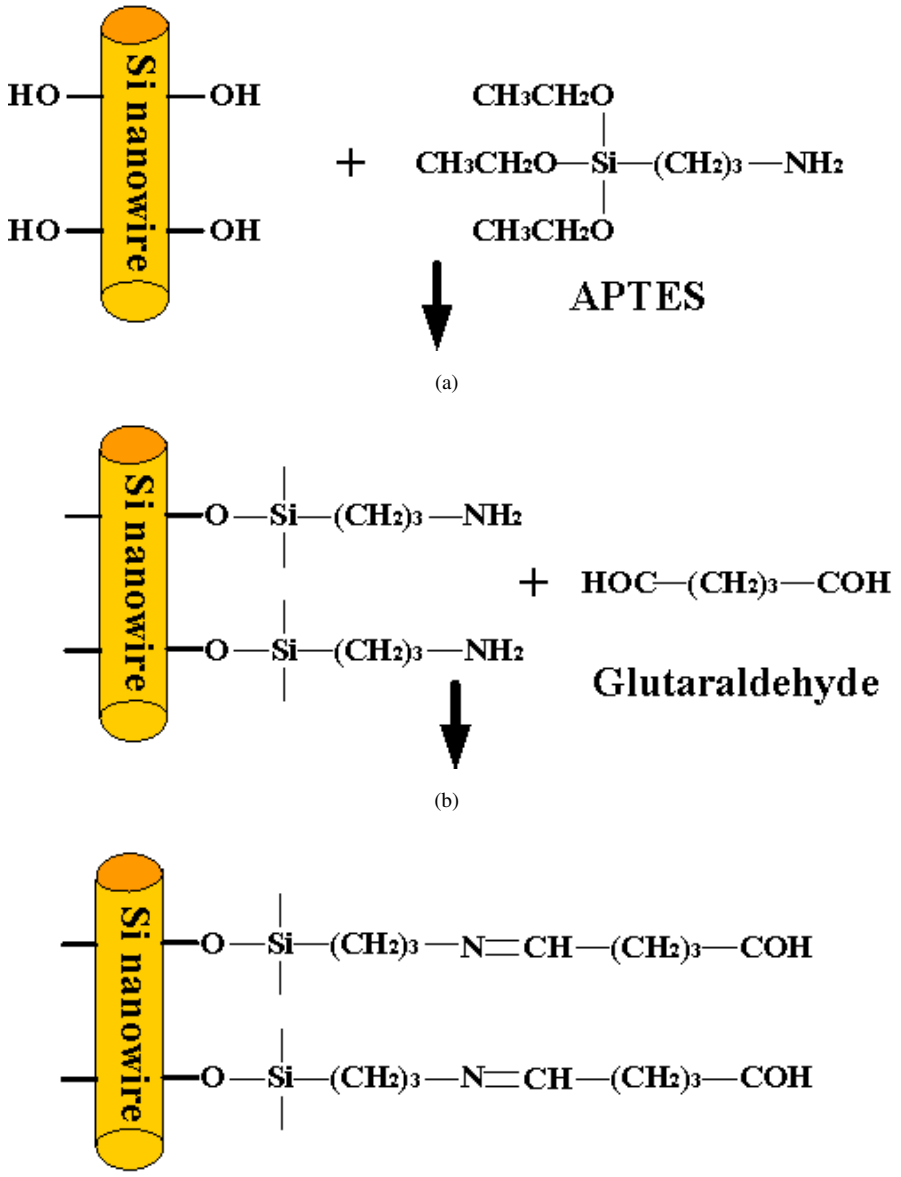


FIGURE 2.12: Schematics of Si nanowire functionallisation. (a) a nanowire after an oxygen plasma or water vapor plasma cleaning, (b) a nanowire after a nanowire surface silanisation process using APTES and (c) a nanowire after a surface modification process with receptors (sensing probes).

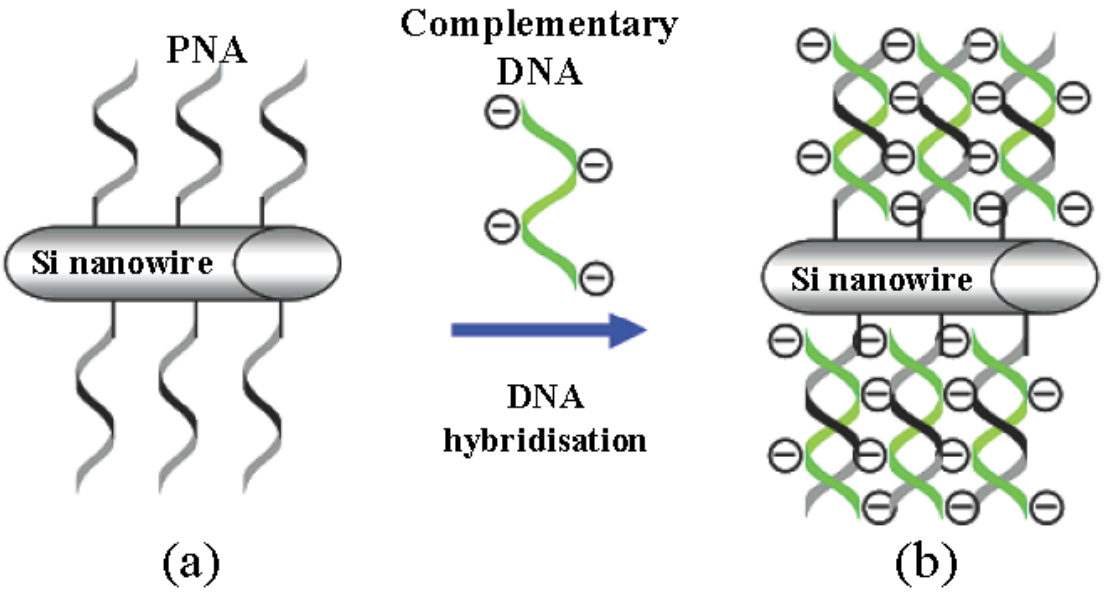


FIGURE 2.13: Schematics of DNA capture on a Si nanowire surface; (a) a Si nanowire with PNA strands immobilised on the surface, (b) the Si nanowire after hybridisation of PNA strands with fully complementary DNA strands. After Gao *et al* [69], copyright ACS

Chapter 3

Theory

In this chapter, the theory of MOSFETs and poly-Si TFTs is reviewed to give the necessary background knowledge for the fabricated Si nanowire biosensors. Initially, MOSFET theory is discussed to give definitions and expressions of electrical parameters, e.g. threshold voltage, drain current and subthreshold slope. Then, Seto's model for the effects of grain boundaries is studied. Finally, analysing techniques for the Raman spectra of amorphous and polycrystalline silicon are also presented.

3.1 Bulk MOSFETs

The basic structure of an n-channel bulk MOS transistor is illustrated in cross section view in Fig. 3.1. It is usually a four terminal device with Gate (subscript g), Source (subscript s), Drain (subscript d) and Substrate (subscript b). The n-channel MOSFET consists of two highly doped n-type (n+) regions, source and drain, connected by a lower doped p-type region. The three doped regions are normally formed by ion implantation. Above the p-type region (channel region), there is an n+ polysilicon or metal gate, which is isolated from the channel region by a thin insulator, called as the gate insulator. When the Gate is grounded, Source and Drain act as two back-back diodes and thus only negligible leakage current flows when a bias is applied between the source and the drain. However, for positive gate biases, carriers in the channel are controlled and hence the transistor can work in different operation modes.

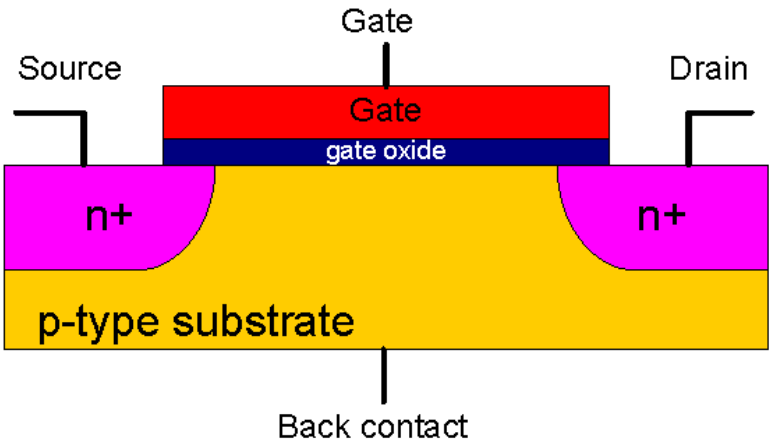


FIGURE 3.1: The cross section structure of an n-channel bulk MOSFET.

3.1.1 MOS capacitor

For simplicity, the effect of gate bias is studied based on the following assumptions: (1) the channel is uniformly doped, (2) the silicon dioxide gate insulator is ideal and there are no trapped charges or interface charges, and (3) the work function difference between the gate and the silicon is negligible. Assumption (1) is dependent on the fabrication process. For assumptions (2) and (3), the influence of interface and trapped charges and work function difference are discussed later. Under these assumptions, the transistor behaves as an ideal MOS capacitor.

3.1.1.1 Surface potential

When the gate is unbiased, the Fermi level should be continuous and thus all energy bands are flat, as shown in Fig. 3.2(a) and this is called the *flat band condition*. When a negative bias is applied to the gate, the Fermi level in the gate is raised with respect to that of the channel, as shown in Fig. 3.2(b). This leads to an electric field attracting holes from the bulk region. Therefore, extra holes are attracted and accumulated in the surface region, called *accumulation*. As the Fermi level along the channel is still flat, there is no net current. When a positive voltage is applied to the gate, the Fermi level in the gate moves downward with respect to the silicon channel. The energy bands in the silicon channel also bend downward and this creates an electric field repelling holes and attracting electrons. As shown in the Fig. 3.2(c), the Fermi level moves towards the intrinsic Fermi level in the surface region and this indicates that the hole concentration near the surface is lower than that in the bulk region, referred as the *depletion condition*.

As the positive bias to the gate further increases, more electrons are attracted to the surface region. As shown in Fig. 3.2(d), the energy bands (including the intrinsic Fermi level) in the silicon channel bend further downwards. Finally, at the surface, the intrinsic Fermi level is bent below the Fermi level and this means that electrons become the majority carriers near the surface. In other words, the surface doping is inverted from p-type to n-type and thus the n+ Source and Drain are connected by a thin n-type channel. This is referred to as the *inversion condition*. When the electron concentration at the surface is equal to the hole concentration in the body, which is $\psi_s = 2\psi_b$, this is defined as the *strong inversion condition*. Here, ψ_b could be calculated using the substrate doping, N_A for p-type, and the intrinsic carrier concentration, n_i, as:

$$\psi_b = \frac{kT}{q} \ln \frac{N_A}{n_i} \tag{3.1}$$

3.1.1.2 Work function difference

In practice, assumption (2) in Section 3.1.1 for an ideal MOS capacitor is not true. The energy band diagram including the vacuum level for a p-type MOS capacitor with an metal gate is shown in Fig. 3.3(a), which is in the flat band condition. The work function difference is defined as the potential difference between the vacuum level and the Fermi level. In the energy diagram, the work functions of the metal and the Si channel are normally different. Taking into consideration that both the vacuum level and the Fermi levels on both sides of the oxide layer should be continuous under zero gate bias, the energy levels in the surface region of the silicon channel have to be bent downwards as shown in Fig. 3.3(b). Therefore, it can be seen from the energy band diagram that the surface region is depleted under zero gate bias. We can also conclude that the flat band condition, shown in Fig. 3.3(a), can be achieved by applying a gate bias, named the flat band voltage V_{fb}, which is the work function difference between the metal gate and the silicon channel as:

$$V_{fb} = \psi_{ms} = \psi_m - \psi_{si} \tag{3.2}$$

where ψ_{ms} is the work function difference between the gate and the channel, and ψ_m and ψ_{si} are the work functions for the gate and the Si channel, repectively.

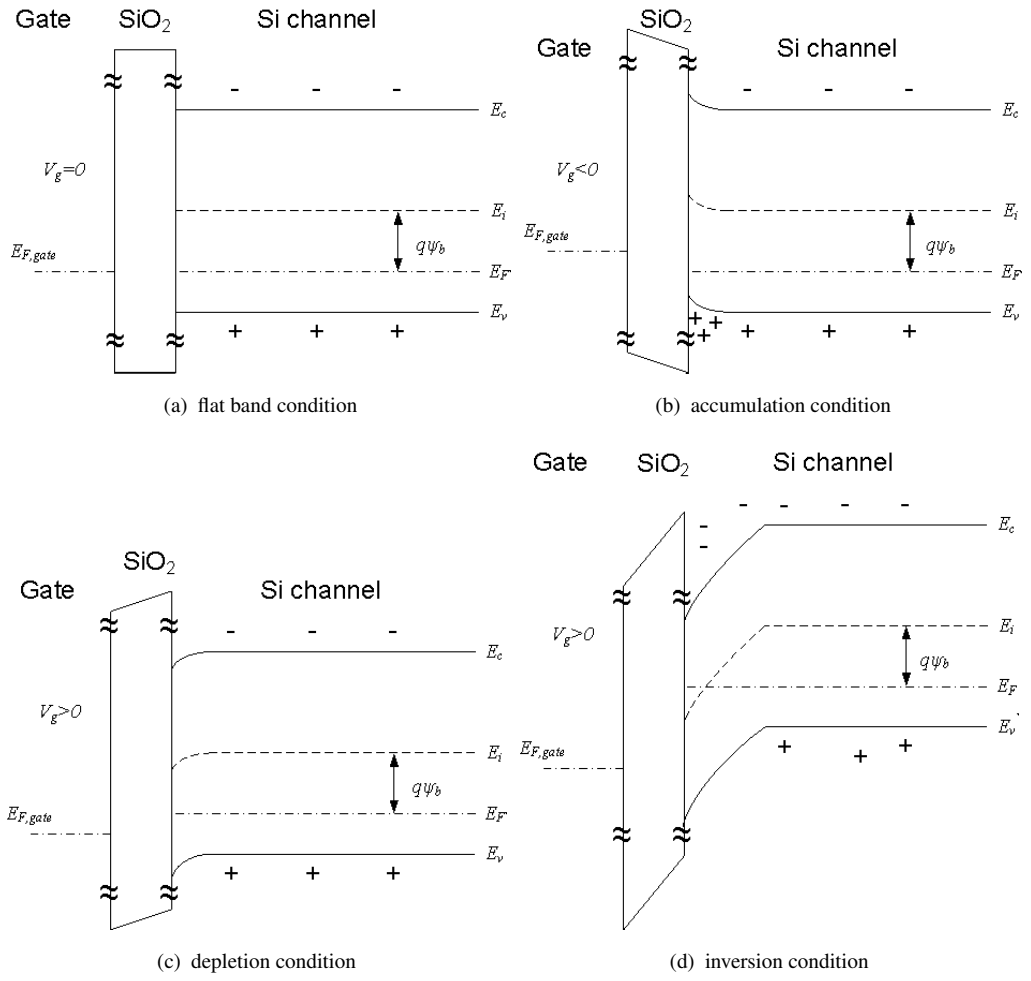


FIGURE 3.2: The energy band diagrams of a p-type MOS capacitor in (a) flat band condition, (b) accumulation condition, (c) depletion condition and (d) inversion condition.

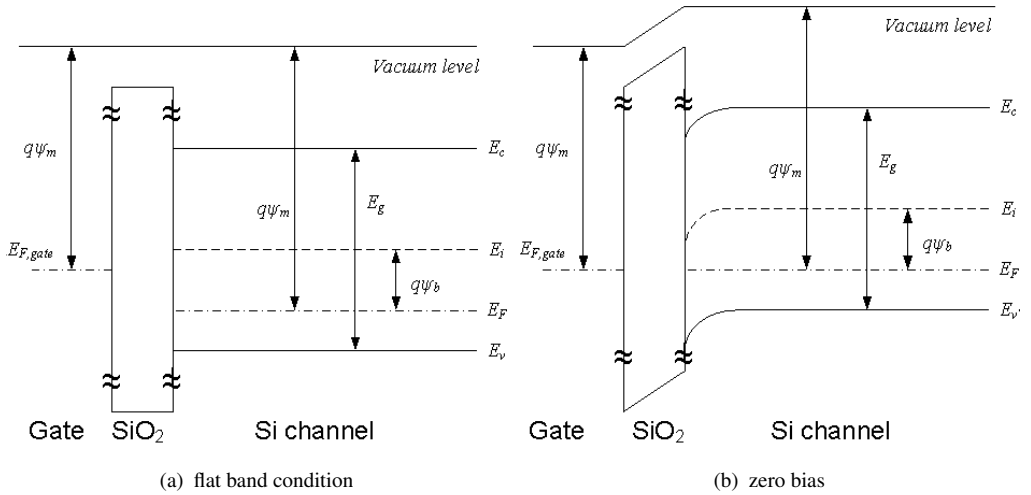


FIGURE 3.3: The energy band diagrams of a p-type MOS capacitor with a metal gate under (a) flat band condition and (b) zero bias.

3.1.1.3 Interface charges in the gate oxide

In the above discussion, the gate oxide was assumed to be an ideal insulator for simplicity. However, this is not the case and hence gate oxide charges and their influence are briefly discussed here. In Deal's work [80], the charges in the gate oxide are illustrated in Fig. 3.4. The four types are modelled [80] as: (1) fixed oxide charges, Q_f, (2) mobile ionic charge, Q_m, (3) oxide trapped charge, Q_{ot}, and (4) interface trapped charge, Q_{it}.

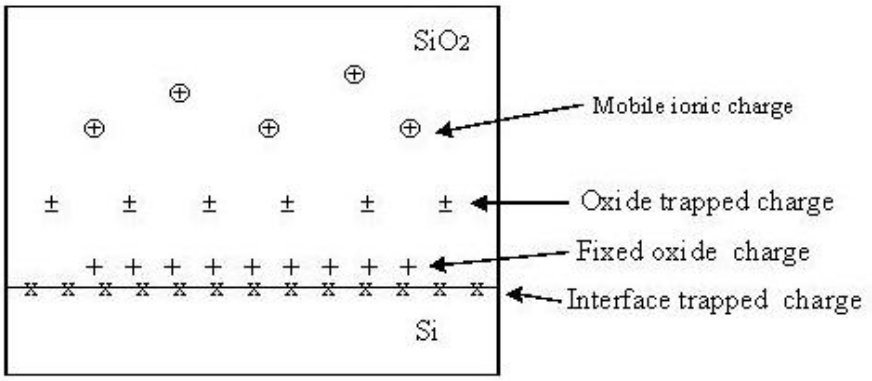


FIGURE 3.4: The modelled charges in gate oxide.

Fixed oxide charges are positive charges in the oxide less than 24 Å from the Si/SiO_2 interface [81] and are mainly caused in the thermal oxidation and subsequent annealing process [81]. The charge density depends on the oxidation process, cooling conditions and the silicon orientation. Mobile ionic charges are mainly due to sodium or potassium contamination during the fabrication process. These mobile ionic charges are positive ions, which can move in the oxide layer. The oxide trapped charges, either electrons or holes, are introduced by bombardment with high energy particles in the fabrication process, such as ion implantation, plasma or reactive etching and electron-beam lithography [82]. Most charges can generally be eliminated by a low temperature anneal around 500°C [82]. The interface charges are located at the Si/SiO_2 interface and are caused by broken bonds at the surface [80]. These charges have also been called surface states, fast states and interface states, respectively. Most interface states can be annealed out by low temperature (450°C) annealing [82].

Since all four modelled charges are defined as an effective net charge at the Si/SiO_2 interface, their effects can be simplified using an effective net interface charge, Q_{IT}. For a p-type channel, positive oxide charges attract electrons and repel holes, helping

the formation of the channel. This in turn reduces the gate bias required for the same carrier concentration. Negative charges play an opposite role in the channel. Therefore, the influence of oxide charges can be modelled together with flat band voltage as:

$$V_{fb} \approx \psi_{ms} - Q_{IT}/C_{ox} \tag{3.3}$$

where Q_{IT} is the effective net interface charge and C_{ox} per unit area is the gate oxide capacitance, $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$. Here, ε_{ox} and t_{ox} are the gate oxide permittivity and the gate oxide thickness, respectively.

3.1.1.4 Electric potential and charge distribution in the silicon channel

To quantitatively study the gate control of the channel, the surface potential and charge can be derived using Poisson's equation. For a MOS capacitor or MOSFET with the Source/Drain grounded, the problem can be solved by a 1-dimensional equation:

$$\frac{d^2\psi}{dy^2} = -\frac{q}{\varepsilon_{Si}}\left[p(y) - n(y) + N_D^+(y) - N_A^-(y)\right] \tag{3.4}$$

where N_D^+ and N_A^- are the concentrations of ionised donors and acceptors, respectively. Here, ε_{Si} is the permittivity of silicon and ψ is defined as band bending in the silicon. At y position from the Si interface, $\psi(y)$ is $\psi_i(y) - \psi_i(\infty)$ and $\psi(y)$ is positive when the band bends downward.

The threshold voltage V_t is commonly defined as the gate bias when the strong inversion, $\psi_s = 2\psi_b$, is achieved. Thus, V_t is written from the Eq. (3.3) in expression of:

$$V_t = V_{fb} + 2\psi_b - \frac{Q_s}{C_{ox}} \tag{3.5}$$

At the onset of the strong inversion, the surface charge is mainly the depletion charge and Q_s, which is solved from Eq. (3.4) (detailed in Appendix A), can be written as:

$$Q_s \approx Q_d = \sqrt{2\varepsilon_{Si} q N_A (2\psi_b)} \tag{3.6}$$

where N_A is the acceptor concentration in the channel and ε_{Si} is the silicon permittivity. The expression for V_t can be obtained by substituting into Eq. (3.5) the expressions of

V_{fb} and Q_s, given in Eq. (3.3), Eq. (3.6), respectively:

$$V_t = \psi_{ms} - \frac{Q_{IT}}{C_{ox}} + 2\psi_b + \frac{\sqrt{4\varepsilon_{Si} q N_A \psi_b}}{C_{ox}} \tag{3.7}$$

where ψ_b is given in Eq. (3.1). The Eq. (3.7) shows that varying the substrate doping can change the threshold voltage. The threshold voltage can also be changed by varying gate oxide thickness and a thinner gate oxide leads to a lower voltage.

Using the expression for Q_d in Eq. (3.6), the depletion width W_d and the depletion capacitance C_d can be solved as:

$$W_d = \frac{-Q_d}{qN_A} = \sqrt{\frac{2\varepsilon_{Si}\psi_s}{qN_A}} \tag{3.8}$$

$$C_d = \frac{\varepsilon_{Si}}{W_d} = \sqrt{\frac{\varepsilon_{Si} q N_A}{2\psi_s}} \tag{3.9}$$

3.1.2 MOSFET I-V characteristics

3.1.2.1 MOSFET I-V model

In the former section, the MOSFET channel formation under a gate bias was detailed using a 1-dimensional model. For the current model, however, the drain bias influence should be taken into consideration in the 1-D MOSFET model, using the gradual channel approximation (GCA). In the GCA, it is assumed that the variation of the electrical field in the channel is mainly determined by the variation in the direction perpendicular to the channel [83]. In other words, the electric field variation in the channel is dominated by the gate bias and this assumption becomes not valid when the drain bias is beyond saturation (pinch-off) and in short channel transistors. In the following discussion, Source and Substrate contact are grounded and a long N-channel MOSFET is discussed. Under a positive drain bias, the channel is in a nonequilibrium condition, in which the electron quasi-Fermi level E_{Fn} is lowered from the equilibrium Fermi level and the hole quasi-Fermi level E_{Fp} remains at the bulk Fermi level in the bulk p-type silicon [84]. Therefore, the electron concentration under a nonequilibrium condition in

the channel is modified as:

$$n(x,y) = \frac{n_i^2}{N_A} \exp \frac{q\left(\psi(y) - V(x)\right)}{kT} \tag{3.10}$$

where V is the bias in the channel due to drain bias, which is in the direction of along the channel. At the Source end and Drain end of the channel, V is 0 and V_{ds}, respectively. Substituting Eq. (3.10) into the Poisson equation, the surface charge distribution can be solved as function of x, which is the distance along the channel from the Source end (x = 0) to Drain end (x = the channel length). From Eq. (3.10), the electron concentration near the drain side is lower than that near the source side.

To simplify the problem, the hole current and the generation and recombination current are ignored. Thus, the current is continuous along the x-direction. The electron current density including both drift and diffusion currents [82] is given by:

$$J_n = -q\mu_n(y)n(x,y)\frac{dV(x)}{dx} \tag{3.11}$$

By integrating J_n over the inversion depth, W_i, and along the channel, the drain current I_{ds} can be obtained as:

$$I_{ds} = \mu_{n,eff}\frac{W}{L}\int_0^{V_{ds}}\int_0^{W_i} qn(x,y)dydV = \mu_{n,eff}\frac{W}{L}\int_0^{V_{ds}} Q_i(V)dV \tag{3.12}$$

where W and L are the width and length of the channel, respectively. Here, $\mu_{n,eff}$ is the *effective electron mobility*, defined as:

$$\mu_{n,eff} = \frac{\int_0^{W_i}\mu_n(y)n(y)dy}{\int_0^{W_i} n(y)dy} \tag{3.13}$$

Due to scattering at the surface of the channel, the effective mobility is lower than the bulk mobility. For this reason, Si/SiO_2 interface quality and surface roughness are critical for transistor performance.

The general drain current is analytically solved using the charge-sheet approximation [85]; that is, all the inversion charges are located at the silicon surface like a sheet of charge and there is no potential drop or band bending across the inversion layer. After the onset of the strong inversion, the surface charge can also be written using Eq. (3.5) as:

$$Q_s = -C_{ox}\left(V_g - V_{fb} - \psi_s\right) \tag{3.14}$$

where the surface potential, ψ_s, is $\psi_s = 2\psi_b + V$. The inversion charge can be calculated from $Q_i = Q_s - Q_d$ using Eqs. (3.14) and (3.6). Substituting Eqs. (3.14) and (A.6) into Eq. (3.12), the drain current is:

$$\begin{aligned} I_{ds} &= \mu_{n,eff}\frac{W}{L}\int_0^{V_{ds}}(Q_s - Q_d) \\ &= \mu_{n,eff}\frac{W}{L}\{\left(V_g - V_{fb} - 2\psi_b - \frac{1}{2}V_{ds}\right)V_{ds} - \frac{2\sqrt{2\varepsilon_{Si}qN_A}}{3C_{ox}}\left[(2\psi_b + V_{ds})^{\frac{3}{2}} - (2\psi_b)^{\frac{3}{2}}\right]\} \end{aligned} \tag{3.15}$$

This equation describes the I-V characteristic of a MOSFET. It can be concluded that the current is proportional to the channel width, whilst the current is inversely proportional to the channel length.

3.1.2.2 Linear operation

When V_g is small ($V_{fb}<V_g<V_t$), gate voltage is not sufficient to create an inversion layer and there is only a depletion layer formed underneath the gate oxide (Fig. 3.5(a)). As no inversion layer is formed, there is no conduction channel between source and drain. Without taking the leakage current into account, the drain current, I_{ds}, is supposed to be zero. This operation is called the *cut-off* operation. When V_g is larger than V_t, an inversion layer is formed and thus the Source and Drain are connected by a conduction channel (Figs. 3.5(b) and (c)). When V_{ds} is small (Fig. 3.5(b)), the conduction the final term in Eq. (3.15) can be approximated as:

$$(2\psi_b + V_{ds})^{\frac{3}{2}} - (2\psi_b)^{\frac{3}{2}} \approx \frac{3}{2}(2\psi_b)^{\frac{3}{2}}V_{ds} \tag{3.16}$$

Using Eq. (3.16), drain current expression of Eq. (3.12) can then be simplified into:

$$I_{ds} = \mu_{n,eff}C_{ox}\frac{W}{L}\left[\left(V_g - V_{fb} - 2\psi_b - \frac{\sqrt{2\varepsilon_{Si}qN_A(2\psi_b)}}{C_{ox}} - \frac{1}{2}V_{ds}\right)V_{ds}\right] \tag{3.17}$$

By putting the expression of Eqs. (3.7) and (3.3) into Eq. (3.17), the drain current expression can be rewritten as:

$$I_{ds} = \mu_{n,eff}C_{ox}\frac{W}{L}\left(V_g - V_t - \frac{1}{2}V_{ds}\right)V_{ds} \tag{3.18}$$

This indicates that the drain current is proportional to the drain bias, as shown in Fig. 3.6, when the drain bias is small and this operation is referred to as *linear operation*.

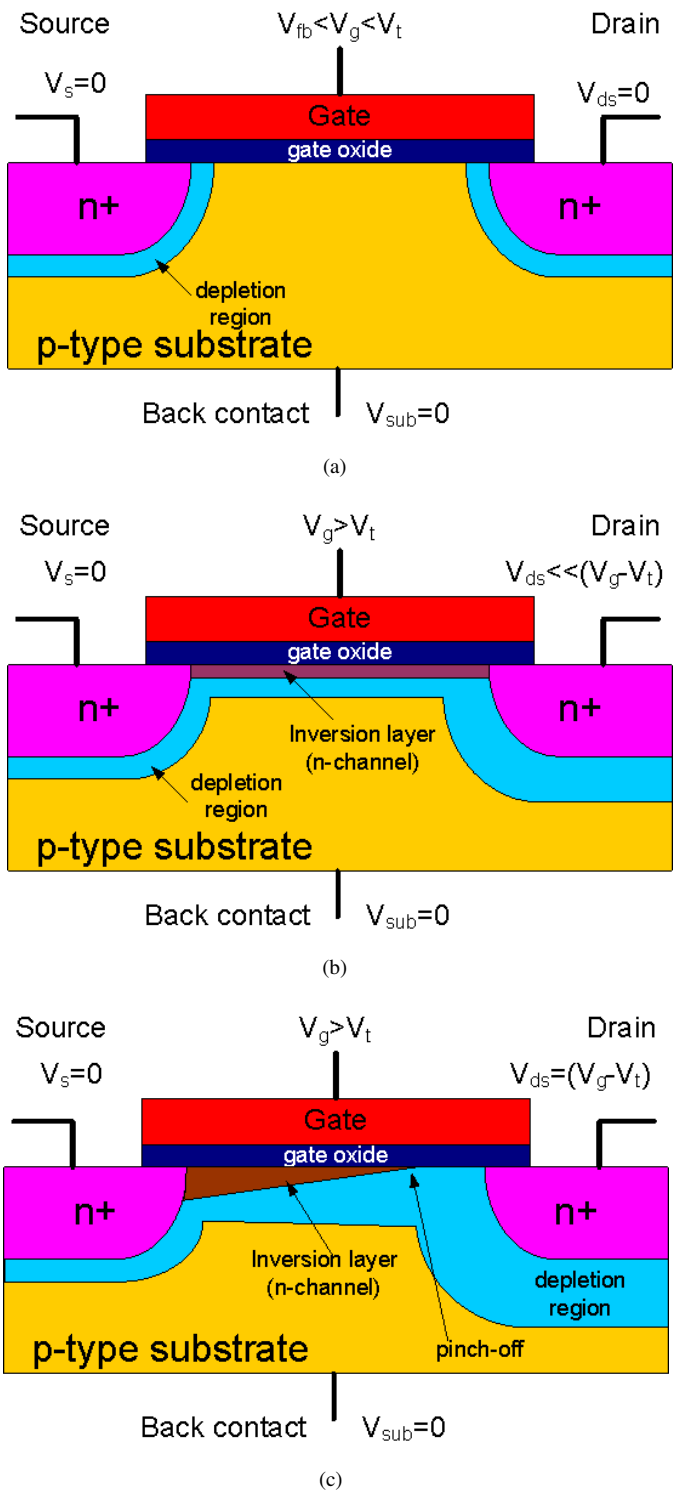


FIGURE 3.5: Schematics of MOSFET operated (a) in the cut-off region and (b) in the linear region and (c) at the onset of the saturation.

The channel acts like a resistor with the resistance modulated by the gate bias.

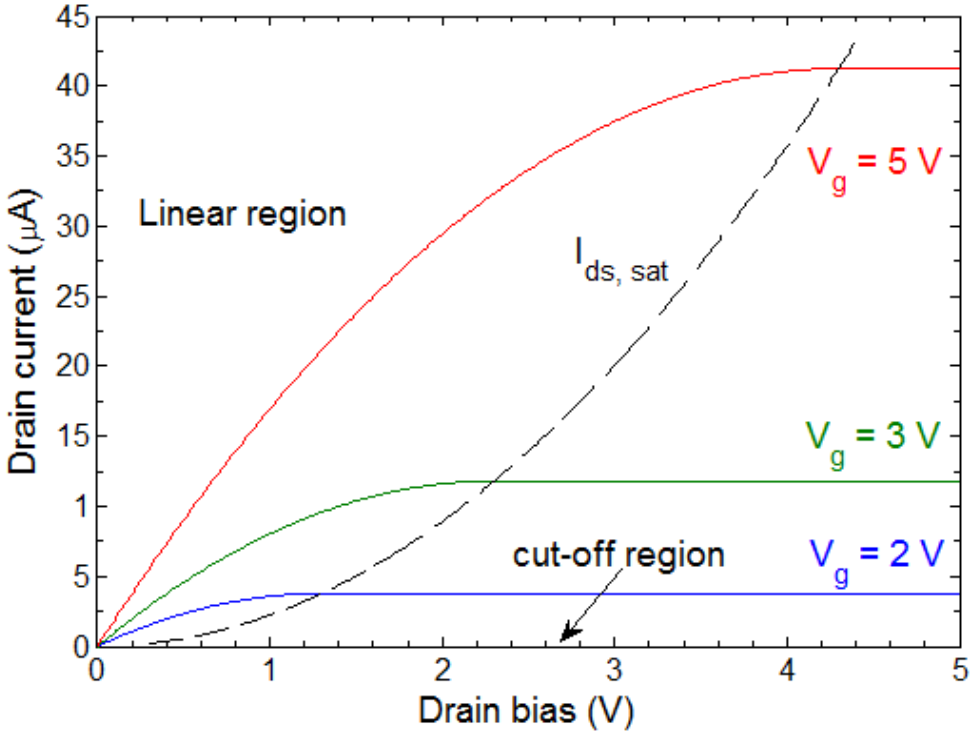


FIGURE 3.6: Idealised output characteristic of an n-type MOSFET with 10 μm channel length, 1 μm channel width and gate oxide thickness of 50 nm.

3.1.2.3 Saturation operation

When the drain bias increases and $V_{ds} = V_g - V_t$, the channel is pinched off, as shown in Fig. 3.5(c), and the drain current saturates. By putting the drain voltage at the onset of saturation, $V_{ds,sat} = V_g - V_t$ into Eq. (3.18), the drain current at saturation operation can be written as:

$$I_{ds,\mathrm{sat}} = \mu_{n,eff} C_{ox} \frac{W}{2L} (V_g - V_t)^2 \tag{3.19}$$

The drain current reaches the maximum value, $I_{ds,\mathrm{sat}}$, and stays constant as drain bias increases further as shown in Fig. 3.6.

3.1.2.4 Subthreshold operation

Besides the linear and saturation regions, another operation region is also discussed in this section. When the gate bias is slightly lower than V_t, that is, $\psi_b < \psi_s < 2\psi_b$, the channel is weakly inverted and hence the inversion charge density does not drop to zero abruptly. Therefore, the drain current in this region, named the *subthreshold current*, is non-negligible and is a critical characteristic for transistors operated at low-voltage for low power applications.

In the linear and saturation regions, the drift current, controlled by the drain source electric field, is the dominant part of the drain current. In the subthreshold region, the current is mainly due to diffusion. In the subthreshold region, the inversion charge is expressed as Eq. (A.9) and the subthreshold current is solved by putting the inversion charge expression into Eq. (3.12) as a function of surface potential, ψ_s as:

$$I_{ds} = \mu_{n,eff} \frac{W}{L} \sqrt{\frac{qN_A\varepsilon_{Si}}{2\psi_s}} \left(\frac{kT}{q}\right)^2 \left(\frac{n_i}{N_A}\right)^2 \exp\left(\frac{q\psi_s}{kT}\right) \left(1 - \exp\left(-\frac{qV_{ds}}{kT}\right)\right) \tag{3.20}$$

When V_{ds} is larger than $\frac{kT}{q}$, the last term containing V_{ds} can be ignored. The relation of ψ_s and gate bias, V_g, is given by considering only depletion charge:

$$V_g = V_{fb} + \psi_s + \frac{\sqrt{2\varepsilon_{Si}qN_A\psi_s}}{C_{ox}} \tag{3.21}$$

This is a similar form of expression as the threshold voltage. Here we consider ψ_s is only slightly deviated from $2\psi_b$, and thus assume $|\psi_s - 2\psi_b| \ll 2\psi_b$. Using a Taylor series, $\sqrt{\psi_s}$ and ψ_s in Eq. (3.21) can be expanded into:

$$\sqrt{\psi_s} \approx \sqrt{2\psi_b} + \frac{1}{2}(2\psi_b)^{-\frac{1}{2}}(\psi_s - 2\psi_b) \tag{3.22}$$

$$\psi_s \approx 2\psi_b + (\psi_s - 2\psi_b) \tag{3.23}$$

Substituting these two expressions into Eq. (3.21):

$$\begin{aligned} V_g &= V_{fb} + 2\psi_b + \frac{\sqrt{2\varepsilon_{Si}qN_A\,(2\psi_b)}}{C_{ox}} + \left(1 + \frac{\sqrt{\varepsilon_{Si}qN_A/(4\psi_b)}}{C_{ox}}\right)(\psi_s - 2\psi_b) \\ &= V_t + m\,(\psi_s - 2\psi_b) \end{aligned} \tag{3.24}$$

where m is defined as the *body-effect coefficient*, given as:

$$m = 1 + \frac{\sqrt{\varepsilon_{Si} q N_A / 4\psi_b}}{C_{ox}} = 1 + \frac{C_d}{C_{ox}} \approx 1 + \frac{3t_{ox}}{W_d} \tag{3.25}$$

By putting Eq. (3.25) into Eq. (3.20), the subthreshold current can be easily solved as:

$$I_{ds} = \mu_{n,eff} \frac{W}{L} \sqrt{\frac{q N_A \varepsilon_{Si}}{4\psi_b}} \left(\frac{kT}{q}\right)^2 \exp \frac{q\,(V_g - V_t)}{mkT} \tag{3.26}$$

This expression indicates that the subthreshold current varies exponentially with gate bias. Thus, a graph of $\log(I_{ds})$ against V_g is linear in the subthreshold region, as shown in Fig. 3.7. It is noted that a steeper subthreshold slope (SS) means that the transistor can be turned on using a lower voltage and the leakage current is lower when the transistor is switched off. The threshold voltage can be extracted from the subthreshold plot curve as shown in Fig. 3.7. The subthreshold slope value is defined as:

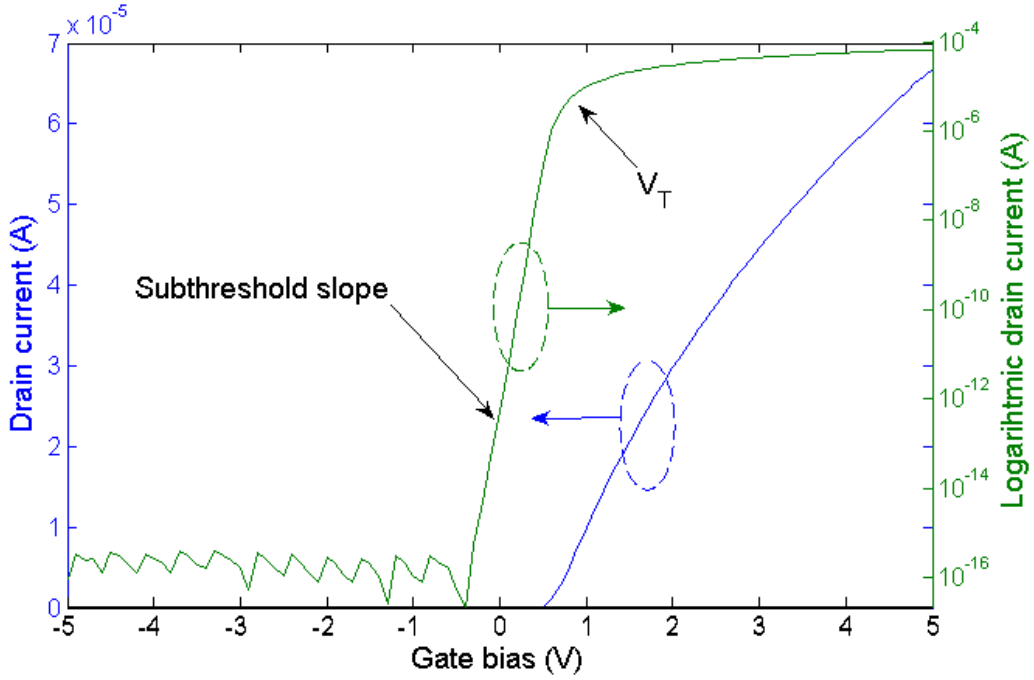


FIGURE 3.7: The I_{ds}-V_{gs} curve plotted on linear and logarithmic scales of I_{ds} [86].

$$SS = \left(\frac{d(\log_{10} I_{ds})}{dV_{ds}}\right)^{-1} = \ln 10 \frac{mkT}{q} = 2.3 \frac{kT}{q} \left(\frac{C_{ox} + C_d}{C_{ox}}\right) \tag{3.27}$$

where the expression for m is given in Eq. (3.25). When $C_d \ll C_{ox}$, SS reaches a theoretical limit, which is 60 mV/decade. Since C_d depends on the channel doping,

N_A, SS is degraded when the channel doping increases. Taking into consideration of the influence of charges in the oxide and at the Si/SiO_2 interface (in Fig. 3.4), SS can be written as:

$$SS = 2.3\frac{kT}{q}\left(\frac{C_{ox} + C_d + C_{it}}{C_{ox}}\right) \tag{3.28}$$

where C_{it} is the capacitance due to charges in the oxide and at the Si/SiO_2 interface. Thus, the SS is degraded by the charges in the oxide and at the Si/SiO_2 interface.

3.2 Polysilicon Thin Film Transistors (Seto's Model)

For a polycrystalline silicon channel, the poly-Si can be considered as crystalline grains with random orientations connected by grain boundaries. Inside each grain, the atoms are arranged in a periodic manner and thus can be considered as single crystal. The grain boundaries have a strong effect on the electrical properties of polysilicon thin film transistors.

To explain the role of grain boundaries, Seto [87] modelled grain boundaries using a trapping model and the proposed model is used to study the carrier mobility and conduction in polysilicon films. In the grain boundary region, it is believed that the disordered atoms result in a large number of defects due to incomplete atomic bonding, which leads to the formation of trapping states [88]. The trapping states have the capability to trap and immobilise the carriers and thus reduce the number of carriers available for conduction. The trapped carriers accumulated at the grain boundaries create an electrostatic potential and this potential works as an energy barrier to impede the movement of carriers.

In Seto's model, only majority carriers are considered and dopant atoms are assumed to be fully ionised and uniformly distributed at a concentration of N. Furthermore, the grain boundary is assumed to be negligibly thin, which is consistent with the measured value of 1 nm obtained from TEM. In addition, the trapping states are assumed to be mono-energetic with a concentration of N_t cm^{-2}. The modelled grain boundary for an n-type channel is illustrated in Fig. 3.8(a). The trapped charges bend the energy bands and deplete the grain near the grain boundary (Fig. 3.8(b)), so that there is an energy band peak at the grain boundary (Fig. 3.8(c)), working as an electron barrier for the conduction. Using Poisson's equation, the potential height can be solved for two cases [87]: (a) $N_t > L_g N$ and (b) $N_t < L_g N$.

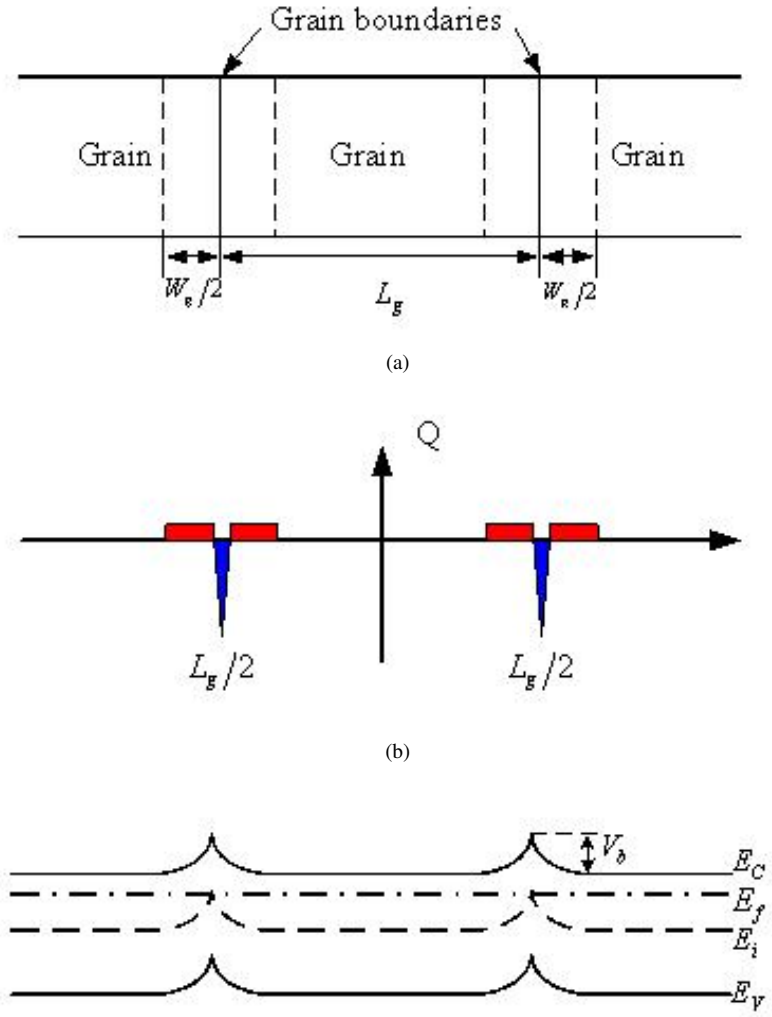


FIGURE 3.8: Seto's model of a polysilicon channel (a) the polysilicon film, (b) the charge distribution in the grain and at the grain boundaries and (c) the energy band structure for the poly-Si film in (a).

For the case of $N_t > L_g N$, the grain is fully depleted and the traps are partially filled. The barrier height, V_b can be solved as [87][89]:

$$\mathrm{V}_b = \frac{qL_g^2 N}{8\varepsilon_{Si}} \tag{3.29}$$

For the case of $N_t < L_g N$, the grain is partially depleted and the traps are fully filled. The potential barrier height then becomes [87][89]:

$$V_b = \frac{qN_t^2}{8N\varepsilon_{Si}} \tag{3.30}$$

Using Eq. (3.29) and Eq. (3.30), the potential barrier height against dopant concentration is plotted in Fig. 3.9 As the dopant concentration increases, the energy barrier

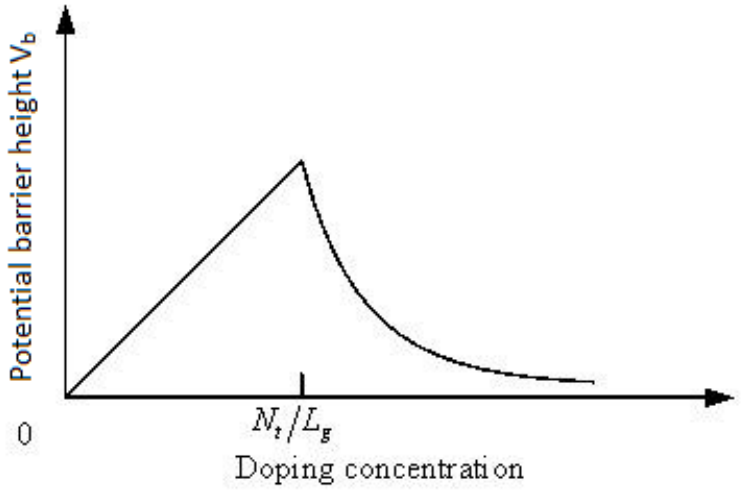


FIGURE 3.9: The relation of the potential and dopant concentration by Seto's model.

height firstly increases linearly, reaching a maximum at $N = {}^{N_t}/_{L_g}$, and then decreases rapidly as $1/N$. The dopant concentration of $N = {}^{N_t}/_{L_g}$ is defined to be the critical concentration.

The effect of the grain boundaries can be taken into account by defining an effective electron mobility [87] [90]:

$$\mu_{ps,n,eff} = \mu_{n,eff} \exp\left(-\frac{qV_b}{kT}\right) \tag{3.31}$$

where $\mu_{n,eff}$ is the effective electron mobility inside the grain and V_b can be calculated from Eq. (3.29) or Eq. (3.30) depending on that the grains are fully depleted and partially depleted. For a highly doped junctionless transistor, the carrier concentration is mainly depended on the channel doping. The Eq. (3.31) shows the mobility is decreased due to grain boundary and thus lower than the mobility for single-crystal silicon. The mobility due to grain boundary at different dopant concentration is illustrated in Fig. 3.10. As the dopant concentration increases up to 1×10^{18} cm^{-3}, the mobility decreases significantly. Above 1×10^{18} cm^{-3}, the mobility increases with the dopant concentration. Comparing Fig. 3.10 with Fig. 3.9, the valley trend of the mobility curve is correlated with the grain boundary height due to dopant concentration.

The drain current of a long-channel thin film transistor at the linear operation is then

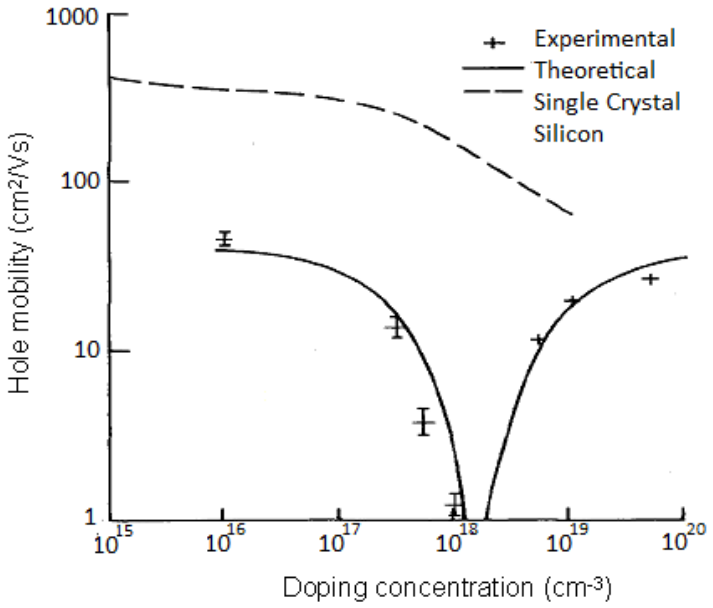


FIGURE 3.10: The hole mobility as a function of dopant concentration from experimental and theoretical results. After Seto [87], copyright AIP.

given by [91]:

$$I_{ds} \approx \mu_{n,eff} \exp\left(-\frac{qV_b}{kT}\right) C_{ox} \frac{W}{L} \left(V_g - V_t - \frac{1}{2}V_{ds}\right) V_{ds} \tag{3.32}$$

The effective mobility in Eq. (3.32) is from μ_{ps} in Eq. (3.31). To add the effect of the trap states in polysilicon, SS is expressed by modifying Eq. (3.28) with an extra term as [92]:

$$SS = 2.3\frac{kT}{q}\left(\frac{C_{ox} + C_d + C_{it} + qN_T}{C_{ox}}\right) \tag{3.33}$$

where N_T is effective trap state density per unit area per eV. Eq. (3.33) shows that SS for polysilicon thin film transistor is higher than for single-crystal silicon MOSFET.

3.3 Raman Analysis of Si Crystallinity

Raman spectroscopy is a common tool used in chemistry to investigate vibrational information about the symmetry of molecules [93]. When monochromic light, hv_0, normally a laser beam, interacts with the electron cloud of a sample, scattering processes occur and can be classified by the emitted light, as shown in Fig. 3.11. When the emitted light has the same frequency as the incident light, it is an elastic scattering process, i.e., a

Rayleigh process, which has the highest probability [93]. When the emitted light has a lower frequency ($\upsilon<\upsilon_0$), it is an inelastic scattering process and is called Stokes Raman scattering. If the emitted light has a higher frequency ($\upsilon>\upsilon_0$), the scattering process is again inelastic, and is called anti-Stokes Raman scattering. Due to a higher intensity of Stokes Raman lines than anti-Stokes Raman lines, only Stokes Raman lines are normally recorded in Raman spectra [93]. The emitted light frequency shift (Raman shift) is typically expressed in wavenumbers, which is in units of inverse length (cm^{-1}). The Raman spectrum is then formed by plotting the measured intensity as a function of the Raman shift. The resulting Raman results can be used to interpret the structure of the material.

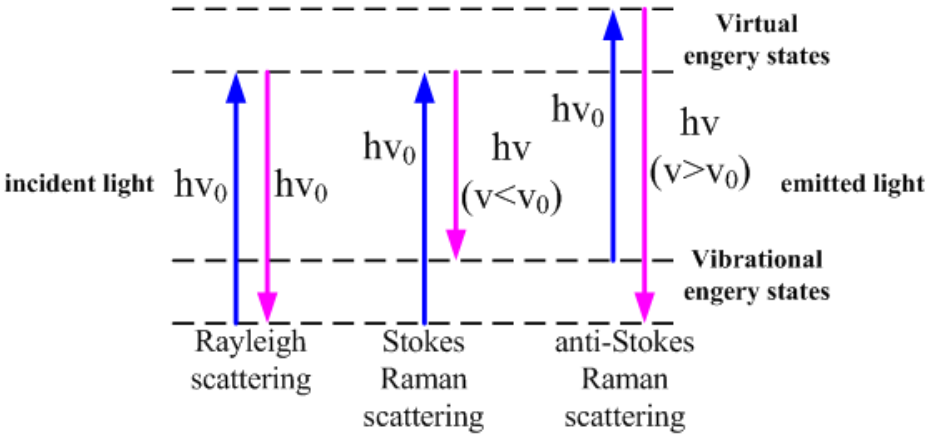


FIGURE 3.11: Schematic diagram of different scattering mechanisms observed when an incident light interacts with a sample.

Raman spectroscopy is an effective tool for Si crystallinity analysis [94][95]. Fig. 3.12 shows the Raman spectra for large-grain polycrystalline silicon (a), small-grain polycrystalline silicon (b) and amorphous silicon (c). For (b) in Fig. 3.12, two peaks can be identified at ≈480 cm^{-1} and ≈520 cm^{-1}, whereas, for (a) and (c), only one main peak is identified at ≈520 cm^{-1} and ≈480 cm^{-1}, respectively. The Raman shift peak at about 520 cm^{-1} is due to crystalline Si, whilst the Raman shift at about 480 cm^{-1} is due to amorphous Si [96]. Thus, the silicon crystallinity can be identified from the Raman peaks at 480 cm^{-1} and 520 cm^{-1}.

To compare the crystallinities of polysilicon films, Raman spectra are normally plotted in normalised intensity [97][98][99], which is the Raman intensity at a given Raman shift divided by the Raman intensity at around 520 cm^{-1} peak. Fig. 3.13 shows normalised Raman spectra for two poly-Si films. The Si crystallinity can be qualitatively assessed from the sharpness of 520 cm^{-1} peak, which can be quantified by measuring

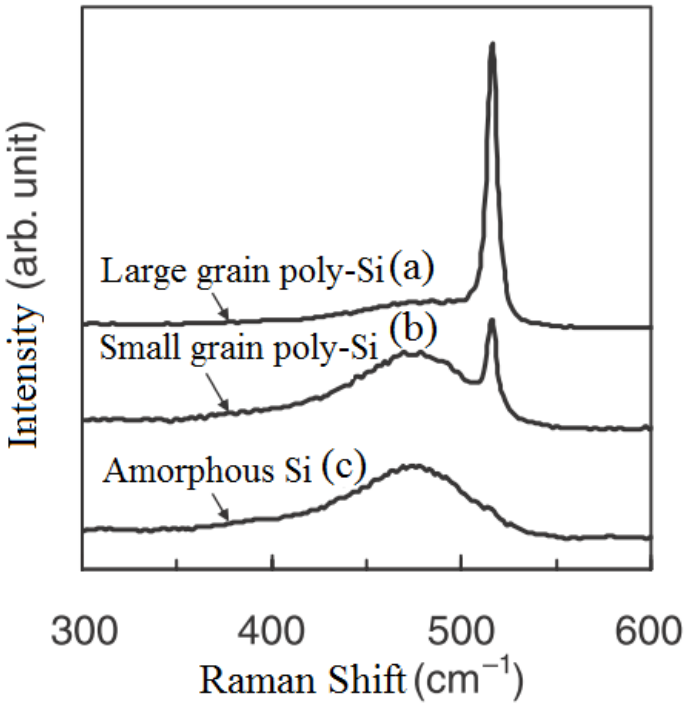


FIGURE 3.12: Raman spectra of large grain polysilicon (a), small grain polysilicon (b) and amorphous silicon (c). After Kitahara *et al* [96], copyright JJAP

the full-width at half-maximum (FWHM) [100]. A smaller value of FWHM shows a higher Si crystallinity, so poly-Si (b) is more crystalline than poly-Si (a).

To further analyse the Si crystallinity, a peak-fitting technique is used to study amorphous and crystalline fractions of the Raman spectra, as shown in Fig. 3.14. The contributions of amorphous (I_a) and crystalline silicon (I_p) are expressed in the areas of the fitted Gaussian curves and thus the crystalline fraction can be defined as [38]:

$$\chi = \frac{I_p}{I_p + yI_a} \tag{3.34}$$

where I_p and I_a are the areas of the fitted Gaussian curves of crystalline silicon and amorphous silicon, respectively, and y is the ratio of the scattering cross sections. Here, y has been reported to vary with grain size and is 0.88 for small grain size [94].

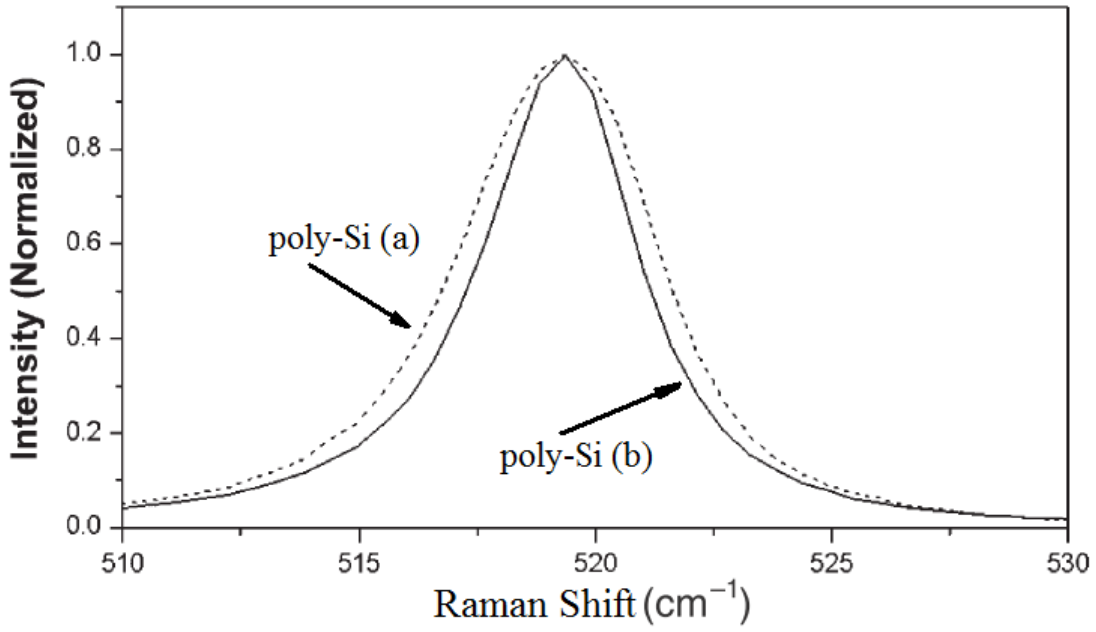


FIGURE 3.13: Normalised Raman spectra of two polysilicon films. The Raman intensity at a given Raman shift has been normalised to the Raman intensity at around 520 cm^{-1}. After Hu *et al* [54], copyright IEEE

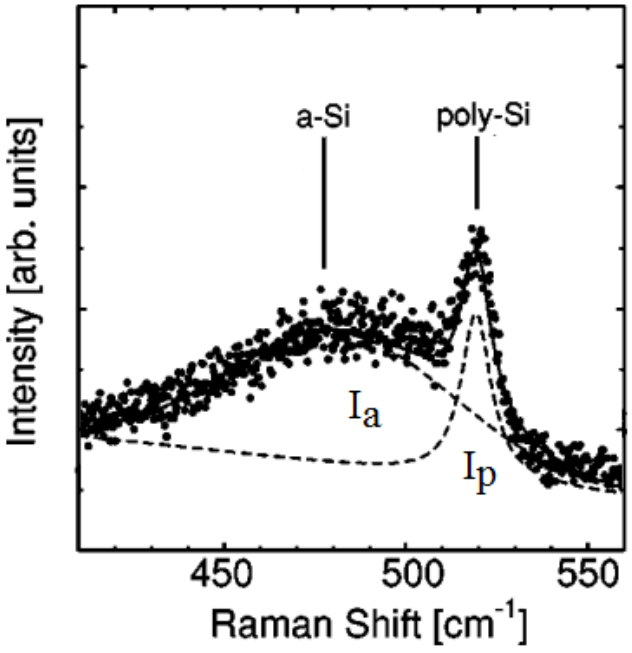


FIGURE 3.14: Raman spectra of polysilicon with two fitted Gaussian curves at peaks of 480 cm^{-1} and 520 cm^{-1}. After Kimura *et al* [38], copyright AIP

Chapter 4

Effect of Fluorine Dose on Amorphous Silicon Metal-induced Lateral Crystallisation

4.1 Introduction

In Chapter 2, it was shown that most Si nanowire biosensors are fabricated by top-down e-beam lithography on Silicon-on-Insulator (SOI) wafers [8][15]. However, current top-down fabrication techniques are high cost and cannot satisfy the requirement for low-cost disposable biosensors. Recrystallised polysilicon by thin-film technology is proposed as an alternative solution for biosensor fabrication, which could lead to a significant cost reduction, particularly if glass substrates are used. However, glass substrates require a process temperature below 450°C to avoid substrate shrinkage and warpage [21][22][23]. Therefore, this requires a lower anneal temperature for metal-induced lateral crystallisation (MILC), which is typically at 550°C [29][53]. However, no work has been reported on MILC at temperatures below 500°C.

Fluorine has been reported to give an increase in MILC length [31] and to improve poly-Si thin film transistor performance by passivation effects from fluorine implantation [26] [101] and CF_4 plasma treatment [102]. Therefore, these earlier researches provide a motivation for studying the influence of the fluorine implantation dose on MILC growth at different temperatures. MILC growth at temperatures below 550°C is of particular interest for nanowire biosensor applications.

4.2 Experimental Procedure

4.2.1 Sample preparation

The process flow for the fluorine implanted samples in this work is shown in Fig. 4.1. The sample fabrication up to and including Ni deposition was done in the KTH clean-

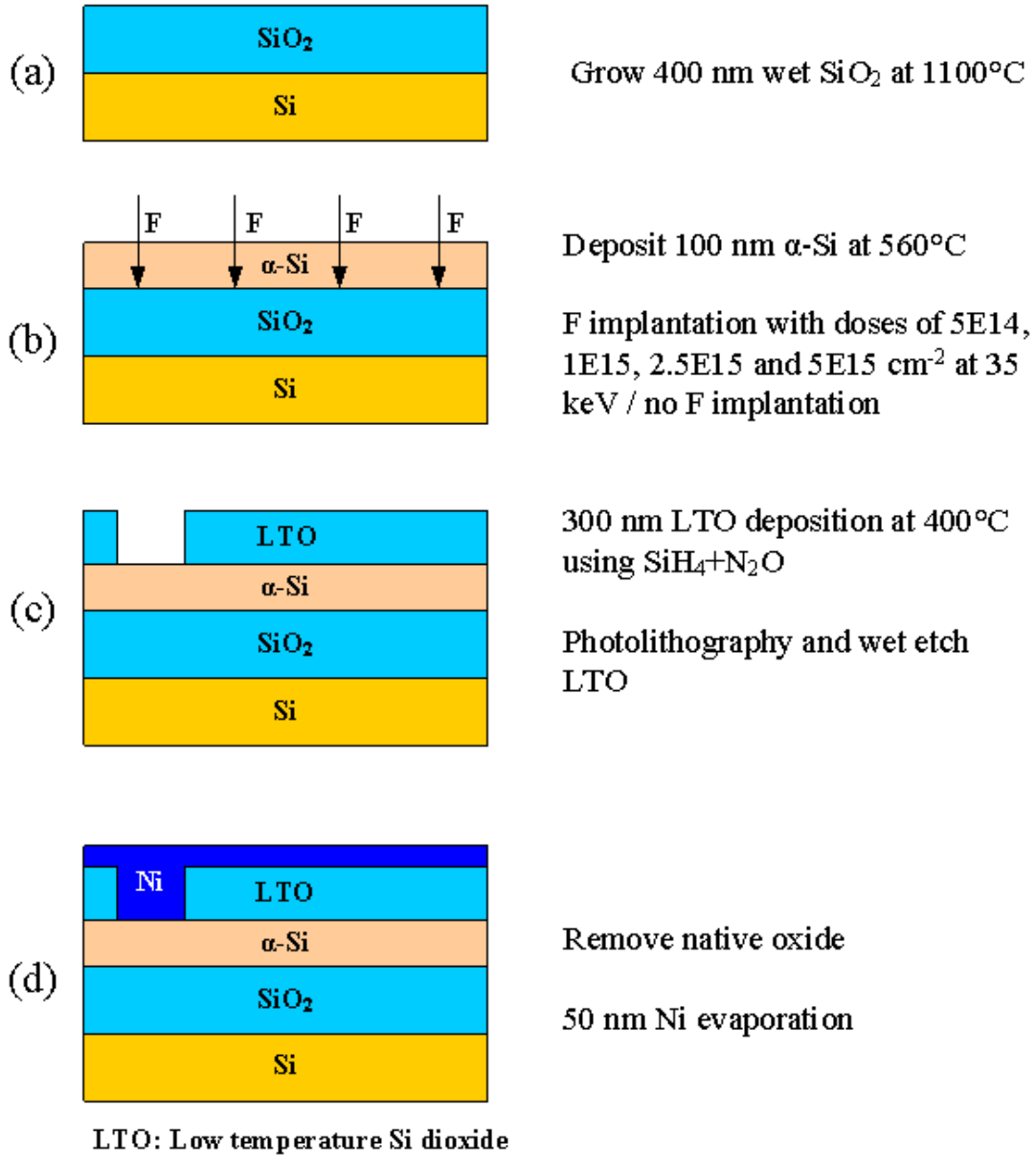


FIGURE 4.1: Process flow for the fabrication of the fluorine implanted samples.

room in Sweden by M. M. A. Hakim, as the Southampton cleanroom was not fully op-

erational after the fire. The furnace anneal and lateral crystallisation experiments were done by the author in the new Southampton Nanofabrication Centre cleanroom. Five p-type <100> oriented Si wafers were cleaned and a 400 nm thermal silicon dioxide was grown by a wet oxidation at 1100°C (Fig. 4.1(a)). Subsequently, a 100 nm undoped amorphous silicon (α-Si) layer was deposited by low pressure chemical vapor deposition (LPCVD) at 560°C. Then, a fluorine implantation was performed at 35 keV with various doses of 5×10^{14} cm^{-2}, 1×10^{15} cm^{-2}, 2.5×10^{15} cm^{-2} and 5×10^{15} cm^{-2} into four wafers (Fig. 4.1(b)). No fluorine implantation was given to the last wafer, which is the control. After a 300 nm low temperature oxide (LTO) was deposited at 400°C using SiH_4 and N_2O, windows were opened in the LTO using photolithography and a wet etch was performed (Fig. 4.1(c)). Immediately after removing the native oxide on top of the α-Si surface by buffered hydrofluoric acid (HF), a 50 nm nickel layer was evaporated (Fig. 4.1(d)). The samples were then cleaved and all samples were furnace annealed at different temperatures between 428°C and 575°C for 3-40 hours in nitrogen. The samples were loaded into the furnace at 400°C and the temperature was then ramped up at 2°C/min. A cross-section view of a typical fabricated sample is shown in Fig. 4.2. The thickness values shown in Fig. 4.2 are mean values of at least 5 measurements on each of the five wafers.

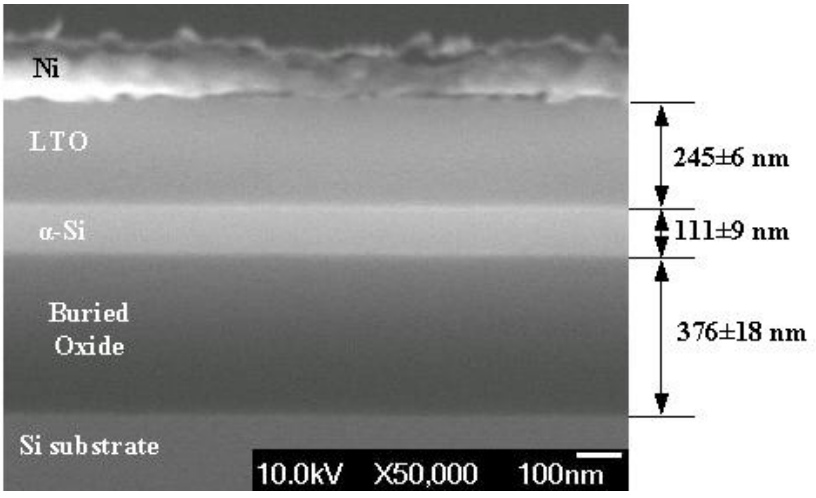


FIGURE 4.2: Cross-section SEM micrograph of a sample fabricated for the fluorine effect experiment. The process flow is shown in Fig. 4.1

4.2.2 SIMS characterisation

In this work, fluorine profiles in the implanted Si samples were studied using Secondary Ion Mass Spectrometry (SIMS), which was carried out by Loughborough Surface Analysis, Ltd. The measured raw data were calibrated and analysed by the author. Fig. 4.3 shows a graph of the measured fluorine intensity in counts as a function of the sputter time for samples with: (a) fluorine implanted into SiO_2 and (b) fluorine implanted into α-Si on top of SiO_2. For F into α-Si, there are two measured curves from two sputtering runs stopped at different times. For both samples, fluorine was implanted at a dose of 2.5×10^{15} cm^{-2}, an energy of 35 keV and a tilt angle of 7° and no anneal was performed. For the F implanted into SiO_2, a main peak can be identified at a sputter time of 170 seconds. However, for the F implanted into α-Si on the SiO_2, two peaks are seen at sputter times of 450 seconds and 605 seconds. The depths of the sputtered craters for F into SiO_2 and α-Si were measured to be 420 nm (shorter time) and 107 nm (one aqua colour), respectively, using a profiler by Dave Sykes at Loughborough Surface Analysis, Ltd. Thus, the SIMS curve in aqua colour stops in the α-Si film. The

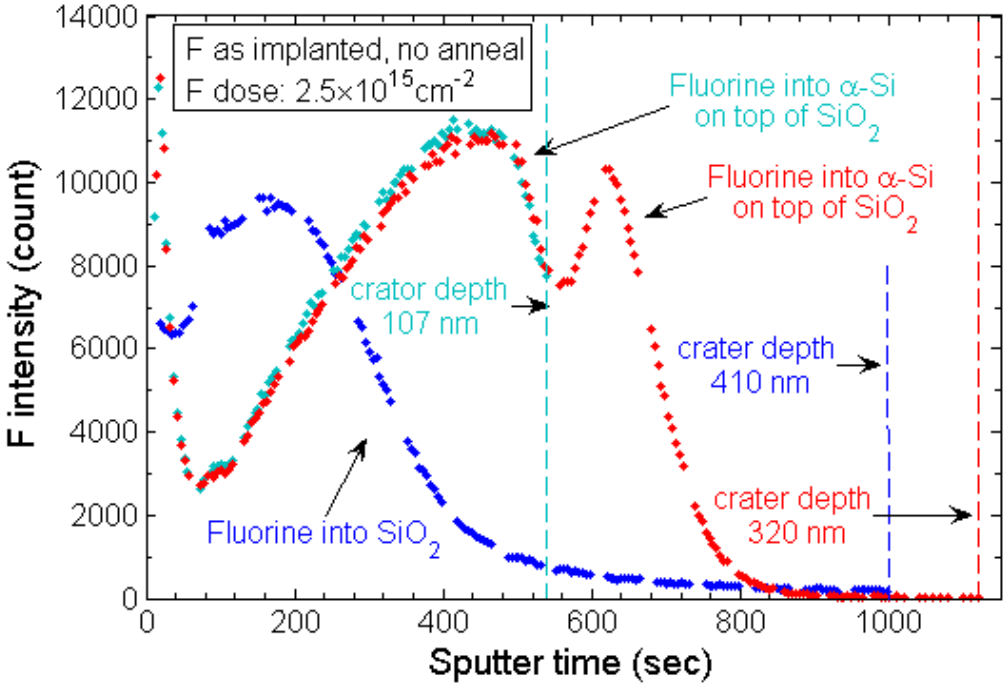


FIGURE 4.3: SIMS raw data for a F implant into SiO_2 and α-Si on SiO_2 with dose of 2.5×10^{15} cm^{-3}, an energy of 35 keV and a tilt angle of 7°. No anneal was given to both samples after the F implantation.

sputter rate of the SiO_2 can be extracted to be 4.2 Å/second from the sputter time and

the crater depth. Using the same method, the sputter rate of the α-Si film is extracted to be 2.1 Å/second from the sputter time of 504 seconds and the measured crater depth of 107 nm. Using these two extracted rates, the total crater depth for the SIMS curve in red colour is calculated to be 330.5 nm for a sputter time of 1124 seconds and this well matches the measured value of 320 nm obtained from the profiler. Using the calculated sputter rates, the depth of the peak at 605 seconds for F implant into α-Si on SiO_2 is calculated to be about 122 nm and this roughly matches the 113 nm α-Si thickness measured by SEM.

For F implanted into SiO_2, the fluorine concentration, F_{con}, is written as:

$$F_{con} = \frac{F_{dose}}{\int_0^{depth} F_{\text{int}}(x)dx} F_{\text{int}} = S_{ox} F_{\text{int}} \tag{4.1}$$

where F_{dose} is the fluorine implant dose, which is measured by the ion implanter, $depth$ is the crater depth of the SIMS measurement, which includes most fluorine, F_{int} is the measured fluorine intensity by SIMS and S_{ox} is defined as the conversion rate for SiO_2. S_{ox} is a constant and was calculated to be 1.99×10^{16} cm^{-3} per count. For F implanted into α-Si on SiO_2, the fluorine concentration in the α-Si film, F_{con}, is written as:

$$F_{con} = \frac{F_{dose} - S_{ox}\int_{t_{Si}}^{depth} F_{\text{int}}(x)dx}{\int_0^{t_{Si}} F_{\text{int}}(y)dy} F_{\text{int}} = S_{Si} F_{\text{int}} \tag{4.2}$$

where t_{Si} is the α-Si thickness and S_{Si} is the conversion rate for α-Si. For the extraction of S_{Si}, data points at depths less than 20 nm are neglected as SIMS results are not valid near the surface [103]. Then, S_{Si} is calculated to be 2.09×10^{16} cm^{-3} per count.

Using the calculated S_{Si} and S_{ox} and the extracted sputter rates above, fluorine concentration profiles can be calculated as a function of depth, as shown in Fig. 4.4. The F profiles from a simulator are also presented for comparison. For the F implant into SiO_2 (Fig. 4.4(a)), a discrepancy can be seen between the simulated profile and the calibrated profile. The measured peak fluorine concentration is about 1.9×10^{20} cm^{-3}, compared with a simulated value of 3.5×10^{20} cm^{-3}. For the F implant into α-Si on SiO_2 (Fig. 4.4(b)), a similar discrepancy can be seen between the simulation and the calibrated SIMS results. The peak fluorine concentration in the α-Si is measured to be 2.3×10^{20} cm^{-3}, compared with 3.1×10^{20} cm^{-3} for the simulation. Both of these discrepancies could be explained if there was some movement of the fluorine during the implantation due to wafer heating. There was some variation in the sputter rates for SIMS runs done on different days. The above procedure was therefore used for sputter rates measured

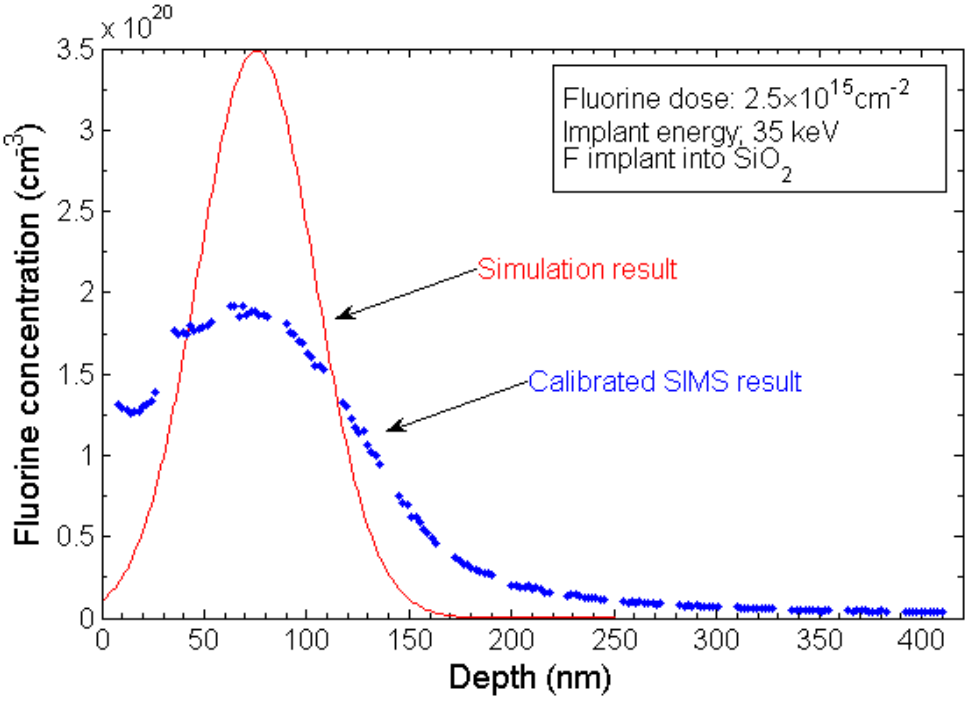
on the day of the SIMS measurement.

4.2.3 MILC characterisation

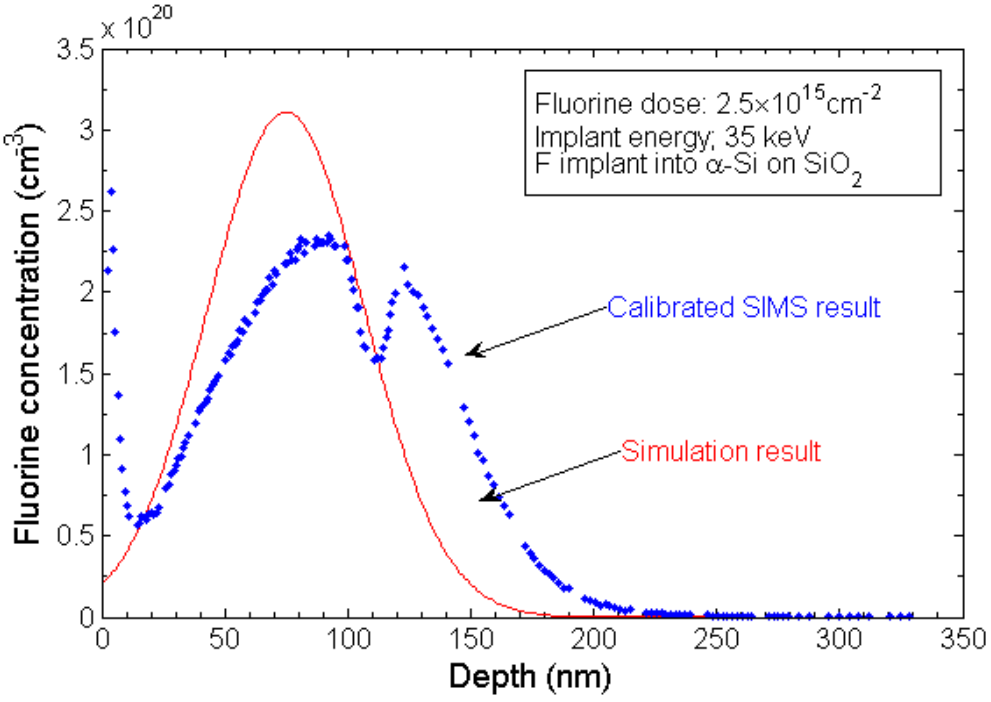
In this work, several techniques were used for MILC length measurements, including Raman spectroscopy, Nomarski optical microscope and field emission scanning electron microscope (FE-SEM). The Raman spectroscopy was performed using a Renishaw inVia laser Raman spectrometer, which is configured with three laser lines of 532 nm, 633 nm and 785 nm. In this work, a green 532 nm laser was initially used and later a 633 nm laser was used instead for measurements in which the laser spot was focused onto the region of interest. To eliminate the influence of the coated Ni layer and the oxide cap, samples were first rinsed in 20:1 buffered hydrofluoric acid (HF) for 6 minutes prior to the Raman measurements to remove the two capping layers on the silicon. By using an optical microscope integrated in the Raman system, the laser spot can be well controlled to focus on a specific location on the sample and hence spot measurements could be performed. By defining a square region on the sample in the Raman operational software, mapping Raman measurements can be performed by serially scanning the selected region spot by spot as pixels the resulting measurement results were then plotted in a two dimensional plot.

The MILC measurements by Nomarski optical microscope were performed with a Nikon Ellipse camera with a 5 megapixel resolution. Photographs can be captured using the Nikon software, Element, during the measurement. The MILC length was measured using the Nikon software. For Nomarski microscope measurements, samples were prepared either with or without a delineation etch in 7:1 buffered HF for 20 minutes. The etchant delineates the lateral crystallisation region by selectively etching the amorphous silicon and nickel disilicide ($NiSi_2$) in the MILC region [31].

SEM observations were made on a JEOL 6500F FE-SEM. For plan view SEM micrographs, an electron acceleration energy of 5 keV was used as a trade-off between resolution and surface charging. The working distance was set to about 10 mm, which gave an enough space to avoid a collision between the mounted sample and the electron tube. In SEM measurements of the MILC length, samples were first delineated in 7:1 buffered HF for 20 minutes [31] to improve the contrast.



(a)

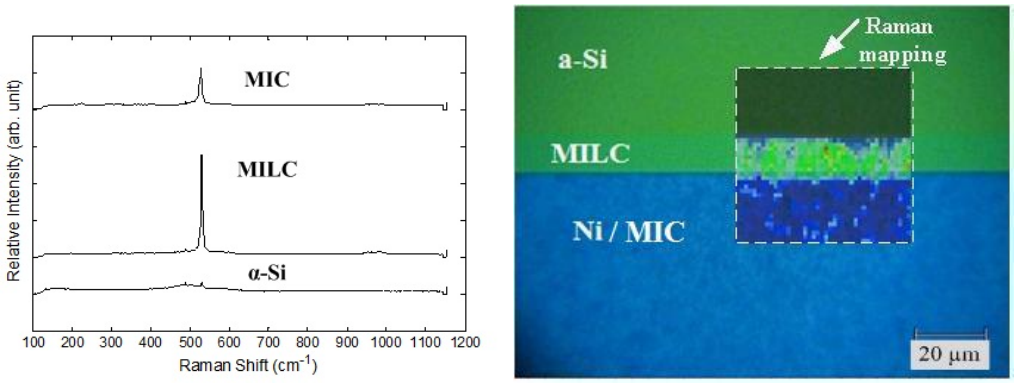


(b)

FIGURE 4.4: Calibrated fluorine concentration profiles for (a) a F implant into SiO_2 and (b) a F implant into α-Si on SiO_2. The fluorine concentration and depth were calculated from the SIMS results shown in Fig. 4.3

4.2.4 Validation of MILC characterisation techniques

In this work, the different techniques for lateral crystallisation measurement length are presented and validated. Fig. 4.5(a) shows Raman spectroscopy results measured on an annealed unimplanted (no F implant) sample. The spectra were measured in the following regions: (a) the MIC region below the Ni, (b) the MILC region and (c) the amorphous silicon (α-Si) region. In the α-Si region, a small broad peak is obtained at a Raman shift of 479 cm^{-1}, in the MILC region, a large and sharp peak is seen at a Raman shift of 521 cm^{-2}, and in the MIC region a small sharp peak is seen at a Raman shift of 521 cm^{-1}. As discussed in Chapter 2, these results can be explained by different silicon crystal structures in the three regions. A broad peak at a Raman shift around 480 cm^{-2} is indicative of the presence of amorphous Si, whereas a sharp peak at a Raman shift around 520 cm^{-1} is indicative of crystalline or polycrystalline Si [104].



(a) (b)

FIGURE 4.5: (a) Raman spectra measured at three different regions for an annealed unimplanted sample after removing the nickel and LTO and (b) Plan-view map of Raman shift at 520 cm^{-1} for an annealed unimplanted sample.

The MILC region can be identified by mapping the Raman shift at 520 cm^{-1}, as shown in Fig. 4.5(b). The relative intensity is indicated by rainbow colours and the bright green region at the centre of Fig. 4.5(b) represents the higher intensities. The length of the MILC region can be measured as 12.3 μm. The MILC region can also be identified from the optical image as a slightly different shade of green. A MILC length of 11.1 μm can be measured from this image, which is in reasonable agreement with the value from the Raman map, given the Raman laser spot size of 1 μm.

Fig. 4.6(a) shows an optical Nomarski micrograph of the same annealed unimplanted MILC sample. The MILC region can be much more clearly identified than in the optical image in Fig. 4.5(b) and the measured MILC length is 11.7 μm. For comparison, Fig.

4.6(b) shows an optical Nomarski image of the same sample after a 20 minute delineation etch in 7:1 buffered HF. The lateral crystallisation region can again be clearly identified by a strong colour change and the MILC length can be measured as 12.2 μm. The black line located at the interface between the MILC region and the amorphous Si is formed from etched holes of nickel disilicide precipitates. Finally, Fig. 4.6(c) shows plan-view FE-SEM micrograph of the sample after a delineation etch. The MILC region can again be clearly identified and the MILC length measured as 11.8 μm.

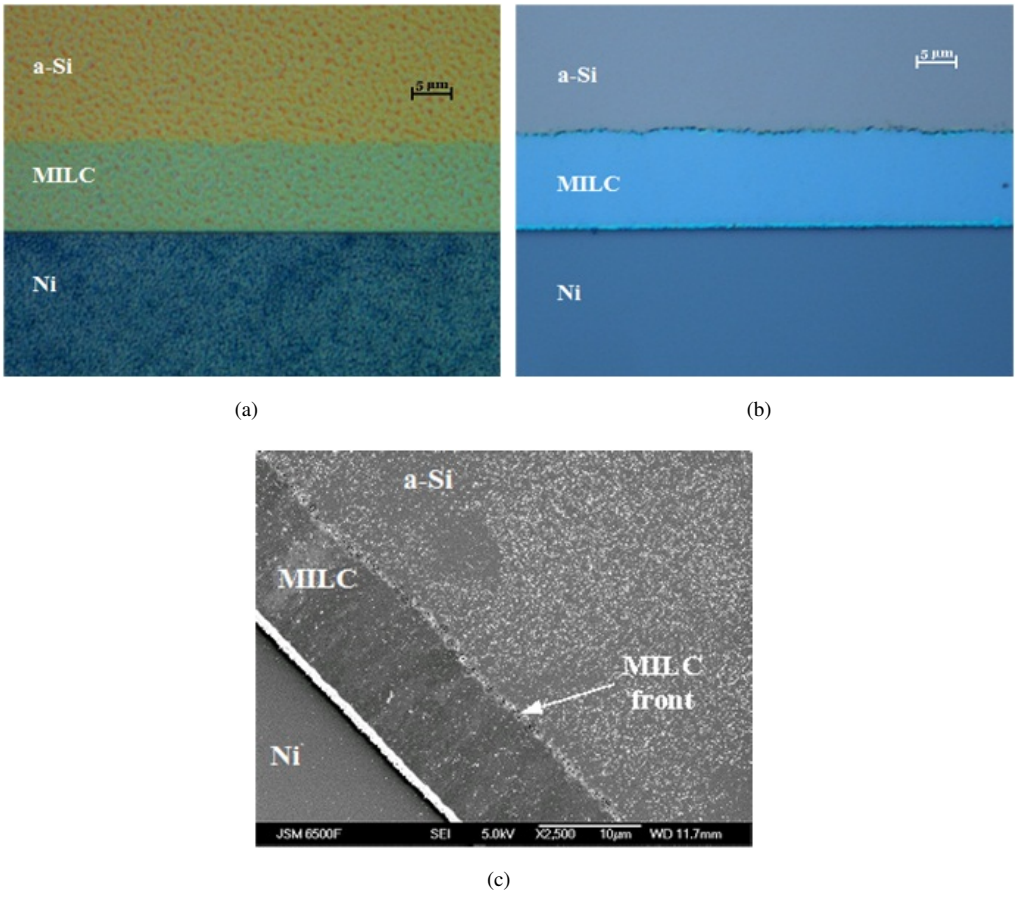


FIGURE 4.6: Micrographs of unimplanted samples after a lateral crystallisation anneal (a) Nomarski image and (b) Nomarski image after a delineation etch in 7:1 buffered HF for 20 minutes and (c) Plan-view field-emission SEM micrograph of the sample after a delineation etch in 7:1 buffered HF for 20 minutes.

Table 4.1 compares the values of lateral crystallisation lengths obtained from measurements using the techniques discussed above. A total of 20 measurements were made on the sample for each technique and means and standard deviations were calculated. The MILC lengths measured by all four methods match very well and all agree within the values of standard deviation. It should be noted that Raman spectroscopy tends to give slightly larger values as the measurement resolution depends on spot size, which is 1

μm. Therefore, it can be concluded that all four measurement techniques are valid for lateral crystallisation measurement, though the Nomarski microscope is the preferred method because it is simple, fast and non-destructive.

TABLE 4.1: Comparison of lateral crystallisation lengths measured using different techniques. Some samples were given a delineation etch and others not.

	Raman spectroscopy with an etch	Optical microscope with no etch	Optical microscope with an etch	SEM with an etch
MILC length (μm)	12.3	11.7±0.7	12.2±0.3	11.8±0.3

4.3 Results

4.3.1 Fluorine profiles before and after anneal

Fig. 4.7 shows measured fluorine profiles for unannealed samples with fluorine implant doses of 5×10^{14} cm^{-2}, 1×10^{15} cm^{-2}, 2.5×10^{15} cm^{-2} and 5×10^{15} cm^{-2}, respectively. Fluorine peaks can be identified at depths of 108 nm, 106 nm, 108 nm and 101 nm, respectively. These depths agree with a measured α-Si thickness of 111 nm obtained from cross-section SEM micrographs. This good agreement indicates that the second fluorine peak in located at the α-Si/SiO_2 interface. The variations in the peak positions between the four samples are due to variations in the α-Si thickness and to inaccuracies in the SIMS depth scale. The fluorine concentration at the α-Si/SiO_2 interface was extracted and the values are summarised in Table 4.2. The F concentrations were extracted to be 7.0×10^{19} cm^{-3}, 1.3×10^{19} cm^{-3}, 3.1×10^{20} cm^{-3} and 7.9×10^{20} cm^{-3} for F implant doses from 5×10^{14} cm^{-2} to 5×10^{15} cm^{-2}, respectively. Thus, the fluorine concentration at the α-Si/SiO_2 interface is approximately proportional to the implanted fluorine dose.

TABLE 4.2: F concentrations at the α-Si/SiO_2 interface measured by SIMS for samples with different fluorine implant doses

F implant dose	F concentration at α-Si/SiO_2 interface
5×10^{14} cm^{-2}	7.0×10^{19} cm^{-3}
1×10^{15} cm^{-2}	1.3×10^{20} cm^{-3}
2.5×10^{15} cm^{-2}	3.0×10^{20} cm^{-3}
5×10^{15} cm^{-2}	7.9×10^{20} cm^{-3}

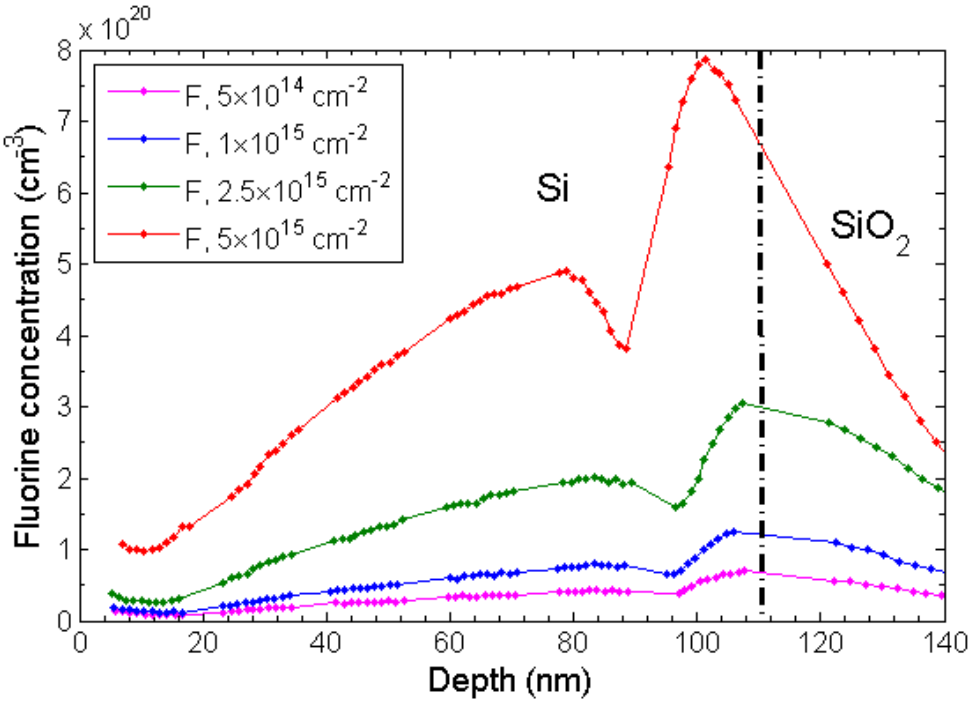
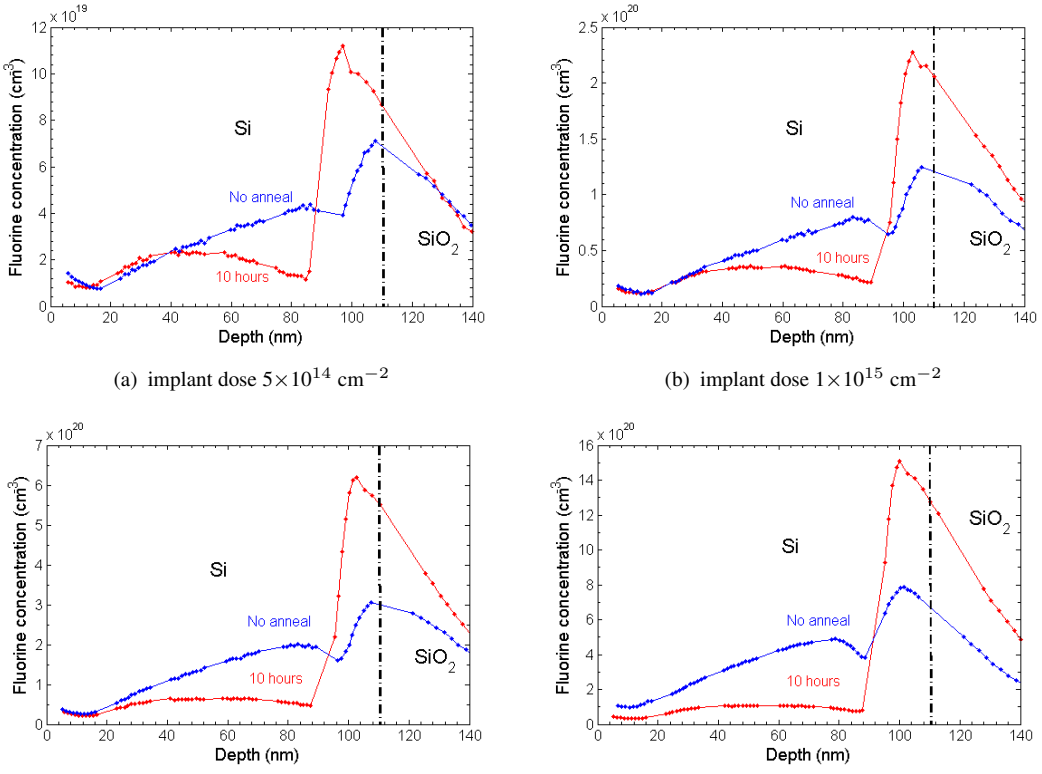


FIGURE 4.7: Fluorine SIMS profiles for samples given a 35 keV fluorine implant at dose in the range 5×10^{14} cm^{-2} to 5×10^{15} cm^{-2}. The samples were measured after oxide and Ni depositions and before a MILC anneal.

SIMS measurements were performed on 550°C 10 hour annealed samples in regions far from the MILC front to study the fluorine profiles of these samples after the MILC anneal. Fig. 4.8(a) shows the F profiles for the 5×10^{14} cm^{-2} sample before and after the MILC anneal. It can be seen that a significant amount of fluorine has migrated towards and accumulated at the Si/SiO_2 interface; 1.1×10^{20} cm^{-3}. Similar F migrations and accumulations are seen on samples implanted with higher fluorine doses in Fig. 4.8(b), (b) and (c). The fluorine concentrations at the interface are extracted to be 2.3×10^{20} cm^{-3} for 1×10^{15} cm^{-2} F, 6.2×10^{20} cm^{-3} for 2.5×10^{15} cm^{-2} F and 15×10^{20} cm^{-3} for 5×10^{15} cm^{-2} F.

4.3.2 Effect of F dose on MILC at 550°C

As the motivation for this work is to find the optimum fluorine dose for MILC, the effect of fluorine dose on MILC was investigated after an anneal of 10 hours at 550°C, which is a typical anneal used for MILC. Fig. 4.9 shows optical Nomarski micrographs for annealed samples without a fluorine implant (Fig. 4.9(a)), and with fluorine implants at doses of 5×10^{14} cm^{-2} (Fig. 4.9(b)), 1×10^{15} cm^{-2} (Fig. 4.9(c)), 2.5×10^{15} cm^{-2}



(a) implant dose 5×10^{14} cm^{-2}

(b) implant dose 1×10^{15} cm^{-2}

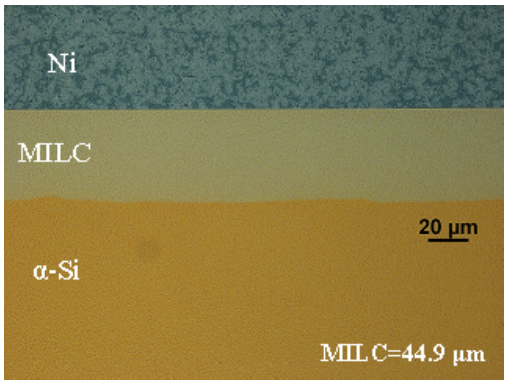
(c) implant dose 2.5×10^{15} cm^{-2}

(d) implant dose 5×10^{15} cm^{-2}

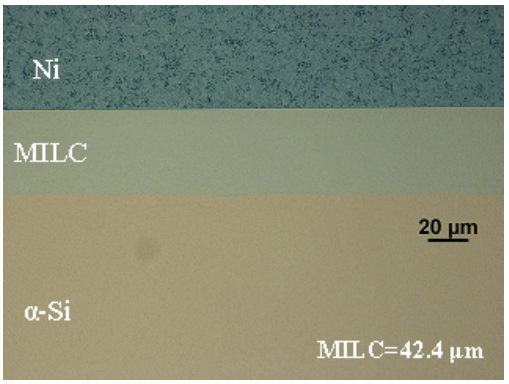
FIGURE 4.8: Fluorine SIMS profiles for samples given a 550°C MILC anneal for 10 hours after a fluorine implant at a dose of (a) 5×10^{14} cm^{-2}, (b) 1×10^{15} cm^{-2}, (c) 2.5×10^{15} cm^{-2} and (d) 5×10^{15} cm^{-2}. The implantation was performed at implant energy of 35 keV.

(Fig. 4.9(d)) and 5×10^{15} cm^{-2} (Fig. 4.9(e)). The MILC region can be identified as the green region between the nickel (in blue) and the α-Si (in brown). The measured MILC lengths shown in Fig. 4.9 are the mean values of 20 measurements from different regions of each sample. The MILC lengths were measured to be 44.9 μm for the unimplanted sample, 42.4 μm for a fluorine dose of 5×10^{14} cm^{-2}, 51.0 μm for a fluorine dose of 1×10^{15} cm^{-2}, 57.4 μm for a fluorine dose of 2.5×10^{15} cm^{-2} and 52.8 μm for a fluorine dose of 5×10^{15} cm^{-2}.

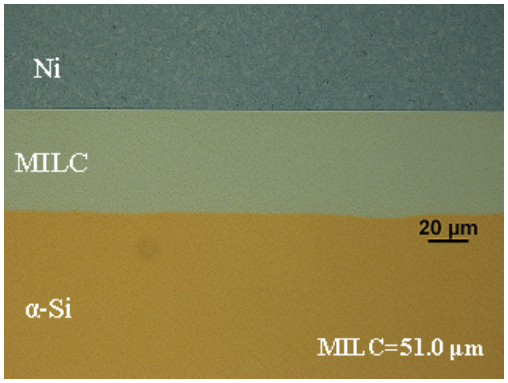
Fig. 4.10 shows a graph of the lateral crystallisation length as a function of fluorine dose for samples given a 10 hour 550°C anneal. The MILC length increases from 42.4 μm to 57.4 μm on increasing the fluorine dose from 5×10^{14} cm^{-2} to 2.5×10^{15} cm^{-2}. As the fluorine dose increases above 2.5×10^{15} cm^{-2} the MILC length decreases down to 52.8 μm, indicating that the optimum fluorine dose is 2.5×10^{15} cm^{-2}, with a MILC length improvement of 28%. In contrast, the lowest fluorine dose of 5×10^{14} cm^{-2} gives a suppression of the MILC length compared with the unimplanted sample.



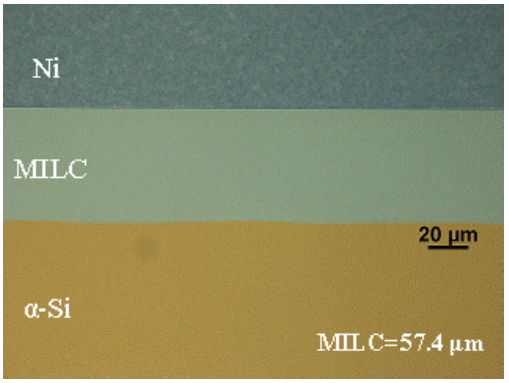
(a) unimplanted



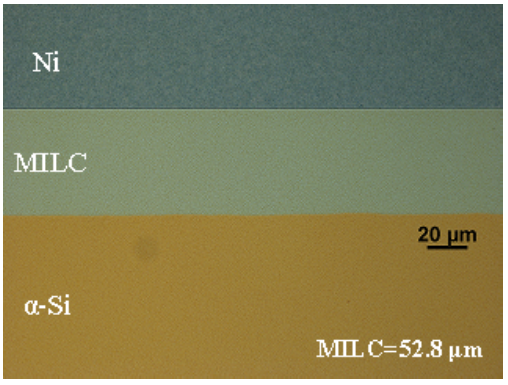
(b) F, 5×10^{14} cm^{-2}



(c) F, 1×10^{15} cm^{-2}



(d) F, 2.5×10^{15} cm^{-2}



(e) F, 5×10^{15} cm^{-2}

FIGURE 4.9: Nomarski micrographs of lateral crystallisations of samples annealed at 550°C for 10 hours with (a) no F implant, (b) F implant, 5×10^{14} cm^{-2}, (c) F implant, 1×10^{15} cm^{-2}, (d) F implant, 2.5×10^{15} cm^{-2} and (e) F implant, 5×10^{15} cm^{-2}. No delineation etch was given to the annealed samples.

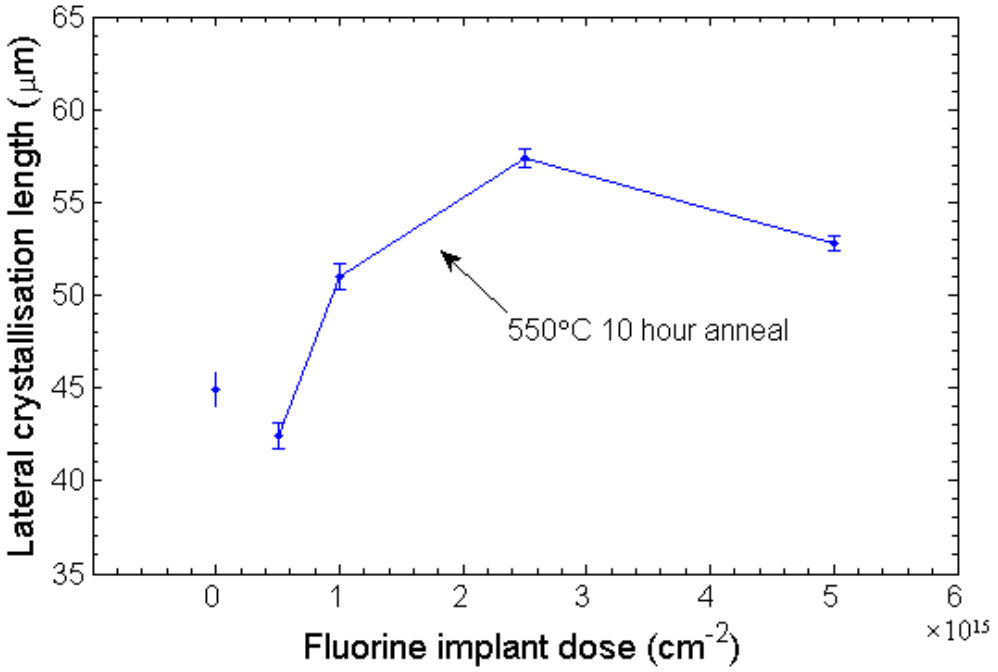


FIGURE 4.10: Lateral crystallisation length as a function of implanted fluorine dose for samples annealed at 550°C for 10 hours. All data are based on measurements by Nomarski microscope.

To investigate the effect of the MILC anneal on random crystallisation of the amorphous silicon, Raman spectroscopy was also performed on the amorphous silicon far from the MILC region and the Raman spectra is normalised by the peak intensity around 520 cm^{-1}, which is detailed in Chapter 3, and then plotted in Fig. 4.11. A sharp peak is seen at a Raman shift of around 520 cm^{-1} for the single-crystal Si sample and the annealed α-Si samples. A high and broad peak is seen at a Raman shift of around 480 cm^{-1} for the sample with a fluorine implant at a dose of 5×10^{14} cm^{-2}. As discussed in Chapter 3, these two peaks, 520 cm^{-1} and 480 cm^{-1}, indicate the presence of crystalline silicon and amorphous silicon, respectively. It can be seen that the Raman peak at around 480 cm^{-1} is significantly larger in the fluorine implanted samples than in the unimplanted sample, which indicates that the fluorine implanted samples are more amorphous. The Si crystalline fractions for all these samples have been calculated using a peak-fitting method [38], which is detailed in Chapter 3. Table 4.3 summarises the calculated Si crystallinities and extracted FWHMs for the samples. These results confirm that the unimplanted sample is more crystalline than the fluorine implanted samples. This result suggests that implantation damage from the fluorine implant has a significant influence on the crystallinity of the α-Si after the MILC anneal. This effect is particularly evident for a F dose of 5×10^{14} cm^{-2}, where the crystalline Si fraction is only 14.2% after the

MILC anneal.

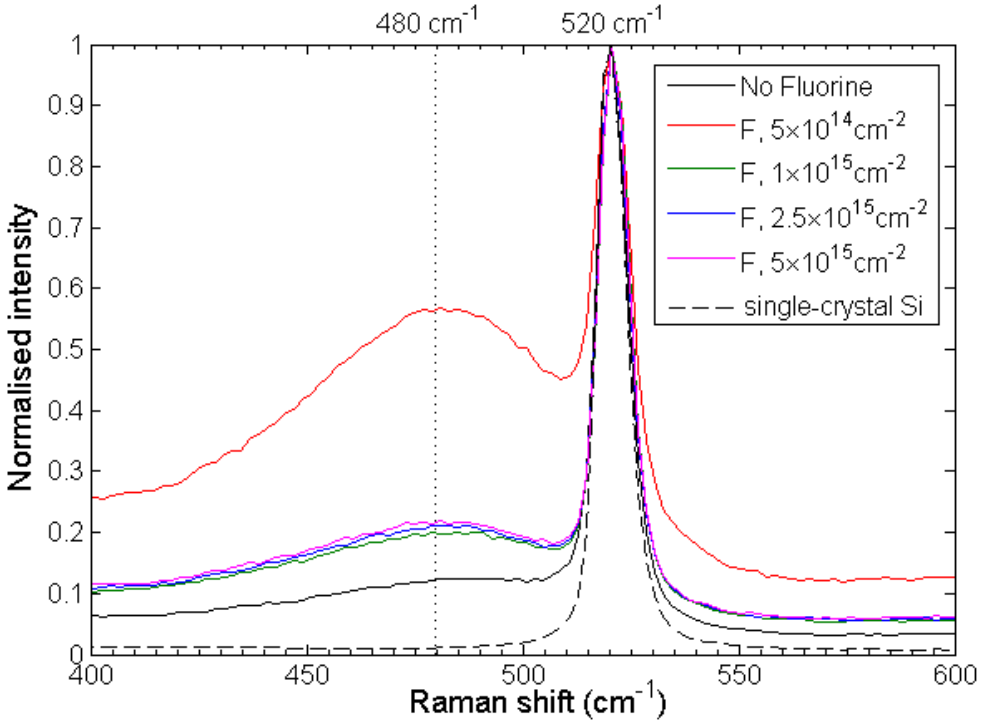


FIGURE 4.11: Normalised Raman spectra measured in the α-Si far from the MILC front for annealed samples without a F implant and with F implants at different doses. All samples were annealed at 550°C for 10 hours. For comparison, a Raman spectrum for single-crystal silicon is shown.

TABLE 4.3: Calculated Si crystalline fractions obtained using a peak-fitting technique and full-width at half maximum (FWHM) of the 520 cm^{-1} peak based on Raman spectra in Fig. 4.11. The samples were annealed at 550°C for 10 hours

F dose (cm^{-2})	unimplanted	5×10^{14}	1×10^{15}	2.5×10^{15}	5×10^{15}	sc-Si
crystal fraction	46.5%	14.2%	35.2%	34.1%	33.3%	100%
FWHM (520 cm^{-1})	8.8 cm^{-1}	12.9 cm^{-1}	9.0 cm^{-1}	8.9 cm^{-1}	8.9 cm^{-1}	8.0 cm^{-1}

To investigate the Si crystalline quality in the MILC region after a 10 hour anneal, Raman spectroscopy was also performed in the middle of the MILC region and the normalised Raman spectra are as shown in Fig. 4.12. The Raman spectrum for a single-crystalline silicon wafer is also plotted in Fig. 4.12 as a reference. The crystalline Si peak around 520 cm^{-1} can be clearly identified, whereas the 480 cm^{-1} peak for amorphous Si cannot be discerned, which indicates the MILC region has crystallised. The values of FWHM for the 520 cm^{-1} peak are 8.6 cm^{-1}, 9.9 cm^{-1}, 8.8 cm^{-1}, 8.7 cm^{-1} and 8.8 cm^{-1} for F implant doses of zero, 5×10^{14} cm^{-2}, 1×10^{15} cm^{-2}, 2.5×10^{15} cm^{-2} and 5×10^{15} cm^{-2}, respectively. These compares with a FWHM for single-crystal

silicon of 8.0 cm^{-1}. These results indicate that high quality polysilicon is obtained for fluorine doses above 5×10^{14} cm^{-2}, but that a fluorine implant of 5×10^{14} cm^{-2} gives interior Si crystallinity.

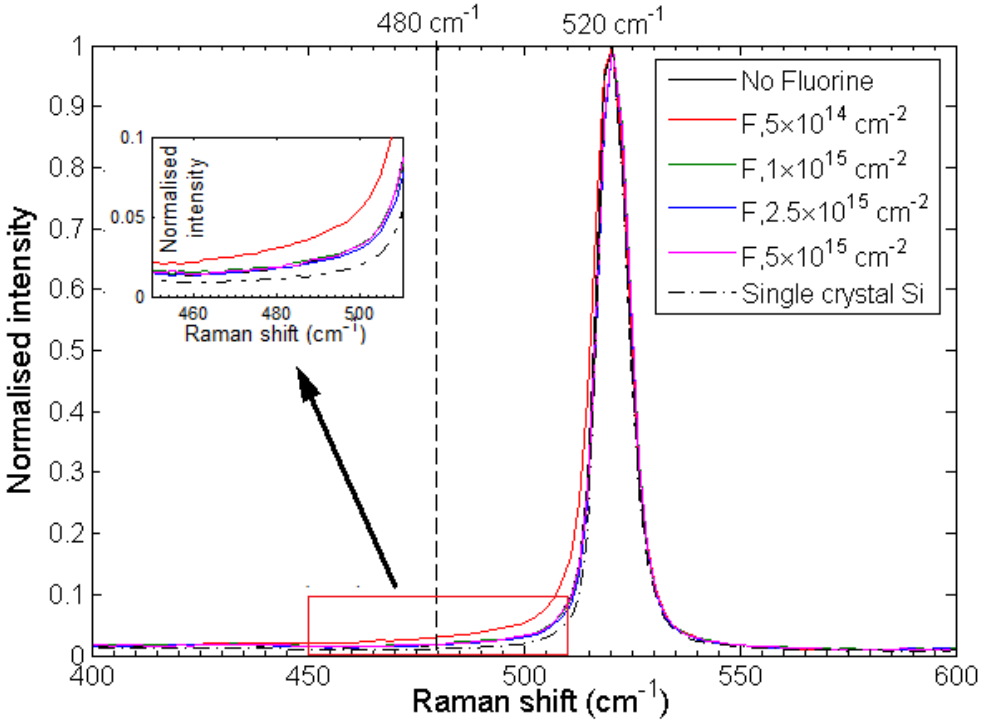


FIGURE 4.12: Normalised Raman spectra measured in the MILC regions of annealed α-Si samples without a F implant and with F implants at different doses. All samples were annealed at 550°C for 10 hours. For comparison, a Raman spectrum for single-crystal silicon is shown.

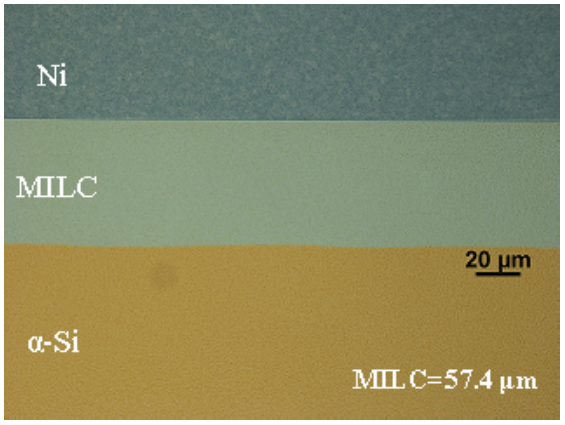
4.3.3 Effect of anneal time on MILC at 550°C

To investigate the effect of anneal time on MILC, Fig. 4.13 shows Nomarski micrographs for 2.5×10^{15} cm^{-2} fluorine implanted samples annealed at 550°C for 10 hours, 20 hours and 40 hours. The MILC length increases from 57.4 μm for a 10 hour anneal to 100.6 μm for a 20 hour anneal and 172.1 μm for a 40 hour anneal. This behaviour is as expected and follows the general trend reported in [31] for samples annealed at 500°C. For samples with a lower fluorine implant dose of 1×10^{15} cm^{-2}, as shown in Fig. 4.14, the MILC length increases from 51 μm after a 10 hour anneal to 84 μm after a 20 hour anneal. However, after a 40 hour anneal, a clearly defined MILC region cannot be discerned, as there is little or no colour change between the MILC region and the

adjacent silicon region. As the colour change is due to the different silicon structures in the two regions, this result suggests that the amorphous silicon region has been crystallised into polysilicon as indicated by the poly-Si label in Fig. 4.14(c). A similar trend is seen in Fig. 4.15(b) to (c) for samples without a fluorine implant. In this case, the MILC region cannot be clearly identified after anneals of 20 and 40 hours. This result indicates that the amorphous Si film is fully crystallised after an anneal of 20 hours. A comparison of Nomarski images in Figs. 4.13 and 4.15 for fluorine implanted and unimplanted samples clearly shows that the fluorine implant has suppressed crystallisation in the amorphous silicon away from the MILC region. Furthermore, it is also clear that this suppression is stronger for a 2.5×10^{15} cm^{-2} F implant than a 1×10^{15} cm^{-2} F implant.

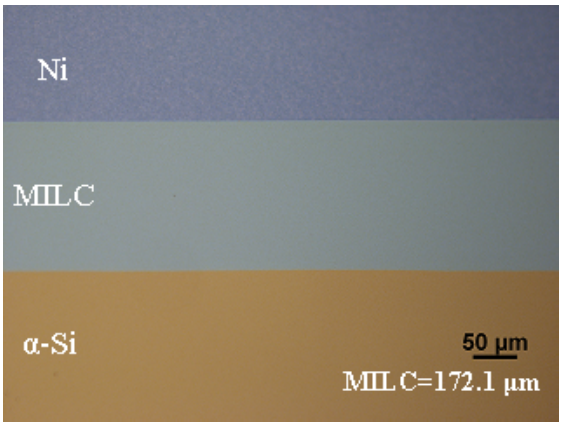
For those samples with poor MILC contrast in Fig. 4.14(c) and Fig. 4.15(b) and (c), a delineation etch in 7:1 buffered HF for 20 minutes was given in an attempt to identify the MILC regions. Fig. 4.16 shows optical Nomarski micrographs after the delineation etch. Comparing the results in Fig. 4.16(a) and Fig. 4.15(b), it can be seen that even after the delineation etch, the colour of the MILC region is almost indistinguishable from that of the adjacent region. This result provides further evidence that the amorphous silicon has been completely recrystallised in this sample. A similar conclusion can be drawn by comparing Fig. 4.16(b) with Fig. 4.15(c) and Fig. 4.16(c) with Figs. 4.14(c). While there is little colour change in these samples, the delineation etch has successfully delineated etch pits at the MILC front, as can be clearly seen in Fig. 4.16(c) and to a lesser extent in Fig. 4.16(b). MILC lengths can therefore be measured in these samples of 55.2 μm and 108.4 μm, respectively.

Fig. 4.17 shows the lateral crystallisation length as a function of anneal time for samples annealed at 550°C. The MILC length was measured using an optical Nomarski microscope and the inset is used to clarify the measurements for shorter anneals. For the two highest fluorine doses of 2.5×10^{15} cm^{-2} and 5×10^{15} cm^{-2}, the MILC length increases linearly with anneal time at short anneals and then increases more slowly at longer anneals. In contrast, for the unimplanted samples, the MILC length initially increases with anneal time from 3 hours to about 10 hours and then saturates completely after a 15 hour anneal. For fluorine doses of 5×10^{14} cm^{-2} and 1×10^{15} cm^{-2}, an intermediate trend is seen, with partial saturation of the MILC length at longer anneals. The inset of Fig. 4.17 shows that there is some cross-over of the curves for the shorter anneals. Samples with a fluorine implant dose above 1×10^{15} cm^{-2} have a significantly longer MILC length than samples without a fluorine implant, whereas a fluorine dose of 5×10^{15} cm^{-2} gives a suppression of the MILC length.



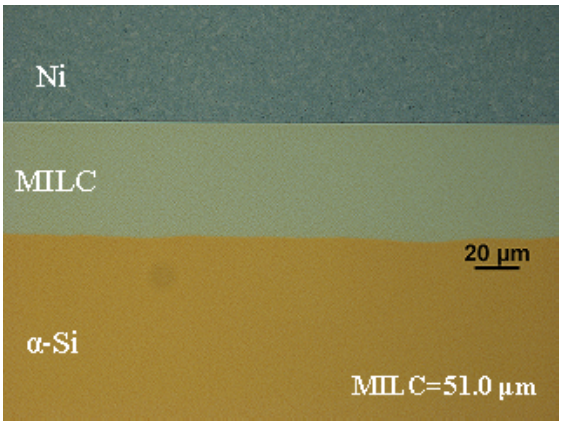
(a) 10 hours

(b) 20 hours



(c) 40 hours

FIGURE 4.13: Nomarski micrographs of 550°C annealed samples with F implant dose of 2.5×10^{15} cm^{-2} after (a) 10 hour anneal, (b) 20 hour anneal and (c) 40 hour anneal. No delineation etch was given to the annealed samples.

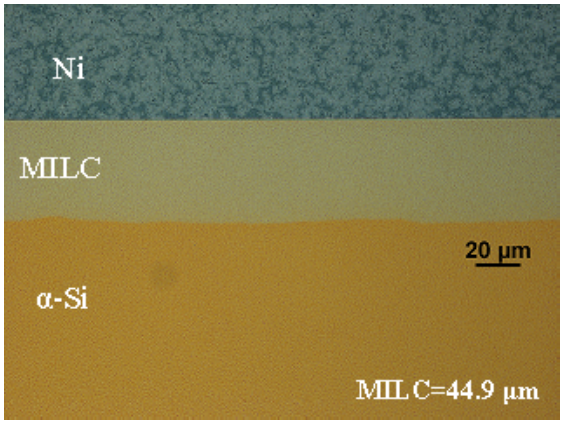


(a) 10 hours

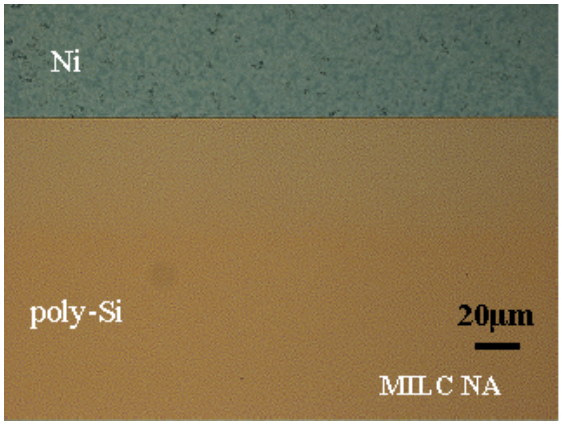
(b) 20 hours

(c) 40 hours

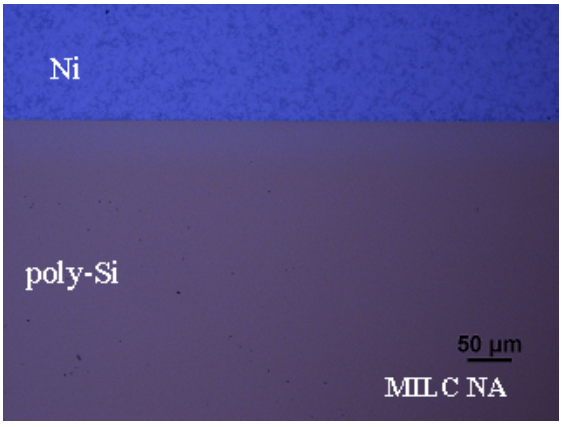
FIGURE 4.14: Nomarski micrographs of 550°C annealed samples with F implant dose of 1×10^{15} cm^{-2} after (a) 10 hour anneal, (b) 20 hour anneal and (c) 40 hour anneal. No delineation etch was given to the annealed samples.



(a) 10 hours

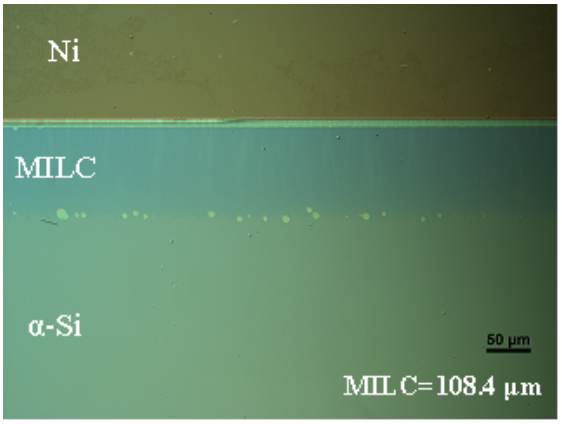


(b) 20 hours

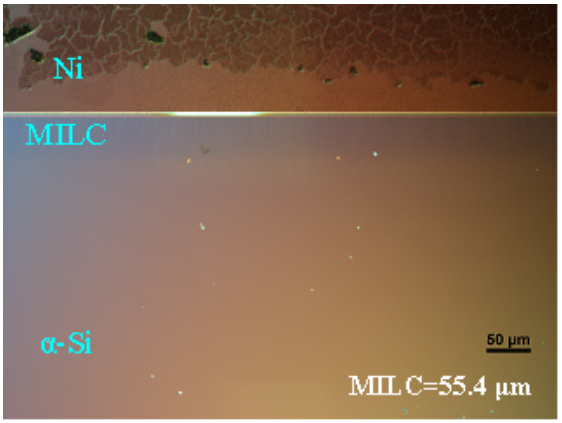


(c) 40 hours

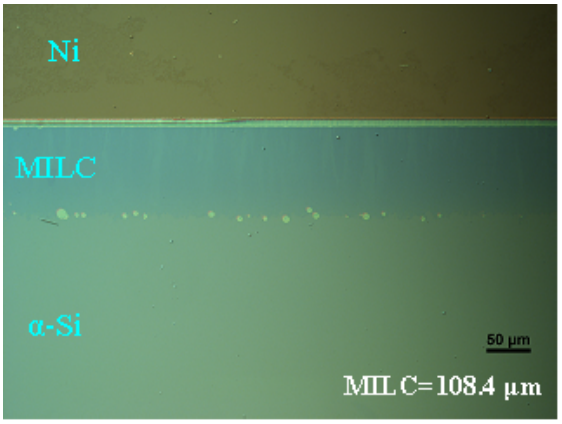
FIGURE 4.15: Nomarski micrographs of 550°C annealed samples with no F implant after (a) 10 hour anneal, (b) 20 hour anneal and (c) 40 hour anneal. No delineation etch was given to the annealed samples.



(a) No F, 20 hours



(b) No F, 40 hours



(c) F 1×10^{15} cm^{-2}, 40 hours

FIGURE 4.16: Nomarski micrographs of 550°C annealed samples with a 20 minute delineation etch in 7:1 buffered HF with (a) no F implant after 20 hour anneal, (b) no F implant after 40 hour anneal and (c) F implant dose of 1×10^{15} cm^{-2} after 40 hour anneal.

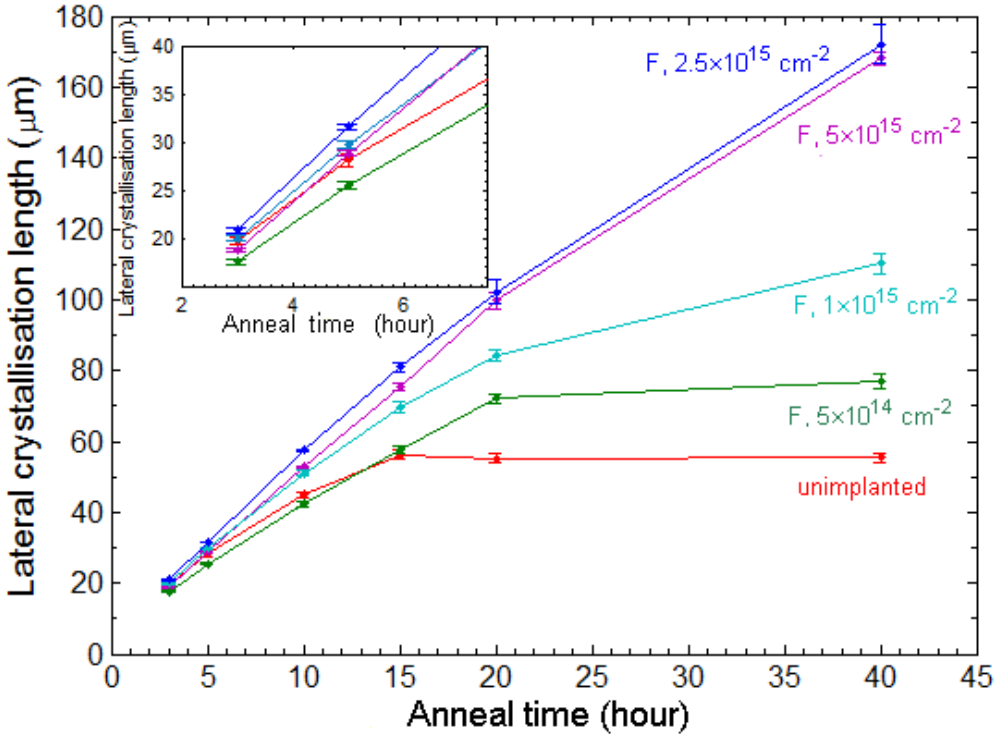


FIGURE 4.17: Lateral crystallisation length as a function of anneal time for unimplanted and fluorine implanted samples annealed at 550°C. All data are based on measurements using Nomarski microscope.

To further investigate the MILC saturation, Raman spectroscopy was used to analyse the silicon crystallinity in regions far from the MILC front. Fig. 4.18(a) shows normalised Raman spectra for unimplanted samples after an anneal at 550°C for different times. A Raman peak at 520 cm^{-1} can be clearly identified for all samples and this peak indicates the presence of crystalline silicon. Another peak at 480 cm^{-1}, which indicates that presence of amorphous silicon, can also be identified for unannealed, 3 hour, 5 hour and 10 hour annealed samples and the peak height at 480 cm^{-1} decreases as the anneal time increases. A decreasing peak height for the 480 cm^{-1} peak indicates an increasing degree of crystallinity. As the anneal time increases to 15 hours, the 480 cm^{-1} peak cannot be discerned and becomes similar to that of single-crystal silicon, which indicates that the region far from the MILC front has been recrystallised into polysilicon after a MILC anneal for 15 hours. The normalised Raman spectra for 2.5×10 cm^{-2} F implanted samples annealed under the identical conditions are shown in Fig. 4.18(b). For all F implanted samples, both 480 cm^{-1} and 520 cm^{-1} can be identified and this indicates the samples are not fully crystallised. There is no significant difference in the 480 cm^{-2} peak height among the fluorine implanted samples after anneals from 3 hours

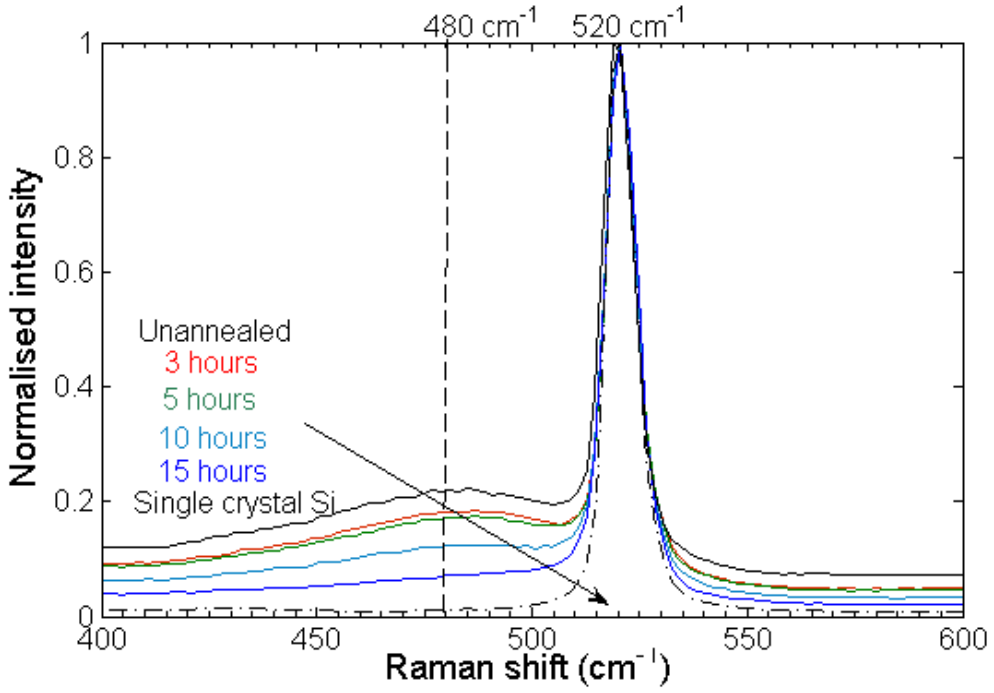
to 15 hours, which indicates a similar amorphous condition for these samples. Thus fluorine implantation has suppressed crystallisation in the α-Si away from the MILC region and this has suppressed the MILC saturation.

Fig. 4.19 summarises the calculated Si crystalline fractions using the peak-fitting technique based on the Raman spectra in Fig. 4.18. Results show that the Si crystalline fraction increases from 34.8% for the unannealed sample to 58.8% for the 15 hour annealed sample. For the fluorine implanted samples, a different trend is seen in which the Si crystalline fraction is roughly unchanged as the anneal time increases from 3 hours to 15 hours. It can be concluded that fluorine suppresses random crystallisation. It is also seen that the Si crystalline fraction for the unannealed F implanted sample is 23.7% compared with 34.8% for the unimplanted, unannealed sample. This indicates that a fluorine implant further amorphises the silicon during the implantation process.

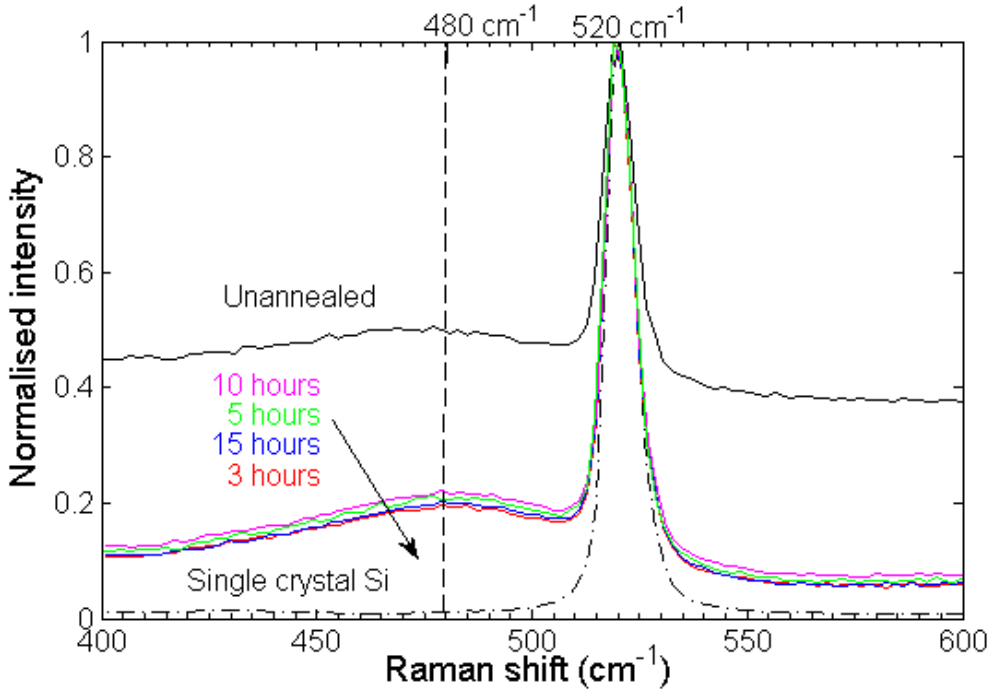
4.3.4 Effect of F dose on MILC at 575°C

In this section, the effect of fluorine dose on MILC is investigated at a higher anneal temperature of 575°C. Fig. 4.20 shows optical Nomarski micrographs of samples implanted with fluorine at different doses and then annealed for 20 hours at 575°C. For the unimplanted sample in Fig. 4.20(a), no colour change can be identified between the MILC region and the adjacent region. Similar behaviour can also be identified in Figs. 4.20(b) and (c) for samples with fluorine doses of 5×10^{14} cm^{-2} and 1×10^{15} cm^{-2}. These results indicate that MILC growth on these samples has saturated due to the complete crystallisation of the amorphous silicon. In contrast, MILC regions can be clearly seen in Figs. 4.20(d) and (e) for samples implanted with fluorine doses of 2.5×10^{15} cm^{-2} and 5×10^{15} cm^{-2}, respectively. MILC lengths of 201 μm and 203 μm, respectively, can be measured for these samples. It can therefore be concluded that a higher fluorine dose is needed to effectively suppress MILC saturation at the higher anneal temperature of 575°C.

Fig. 4.21 shows the lateral crystallisation length as a function of fluorine dose for samples after a lateral crystallisation anneal at 575°C for 20 hours. For those samples with no clearly defined MILC region, a delineation etch in buffered HF was performed and the MILC length measured from the position of the etch pits at the MILC front. The MILC length increases as the fluorine dose increases from 5×10^{14} cm^{-2} to 2.5×10^{15} cm^{-2} and then increases only slightly as the fluorine dose is further increased to 5×10^{15} cm^{-2}.



(a) unimplanted



(b) F, 2.5×10^{15} cm^{-2}

FIGURE 4.18: Normalised Raman spectra measured in the α-Si far from the MILC regions for samples annealed at 550°C for different durations. (a) no F implant and (b) F implant at a dose of 2.5×10^{15} cm^{-2}.

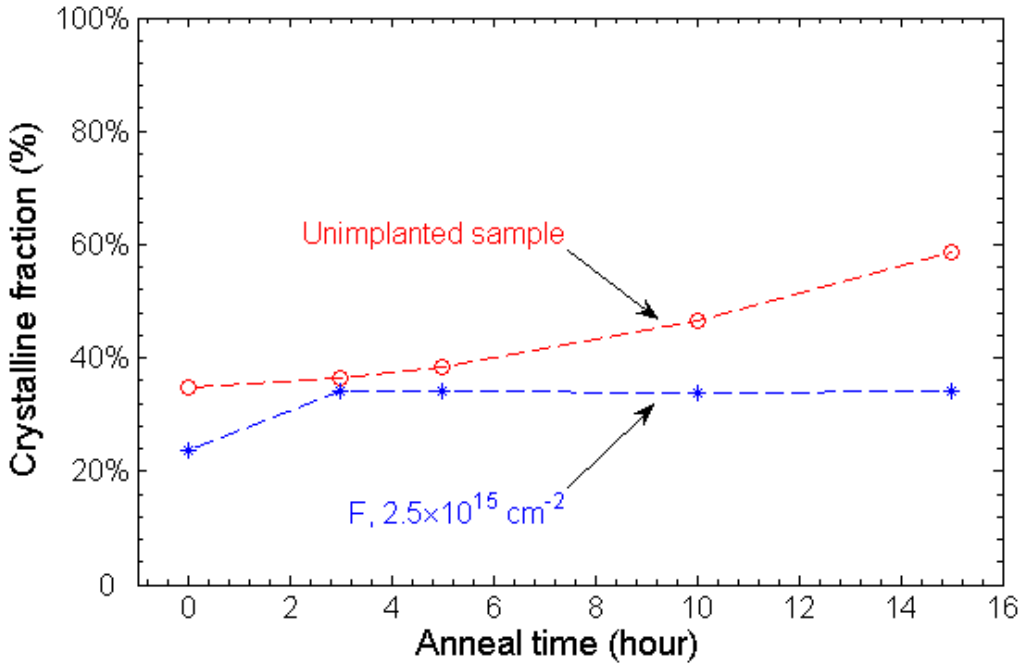


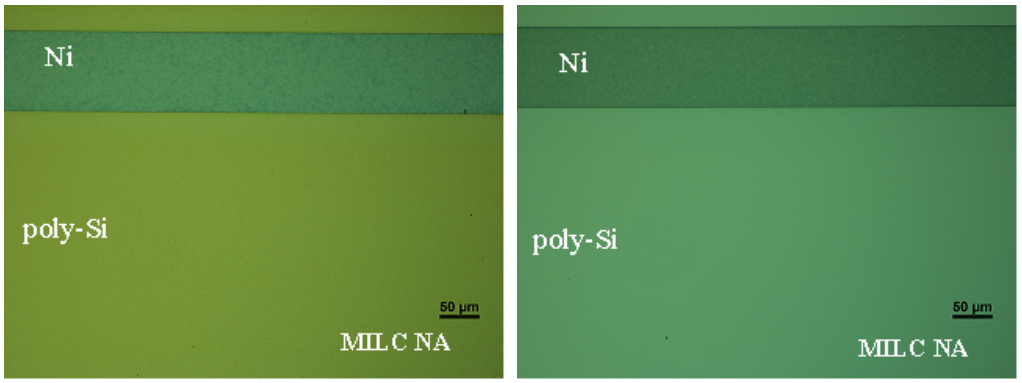
FIGURE 4.19: Si crystalline fraction measured at the α-Si far from MILC for unimplanted and F (2.5×10^{15} cm^{-2}) implanted samples after anneals at 550°C for different durations.

4.3.5 MILC at lower anneal temperatures

MILC at lower temperatures is investigated to determine the temperature limit for lateral crystallisation. A temperature below 450°C is needed for device fabrication on cheap glass substrates. Fig. 4.22 shows optical Nomarski micrographs of unimplanted samples after a 20 hour anneal at a temperature in the range 525°C to 428°C. Clear colour changes can be seen on all samples, indicating that the MILC growth has not occurred in any of these anneal temperatures.

Fig. 4.23 shows a graph of lateral crystallisation length as a function of anneal temperature for samples annealed for 20 hours at temperatures from 525°C down to 428°C. It can be seen that the MILC length decreases from 37.6 μm to 1.2 μm as the anneal temperature decreases from 525°C to 428°C. Nevertheless, a MILC length of about 3.2 μm can be achieved using an anneal temperature as low as 450°C and a MILC length of about 1.2 μm can be achieved when the anneal temperature was further reduced to 428 °C. The slow rate of MILC rate decrease at low temperatures in Fig. 4.23 suggests that the MILC anneal temperature might be further decreased.

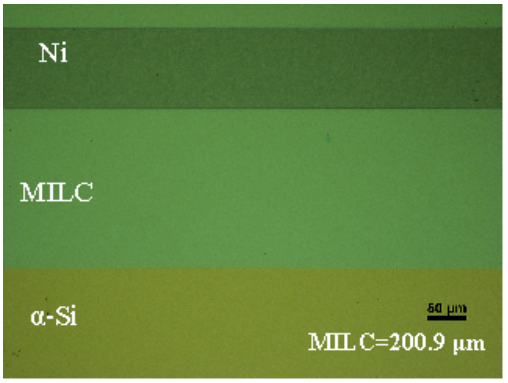
To further investigate MILC at low temperature anneals, Raman spectroscopy was used



(a) unimplanted

(b) F, 5×10^{14} cm^{-2}

(c) F, 1×10^{15} cm^{-2}



(d) F, 2.5×10^{15} cm^{-2}

(e) F, 5×10^{15} cm^{-2}

FIGURE 4.20: Nomarski micrographs of samples annealed for 20 hour at 575°C with (a) no F implant, (b) a F implant dose of 5×10^{14} cm^{-2}, (c) a F implant dose of 1×10^{15} cm^{-2}, (d) a F implant dose of 2.5×10^{15} cm^{-2} and (e) a F implant dose of 5×10^{15} cm^{-2}. No delineation etch was given to the samples.

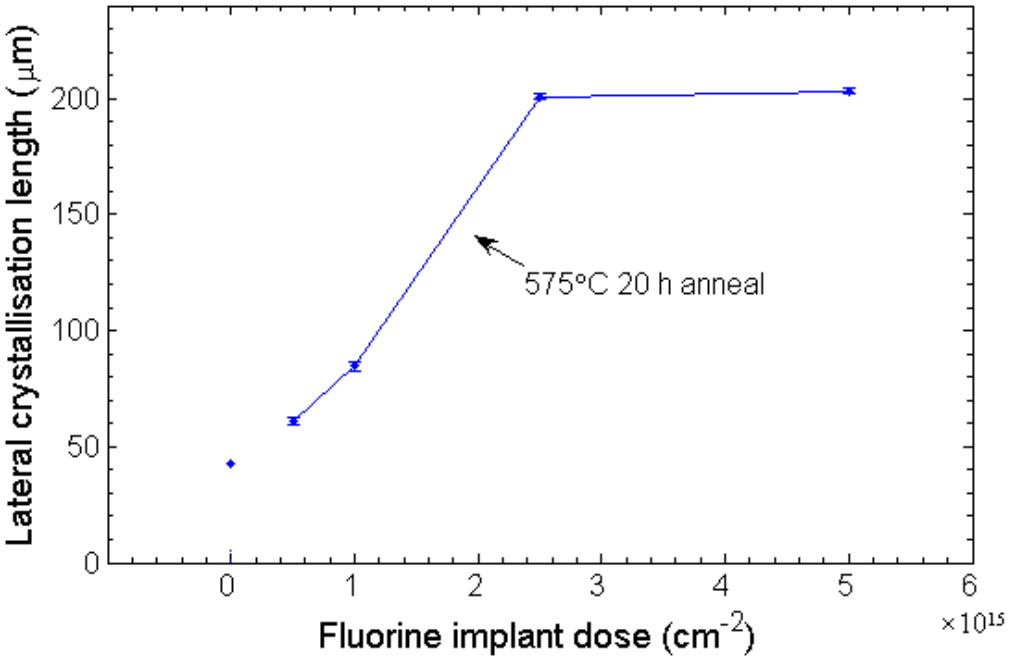


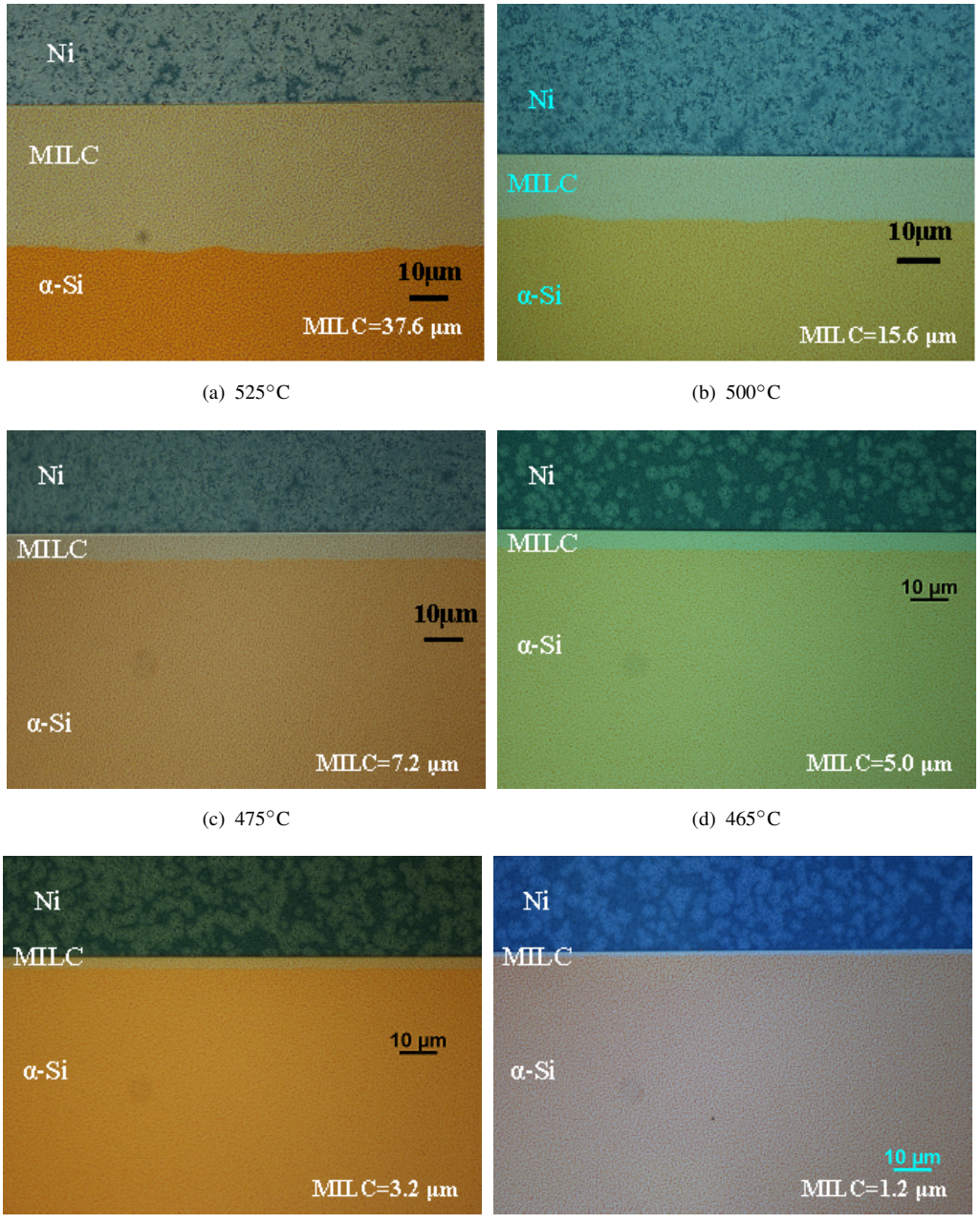
FIGURE 4.21: Lateral crystallisation length as a function of implanted fluorine dose for samples annealed at 575°C for 20 hours. All data are based on measurements by Nomarski microscope.

to analyse the silicon crystallinity in the MILC regions on unimplanted samples after a 20 hour anneals at 450°C and 428°C and the normalised Raman spectra are shown in Fig. 4.24. For both samples, a Raman peak at 520 cm^{-1} can be clearly identified whilst no 480 cm^{-1} peak can be identified. This further confirms that the amorphous silicon was recrystallised by MILC at temperatures down to 428°C.

4.3.6 Effect of F dose on MILC at lower temperatures

The effect of fluorine dose on MILC is investigated at lower temperatures from 525°C down to 428°C. Fig. 4.25 shows optical Nomarski micrographs of samples implanted with different doses of fluorine and then annealed for 20 hours at 525°C. The MILC regions of all samples can be clearly identified, indicating that MILC saturation has not occurred in any of these samples. MILC lengths of 37.6 μm, 34.5 μm, 41.1 μm, 43.9 μm and 40.6 μm, can be measured for doses of zero, 5×10^{14} cm^{-2}, 1×10^{15} cm^{-2}, 2.5×10^{15} cm^{-2} and 5×10^{15} cm^{-2}, respectively.

Fig. 4.26 shows the lateral crystallisation length as a function of fluorine dose for sam-



(a) 525°C (b) 500°C

(c) 475°C (d) 465°C

(e) 450°C (f) 428°C

FIGURE 4.22: Nomarski micrographs of unimplanted samples after a 20 hour anneal at (a) 525°C, (b) 500°C, (c) 475°C, (d) 465°C, (e) 450°C and (f) 428°C. No delineation etch was given to the samples.

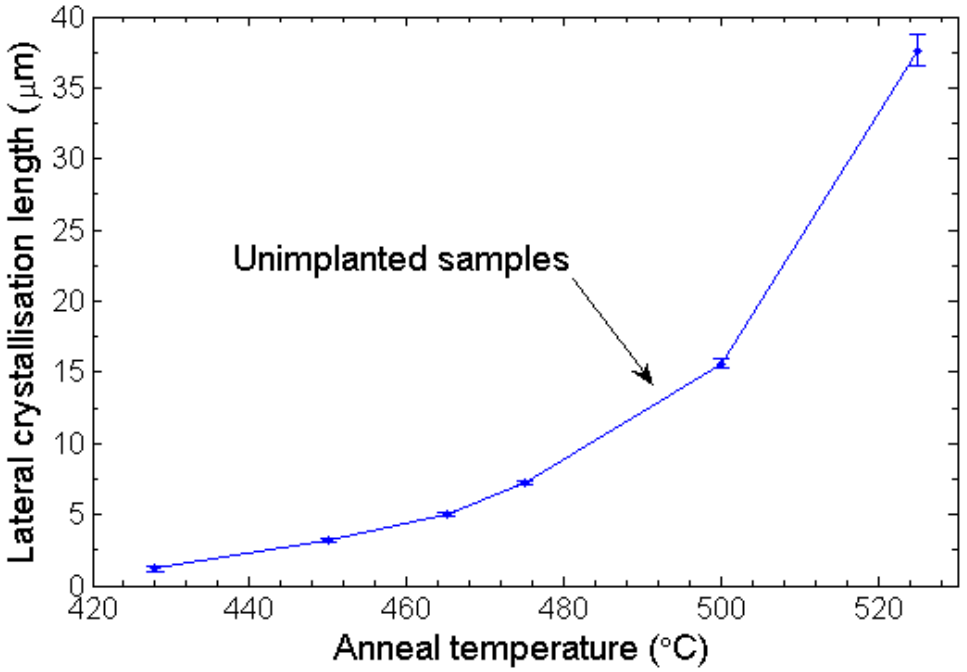


FIGURE 4.23: Lateral crystallisation length as a function of anneal temperature for unimplanted samples annealed for 20 hours at temperatures from 525°C down to 428°C. All data are based on measurements by Nomarski microscope.

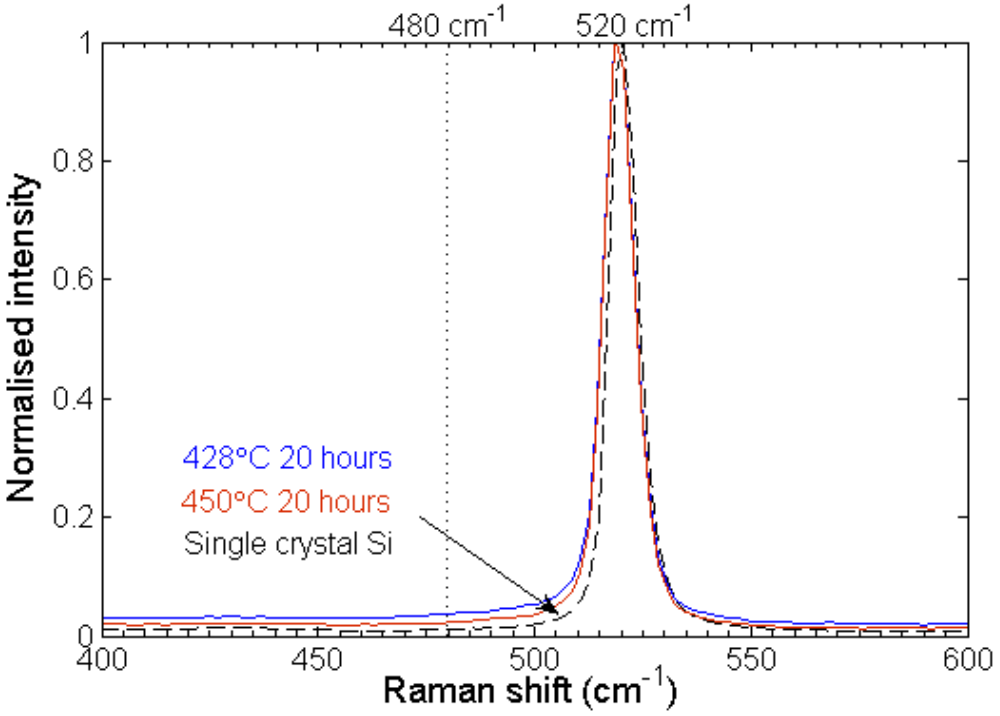
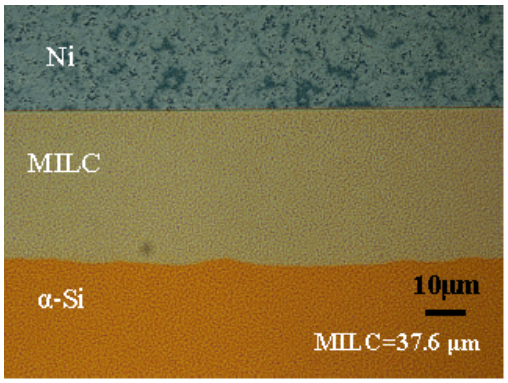
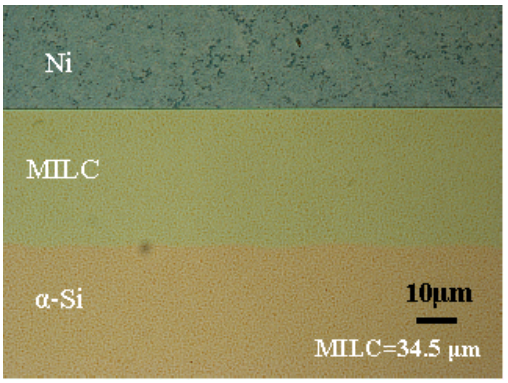


FIGURE 4.24: Normalised Raman spectra measured in the α-Si in the MILC regions for samples annealed at 450°C and 428°C for 20 hours.

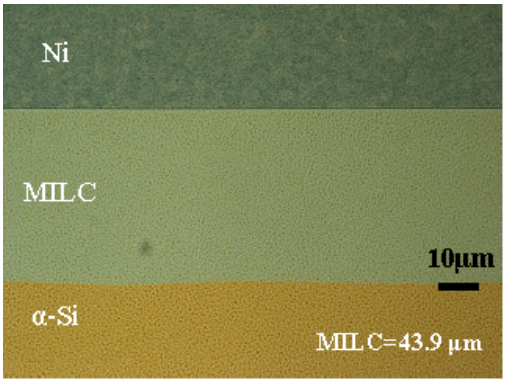


(a) unimplanted

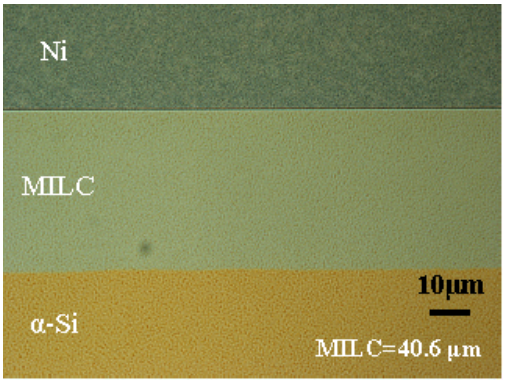


(b) F, 5×10^{14} cm^{-2}

(c) F, 1×10^{15} cm^{-2}



(d) F, 2.5×10^{15} cm^{-2}



(e) F, 5×10^{15} cm^{-2}

FIGURE 4.25: Nomarski micrographs of 20 hour 525°C annealed samples with (a) no F implant, (b) F implant of 5×10^{14} cm^{-2}, (c) F implant of 1×10^{15} cm^{-2}, (d) F implant of 2.5×10^{15} cm^{-2} and (e) F implant of 5×10^{15} cm^{-2}. No delineation etch was given to the annealed samples.

ples annealed for 20 hours at 525°C. The results show a similar trend as Fig. 4.10 for the 550°C anneal. A fluorine dose above 1×10^{15} cm^{-2} gives a significant improvement in MILC length, whilst a fluorine dose of 5×10^{14} cm^{-2} gives a suppression of MILC length. The optimum fluorine dose for maximum MILC length is 2.5×10^{15} cm^{-2}.

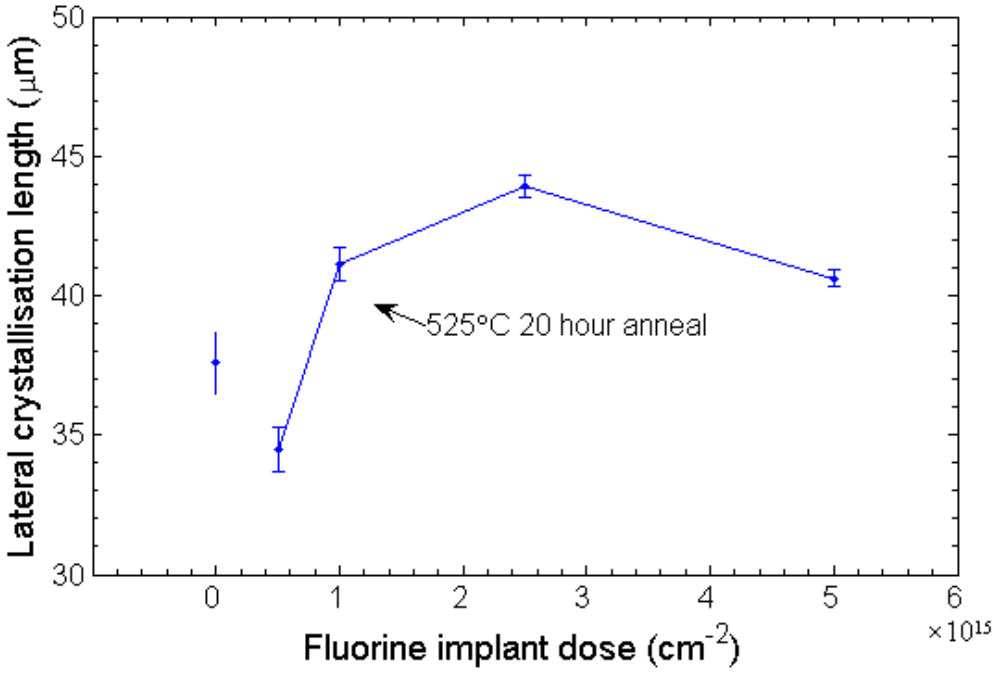


FIGURE 4.26: Lateral crystallisation length as a function of implanted fluorine dose for samples annealed at 525°C for 20 hours. All data are based on measurements by Nomarski microscope.

Fig. 4.27 shows the crystallisation length as a function of fluorine dose for samples after a 20 hour anneal at different temperatures below 525°C. For all of these temperatures, fluorine does not improve the MILC length at any dose. In fact, for an anneal at 465°C and below, fluorine suppresses MILC and the suppression becomes more significant as the fluorine dose increases.

4.4 Discussion

Metal-induced lateral crystallisation by nickel is a nickel disilicide-mediated solid-phase transformation process. The mechanism of MILC for Ni was proposed by Hayzelden *et al* [46][48] to be nickel diffusion from the $NiSi_2$/crystalline Si interface to the $NiSi_2$/α-

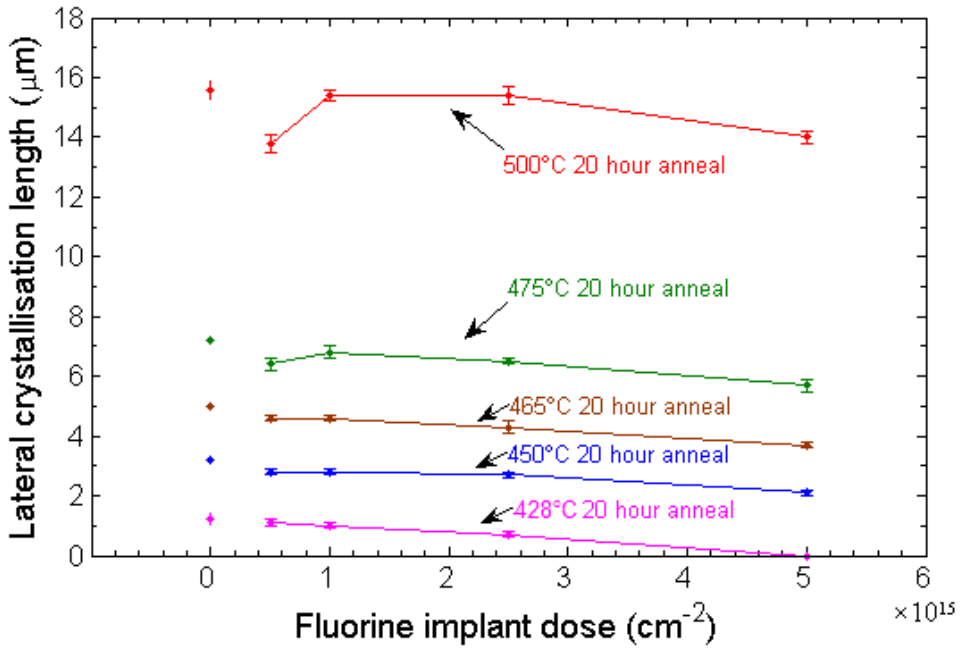


FIGURE 4.27: Lateral crystallisation length as a function of implanted fluorine dose for samples annealed at different temperatures for 20 hours. All data are based on measurements by Nomarski microscope.

Si interface due to a chemical potential difference between the two interfaces. As the lattice mismatch between crystalline $NiSi_2$ and crystalline Si is about 0.4%, nickel atoms diffuse into α-Si region and leave a polycrystalline Si trail behind. Thus, the Si crystallisation anneal temperature for MILC is about 550°C [105] and significantly lower than that of Si solid-phase crystallisation (SPC), typically at 600°C [35]. During the MILC anneal, random crystallisation also occurs in the α-Si region with preferred locations at the α-Si/SiO_2 interface due to tensile stress [39]. Some small grains of polysilicon may also be present after the α-Si deposition [35]. As the Ni diffusion is driven by the chemical potential difference, the polysilicon grains generated by random crystallisation can reduce the chemical potential due to the crystalline contrast and this can retard the MILC process [106]. As random grains grow larger, by the same mechanism, the crystalline fraction of α-Si increases and this leads to a reduction of the MILC rate. Finally, nickel atoms can be fully stopped and trapped in the MILC front region of the Si film, leading to the saturation of MILC growth [107].

In the work, it was found that lateral crystallisation can occur at a temperature as low as 428 °C (Fig. 4.23). To the best knowledge of the author, this is the lowest reported temperature for MILC growth. This MILC growth temperature agrees with the nucle-

ation temperature of $NiSi_2$ reported in Cammarata's work [52] which showed that $NiSi_2$ nucleation was found at temperatures down to 400°C. It was also found that a MILC length of 3.2 μm can be obtained using an anneal at 450°C for 20 hours. These MILC anneals are consistent with the maximum temperature of 450°C, needed for the used of Corning 2000 glass. Thus these results demonstrate the possibility of using low-cost glass substrates for biosensor fabrication.

In this work, a fluorine implant dose of 2.5×10^{15} cm^{-2} was found to give the maximum MILC length for anneals at 525°C and 550°C, as shown in Fig. 4.26 and Fig. 4.10, respectively. The effect of fluorine on the MILC length was studied by Hakim and Ashburn [31] and they found that a F implant at a dose of 5×10^{15} cm^{-2} either into α-Si or the underlying SiO_2 (before the α-Si deposition) gave a significant increase in MILC length for samples annealed at 500°C. Hakim proposed that fluorine significantly suppresses random crystallisation at the α-Si/SiO_2 interface, and this explanation was supported by cross-section SEM views [31]. This explanation can also be used to explain the increase in MILC length observed in our work for a F dose of 2.5×10^{15} cm^{-2} and a MILC anneal at 525°C or 550°C.

It is now to explain the fluorine dose influence and why a fluorine implant dose of 2.5×10^{15} cm^{-2} is the optimum value at 525°C (in Fig. 4.26) and 550°C (in Fig. 4.10). It can be seen from the SIMS results in Fig. 4.8 that a higher fluorine concentration accumulates at the α-Si/SiO_2 interface for higher fluorine implant doses. In Hakim's model, fluorine at the α-Si/SiO_2 interface influences MILC by suppressing random grain growth at the α-Si/SiO_2 interface. Thus a higher fluorine implant dose is expected to give a more effective suppression. Hakim [31] provided no direct evidence of the presence of fluorine at the α-Si/SiO_2 interface, but the results in Fig. 4.8 show the presence of a large concentration of fluorine at this interface. This result therefore confirms Hakim's mechanism and explains the rise in MILC length on increasing the F dose from 5×10^{14} cm^{-2} to 2.5×10^{15} cm^{-2}. The results in Fig. 4.26 and Fig. 4.10 also show a decrease in MILC length for fluorine doses above 2.5×10^{15} cm^{-2} and a lower MILC length for a 5×10^{14} cm^{-2} F implant than for no implant. These results can be explained by the damage introduced into the α-Si by the F implant. Tsai *et al* [108] showed that a F dose of 1×10^{15} cm^{-2} is above the amorphisation threshold for a 130 keV fluorine implant. In this work, it would therefore be expected that the 5×10^{14} cm^{-2} F implant to be below the amorphisation threshold. As implantation damage is more difficult to anneal below the amorphisation threshold [109], we would expect that the samples implanted with 5×10^{14} cm^{-2} would be less crystalline than the unimplanted samples. The Raman results in Fig. 4.11 confirm that this is the case in the α-Si far from the MILC front.

TABLE 4.4: Si disorder created by F implantation at different doses calculated using the SUSPRE simulator

F implant dose (cm^{-2})	5×10^{14}	1×10^{15}	2.5×10^{15}	5×10^{15}
Max. disorder/depth (nm)	52%/24 nm	77%/30 nm	97%/40 nm	100%/66 nm
Disorder at αSi/SiO_2 interface	10%	19%	44%	65%

A similar argument could be applied in the MILC region, which would then explain why the MILC length is lower for a 5×10^{14} cm^{-2} F implant than for no F implant (e.g. in Fig. 4.10). Amorphisation might also explain the decrease in MILC length for a F dose of 5×10^{15} cm^{-2} (in Figs. 4.10 and 4.26). Amorphisation occurs initially around the peak of the F implant and then broadens at as the F dose increases. For a 5×10^{15} cm^{-2} F implant the amorphous layer may be thick enough to reach the α-Si/SiO_2 interface. If this was the case, both the F concentration at the α-Si/SiO_2 interface and the random grain nucleation could be affected. Some support for this explanation comes from SUSPRE simulations, as shown in Table 4.4. An implant energy of 35 keV and an α-Si thickness of 110 nm were used in the simulations. For a F dose of 5×10^{15} cm^{-2}, the simulated results show around the implant peak a maximum disorder of 100% and a disorder of 65% at the α-Si/SiO_2 interface. These simulations are able to explain the results in Figs. 4.10 and 4.26 if the amorphisation threshold occurs at a percentage disorder between 52% and 65%.

For unimplanted samples, MILC growth saturates after 15 hour anneal as shown in Fig. 4.17. This is explained by the complete crystallisation of the amorphous silicon film, which finally stops the Ni migration and thus the MILC growth. This behavior is confirmed by the Raman result in Fig. 4.18 that the 480 cm^{-1} peak becomes present then absent for unimplanted samples after a 15 hour anneal at 550°C. This can also be confirmed by a calculation using the model in [35]. For unimplanted samples, the random grain growth rate by SPC follows on Arrhenius behavior as shown in Fig. 2.1. Growth rates at 575°C and 550°C can be calculated from the Arrhenius plot to be about 0.01 nm/sec and 0.002 nm/sec, respectively. Assuming that MILC saturation occurs when random grain size reaches 100 nm, the anneal times needed for anneals at 575°C and 550°C are calculated to be about 2.8 hours and 14 hours, respectively. The calculated time of 14 hours is in good agreement with the value of between 10 hours and 15 hours from Fig. 4.17. For samples with a fluorine implant dose above 1×10^{15} cm^{-2} , MILC growth does not saturate even after a 40 hour anneal at 550°C. Raman analysis of F implanted samples (2.5×10^{15} cm^{-2}) shows that the 480 cm^{-1} peak is still discernible after a 15 hour anneal and this indicates the presence of amorphous silicon. The fluorine suppression of MILC growth saturation is attributed to the suppression of random

crystallisation in the α-Si.

In this work, at MILC temperatures $\leq$ 500°C a fluorine implant was found to suppress MILC (Fig. 4.27). This result can be partly explained by the lack of fluorine migration at low temperature. Tsai *et al* [108] showed that no F migration occurs at 500°C and this result was confirmed by Jeng *et al* [110]. If there is no migration of fluorine towards the α-Si/SiO_2 interface at 500°C then fluorine cannot suppress random grain nucleation at the interface. A further contribution to the suppression of MILC at low temperatures might arise from the difficulty in annealing the implant damage from the fluorine implant.

4.5 Conclusions

In this work, metal-induced lateral crystallisation of α-Si has been achieved at temperatures down to 428°C. A crystallisation length of 1.2 μm has been achieved for a MILC anneal at 428°C, which is the lowest temperature reported for MILC. This MILC temperature satisfies the process temperature constraint of 450°C, which is imposed by the use of low-cost glass. These results therefore demonstrate the feasibility of using low-cost glass as a substrate for Si nanowire biosensor fabrication.

The effect of fluorine dose on Si MILC has been investigated and an optimum fluorine dose of 2.5×10^{15} cm^{-2} has been identified for MILC at 525°C and 550°C. The use of an optimum fluorine dose of 2.5×10^{15} cm^{-2} gives an increase in MILC length by 29% for a 10 hour MILC anneal at 550°C and by 17% for a 20 hour MILC anneal at 525°C. The action of the F is explained by the suppression of random grain nucleation at the α-Si/SiO_2 interface [31]. The MILC length decreases for a higher F dose, which has been explained by the effect of amorphisation at the α-Si/SiO_2 interface arising from the F implant.

At temperatures $\leq$ 500°C, fluorine was found to give a suppression of the MILC length. This result can be partially explained by the lack of F migration at these low temperatures. Another contributing factor may be difficulties in annealing the implantation damage from the F implant at such low temperatures.

Chapter 5

Metal-induced Lateral Crystallisation of Si Ribbons and Nanowires for Biosensor Applications

5.1 Introduction

In Chapter 2, it was shown that most Si nanowire biosensors are fabricated by top-down e-beam lithography on Silicon-on-Insulator (SOI) wafers. The Si nanowire surface is then functionallised by a silanisation process on its oxide surface [111]. From the point of view of surface chemistry, the functionalisation needs to be selective so that biomolecules attach to the nanowire, but not to the silicon dioxide substrate (the buried oxide layer). Unlike SOI, thin film technology gives various options for the insulator material on which the nanowires are fabricated. Thus, silicon nitride might be adopted as the insulator material for an improved selectivity compared with silicon dioxide during the silanisation process [112]. In addition, suspended nanowires would be of interest because they would provide a larger sensing surface area and hence a higher sensitivity. Thus, in this chapter, a study is undertaken of the metal-induced lateral crystallisation (MILC) of amorphous silicon ribbons, nanowires and sheets on different substrates, Si-on-Nitride, Si-on-Oxide and Si-on-Air.

In TFT technology, the amorphous silicon can be deposited by low pressure chemical vapour deposition (LPCVD) or plasma enhanced chemical vapour deposition (PECVD). This work also investigates and compares MILC of amorphous Si films deposited by these two techniques. In addition, a comparison is made of the crystallisation of amor-

phous Si sheets and ribbons, which are of interest as an alternative to Si nanowires for biosensing [12]. The effect of the ribbon width is studied and compared with MILC results of nanowires.

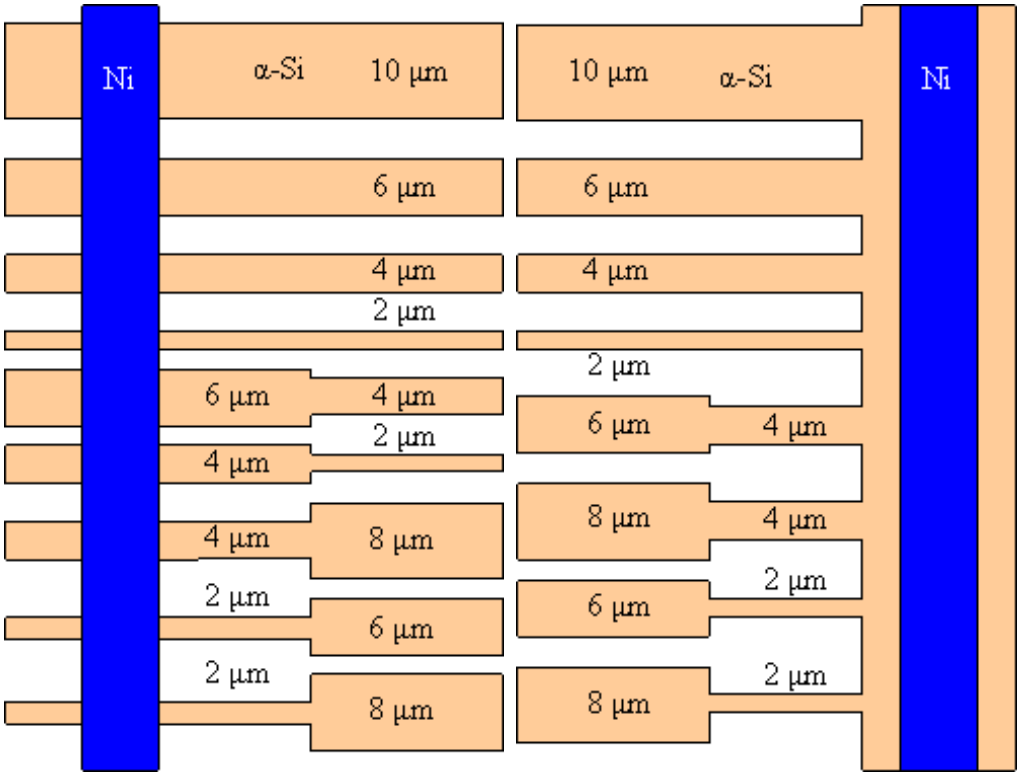
5.2 Amorphous Silicon Ribbon Design

In this section, the ribbon designs for the crystallisation studies are introduced as shown schematically in Fig. 5.1. Two different crystallisation strategies for amorphous silicon ribbons are investigated. Fig. 5.1(a) shows a mask layout in which the nickel bar is located on top of the ribbon. In this case the crystallisation occurs in two directions along the amorphous silicon ribbon. For comparison, Fig. 5.1(b) shows a mask layout in which the nickel bar is placed on the source pad, so that the crystallisation occurs from the source pad onto the ribbon. These two different ribbon crystallisation strategies are compared with crystallisation on a sheet structure, as shown in Fig. 5.1(c).

5.3 Experimental Procedure

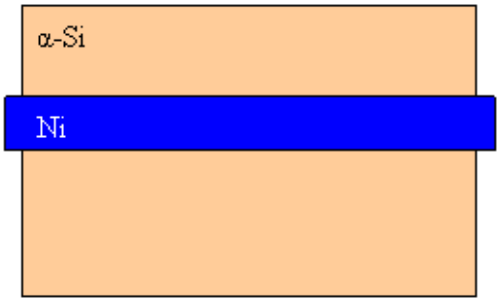
5.3.1 Sample preparation

The process flow for the MILC experiments is shown in Fig. 5.2. The LPCVD α-Si sample fabrication up to and including the amorphous silicon deposition was done in the KTH cleanroom in Sweden by M. M. A. Hakim, as the Southampton cleanroom was not fully operational after the fire. The silicon patterning, dry etch and other following processes were done by the author in the new Southampton Nanofabrication Centre cleanroom. For the PECVD α-Si samples, only the PECVD α-Si deposition was carried out by Oxford Instrument Plasma Technology, Ltd and all other processes were done by the author. Four p-type <100> oriented Si wafers were cleaned and a 100 nm silicon nitride (SiN_x) layer was grown on the Si-on-Nitride wafer (Fig. 5.2(a)). Then, a 500 nm silicon dioxide (SiO_2) layer was deposited on the Si-on-Oxide and the Si-on-Air wafers (Fig. 5.2(b)). Then a 100 nm undoped amorphous silicon layer was deposited on three wafers by LPCVD at 560°C and on one wafer by PECVD at 250°C (Fig. 5.2(c)). Subsequently, all wafers were patterned by photolithography (mask *DP*) and then dry etched in OIPT RIE 80 plus etcher using SF_6 (20 sccm) and O_2 (10 sccm)



(a) Ni on ribbons

(b) Ni on source pad



(c) Ni on Si sheet

FIGURE 5.1: Schematic layouts for metal-induced lateral crystallisation experiments on amorphous silicon ribbons and sheets; (a) Si ribbons with a Ni bar on the ribbons, (b) Si ribbons with a Ni bar on the source pad and (c) a Ni bar on a Si sheet.

at 20°C (pressure 15 mTorr and 13.5 MHz RF power 20 W) (Fig. 5.2(d)). For the Si-on-Air wafer, α-Si ribbons were freed from the underlying oxide using a 7:1 buffered hydrofluoric acid (HF) etch (Fig. 5.2(e)). Then, all the wafers were patterned using photolithography (mask *Ni*). Immediately after a buffered HF dip to remove any native oxide, a 20 nm nickel (Ni) layer was evaporated on all wafers. Then, the Ni was lifted off by dipping the wafers in acetone for 10 minutes at room temperature (Fig. 5.2(f)). Finally, wafers were cleaved into chips and metal-induced lateral crystallisation anneal was carried out in nitrogen for time of 3-20 hours and at temperatures of 428-550°C. The α-Si nanowires used in the crystallisation studies were fabricated using the process

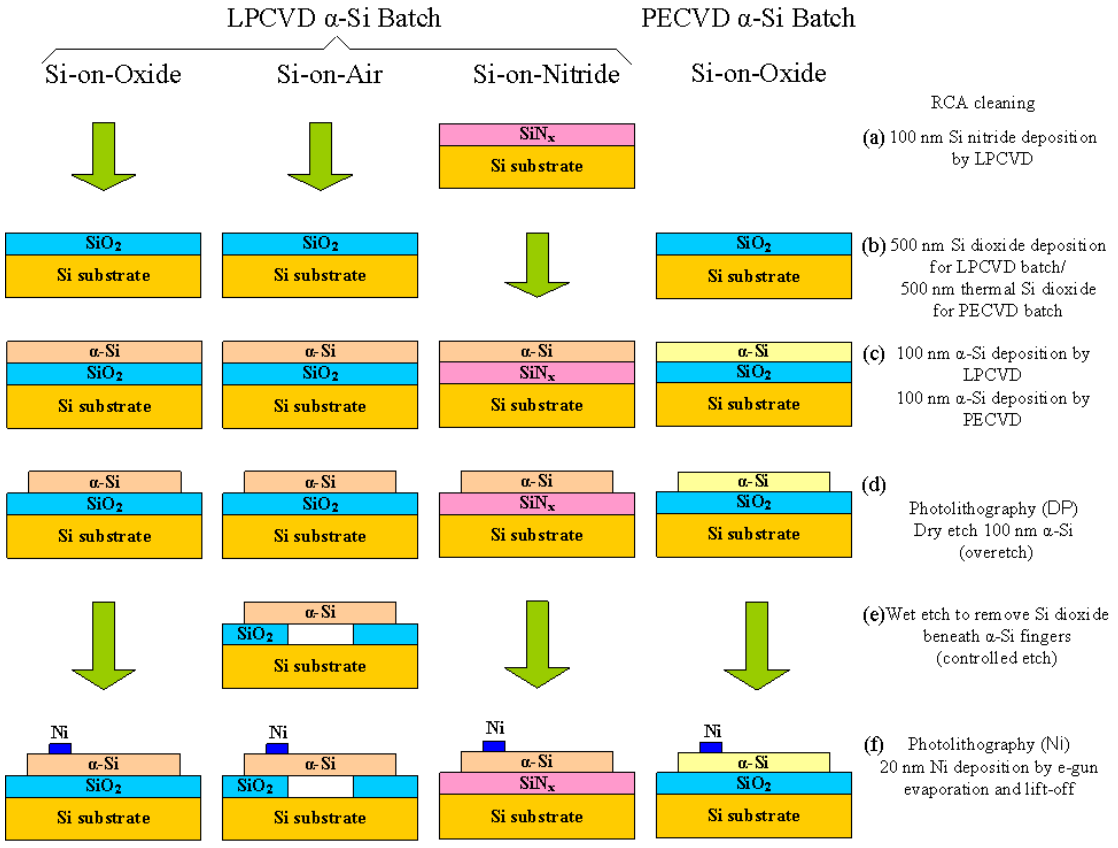
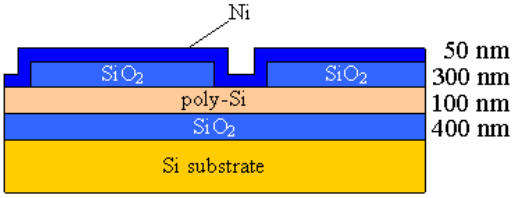


FIGURE 5.2: Process flow for the experiments on the metal-induced lateral crystallisation of amorphous silicon ribbons.

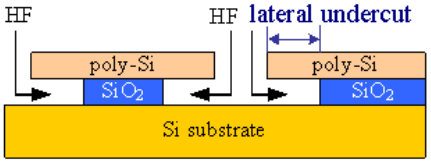
described in Chapter 6. Crystallisation experiments were also performed on α-Si sheets with an oxide cap deposited by chemical vapour deposition. These samples were fabricated using the process in Chapter 4. As the α-Si for the samples in this chapter and the Chapter 4 were deposited in the same run and only Ni was deposited with different evaporators, a comparison between the two sets of samples is valid.

5.3.2 Calibration of SiO_2 wet etch

In this work, the SiO_2 wet etch rate was characterised to give a controlled wet etch for forming the Si-on-Air structures. The samples used in these experiments are shown in Fig. 5.3(a). The samples were dipped in 7:1 buffered HF for durations from 8 minutes to 40 minutes. HF rapidly removes Ni and $NiSi_2$ [31] and then undercuts the polysilicon, as shown in Fig. 5.3(b). The lateral etch of the silicon dioxide was measured using a Nomarski microscope.



(a)



(b)

FIGURE 5.3: Schematics of samples for wet etch calibration (a) before wet etch and (b) after buffered HF etch.

5.3.3 Raman spectroscopy

To investigate the crystallinity of the annealed samples, Raman spectroscopy measurements were performed on both MILC and α-Si regions, as shown in Fig. 5.4. In this work, 633 nm laser was used and the scanning range of Raman shift was from 400 cm^{-1} to 600 cm^{-1}, which includes the crystalline Si peak at 520 cm^{-1} and the amorphous Si peak at 480 cm^{-1} [104]. As for the Raman analysis in Chapter 4, the Raman spectra in this chapter are presented as normalised intensity, which is obtained by dividing the measured intensity with the peak intensity at 520 cm^{-1}. In the normalised Raman spectra, the 480 cm^{-1} peaks for different Si films can be compared.

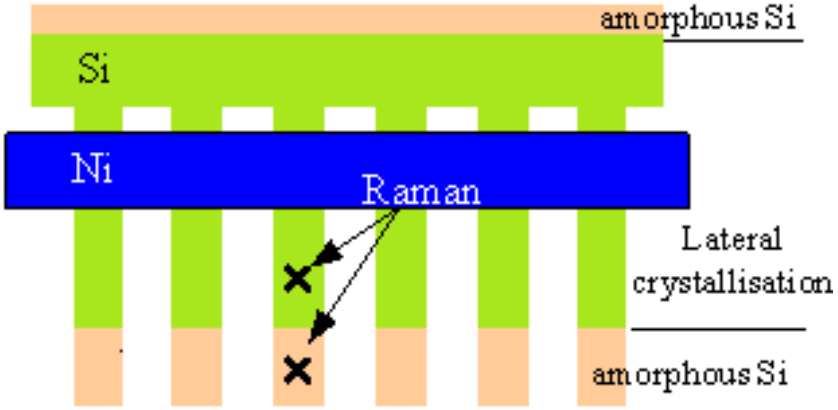
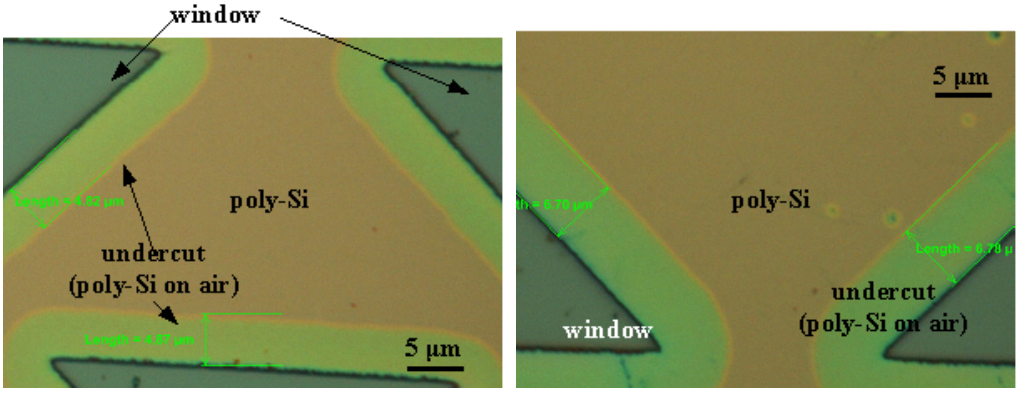


FIGURE 5.4: Schematic diagram showing the locations used for the Raman measurements.

5.4 Results

5.4.1 Etch calibration for Si-on-Air structures

Fig. 5.5(a) shows an optical micrograph of samples etched in 7:1 buffered HF for 30 minutes. The oxide etch undercut can be clearly identified as a yellow-green colour between the etched Si window (in dark green) and the poly-Si (in brown) and can be measured to be about 4.8 μm. A similar result for 40 minute HF etch is shown in Fig. 5.5(b). The undercut was measured to be about 6.7 μm.



(a) (b)

FIGURE 5.5: Nomarski microscope images of samples used for HF etch calibration (a) after a 20 min. HF etch and (b) after a 40 min. HF etch.

Fig. 5.6 shows the lateral undercut as a function of wet etch time in 7:1 buffered HF.

For each etch condition, five measurements were performed and the mean and standard deviation are calculated. The undercut shows a linear characteristic behaviour with etch time and the etch rate is extracted to be 174 nm/min using a linear fitting method. The offset on the x-axis is due to the time taken for the HF to etch through the $Ni/NiSi_2$ and to etch vertically through the SiO_2 layer. We can conclude that the wet etch of SiO_2 can be well controlled by setting the etch time.

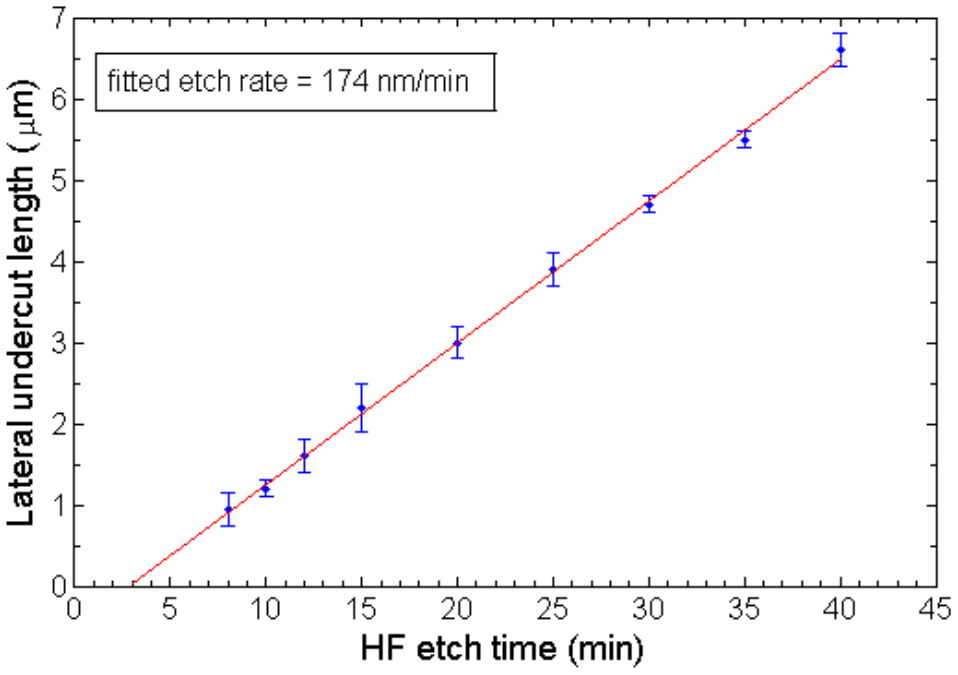


FIGURE 5.6: Calibration of the silicon dioxide etch in 7:1 buffered HF.

The Si-on-Air ribbons were wet etched and characterised by optical microscopy after fabrication. In all cases it was found that the ribbons had sagged in the middle and rested on the underlying silicon surface. Nevertheless, in most cases there was no evidence of breaks in the ribbons, as shown in Fig. 5.7, and hence meaningful MILC experiments could be performed.

5.4.2 Initial amorphous silicon structure before MILC anneal

The deposited amorphous silicon thicknesses were measured to be 100 nm and 60 nm for LPCVD α-Si and PECVD α-Si, respectively, using cross-section SEM. The silicon structure before MILC anneal was investigated using Raman spectroscopy. Fig.

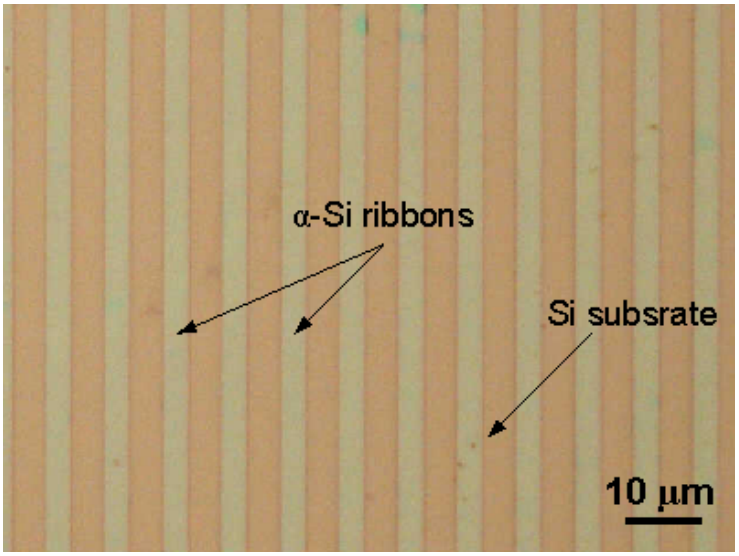


FIGURE 5.7: Nomarski micrograph of Si-on-Air LPCVD α-Si ribbons after a removal of the underlying oxide using 7:1 buffered HF.

5.8 shows normalised Raman spectra for as-deposited LPCVD α-Si deposited on oxide, LPCVD α-Si deposited on nitride and PECVD α-Si deposited on oxide. For the PECVD α-Si deposited on oxide, the 480 cm^{-1} peak is larger in area than the 520 cm^{-1} peak, indicating a mainly amorphous structure. The Si crystalline fraction is calculated using a peak-fitting technique [38][94] to be 1% and this confirms that it is almost fully amorphous. For the LPCVD α-Si deposited on oxide and nitride, the 480 cm^{-1} peak is significantly smaller in area than for the PECVD sample and it is also smaller in area than the 520 cm^{-1} peak. These results indicate the amorphous Si deposited by PECVD is more amorphous than that deposited by LPCVD, which is not superising given the lower deposition temperature for PECVD than LPCVD. The Si crystalline fractions for α-Si deposited on nitride and oxide were calculated to be 17% and 36%, respectively. This difference could be due to the different stresses in amorphous silicon deposition deposited on silicon nitride and silicon dioxide.

5.4.3 Effect of α-Si deposition method on metal-induced lateral crystallisation

Fig. 5.9 compares the results of MILC experiments on amorphous silicon films deposited by PECVD and LPCVD. Fig. 5.9(a) shows results for 4 μm PECVD ribbons after a 550°C MILC anneal for 10 hours and a delineation etch of 20 minutes in 7:1 buffered HF to improve the contrast of the MILC region. The Ni was removed by the delineation etch, leaving a break in the ribbons. The MILC region can be identified as

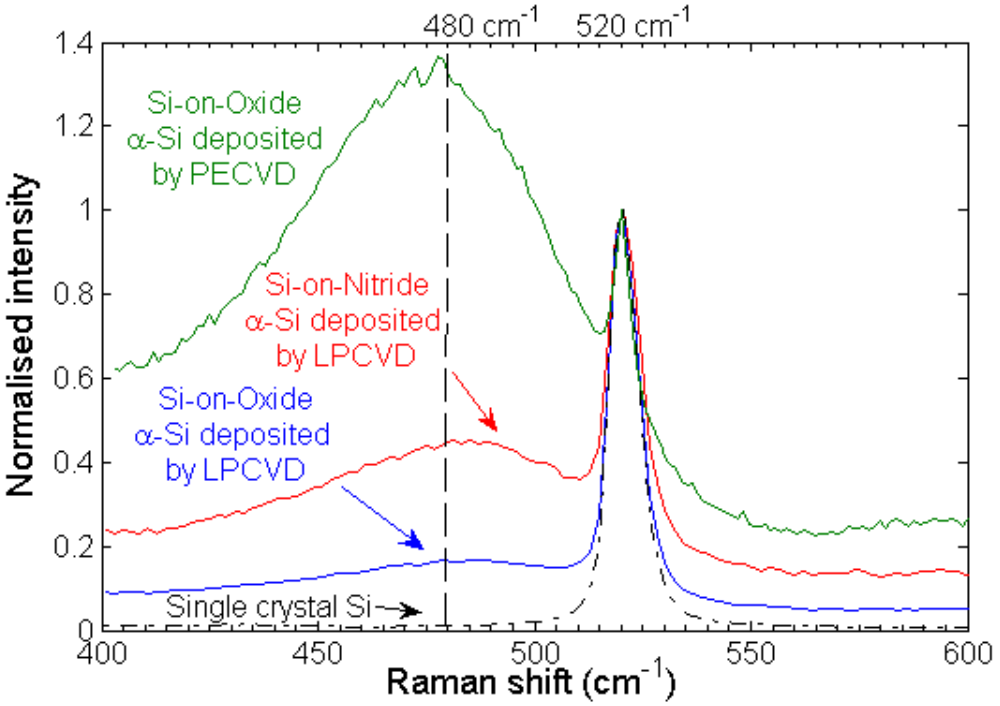
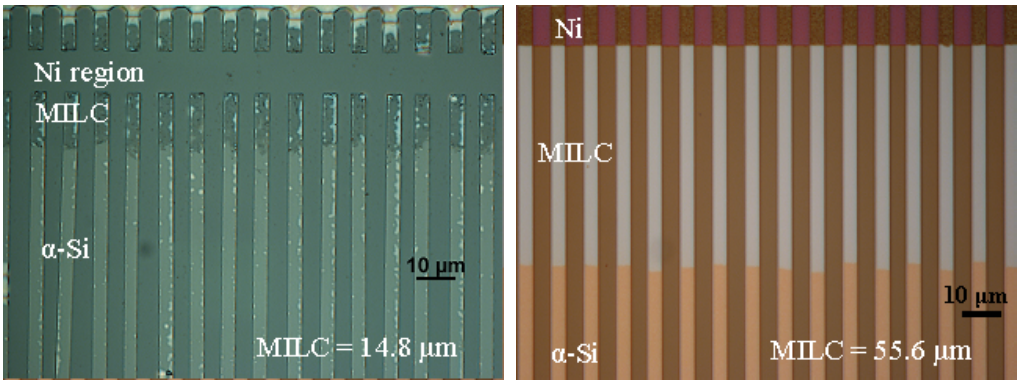


FIGURE 5.8: Raman spectra of as-deposited α-Si deposited by LPCVD and PECVD on SiO_2 and SiN_x.

the dark grey region and MILC length was measured to be 15$\pm$1 μm. The measured values are based on 20 measurements on different ribbons. Fig. 5.9(b) shows similar results for 4 μm α-Si ribbons deposited by LPCVD. No delineation etch was necessary in this case because the MILC region can be clearly identified as pale green region between the Ni (dark red) and α-Si regions (brown). The MILC length was measured to be 56$\pm$1 μm. It is clear therefore that LPCVD α-Si ribbons give a significantly longer MILC length than PECVD α-Si ribbons.

Fig. 5.10 shows the lateral crystallisation length as a function of anneal time for α-Si ribbons deposited by PECVD and LPCVD after anneals at 550°C. Measurements of MILC length were made in 20 locations using an optical Nomarski microscope. It can be seen that the MILC length varies linearly with anneal time for α-Si deposited by both LPCVD and PECVD. LPCVD deposited α-Si gives a significantly longer MILC length than PECVD deposited α-Si. The MILC rates extracted from the slopes are 5.1 μm/hour for LPCVD and 1.3 μm/hour for PECVD.

Fig. 5.11(a) shows Raman spectra measured in the α-Si region of sheet structures after a 550°C 15 hour MILC anneal. Results are shown for samples in which the α-Si was deposited by PECVD and LPCVD. It can be seen that the peak at 480 cm^{-1} is



(a) α-Si deposited by PECVD (b) α-Si deposited by LPCVD

FIGURE 5.9: Nomarski micrographs of α-Si ribbons on oxide after a 10 hour MILC anneal at 550°C. (a) amorphous silicon deposited by PECVD and (b) amorphous silicon deposited by LPCVD. A delineation etch of 7:1 buffered HF for 20 minutes was given to the PECVD α-Si sample but no etch was given to the LPCVD α-Si sample.

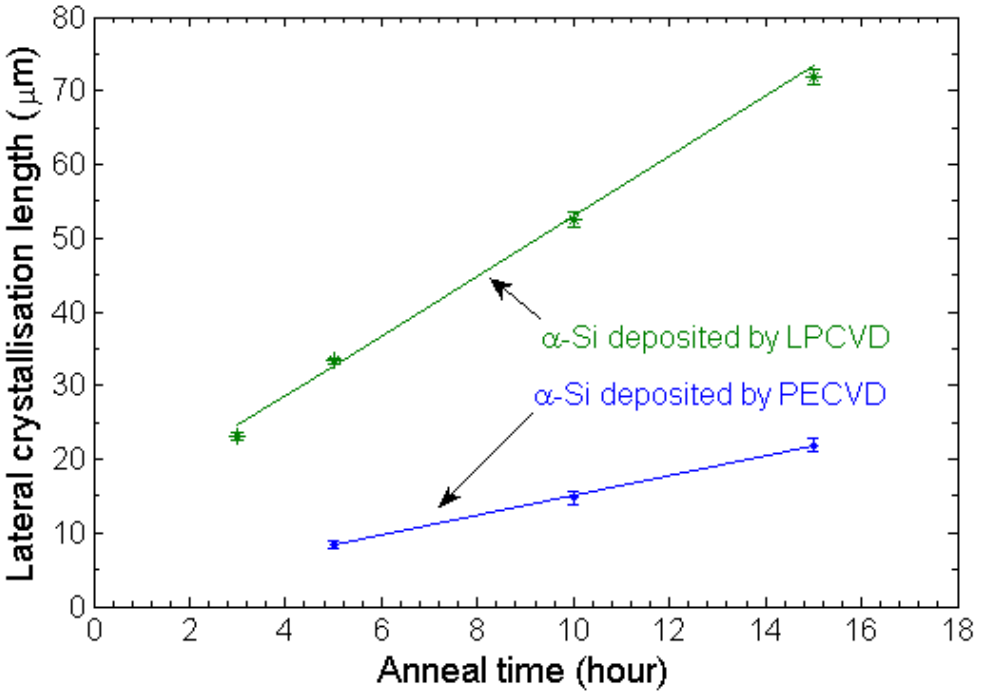


FIGURE 5.10: Lateral crystallisation length as a function of anneal time at 550°C for 4 μm α-Si ribbons on oxide deposited by PECVD and LPCVD. The data is based on measurements using a Nomarski microscope.

clearly visible in the PECVD sample, but cannot be clearly discerned in the LPCVD sample. The values of FWHMs for the 520 cm^{-1} peak are 8.3 cm^{-1} and 9.5 cm^{-1} for the LPCVD and PECVD samples, which indicates that the LPCVD sample is more crystalline. Using the peak-fitting technique, the crystalline fractions can be calculated to be 53% for the LPCVD sample and 30% for the PECVD sample. This result shows that the LPCVD α-Si film is significantly more crystalline than the PECVD α-Si film.

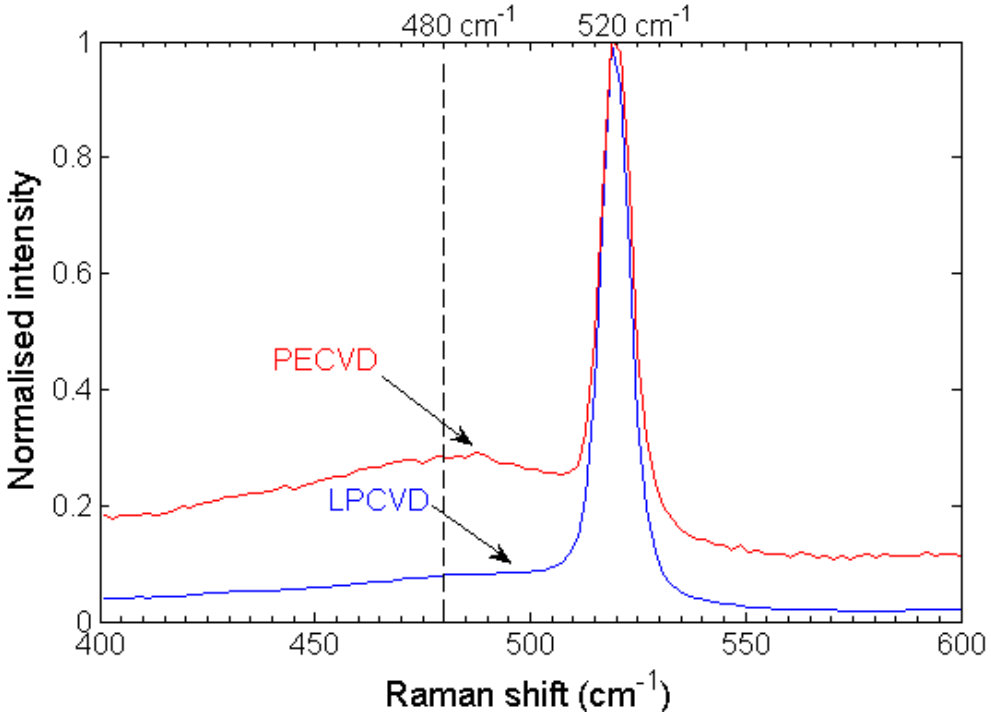
Fig. 5.11(b) shows Raman spectra measured in the MILC region for annealed PECVD and LPCVD samples. In both cases, the 480 cm^{-1} peak is barely discernable and the 520 cm^{-1} peak is sharper for the LPCVD sample (FWHM = 8.3 cm^{-1}) than the PECVD sample (FWHM = 9.4 cm^{-1}). Both of these trends indicate a higher crystallisation fraction. The crystalline fractions for the annealed PECVD and LPCVD samples in the MILC region have been calculated to be 48% and 100%, respectively.

As a dehydrogenation anneal was given to the PECVD sample before the MILC anneal, its effect on MILC was also investigated. Two PECVD α-Si samples with and without a 430°C 30 minute dehydrogenation anneal were given a MILC anneal at 550 °C for 10 hours and their Nomarski micrographs are shown in Fig. 5.12. The MILC anneal was performed in a tube furnace in the temporary cleanroom in which the temperature accuracy was poor, so this result should not be compared with other results in this thesis. The MILC lengths for the samples without and with a dehydrogenation anneal are 11$\pm$0.5 μm and 10$\pm$0.6 μm, respectively. As these values of MILC length fall within the standard deviations (20 measurements), it can be concluded that a dehydrogenation anneal has not had a significant effect on the MILC length.

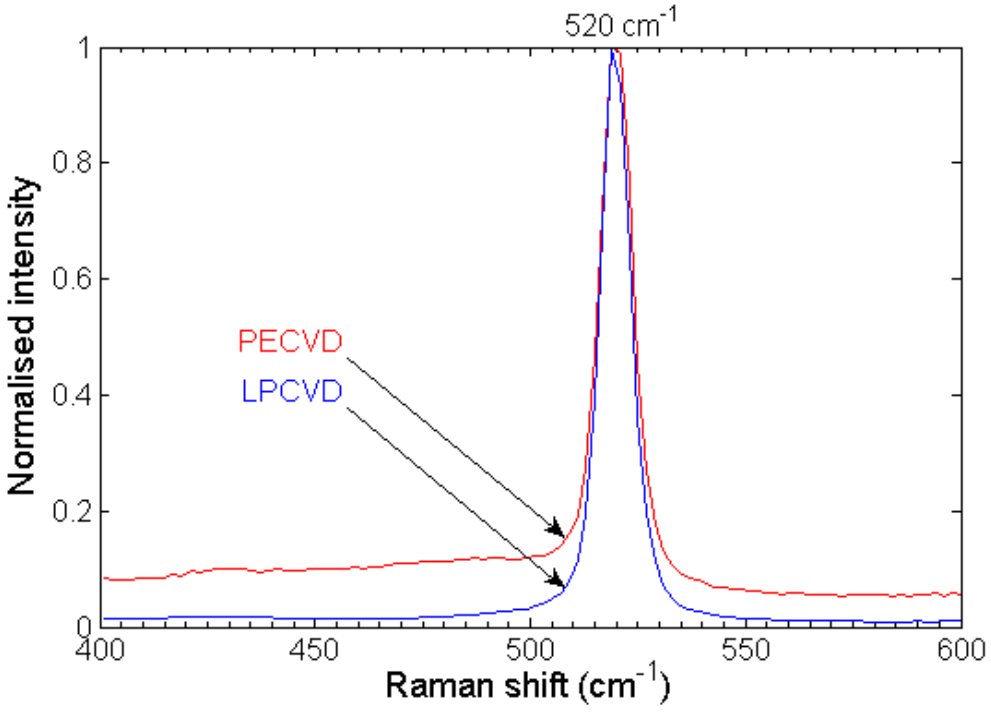
5.4.4 Effect of ribbon width on metal-induced lateral crystallisation

Fig. 5.13 shows an optical micrograph of Si ribbons of different widths for LPCVD α-Si deposited on oxide and annealed at 550°C for 10 hours. No delineation etch was given to the sample. The ribbon widths for mask layouts of 10 μm, 6 μm, 4 μm and 2 μm were measured to be 9.8 μm, 5.7 μm, 3.7 μm and 2.1 μm, respectively. These dimensions are in good agreements with the designed dimensions and thus ribbons are referred to by their mask layout widths. MILC lengths in Fig. 5.13 were measured to be 56.8 μm, 56.5 μm, 52.9 μm and 47.4 μm for ribbon widths of 10 μm, 6 μm, 4 μm and 2 μm, respectively. It can be clearly seen that the MILC length decreases with decreasing ribbon width.

Fig. 5.14 summarises the lateral crystallisation length as a function of ribbon width and

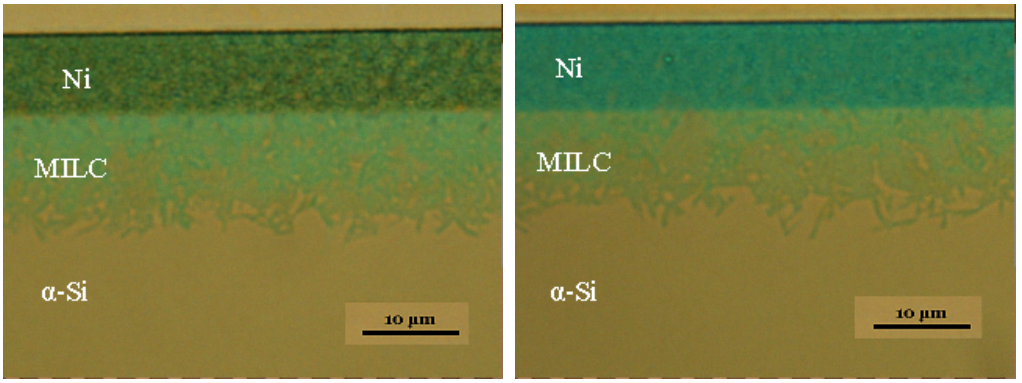


(a) α-Si region



(b) MILC region

FIGURE 5.11: Raman spectra of LPCVD and PECVD α-Si after 15 hour anneal at 550°C (a) Raman spectra from the α-Si region and (b) Raman spectra from the MILC region.



(a) with 430°C anneal (b) without 430°C anneal

FIGURE 5.12: Nomarski micrographs of PECVD α-Si sheet samples after a 10 hour 550°C MILC anneal with (a) and without (b) a dehydrogenation anneal of 30 minutes at 430°C. No delineation etch was given to either samples.

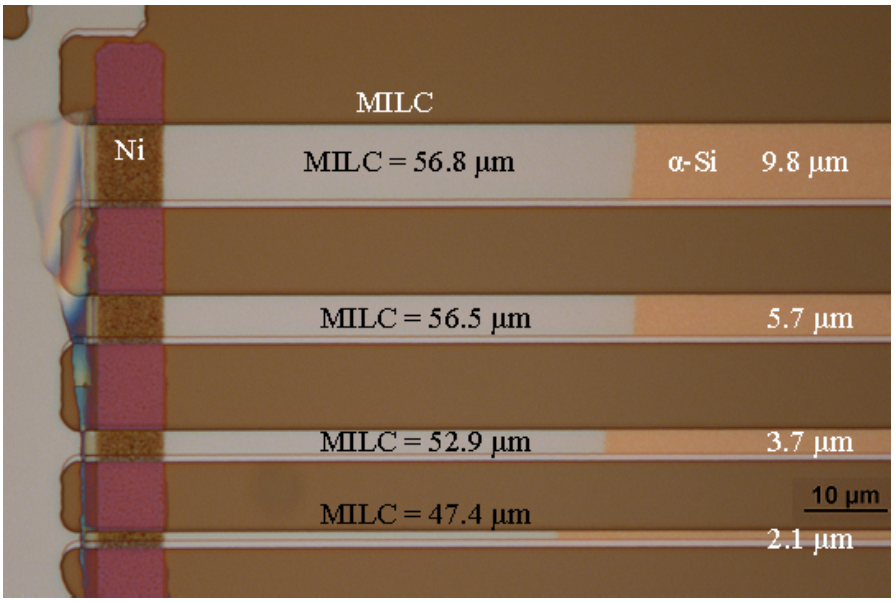


FIGURE 5.13: Nomarski micrograph of lateral crystallisation on LPCVD α-Si ribbons of different widths on oxide after a 550°C anneal for 10 hours. No delineation etch was given to the sample.

makes a comparison with the MILC length on sheet samples. It can be seen that the MILC length decreases from 57 μm to 47 μm as the ribbon width reduces from about 10 μm to 2 μm and the MILC length for the ribbons is slightly less than that for the Si sheet. The rate of decrease of MILC length increases as the ribbon width becomes smaller.

The results in Fig. 5.15 investigate the effect of the Ni location on the MILC length and shows results for Ni placed on the α-Si source pad. Results are shown for LPCVD α-Si

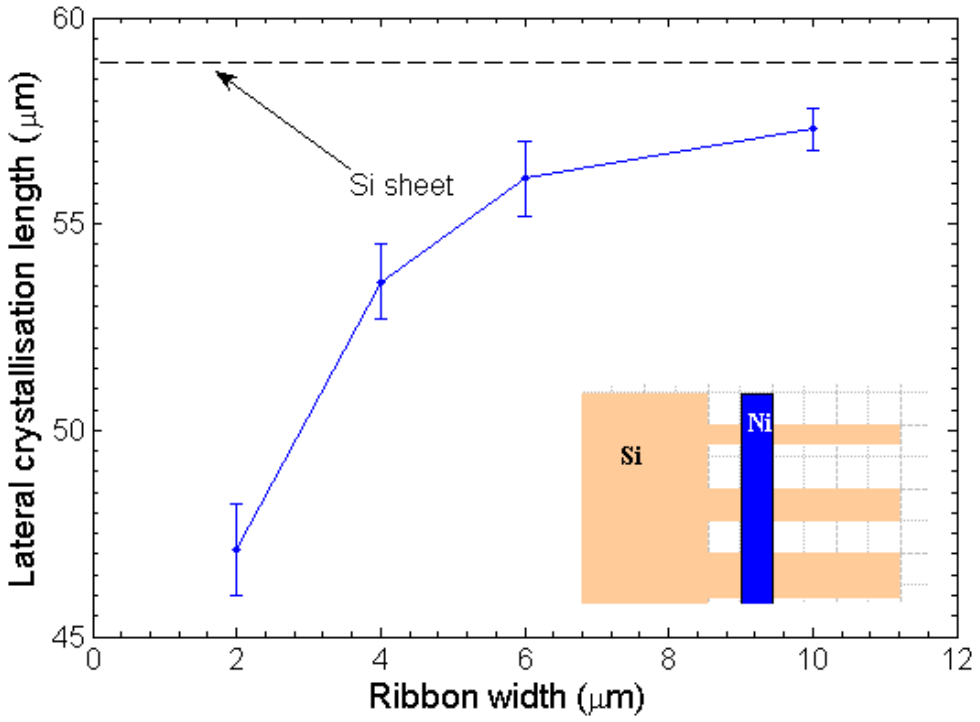


FIGURE 5.14: Lateral crystallisation length as a function of ribbon width for Ni on LPCVD α-Si ribbons on oxide after a 550°C anneal for 10 hours.

deposited on oxide after a 550°C anneal for 10 hours. The widths of these ribbons are the same as those in Fig. 5.13. MILC lengths of 58.7 μm, 57.8 μm, 56.5 μm and 51.8 μm were measured for ribbon widths of 10 μm, 6 μm, 4 μm and 2 μm, respectively.

The measured MILC lengths are summarised in Fig. 5.16 as a function of ribbon width and are compared with results from Fig. 5.14. It can be seen that the MILC lengths are longer when the Ni is placed on the source pad than when it is placed on the ribbon itself. For 10 μm wide ribbons, the MILC length is the same as that measured for the Si sheet.

Fig. 5.17 shows similar results after a MILC anneal at 550°C for 15 hours. This figure shows the same trends as Fig. 5.16, except that MILC lengths are generally longer. For wider ribbons, the MILC lengths are the same as that obtained for an α-Si sheet.

Fig. 5.18 shows results for Ni on the ribbons and compares results for tapers from a wide ribbon to a narrow ribbon (ribbons 1) with results for a taper from a narrow ribbon to a wide ribbon (ribbons 3-5). Ribbon 1 gives a longer MILC length of 52.5 μm than Ribbon 2 with a MILC length of 47.9 μm, which indicating taping to narrow width structure gives a longer MILC length than taping to wide width structure. In addition,

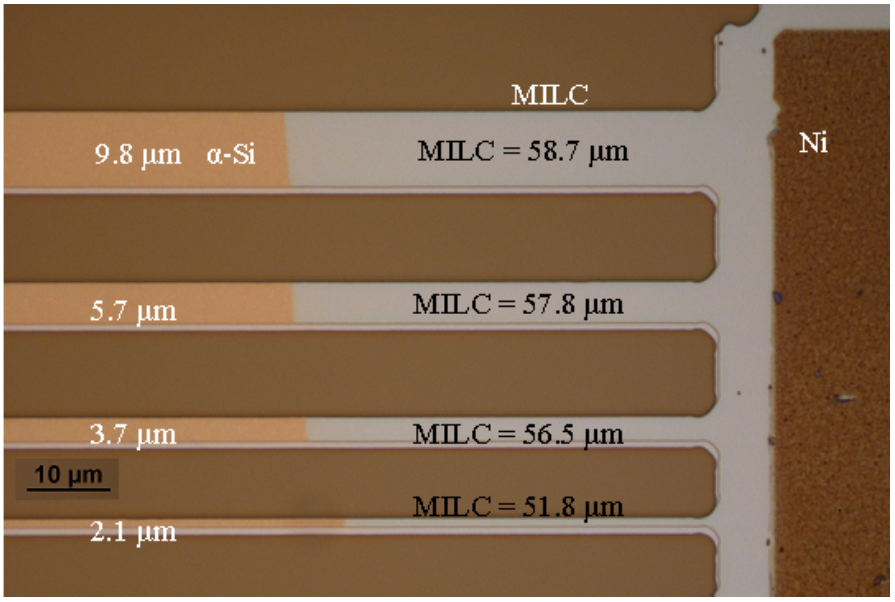


FIGURE 5.15: Nomarski micrograph of lateral crystallisation on Si ribbons of different widths on oxide with Ni on the source pad 550°C anneal for 10 hours. No delineation etch was given.

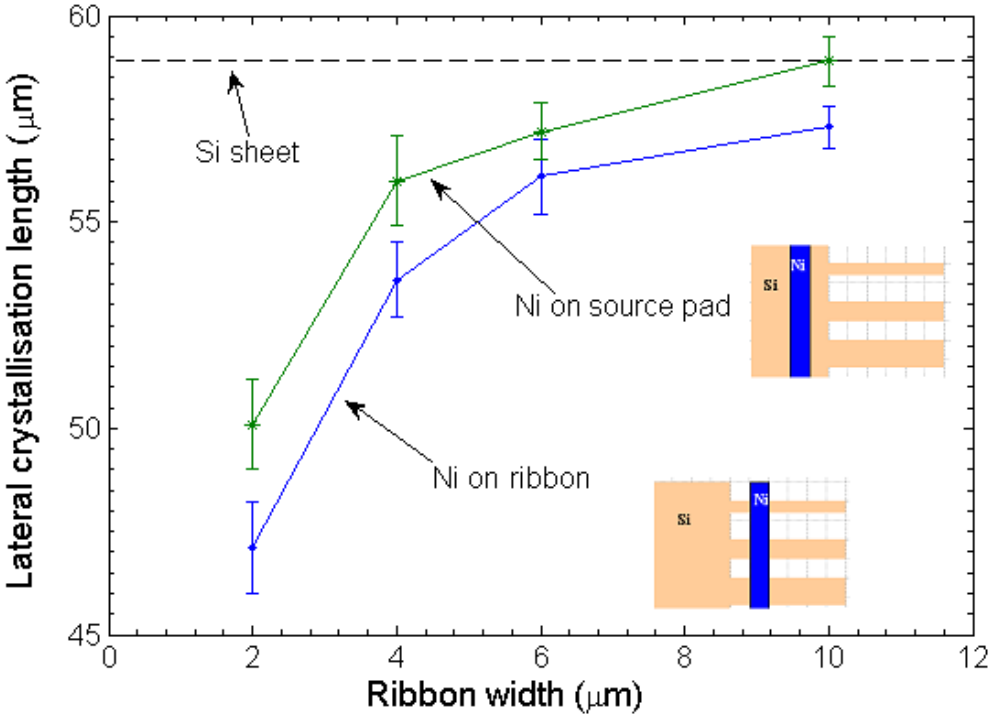


FIGURE 5.16: Lateral crystallisation length as a function of ribbon width for LPCVD α-Si ribbons on oxide after a 550°C anneal for 10 hours. Results are shown for Ni placed on the source pad and the ribbon.

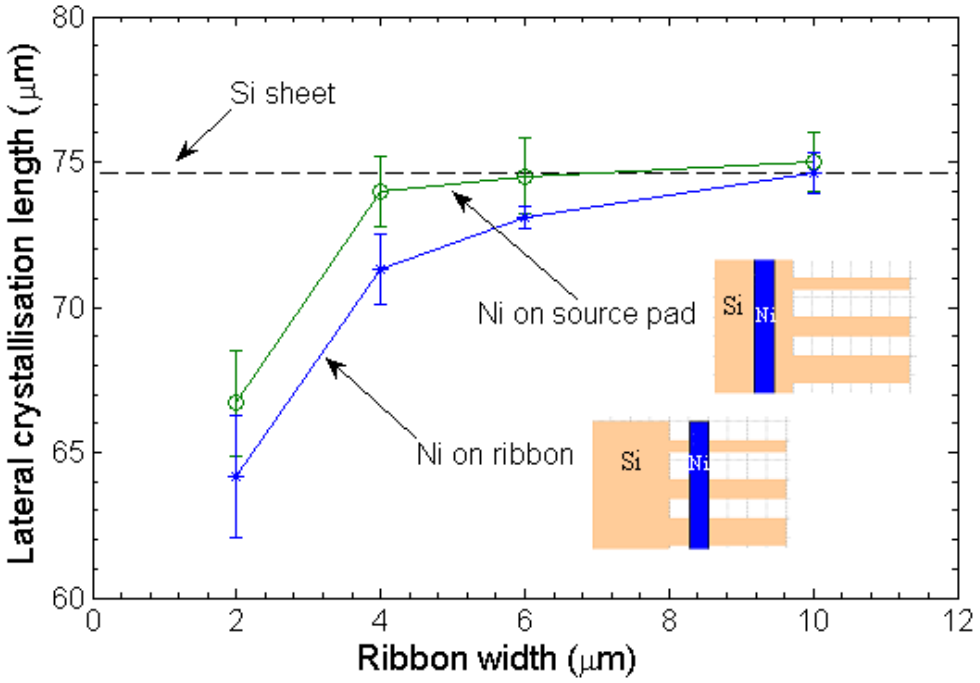


FIGURE 5.17: Comparison of lateral crystallisation length as a function of ribbon width for LPCVD α-Si ribbons on oxide after 550°C anneal for 15 hours. Results are shown for Ni placed on the source pad and the ribbon.

ribbon 4 gives a shorter MILC length of 34.5 μm than Ribbon 3 with a MILC length of 38.1 μm. This shows MILC length decreases when the ribbon taping to a wider width.

Table 5.1 compares lateral crystallisation lengths of ribbons tapering to a wide width and tapering to a narrow width. The MILC lengths for 4 μm and 2 μm ribbons from Fig. 5.16 are also presented in Table 5.1 for a comparison. For Ni on ribbons, MILC length of ribbons tapering from 4 μm to 2 μm is shorter than the MILC length of 4 μm but larger than MILC length of 2 μm ribbons. Thus ribbons tapering to a narrow width give no MILC length increase compared with ribbons without taper. Compared the ribbons without tapers, ribbons tapering from 4 μm to 8 μm give a shorter MILC length. Similar decrease for ribbons tapering to a wide width are seen for ribbons tapering from 2 μm to 6 μm and from 2 μm to 8 μm. For Ni on the source pad, a similar trend is seen that MILC length decreases for ribbons tapering to a wider width.

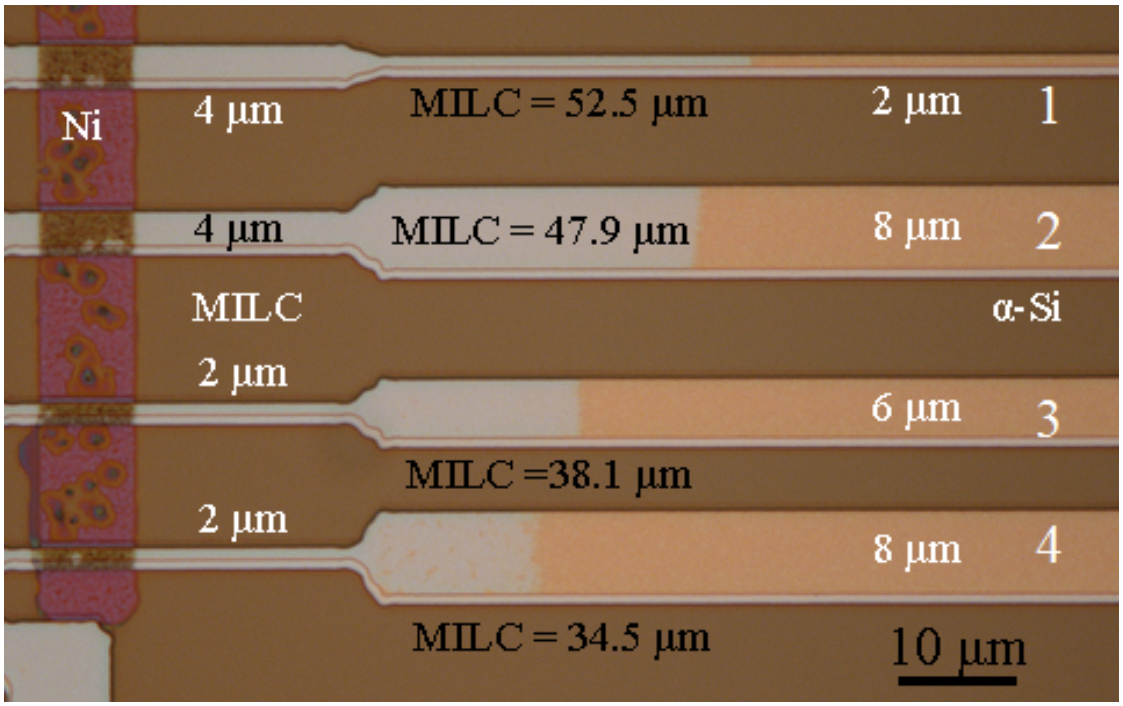


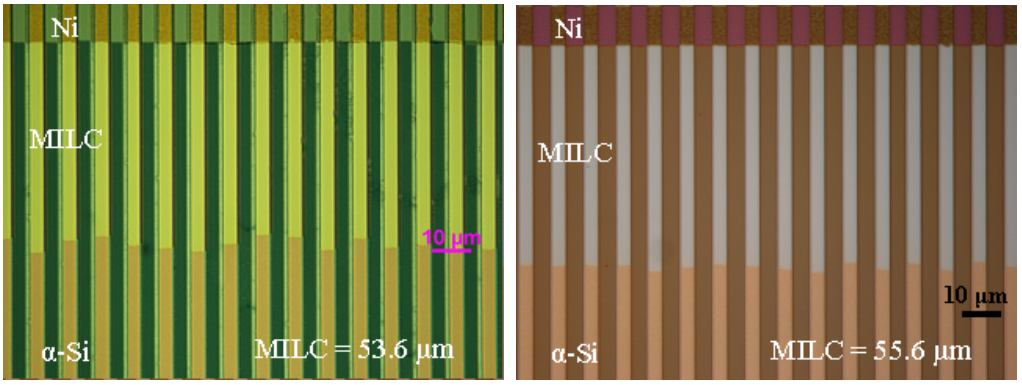
FIGURE 5.18: Nomarski micrographs of LPCVD α-Si ribbons of various widths with Ni on ribbons. The samples were annealed at 550°C for 10 hours and given no delineation etch.

TABLE 5.1: MILC length comparison of ribbons of various widths after a 550°C anneal for 10 hours

ribbon width (μm)	2 / 2	4 / 2	4 / 4	4 / 6	4 / 8
Ni on ribbons MILC (μm)	47.1±1.1	51.2±1.0	53.6±0.9	-	47.9±0.8
Ni on source pad MILC (μm)	50.1±1.1	-	56.0±1.1	54.5±1.4	51.1±1.1
ribbon width (μm)	2 / 2	2 / 6	2 / 8		
Ni on ribbons MILC (μm)	47.1±1.1	38.1±0.5	33.5±0.9		
Ni on source pad MILC (μm)	50.1±1.1	42.8±0.7	39.1±0.7		

5.4.5 Comparison of metal-induced lateral crystallisation on SiN_x and SiO_2

For biosensors, SiN_x may be a better choice of substrate than SiO_2 because it is easier to selectively functionalise nanowires on SiN_2 than SiO_2. In this section, we therefore compare the lateral crystallisation of LPCVD α-Si on SiN_x (Nitride) and SiO_2 (Oxide). Fig. 5.19(a) shows an optical Nomarski micrograph of Si-on-Nitride ribbons after a 550°C MILC anneal for 10 hours. The widths of the Si ribbons were measured to be 3.5 μm. The MILC length is measured to be 54$\pm$2 μm. Results for equivalent Si-on-Oxide samples are shown in Fig. 5.19(b) and the measured MILC length is 56$\pm$1 μm. The MILC length of the Si-on-Nitride is therefore slightly shorter than that of the Si-on-Oxide samples by less than 10%.



(a) Si-on-Nitride (b) Si-on-Oxide

FIGURE 5.19: Nomarski micrographs of LPCVD α-Si samples given a 550°C 10 hour anneal (a) Si-on-Nitride sample and (b) Si-on-Oxide sample. No delineation etch was given to samples.

Fig. 5.20 shows the lateral crystallisation length as a function of anneal time for Si-on-Nitride and Si-on-Oxide LPCVD α-Si ribbons annealed at 550°C. This result confirms that the MILC length for Si-on-Oxide samples is slightly longer than that for Si-on-Nitride samples. For the Si-on-Nitride sample, the MILC length has a linear characteristic with anneal time up to an anneal time of 10 hours and then starts to saturate. Using a linear fit, the MILC rate for shorter anneal times ($\leq$ 10 hours) is 5.0 μm/hour. For the Si-on-Oxide sample, the characteristic is not linear even at low anneal times. However, it is nevertheless clear that the MILC rate for both Si-on-Nitride and Si-on-Oxide samples decreases with anneal time. It can also be seen that the MILC lengths for the two types of samples are roughly the same at a given anneal time.

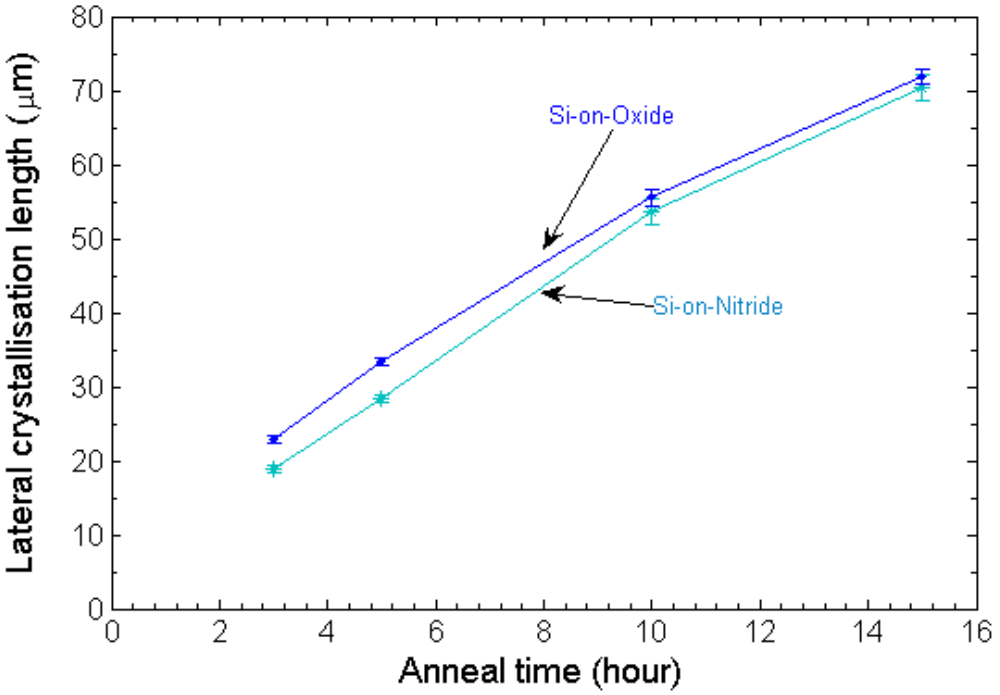


FIGURE 5.20: Lateral crystallisation length as a function of anneal time for Si-on-Nitride and Si-on-Oxide LPCVD α-Si ribbons (width = 4 μm) annealed at 550°C. All data are based on measurements using a Nomarski microscope.

Fig. 5.21 shows the lateral crystallisation length as a function of anneal time for Si-on-Nitride and Si-on-Oxide ribbons annealed at the lower temperature of 500°C. The results show similar trends to those in Fig. 5.20 and in particular the MILC length of Si-on-Nitride samples is slightly shorter than that of Si-on-Oxide samples at this temperature for a given anneal time.

To investigate whether lateral crystallisation can be achieved at temperatures below 500°C, Fig. 5.22 shows the lateral crystallisation as a function of anneal temperature between 428°C and 525°C for 4 μm Si ribbons on Nitride and Oxide substrates after a 20 hour anneal. As found in Chapter 4, MILC for Si-on-Oxide occurs at a temperature as low as 428°C. A similar result is seen for Si-on-Nitride samples. A MILC length of 1 μm can be achieved at an anneal temperature of 428°C. As expected, the MILC rate decreases with decreasing temperature, though it is interesting to note that the rate of decrease reduces as the temperature decreases. This result suggests that lateral crystallisation could be achieved at even lower temperatures. For the same anneal temperature, the MILC length for the Si-on-Oxide samples is about 10% higher than that for the Si-on-Nitride samples.

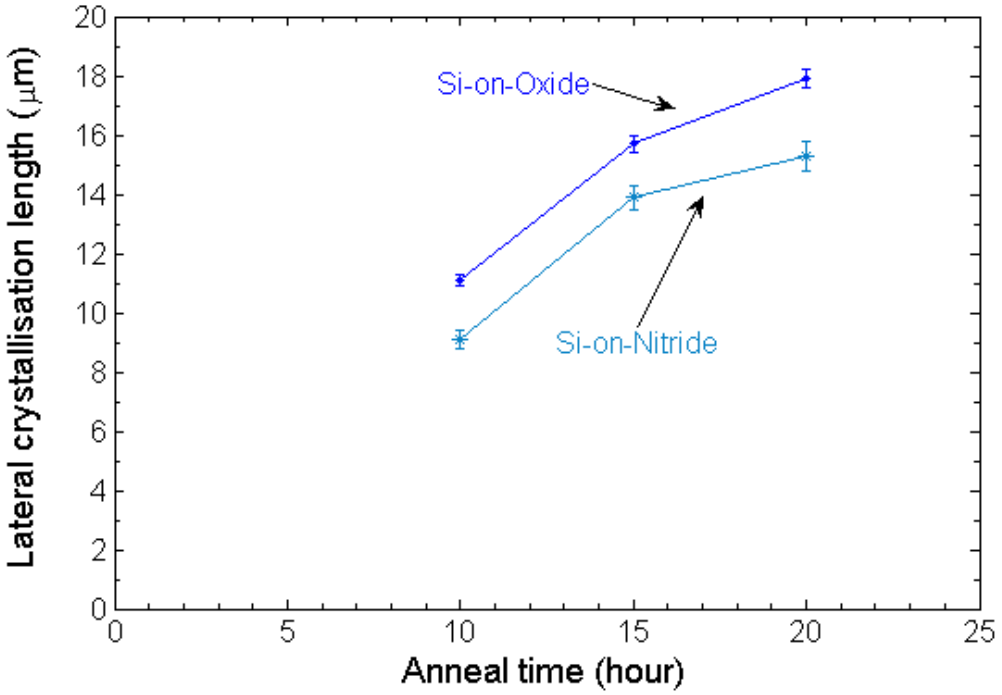


FIGURE 5.21: Lateral crystallisation length as a function of anneal time for Si-on-Nitride and Si-on-Oxide LPCVD α-Si ribbons (width = 4 μm) annealed at 500°C. All data are based on measurements using a Nomarski microscope.

To investigate the crystallinity of Si-on-Nitride and Si-on-Oxide samples, Fig. 5.23 shows Raman spectra in different regions of the sample. Fig. 5.23(a) shows results from the α-Si region well away from the MILC region. The α-Si was deposited by LPCVD and the sample was given a MILC anneal at 550°C for 15 hours. It can be seen that the 480 cm^{-1} peak is significantly bigger for the Si-on-Nitride sample than the Si-on-Oxide sample. Furthermore, the 520 cm^{-1} peak for the Si-on-Oxide sample (FWHM = 8.3 cm^{-1}) is slightly sharper than for the Si-on-Nitride sample (FWHM = 9.4 cm^{-1}), which indicates that the Si-on-Oxide sample is more crystalline. The crystalline fractions calculated to be 32% for the Si-on-Nitride sample and 53% for the Si-on-Oxide sample using the peak division technique. This shows that the Si-on-Nitride sample is more amorphous than the Si-on-Oxide sample.

Fig. 5.23(b) shows Raman spectra measured in the MILC region. The 520 cm^{-1} peak can be identified for both Si-on-Nitride and Si-on-Oxide samples, indicating that MILC regions on both samples are crystalline. No significant difference in the peak sharpness can be identified between the Si-on-Nitride and Si-on-Oxide samples, indicating that the crystallised Si films for the two types of samples have a similar crystalline quality.

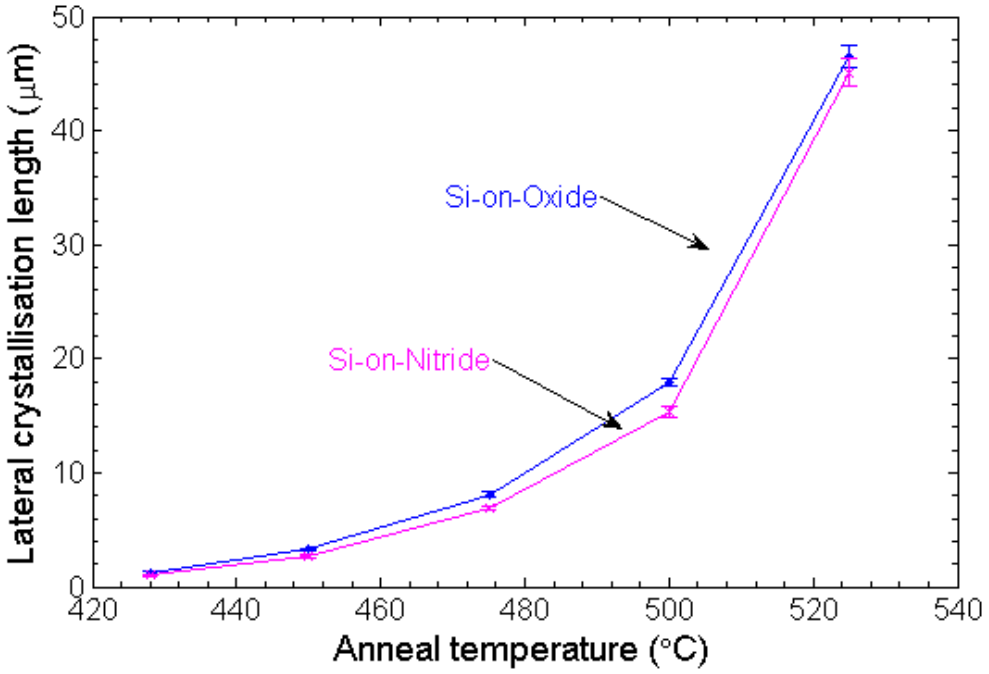
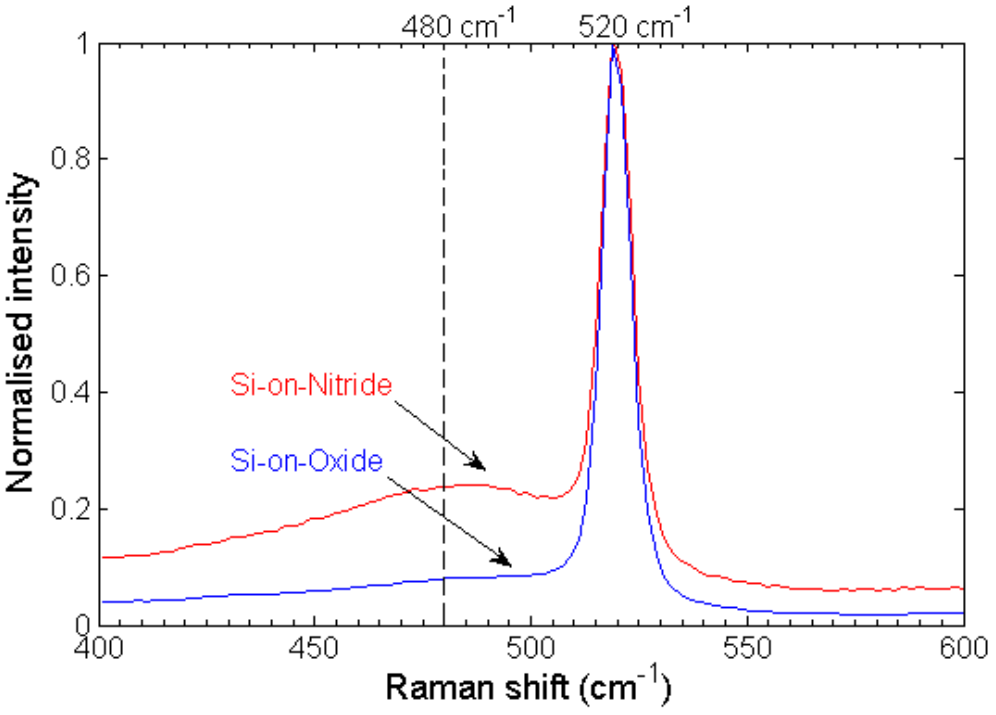


FIGURE 5.22: Lateral crystallisation length as a function of anneal temperature for LPCVD α-Si, 4 μm wide ribbons on nitride (Si-on-Nitride) and oxide (Si-on-Oxide) after 20 hour anneal. All data are based on measurements using a Nomarski microscope.

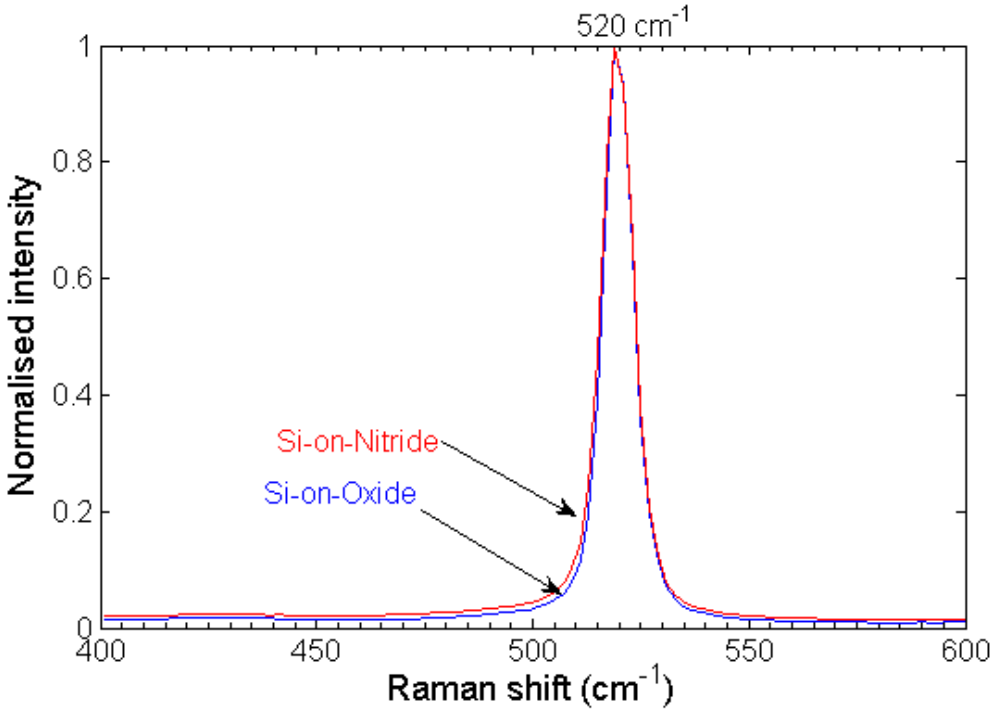
5.4.6 Metal-induced lateral crystallisation of nanowires

Amorphous silicon nanowires fabricated on oxide using the process described in Chapter 6 were also given a MILC anneal at 550°C for 10 hours. Results are shown in Fig. 5.24 and the MILC region can be identified from the white contrast adjacent to the Ni region. The MILC length is variable from nanowire to nanowire and in Fig. 5.24 varies from 10 μm to 14 μm. Measurements on 20 different nanowires give a MILC length of 12.6$\pm$4.4 μm.

A comparison of MILC on nanowires and ribbons after a 550°C MILC anneal for 10 hours as shown in Fig. 5.25, where the MILC length is plotted as a function of ribbon or nanowire width. The MILC length for the nanowire is below the trend for the ribbons, indicating that lateral crystallisation is more difficult in nanowires than ribbons. It is also seen that the MILC length variation for nanowires is significantly larger than ribbons. Nevertheless, these results do show that polysilicon nanowires can be fabricated by MILC at a temperature that is significantly lower than the typical polysilicon deposition temperature of around 625°C.



(a) α-Si region



(b) MILC region

FIGURE 5.23: Raman spectra of LPCVD deposited α-Si on nitride (Si-on-Nitride) and oxide (Si-on-Oxide) after a 15 hour anneal at 550°C at (a) signal measured in the Si region far from MILC front and (b) signal measured in the MILC region.

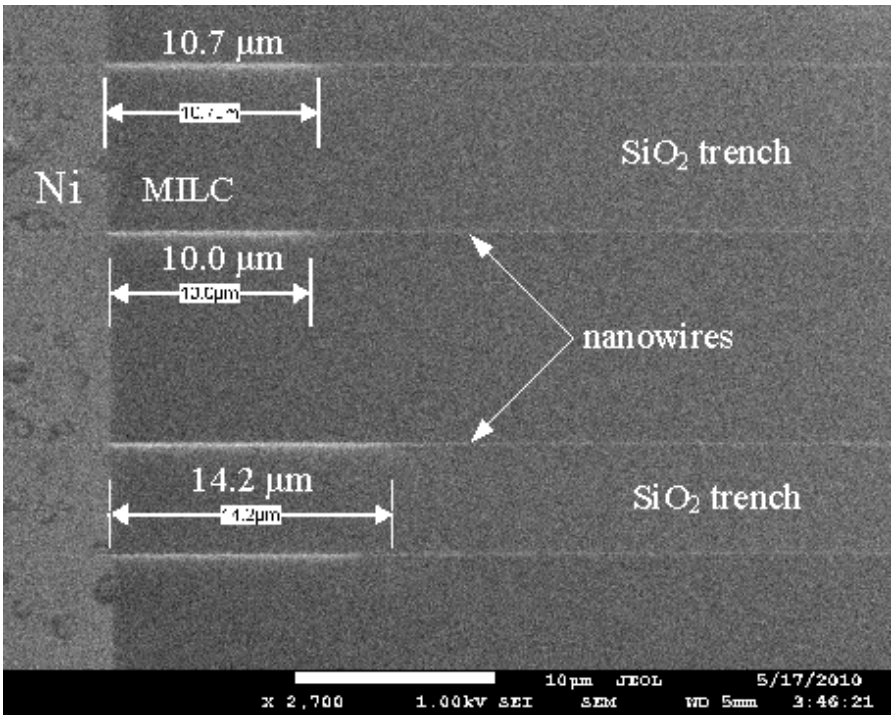


FIGURE 5.24: Plan view SEM micrograph of crystallised LPCVD α-Si nanowires on oxide after a 550°C anneal for 10 hours. No delineation etch was given.

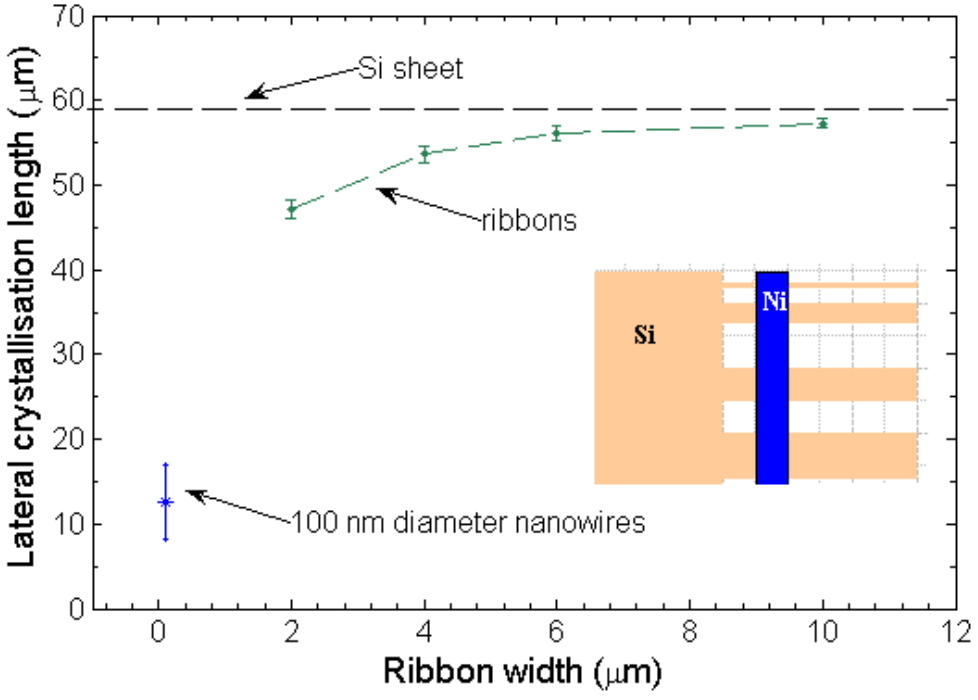


FIGURE 5.25: Lateral crystallisation length as a function of ribbon width for LPCVD α-Si ribbons and nanowires on oxide after a 550°C anneal for 10 hours. Nanowires and ribbons were formed by LPCVD α-Si.

5.4.7 Metal-induced lateral crystallisation of Si-on-Air ribbons

As discussed above, suspended nanowires or ribbons should provide increased sensitivity for biosensing because functionalisation could be performed on all sides of the nanowire or ribbon. In addition, the work in Chapter 4 shows the Si/SiO_2 interface is the preferred location for random crystallisation, which suppresses MILC growth. In this section, the results of MILC experiments on Si-on-Air structures are presented and compared with the results of Si-on-Oxide structures without and with an oxide cap. These samples can be considered as α-Si sheets with oxide on one side and oxide on both sides, respectively.

Fig. 5.26 compares the results of MILC experiments on Si-on-Air and Si-on-Oxide ribbons and on Si-on-Oxide sheets with and without an oxide cap after a 550°C anneal for 10 hours. The lateral crystallisation length for Si-on-Air ribbons is measured to be 72$\pm$3 μm from the colour change in Fig. 5.26(a). For comparison, the MILC length of the Si-on-Oxide ribbons (in Fig. 5.26(b)) is measured to be 56$\pm$1 μm. Thus, Si-on-Air samples show a significant improvement in MILC length of 32%. For Si sheet samples, the MILC lengths for Si-on-Oxide α-Si sheets with and without an oxide cap are measured to be 57$\pm$1 μm and 45$\pm$1 μm, respectively. Thus the samples without an oxide cap show a significant improvement in MILC length of 27%. These results indicate that the MILC length can be increased by removing the Si/SiO_2 interface at either side of the α-Si sheet.

Fig. 5.27 shows the lateral crystallisation length as a function of anneal time at 550°C for 4 μm Si-on-Air and Si-on-Oxide ribbons and Si-on-Oxide sheets with and without an oxide cap. The Si-on-Air samples show a significantly improved MILC length for all anneal times. Compared with the Si-on-Oxide sheet with an oxide cap, the Si-on-Oxide sheet without an oxide cap gives a significant increase in MILC length. Therefore, these results further confirm that the Si-on-Air structure gives an increase in MILC length compared with the Si-on-Oxide structure and that an oxide cap degrades the MILC length. The slightly higher MILC length for the Si-on-Oxide sheet than the Si-on-Oxide ribbons has been seen before in Fig. 5.16.

5.5 Discussion

Much work has been done on the lateral crystallisation of amorphous silicon deposited by LPCVD, covering anneals ranging from 500°C to 565°C [31][32][47] [53][54][57]

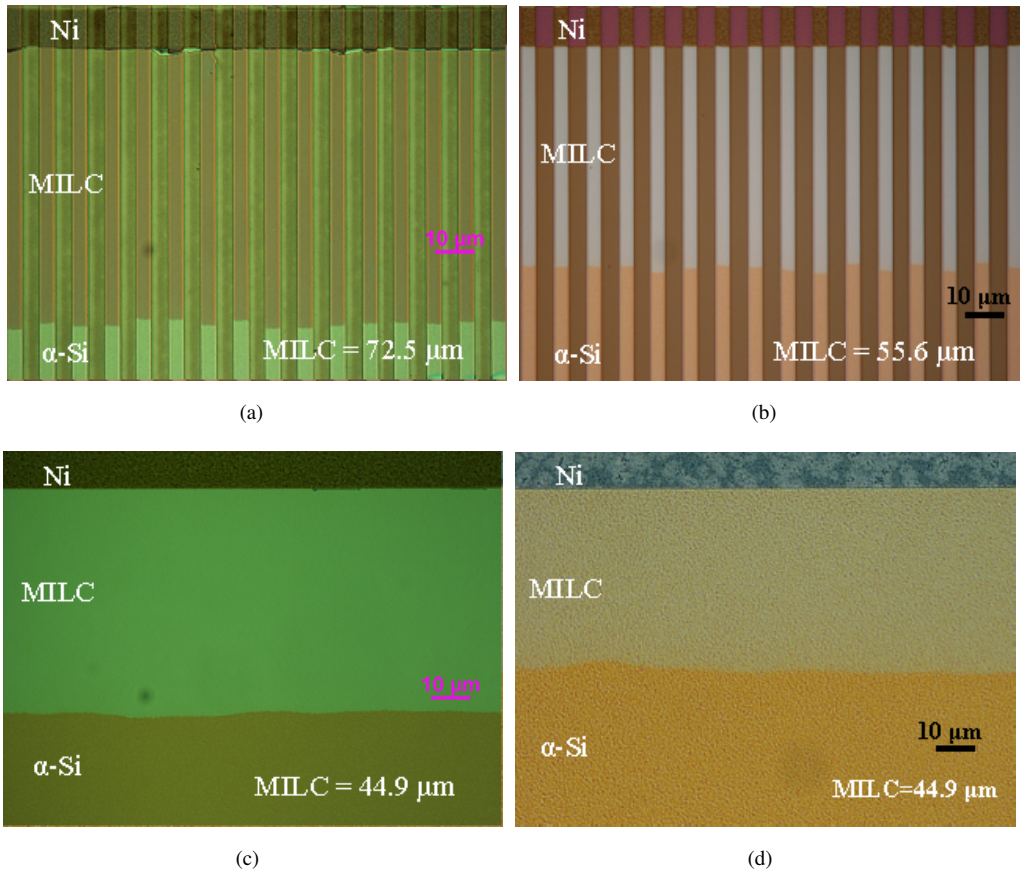


FIGURE 5.26: Nomarski micrographs of LPCVD α-Si samples annealed at 550°C for 10 hours (a) 4 μm wide α-Si ribbons on air (Si-on-Air), (b) 4 μm wide α-Si ribbons on oxide (Si-on-Oxide), (c) α-Si sheets without an oxide cap and (d) α-Si sheets with an oxide cap.

[61][63][65][70][113][114][115]. There are also some published results on poly-Si thin film transistors fabricated using PECVD α-Si [32][57], but only a few results have been reported on MILC rates in PECVD α-Si [60][116]. So far, no work has been published that compares MILC in PECVD and LPCVD under the same anneal conditions. A comparison of the MILC rates obtained at 550°C in this work with those reported in literature is shown in Table 5.2. The MILC rate for Si-on-Oxide samples in this work of 5.1 μm/hour is slightly higher than the reported MILC rate of 3.6-4.0 μm/hour, but is nevertheless reasonably consistent with the literature values. For the PECVD α-Si film, the MILC rate in this work is very similar to that in [60], which was deposited under similar conditions. The α-Si deposition temperature was not given in [116] and hence it is not possible to draw any conclusions on why their MILC rate was higher.

The Raman results in Fig. 5.11 show that the PECVD samples are less crystalline than the LPCVD samples after a MILC anneal of 550°C for 15 hours. It is also found in

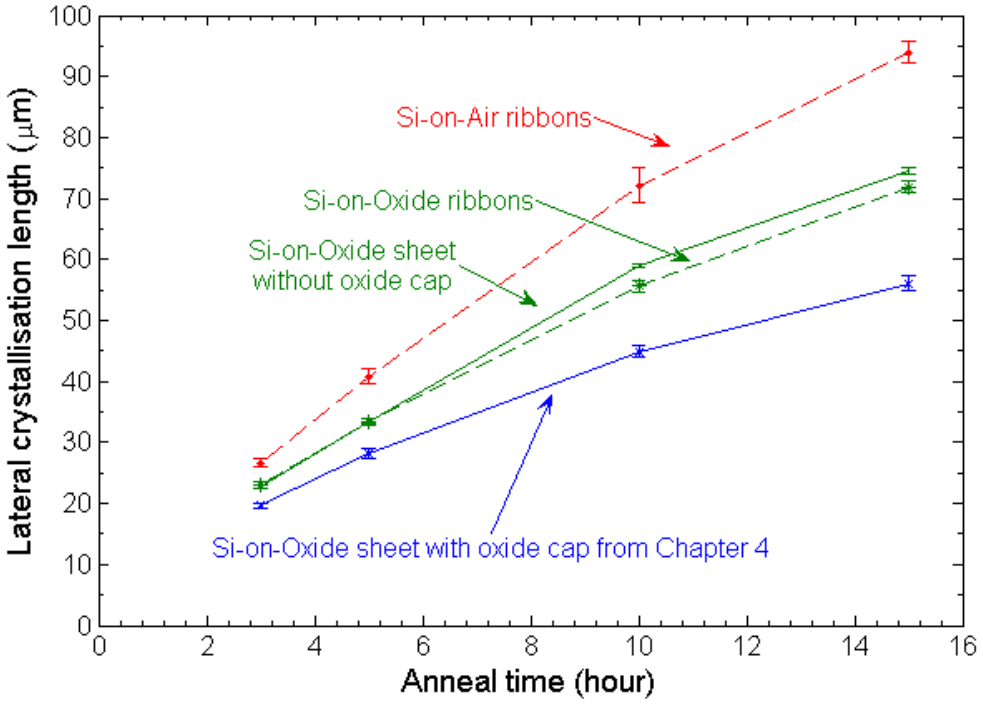


FIGURE 5.27: Lateral crystallisation length as a function of anneal time for Si-on-Air and Si-on-Oxide 4 μm wide ribbons and Si-on-Oxide sheets without and with an oxide cap after a 550°C anneal. On all samples, the α-Si was deposited by LPCVD. All data are based on measurements using a Nomarski microscope.

TABLE 5.2: Comparison of MILC rates obtained on Si-on-Oxide samples after a 550°C MILC anneal in this work and in the literature

	Substrate	MILC rate	α-Si deposition	Deposit. Temp.	α-Si thickness
this work	SiO_2	1.3 μm/h	PECVD	250°C	60 nm
this work	SiO_2	5.1 μm/h	LPCVD	560°C	110 nm
this work	SiN_x	5.0 μm/h	LPCVD	560°C	100 nm
[57]	SiO_2	3.6 μm/h	LPCVD	550°C	50 nm
[65]	SiO_2	4.0 μm/h	LPCVD	500°C	60 nm
[61]	SiO_2	3.8 μm/h	LPCVD	550°C	100 nm
[70]	SiO_2	3.6 μm/h	LPCVD	450°C	50 nm
[116]	SiO_2	3.5 μm/h	PECVD	unknown	50-100 nm
[60]	SiO_2	1.4 μm/h	PECVD	250°C	100 nm

Fig. 5.8 that the PECVD α-Si was significantly more amorphous than the LPCVD α-Si immediately after deposition. This result is consistent with the lower deposition temperature used for the PECVD films, as shown in Table 5.2. The dramatically lower MILC rate for the PECVD α-Si samples therefore indicates that the presence of some small grains of polysilicon in the α-Si aids lateral crystallisation.

Si-on-Nitride samples were found to give a slightly shorter MILC length than equivalent Si-on-Oxide samples (Fig. 5.22). The Raman results (in Fig. 5.23) show that the Si-on-Nitride samples are more amorphous than the Si-on-Oxide samples after the MILC anneal. The Raman results in Fig. 5.8 also show that the Si-on-Nitride samples are more amorphous than the Si-on-Oxide samples after deposition. Thus the crystallinity of the as-deposited α-Si layer has a strong influence on the MILC length, as was observed for the samples deposited by PECVD and LPCVD (in Fig. 5.10). For Si-on-Oxide structures, Hakim *et al* [31] showed that the MILC rate is limited by random grain nucleation at the bottom of the α-Si layer, which is due to a tensile stress induced by the SiO_2 layer [38]. The difference in crystallinity for the Si-on-Oxide and the Si-on-Nitride could therefore be attributed to a different stress in the Si-on-Oxide and Si-on-Nitride samples. Kimura *et al* [38] reported that a SiN_x cap suppressed solid-phase crystallisation due to the suppression of random crystallisation, as a result of the compressive stress introduced by the silicon nitride layer. Therefore, the shorter MILC length for PECVD α-Si samples and the shorter MILC length for Si-on-Nitride samples could both be explained by a more amorphous layer after the deposition.

As Ni transport in silicon contributes to the MILC growth, the MILC rate can be modelled using a similar expression to that used to model Ni diffusion [107]:

$$v_{MILC} = A_0 \exp(-\frac{E_a}{kT}) \tag{5.1}$$

where v_{MILC} is the MILC growth rate and A_0 and E_a are the MILC growth coefficient and activation energy, respectively. To extract A_0 and E_a, the expression of Eq. (5.1) can be rewritten as:

$$\ln v_{MILC} = -\frac{E_a}{kT} + \ln A_0 \tag{5.2}$$

Here, E_a and A_0 can be calculated from the slope and offset of a graph of $\ln v_{MILC}$ against E_a. At lower temperatures ($\leq$ 525°C), spontaneous crystallisation is assumed to be insignificant and thus the MILC length is assumed to vary linearly with anneal time, as shown in Fig. 5.20. Neglecting the nucleation time, the MILC rates at different temperatures can be calculated from the MILC length divided by 20 hours. Fig. 5.28

presents a plot of MILC rate against $1/kT$ for Si-on-Oxide and Si-on-Nitride samples. The trend line from data in [106] is also plotted for comparison. It can be seen that the two plotted curves are parallel and linear, indicating that Eq. (5.1) is valid at temperatures from 525°C down to 428°C. A similar trend was seen in Cheng's work [106] but at temperatures above 550°C. The activation energies, E_a, for Si-on-Nitride and Si-on-Oxide, can therefore be extracted to be 1.86 eV and 1.82 eV, respectively, whilst the MILC growth coefficients, A_0, for Si-on-Nitride and Si-on-Oxide, can be extracted to be 9.9×10^{11} μm/hour and 6.2×10^{11} μm/hour, respectively. The activation energies are similar for Si-on-Oxide and Si-on-Nitride samples, indicating a similar growth mechanism for both types of sample. An activation energy of 2.08 eV was reported in Cheng's work [106], which is higher but reasonably consistent, given difference in amorphous silicon deposition conditions.

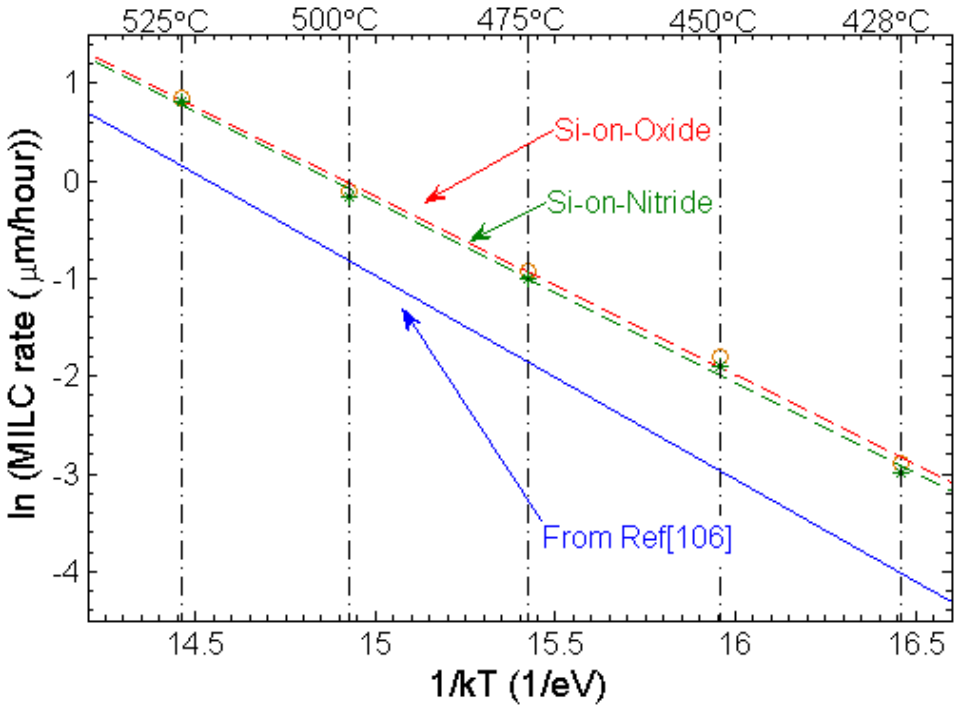


FIGURE 5.28: MILC rate as a function of $1/kT$ for Si-on-Oxide and Si-on-Nitride samples. The data from [106] is also presented for comparison.

The results in Fig. 5.27 show that Si-on-Air structures have significantly increased MILC lengths compared with the Si-on-Oxide structures and that Si-on-Oxide structures without an oxide cap have significantly longer MILC lengths than Si-on-Oxide sample with an oxide cap. As discussed in Chapter 4, MILC length is increased by suppressing random crystallisation, which occurs preferentially near the α-Si/SiO_2 in-

terface [31]. The Si-on-Oxide structure with no oxide cap can be considered as one surface 'on air' and the other surface 'on oxide', whilst the Si-on-Oxide structure with an oxide cap can be considered as both surfaces 'on oxide'. When the α-Si/SiO_2 interface is removed, it would be expected that random crystallisation would be significantly suppressed [41]. Therefore, the MILC improvements for the Si-on-Air structure over the Si-on-Oxide structure and the Si-on-Oxide structure without an oxide cap over the Si-on-Oxide structure with an oxide cap could be explained by the suppression of random crystallisation due to the removal of the α-Si/SiO_2 interface.

To further investigate the effect of an oxide cap, fluorine has been implanted into samples with and without an oxide cap. A comparison of MILC lengths is presented in Fig. 5.29. An oxide cap gives an apparent suppression of the MILC length and this suppression can be counteracted by a F implant. This is explained by the suppression of random crystallisation at the α-Si/SiO_2 interface by the fluorine. Results also show that a fluorine implant gives a more significant improvement of the MILC length for samples with an oxide cap than samples without an oxide cap and this is expected as samples with an oxide cap have two α-Si/SiO_2 interfaces that cause random crystallisation.

The metal-induced lateral crystallisation length was found to decrease with decreasing ribbon width (Fig. 5.16) in Si-on-Oxide samples. Grain growth during MILC tends to occur in two main directions, with needle-like grains lying along 70° and 110° directions [58]. When MILC occurs in sheet samples, the grain growth can occur without any geometrical constraints and in this case the MILC length is limited by random grain nucleation at the bottom of the α-Si film, as discussed above. In α-Si ribbons, grain growth during MILC is likely to be inhibited when the growing grains intersect the edge of the ribbon as nickel can become trapped. This mechanism would be expected to reduce the MILC rate and would explain the decreasing MILC length with decreasing ribbon width in Fig. 5.16. The slightly longer MILC length for the structure with the Ni bar on the source pad (Fig. 5.16) could be explained by the same model, as MILC growth is faster in the sheet region than ribbons. The results in Fig. 5.18 for tapered ribbons could also be explained by a similar mechanism. The lower MILC length for α-Si ribbons that taper from a narrow width to a wide width could be explained by the effect of the narrow ribbon in limiting the supply of Ni to the wide ribbon due to Ni trapping at the ribbon edges.

As far as the author is aware, no results have been reported on metal-induced lateral crystallisation in α-Si nanowires. The results in Fig. 5.25 show that the MILC length for the α-Si nanowires lies below the trend line for the α-Si ribbons. Additional factors

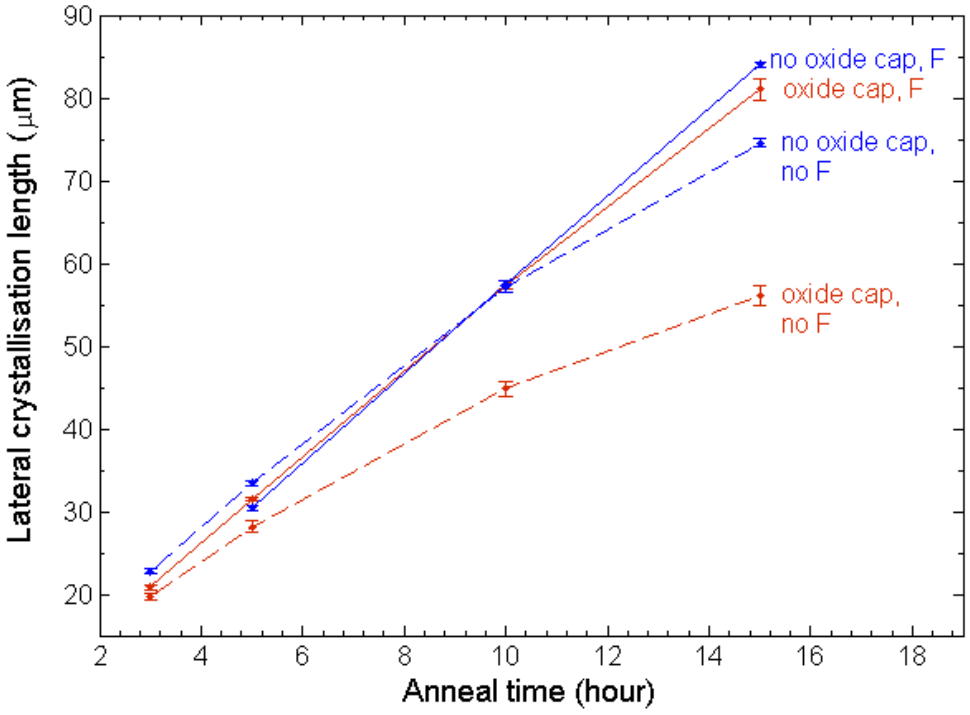


FIGURE 5.29: Lateral crystallisation length as a function of anneal time at 550°C for Si-on-Oxide sheets with and without an oxide cap and with and without a fluorine implant. On all samples, the α-Si was deposited by LPCVD. F was implanted into α-Si at a dose of 2.5×10^{15} cm^{-2} and an energy of 35 keV. All data are based on measurements using a Nomarski microscope.

in nanowires therefore appear to reduce the MILC rate in nanowires. The results in Chapter 6 show that the nanowires have a rather rough surface, which might be expected to reduce the MILC rate. Furthermore, nanowires may have higher dry etch damage than ribbons due to the larger surface area and this too might be expected to reduce the MILC rate. Further work is needed to clarify these issues.

In this work, polysilicon nanowires were achieved using metal-induced lateral crystallisation at 550°C. Compared with process temperatures needed to produce polysilicon by solid-phase crystallisation or direct polysilicon deposition, which are typically 600°C [105] and 625°C [117], respectively, metal-induced lateral crystallisation reduces the process temperatures by 50°C and 65°C, respectively. Therefore, MILC in nanowires is advantageous. There is some potential to lower the MILC temperature for nanowires, as MILC at 428°C has been demonstrated for ribbons. However, further work is needed to investigate how much lower the MILC temperature could be reduced.

5.6 Conclusions

In this chapter, results on the lateral crystallisation of α-Si nanowires have been reported for the first time and a crystallisation length of 13 μm has been achieved for a MILC anneal at 550°C. This crystallisation length is ample for nanowire biosensors and has been achieved at a temperature that is 75°C lower than the typical polysilicon deposition temperature of 625°C [117]. The MILC length in α-Si ribbons has also been studied and decreases with decreasing ribbon width. The MILC length in nanowires lies below the trend line for the ribbons, indicating that lateral crystallisation is more difficult in nanowires than ribbons. This result has been tentatively explained by a combination of surface roughness and dry etch damage. Longer MILC lengths have been obtained on LPCVD α-Si than on PECVD α-Si and on Si-on-Air structures than Si-on-Oxide structures. Si-on-Nitride structures give only slightly shorter MILC lengths than Si-on-Oxide structures. Lateral crystallisation of Si-on-Nitride structures can be achieved at a temperature as low as 428°C, which is compatible with the process temperature of 450°C imposed by glass substrates.

Chapter 6

Poly-Si Nanowire Biosensor Fabrication and Characterisation

6.1 Introduction

Silicon nanowire biosensors, as discussed in Chapter 2, have been gaining much attention for applications such as biosensing for medical diagnosis, drug discovery and national security. In a Si nanowire biosensor (Fig. 6.1(a)), the nanowire is functionalised using protein receptors that are able to immobilise target biomarkers in the blood or sputum sample. As the biomarkers are selectively captured on the Si nanowire surface, bio-information can be read from the change of nanowire conductivity. The large surface to volume ratio of silicon nanowires makes them ideal for real-time, high sensitivity biosensing.

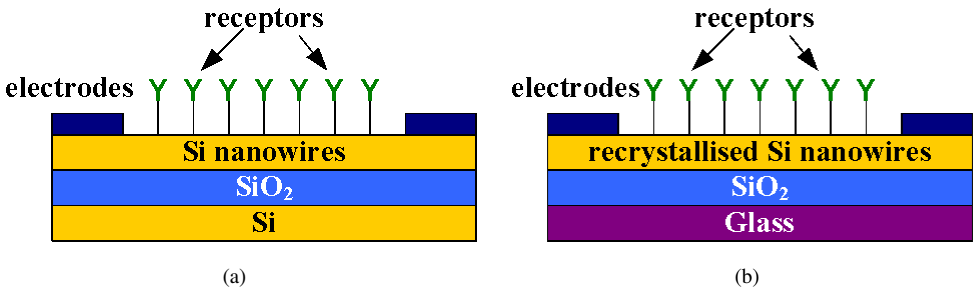


FIGURE 6.1: Schematic diagrams of Si nanowire biosensors using (a) an SOI substrate and (b) TFT technology.

Most Si nanowire research has used Silicon-on-Insulator (SOI) substrates (Fig. 6.1(a))

[8][15] and e-beam lithography for the nanowire fabrication [16][75]. However, this approach is very high cost and unsuitable for disposable diagnostic kits for point-of-care diagnosis. In this work, a cheaper approach is investigated based on thin film transistor (TFT) technology, as shown in Fig. 6.1(b). The use of metal-induced lateral crystallisation offers the additional possibility of a low temperature processing and hence the use of low cost glass substrates.

6.2 Biosensor Design

In the Si nanowire biosensor fabrication, a Si spacer etch technique is used as a low-cost alternative to electron beam lithography for nanowire fabrication. The concept of the Si nanowire formation is illustrated in Fig. 6.2. An α-Si layer is deposited on a SiO_2

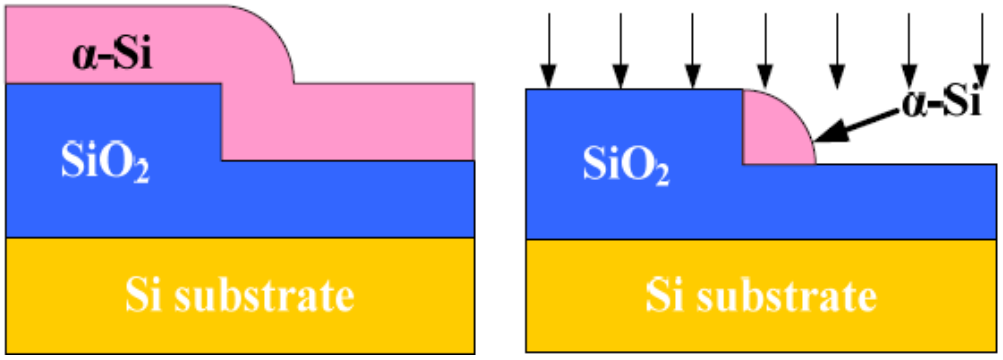


FIGURE 6.2: Cross-section schematics of nanowire formation (a) after α-Si deposition and (b) after α-Si anistropic dry etch.

layer in which a sharp step has been etched using an anisotropic SiO_2 etch (Fig. 6.2(a)) The thickness of the α-Si over the step is the sum of the α-Si thickness and the SiO_2 step height. After an anisotropic Si dry etch (Fig. 6.2(b)), an α-Si nanowire (spacer) is left on the side of the oxide step. The dimensions of the nanowire are independent of the photolithography used to define the step, but instead are determined by the step height and α-Si thickness. Therefore, spacer nanowires can be defined by choosing a nanoscale SiO_2 step height and a nanoscale α-Si thickness. In this process, the etch anisotropy is very critical for the nanowire formation.

The biosensor design is shown in a mask layout and schematic cross-sections in Fig. 6.3. Detailed information on the different types of biosensor on the mask design are listed in Appendix F. The biosensors are designed to include 20, 50 and 100 parallel nanowires

of 10, 15 and 20 μm in length, respectively. The biosensor fabrication process is very simple and uses just four masks. Mask *NW* is used to define the nanowire locations by patterning the steps in SiO_2 layer, mask *DP* is used to define heavily doped Si pads (Source/Drain) to make low resistance contacts to the nanowires, mask *MT* defines Al electrodes and mask *SU* is used to open sensing windows in a passivation layer. An SU8-2 passivation layer is used to isolate the Source and Drain and metallisation from a direct electrical contact with the liquid. Thus, the SU8-2 sensing window gives the nanowires access to the liquid.

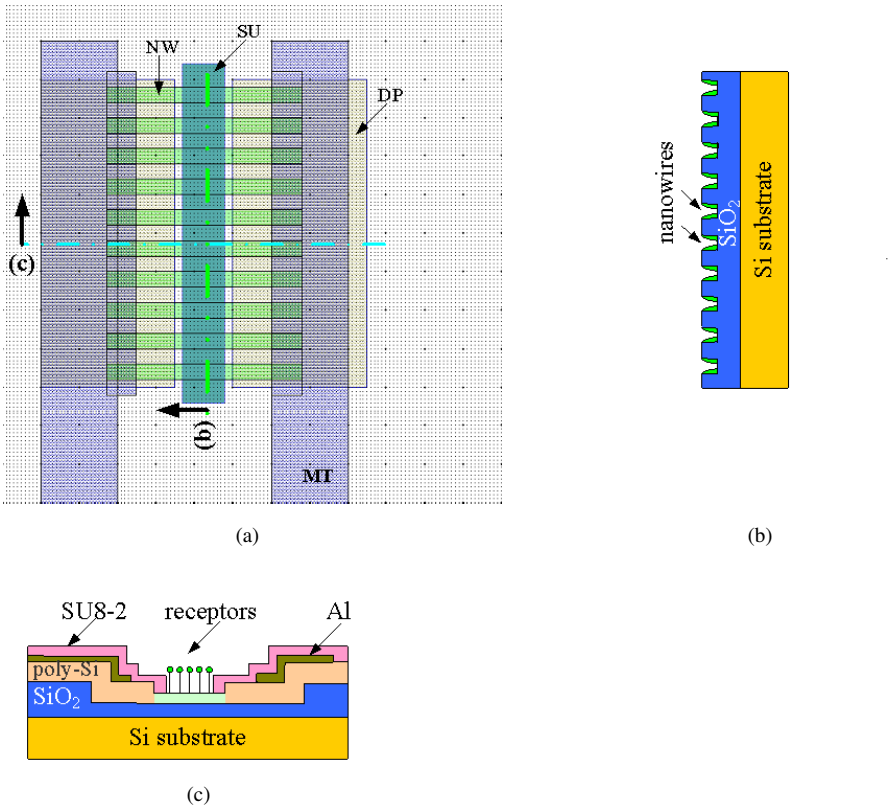


FIGURE 6.3: Schematic illustration of designed Si nanowire biosensor (a) mask layout, (b) cross-section view at cutline *b* and (c) cross-section view at cutline *c*.

6.3 Experimental Procedure

In this section, the overall fabrication process for the Si nanowire biosensor is introduced. Subsequently, the critical process steps in the fabrication are discussed in detail. First, the development of the photolithography processes for photoresists, S1813,

AZ2070 and SU8-2, are discussed, where the aim is to optimise exposure times for dimension control. Second, the Si nanowire etch process using the STS Pegasus deep Si etcher is discussed. Finally, the Al lift-off process for electrode formation is discussed.

6.3.1 Overall process flow

Fig. 6.4 shows a schematic illustration of the Si nanowire biosensor fabrication. A thermal silicon dioxide of about 700 nm was grown on 4-inch <100> phosphorus doped Si wafers (Fig. 6.4(a)). Then, the SiO_2 layer was patterned using an EVG620TB aligner using photoresist S1813. Subsequently, a dry etch of 120 nm was performed to form SiO_2 steps (Fig. 6.4(b)). The SiO_2 etch recipe was Ar 32 sccm, CHF_3 18 sccm, RF Power 200 W and pressure 30 mTorr for 190 seconds. Samples were then sent to Philips Research MiPlaza at Eindhoven for 100 nm α-Si deposition (Fig. 6.4(c)) using low pressure chemical vapour deposition (LPCVD) at 560°C with a deposition rate of 1.7 nm/min. After the deposition, the wafers were patterned by photolithography using a positive resist to cover the Source/Drain regions. The wafers were then given an anisotropic Si dry etch using an STS Pegasus deep Si etcher to form the Si spacer nanowires (Fig. 6.4(d)) and the Source and Drain pads. The Si etch process development is described in more detail in Section 6.3.3.

After the formation of the Si nanowires, the wafers were sent to the Surrey Ion Beam Centre for ion implantation. Two phosphorus implantations were performed at a dose of either 1×10^{13} cm^{-2} or 2×10^{13} cm^{-2}, an energy of 10 keV and at a tilt angle of $\pm45°$. These implants were used to dope the nanowires and the two doses were chosen to give dopant concentrations of approximately 1×10^{18} cm^{-3} and 2×10^{18} cm^{-3} for a good sensitivity [78]. At this point, the Source/Drain mask was used for a second time, but this time a negative photoresist was used to open windows over the Source/Drain regions. The wafers were then given a high dose phosphorus implantation at dose 1×10^{15} cm^{-2}, an energy of 35 keV and a tilt angle of 7°. This implant is used to heavily dope the two ends of the nanowire (source and drain) so that a low resistance ohmic contact can be made to the metal. A tube furnace anneal of 24 hours at 600°C in nitrogen was given to crystallise the α-Si nanowires into poly-Si nanowires and activate the implanted dopants. Subsequently, 10 nm oxide was grown on some wafers using a dry oxidation at 900°C for 20 minutes, 17 seconds, whereas no thermal oxidation was given on the other wafer. The aim of this batch split was to investigate the effect of the nanowire surface on conduction. Then wafers were patterned by photolithography using photoresist AZ2070. Immediately after a HF dip in 20:1 buffered HF to remove any oxide on the

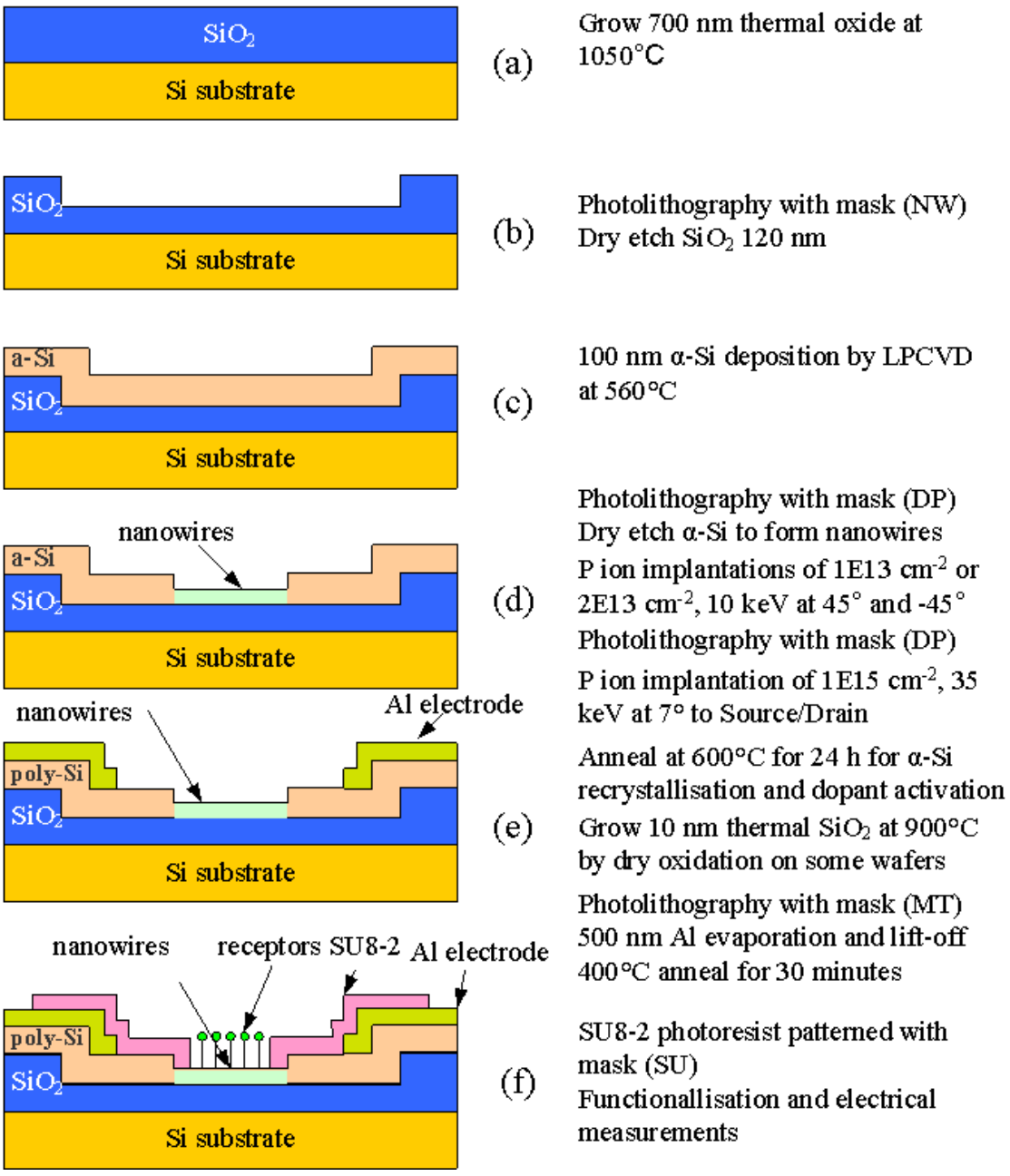


FIGURE 6.4: Overall Si nanowire biosensor process flow.

Si surface, 500 nm Al was evaporated in a BAK 600 e-gun evaporator at a rate of 0.5 nm/min. Al lift-off (Fig. 6.4(e)) was subsequently performed using either an OPTI Wet ST 30 lift-off tool or manually in a beaker. The wafers were then annealed in nitrogen at 400°C for 30 minutes to improve the Al contact with the Si. It should be noted that a forming gas (a hydrogen and nitrogen mixture) anneal would have been preferred but was not available in the cleanroom at the time of processing. Finally, wafers were coated with SU8-2 photoresist and then patterned using photolithography to open the sensing windows and probing windows over the bond pads. Finally, the wafers were diced into chips for functionalisation experiments and electrical measurements. Etched nanowires were inspected by Scanning Electron Microscope (SEM) and Helium Ion Microscope for its longer focus depth. The operation of Helium Ion Microscope was operated by Stuart Boden.

6.3.2 Photolithography process development

In this work, several kinds of photoresists were used for different process uses, such as dry etch, lift-off and passivation layer formation. For each photoresist, the procedures of exposure and development are described in different sections. The mask alignment procedure in photolithography is also introduced.

6.3.2.1 Photolithography with S1813

The positive photoresist S1813 was used for the dry etch processes in this work. To get a good control of feature size, the exposure dose of S1813 was intensively investigated to determine the optimum dose.

The experimental procedure is given as follows. The Si wafers were baked overnight in an oven at 210°C to remove moisture and photoresist S1813 was spun onto the wafers at 5000 RPM for 30 seconds. Then the wafers were given a soft-bake on a hot-plate at 95°C for 1 minute to evaporate the solvent in the photoresist. After the soft-bake, the wafers were cooled down to room temperature (≈5 minutes). The wafers were subsequently loaded into an EVG 620T aligner and exposed at various doses from 30 mJ/cm^2 to 90 mJ/cm^2 without an i-line filter. To reduce the development time, an opaque cover was used to expose only part of the wafer for each dose so that all the different exposures were performed on two wafers. The exposure times were calculated from the lamp intensity, which was measured to be 18 mJ/cm^2 per second. Then the exposed wafers were

manually developed in developer MIF 319. Development times of 25 seconds and 30 seconds were used for dark field (removes a small fraction of the photoresist) and light field (removes most of the photoresist), respectively. After photoresist development, the wafers were inspected using an optical Nomarski microscope.

6.3.2.2 Photolithography with AZ2070

The negative photoresist AZ2070 was used for Al lift-off for its higher thickness and negative sidewall slope. To get a good control of feature size, the exposure dose of AZ2070 was investigated to determine the optimum dose.

The experimental procedure is given as follows. The Si wafers were baked overnight in an oven at 210°C to remove moisture and photoresist AZ2070 was spun onto the wafers at 6000 RPM for 40 seconds. Then the wafers were given a soft-bake at 110°C for 1 minute on a hot plate. After the wafers had cooled down for ≈5 minutes, they were subsequently loaded into an EVG 620TB aligner and exposed at various doses from 45 mJ/cm^2 to 115 mJ/cm^2 with an i-line filter (365 nm). The use of the i-line filter is because AZ2070 has a narrow absorption spectrum and is mainly sensitive to i-line [118]. Multiple exposures were again performed on each wafer using the opaque cover. The lamp intensity with the i-line filter was measured to be 9.5 mJ/cm^2 per second. The exposed wafers were post-baked on the hot plate at 110°C for 1 minute to further cross-link the exposed photoresist and manually developed in AZ726 MIF developer for 75 seconds. After photoresist development, features on wafers were inspected using an optical Nomarski microscope. Prior to Al evaporation, any remaining photoresist in the open windows was removed by an oxygen descum using an OIPT RIE 80 plus. The recipe used a pressure of 50 mTorr, a forward power of 100 W and O_2 flow of 50 sccm for 1 minute at 20 °C.

6.3.2.3 Photolithography with SU8-2

The negative photoresist SU8-2 was used as a passivation layer on top of the device to isolate Source/Drain and metal from direct contact with the liquid during sensing. We developed the exposure dose for SU8-2 by modifying a recipe from its technical data sheet [119].

The experimental procedure was as follows. The photoresist SU8-2 was kept at room temperature overnight to eliminate bubbles and the Si wafers were baked overnight in

the oven at 210°C. The photoresist SU8-2 was spun onto the wafer at 500 RPM for 12 seconds and then at 2000 RPM for 40 seconds. The wafers were soft-baked on a hot plate at 65°C for 1 minute and then heated up to 95°C for 3 minutes. After the wafers had cooled down for about 5 minutes, they were subsequently loaded into EVG 620T/620TB aligner and exposed at various doses from 36 mJ/cm^2 to 104 mJ/cm^2 with a 365 nm i-line filter. Multiple exposures on a single wafer were again performed. The exposed wafers were post-baked on the hot plate at 65°C for 1 minute and then heated up to 95°C for 3 minutes. Subsequently, the wafer was manually developed in SU8 developer for 45 seconds and cleaned in isopropanol (IPA), followed by a nitrogen blow dry. An optical Nomarski microscope and SEM was used to inspect developed photoresist features.

6.3.2.4 Alignment in photolithography

In this work, the pattern alignments in the EVG620T and EVG620TB aligners were both handled manually. The procedure for the alignment was as follows. Firstly, the mask was loaded into the aligner and the two lenses were moved to search for the alignment marks. The locations can be saved and loaded for further use. After manually reducing the rotation of the mask, the wafer was loaded into the aligner and patterns on both the mask and wafer can be identified by adjusting the focus of the microscope lens. For the loaded wafer, the wafer rotation mismatch was reduced first. It should be noted that the *wafer rotation mismatch* is the mismatch between mask and substrate features on each microscope view and the *view mismatch* between the two microscopes does not affect the alignment. The mask and wafer were then aligned by moving the wafer to put the main alignment mark on the mask at the centre of the alignment mark on the wafer, illustrated in Fig. 6.5(a). Subsequently, the alignment was checked using the fine alignment features (in Fig. 6.5(a)) after bringing the mask and substrate into contact. Then the mask and substrate were separated and moved based on the mismatch inspection results. These contact and separation steps were then repeated until a good alignment was achieved between the fine alignment features on the mask and wafer under contact conditions. Here, digital magnifications of $\times 2$ and $\times 4$ were used to help the alignment check. After the alignment and a photoresist development, the misalignment can be read from designed misalignment measurement features (in Fig. 6.5(b)) by identifying which two bars are most aligned in x and y directions. From the central bar, misalignment can be measured in an accuracy of 100 nm.

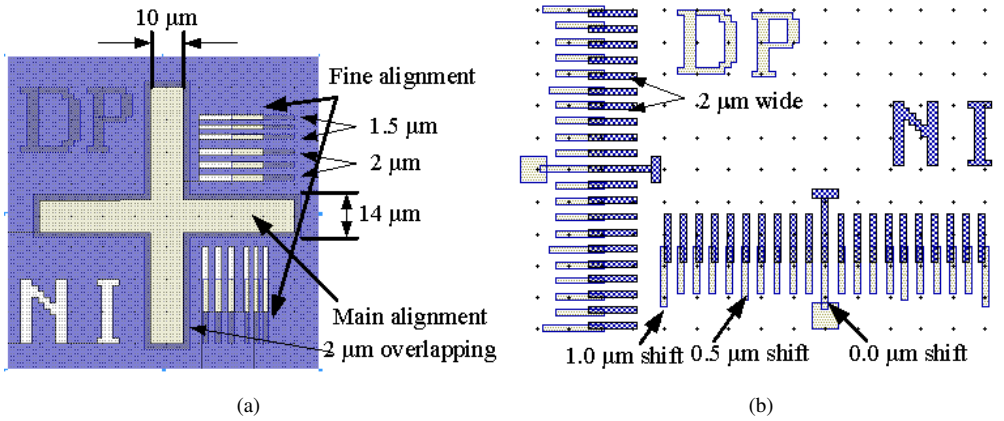


FIGURE 6.5: Mask layouts of features for (a) alignment and (b) misalignment measurement.

6.3.3 Nanowire etch process development

The nanowire etch process was developed on a test wafer that was cleaved into chips of 2.26 cm $\times$ 1.13 cm. The cleaved chips were etched using a Bosch process on a STS Pegasus ICP etcher. The Si etch process is performed in two steps, namely a silicon plasma etch and a protection layer deposition to protect the sidewall against the silicon etch. Thus, the etch time is counted by the number of these 'cycles'. The wafer was maintained at 10°C during the etching by using liquid nitrogen cooling. For the deposition step, C_4F_8 was supplied for 3 seconds with a gas flow of 80 sccm. For the etch step, a mixture of SF_6 (50 sccm) and O_2 (5 sccm) was supplied for 2 seconds with a 13.56 MHz ICP power of 250 W and a 380 kHz RF power of 11 W. Then Si chips were etched for different numbers of cycles and the Si thickness was calibrated by cross-section inspection using a JEOL 6500F SEM, and by Elliposometer measurements.

6.3.4 Metallisation process development

The Al lift-off process needs to be very well controlled to avoid damaging the spacer nanowires. In the initial experiments, the lift-off process was performed manually in a beaker, but in later experiments performed in an OPTI Wet ST 30 lift-off machine. For the manual lift-off process, the wafer with patterned photoresist and evaporated 500 nm Al on the top was rinsed for 4 hours in a big beaker filled with N-Methyl-2-pyrrolidine (NMP) at room temperature. The Al was then lifted-off by shaking the beaker and then blowing NMP through a pipette. Finally, the wafer was cleaned in acetone and isopropanol, followed by a DI water clean. For the lift-off process using the lift-off

machine, 60°C heated NMP was first sprayed onto the wafer and then rinsed in cycles. Each cycle included a spray of NMP on the wafer rotated at 500 RPM and then a rinse in NMP for 2 minutes. This cycle was repeated five times, giving a total rinse time of about 10 minutes. Subsequently, high pressure heated NMP (2 ATM) was blown over the wafer with the nozzle moving from one side to the other and the wafer rotating at 1000 RPM. Finally, the wafer was cleaned with high pressure (2 ATM) DI water and then dried by spinning and nitrogen blowing. Then the wafers were inspected by SEM and Nomarski microscope.

6.3.5 Electrical measurements

The fabricated biosensor devices were calibrated using a 4-probe station and an Agilent B1500A semiconductor device analyser. Fig. 6.6 shows a schematic of the probe setup used for device measurements in a dry environment. Three probes were used with two probes connected to Source and Drain through Al electrodes and the third connected to the substrate by a connection through the chuck of the probe station. The resistance was extracted by I_{ds} - V_{ds} measurement. The Source was grounded by applying 0 V, and a variable bias (0 - 5 V) was applied to the Drain. The substrate, referred to as the back-gate, was connected to a constant bias in the range 0 to 15 V. The measurement sequence was performed in order of 5 V, 10 V and 15 V on each device. For I_{ds}-V_{bg} measurements, the current I_{ds} was measured by sweeping V_{bg} from 0 to 15 V and 0 to -15 V under V_{ds} = 1V.

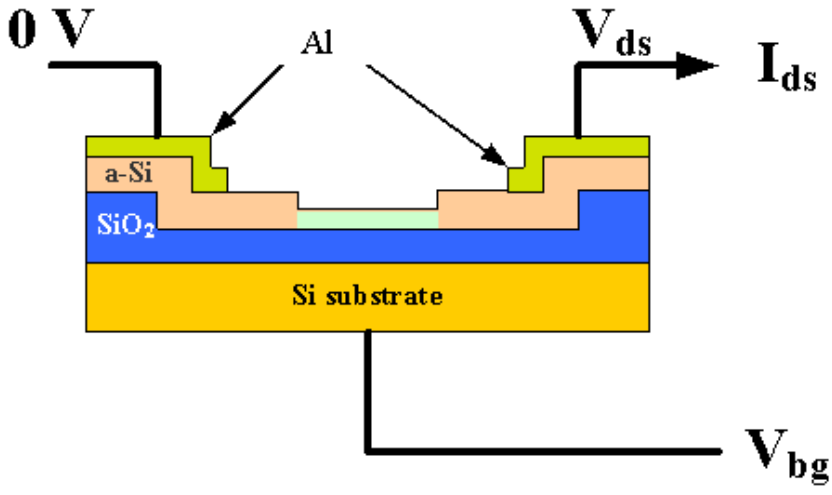


FIGURE 6.6: Schematic of probe connections for electrical measurements in a dry environment.

For the pH measurements, the work was carried out in collaboration with Marta Lombardini. Using a pipette, 5 μL droplet of a certain pH solution was put on top of nanowires. Then the drain current was measured by sweeping V_{bg} from 0 V to 5 V at a fixed V_{ds} of 10 V. Then 5 measurements were performed continuously and then the droplet was removed by a pipette. Before putting a different pH solution, the nanowires were cleaned with deionised water to avoid deposition of salt. The used solutions were at pH values of 4, 7 and 10, which are solutions of potassium hydrogen phthalate (KHP) and potassium dihydrogen phosphate (KH_2PO_4)/disodium hydrogen phosphate (Na_2HPO_4) in DI water for pH = 4, potassium hydrogen phthalate (KHP) and potassium dihydrogen phosphate (KH_2PO_4)/disodium hydrogen phosphate (Na_2HPO_4) in DI water for pH = 7, and disodium hydrogen phosphate (Na_2HPO_4) in DI water for pH = 14.

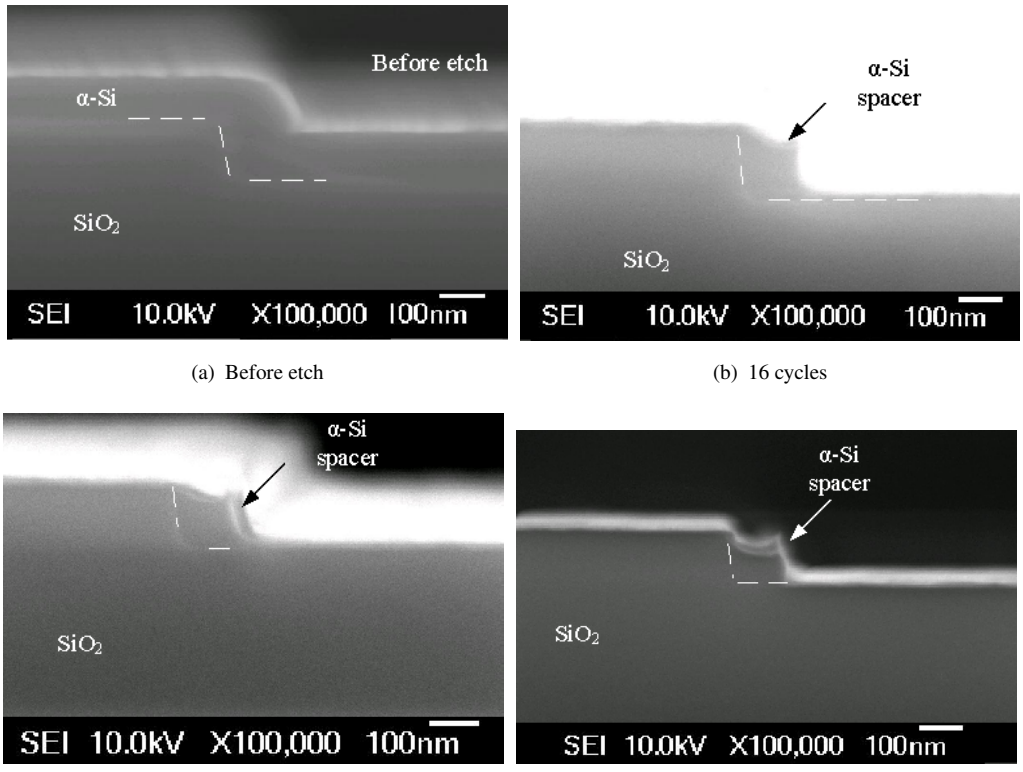
6.4 Results

In this section, only results of spacer etch development are presented and the results of photolithography development and metallisation development are presented in detail in Appendix C and D, respectively. Then, the final fabricated devices are presented and characterised by electrical measurements.

6.4.1 Nanowire etch development

Fig. 6.7(a) shows a cross-section SEM image of a sample after α-Si film deposition over a SiO_2 step. The α-Si layer can be identified on top of the thermal oxide layer and measured to be about 110 nm in thickness. Figs. 6.7(b), (c) and (d) show cross-section SEM images of the samples, after etches with 16, 20 and 25 cycles, respectively. In Fig. 6.7(b), the α-Si layer has not been completely etched and a thin layer of about 20 nm remains on the SiO_2. When an extra four etch cycles were given, the α-Si layer was fully removed (Fig. 6.7(c)). The nanowire width and height were measured to be 111 nm and 100 nm, respectively. When a further five etch cycles were given, the nanowire height reduced to 67 nm but the nanowire width remained 111 nm (Fig. 6.7(d)).

The nanowire height and width are plotted against the number of etch cycles in Fig. 6.8. The SiO_2 step height is also plotted in red dot line in Fig. 6.8. It can be seen that the Si height decreases with etch time from 210 nm to 37 nm but the Si width remains almost



(a) Before etch (b) 16 cycles

(c) 20 cycles (d) 25 cycles

FIGURE 6.7: Cross-section SEM micrographs of samples (a) before α-Si spacer etch, (b) after a 16 cycle etch, (c) after a 20 cycle etch and (d) after a 25 cycle etch.

the same up to 25 etch cycles. Compared with the deposited α-Si thickness of about 110 nm and the step height of 120 nm, it can be concluded that the nanowire dimensions can be well defined by choosing the α-Si thickness for width control and the step height and etch time for height control. In addition, the α-Si layer is removed after about 19 etch cycles. It can be concluded that an overetch of 10% (20 cycles) is quite safe to ensure that the α-Si nanowires are reliably formed.

Fig. 6.9 shows how the wafer size influences the nanowire etching. Results are shown for etches performed on 4-inch wafers and on 22.6 mm $\times$ 11.3 mm chips. This figure shows that more etch cycles are required for the 4-inch wafers than the chips. This result is due to a reduction of the etchant density as the sample surface area increases.

To investigate the continuity of the nanowires, Fig. 6.10(a) shows a plan-view Nomarski optical image of the nanowires after a delineation etch in 20:1 buffered HF for 2 minutes. The nanowires appear to be continuous and there is no evidence of breaks on any of the nanowires. Further electrical measurements of nanowire continuity will be made later in the chapter. With a longer buffered HF etch of 5 minutes (Fig. 6.10(b)), the nanowires can be freed from the underlying SiO_2 layer.

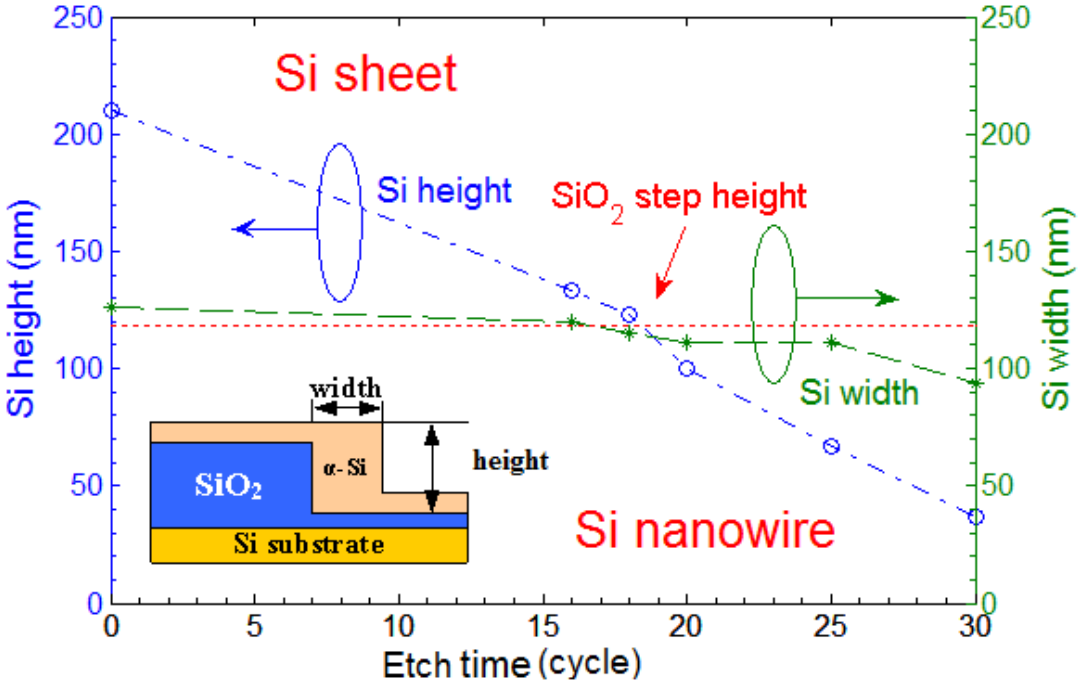


FIGURE 6.8: Nanowire width and height dimensions, measured by cross-section SEM, as a function of etch time in cycles.

6.4.2 Completed biosensor characterisation

A typical fabricated biosensor is shown in the optical Nomarski micrograph in Fig. 6.11. An SU8-2 window has been opened to expose the nanowires to the solution. In the SU8-2 photoresist window, 20 spacer nanowires can be seen, indicating that the nanowires have survived the Al lift-off process. The nanowire length is about 14 μm, which is in good agreement with the designed length of 15 μm. The measured offsets, which are the distances between the SU8-2 window edges and the nearest Source/Drain, are 2.1 μm and 2.3 μm, respectively, indicating excellent alignment control. These offsets ensure that there is no connection between Source and Drain through the liquid when the sensor is exposed to liquid.

Fig. 6.12(a) shows a plan-view SEM micrograph of the nanowires in a completed biosensor. The nanowires can be seen on the side of the oxide step and a good contact to the poly-Si source/drain pad can also be seen. From Fig. 6.12(a), the nanowire width was measured to be 120$\pm$13.5 nm, which is obtained from 10 different positions along the nanowire. The white features on the nanowire surface may be polymer formed during the dry etch process. This polymer could be removed by cleaning in an O_2 plasma. Fig. 6.12(b) shows a high magnification cross-section SEM micrograph of

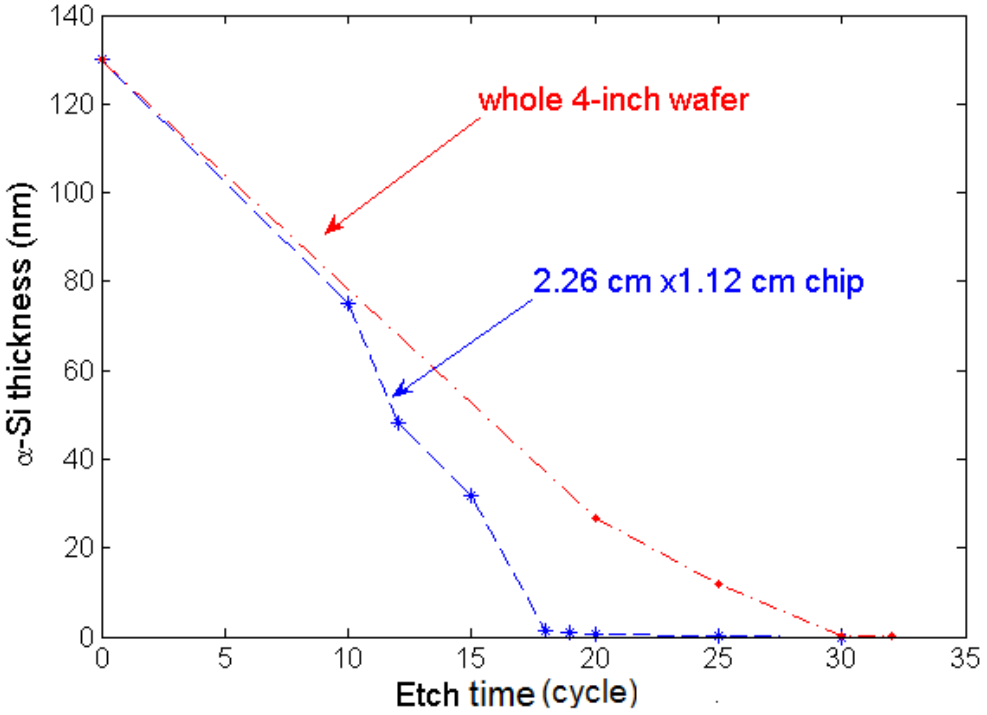
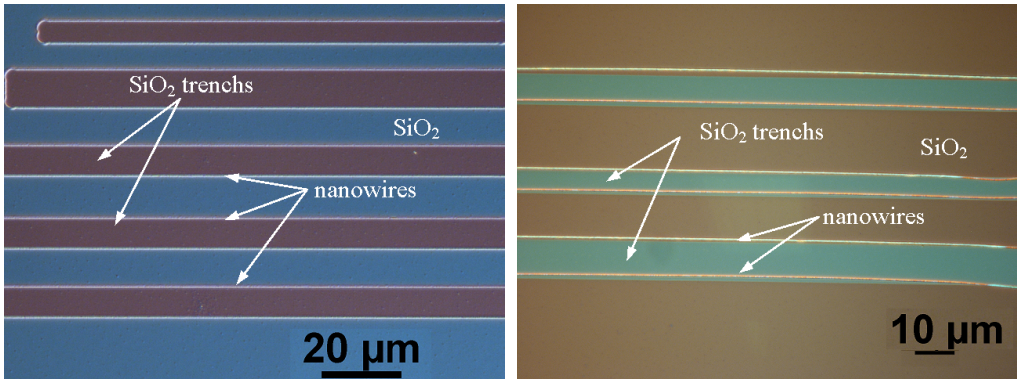


FIGURE 6.9: α-Si sheet thickness measured by ellipsometer as a function of etch time in cycles for etches performed on whole 4-inch wafers and 2.26 cm $\times$ 1.13 cm chips.



(a) (b)

FIGURE 6.10: Plan-view optical Nomarski micrographs after a etch in 20:1 buffered HF for (a) 2 minutes to reduce the thickness of the underlying oxide and (b) 5 minutes to completely free nanowires from the underlying oxide.

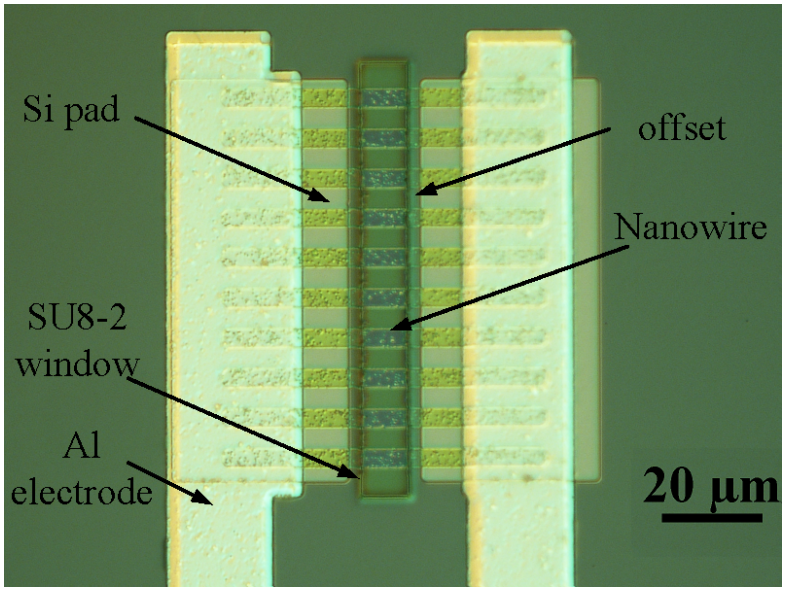


FIGURE 6.11: Nomarski micrograph of a completed nanowire biosensor.

a nanowire in a complete biosensor. The nanowire width was measured to be 101 nm at the bottom of the pillar and the height to be 80 nm. It should be noted that this width of 101 nm is not in very good agreement with the width of 120 nm measured from Fig. 6.12(a). The discrepancy can be accounted for by noting that the oxide sidewall is not perfectly vertical. If the nanowire width is measured from the top of the pillar, a value of 121 nm is obtained, which is in an excellent agreement with the value obtained from Fig. 6.12(a). The shape of the nanowire in Fig. 6.12(b) is triangular, whereas rectangular nanowires were obtained during process development, as shown previously in Fig. 6.7(c). The nanowire roughness can also be identified in the micrograph (Fig. 6.12(c)) by Helium Ion Microscope. This result will be discussed in more detail later in this chapter.

6.4.3 Effect of back-gate bias for 100 nm oxidised nanowire biosensors

Fig. 6.13 shows I_{ds}-V_{ds} characteristics of a typical fabricated nanowire biosensor under different gate biases. The plotted biosensor comprises 100 nanowires in parallel, each of which is 10 μm in length. The characteristics show a slow turn-on for values of V_{ds} below about 2 V, which is typical of contact resistance problems arising from the formation of Schottky barriers at the source and/or drain. However, for values of V_{ds} above 2 V, the characteristics vary linearly with drain bias for all back-gate biases. The

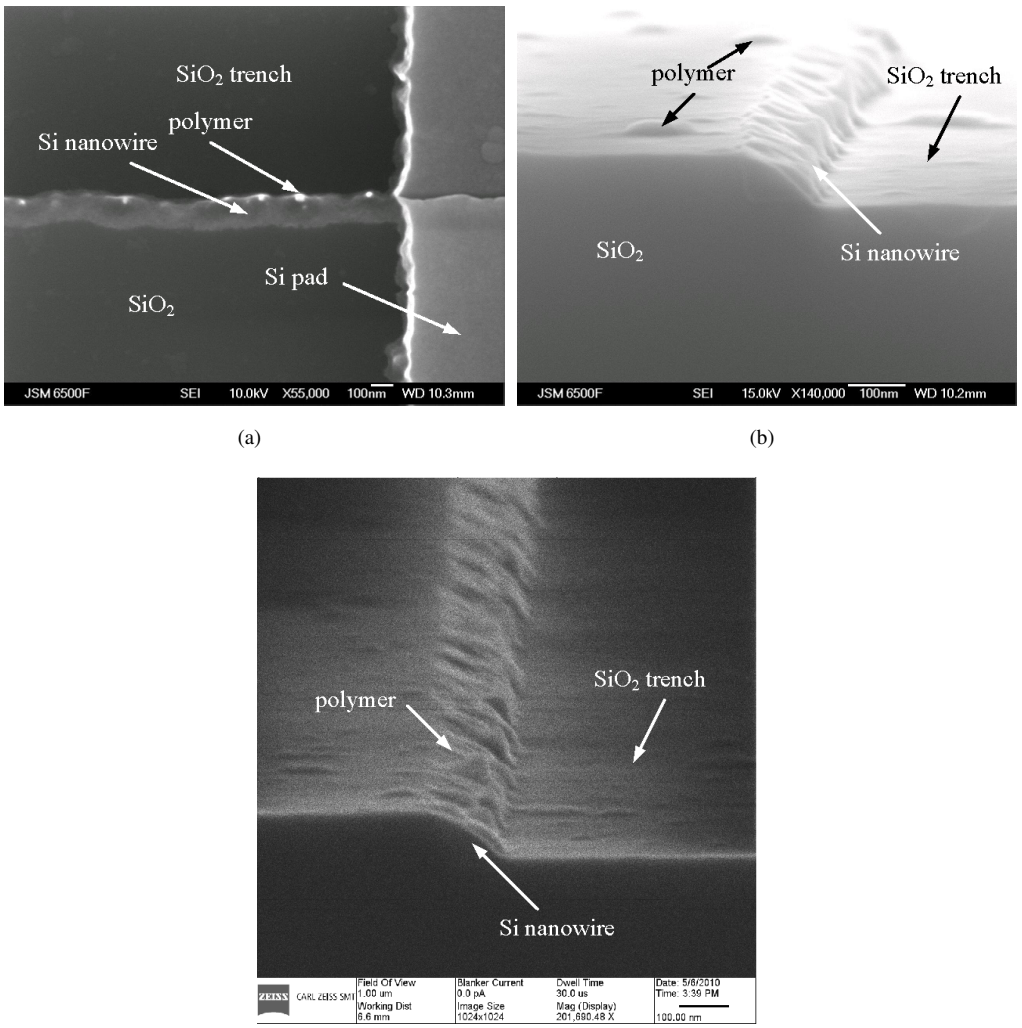


FIGURE 6.12: Micrographs of a nanowire in a completed biosensor; (a) plan SEM view and (b) cross-section SEM view after a delineation etch and (c) cross-section Helium Ion Microscope view after a delineation etch.

drain current at a given drain bias increases with an increase in back-gate bias. This shows that the conductance of the nanowire biosensor can be tuned by applying a back-gate bias. This behaviour is as expected, because increasing positive back-gate bias would accumulate electrons in the n-type nanowire and hence would increase the drain current.

6.4.4 Repeatability

To investigate the repeatability of the nanowire I-V characteristics, 12 identical nanowire biosensors were measured on four chips at the centre of the wafer. Fig. 6.14(a) shows

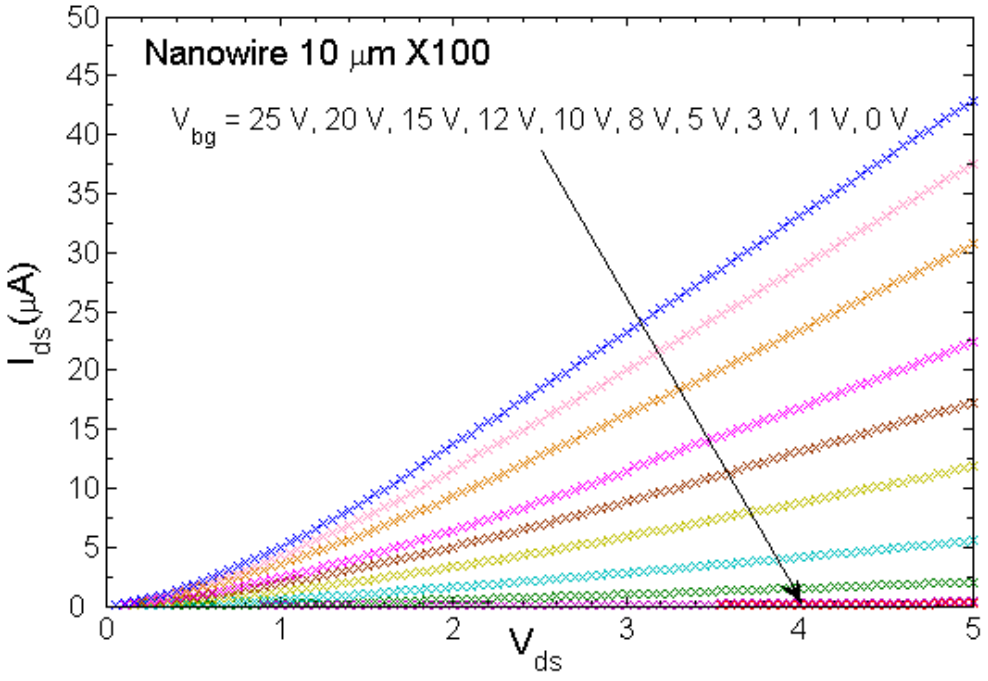
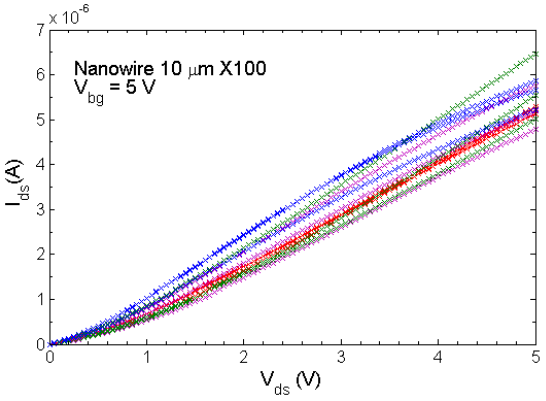


FIGURE 6.13: I_{ds}-V$_{ds}$ characteristics of an oxidised biosensor. The biosensor comprises 100 nanowires in parallel, each of which is 10 μm long. The oxide thickness on the nanowire was 10 nm and the back-gate bias, V_{bg}, was varied from 0 V to 25 V.

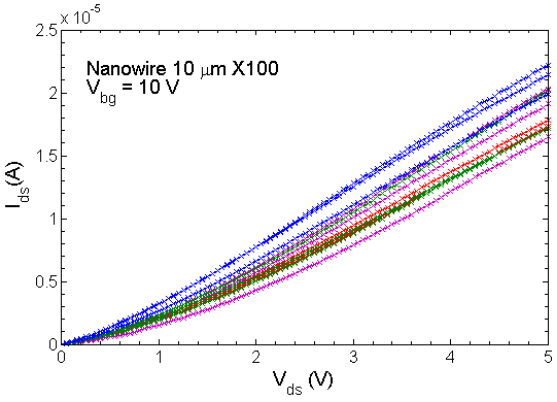
I_{ds}-V_{ds} curves for a back-gate bias of 5 V with devices on the same chip being plotted in the same colour. For values of V_{ds} above 2 V, the device resistance can be calculated from the slope using a linear fit method and is found to be 871$\pm$69 kΩ. This represents an 8% variation in device resistance. Similar trends were found for back-gate biases of 10 V and 15 V, as shown in Figs. 6.14(b) and (c), respectively. The resistances under 10 V and 15 V back-gate biases are calculated to be 253$\pm$25 kΩ and 141$\pm$16 kΩ, respectively. These results represent percentage variations of 10% and 11%, respectively. Thus, it can be concluded that the fabricated nanowire biosensors have repeatable I-V characteristics at least in the central portion of the wafer.

6.4.5 Effect of nanowire length on resistance

The resistances of nanowires of different lengths were investigated by measuring I_{ds}-V_{ds} characteristics on 12 nanowire biosensors with lengths of 15 μm and 20 μm at a back-gate bias of 10 V as shown in Fig. 6.15. Resistances of 320$\pm$37 kΩ and 410$\pm$36 kΩ were extracted for the 100 parallel nanowires of 15 μm and 20 μm in length, respectively, using a linear fit.



(a)



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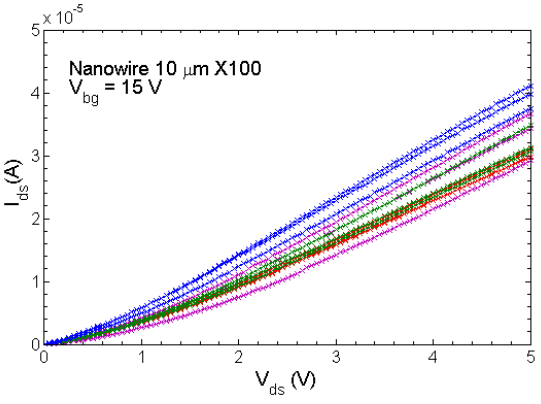


(c)

FIGURE 6.14: I_{ds}-V_{ds} characteristics of 12 100 $\times$ 10 μm oxidised, nanowire biosensors at various values of back-gate bias, V_{bg} (a) 5 V, (b) 10 V and (c) 15 V.

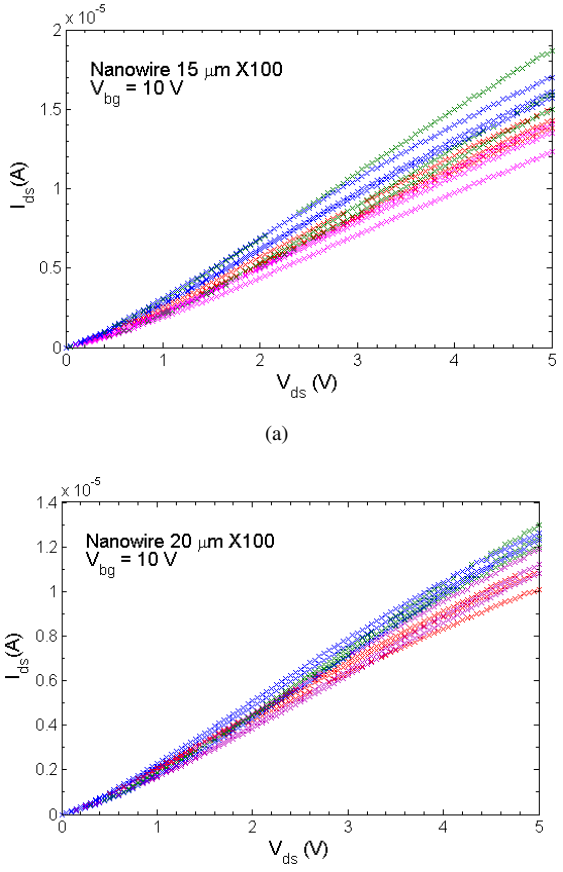
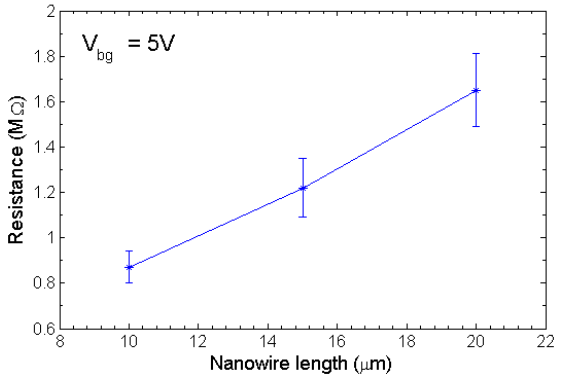


FIGURE 6.15: I_{ds}-V_{ds} characteristics of twelve oxidised biosensors comprising 100 parallel nanowires of lengths (a) 15 μm and (b) 20 μm. The devices were measured at a back-gate bias, V_{bg}, of 10 V.

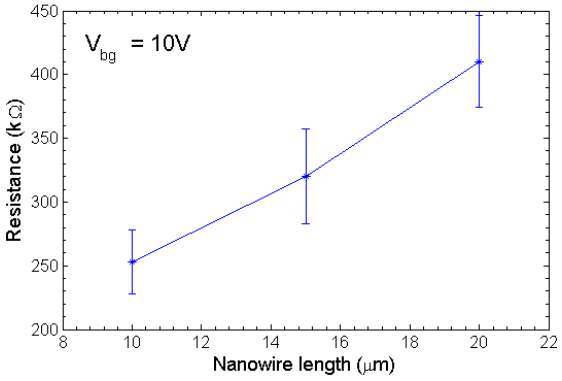
Fig. 6.16(a) shows resistance as a function of nanowire length for devices with 100 parallel nanowires measured at back-gate bias of 5 V. The resistance is not exactly linear with nanowire length; the curve slope is higher between nanowire lengths of 15 and 20 than between 10 and 15. Similar trends are seen for back-gate biases of 10 V and 15 V, as shown in Fig. 6.16(b) and Fig. 6.16(c), respectively. This non-linear relationship between resistance and nanowire length might be explained by the presence of source/drain contact resistance, as has already been seen in the output characteristic in Fig. 6.13.

6.4.6 Effect of the number of parallel nanowires on conductance

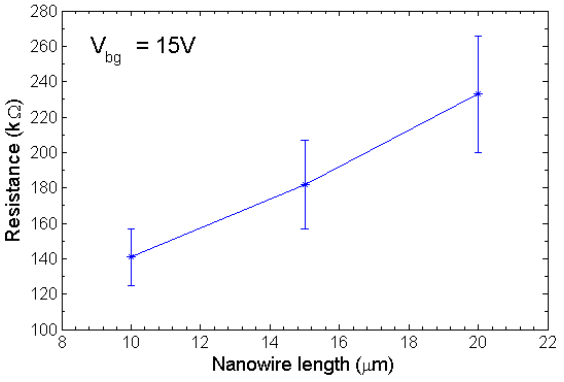
Conductances of devices with different numbers of parallel nanowires have also been investigated by making I_{ds}-V_{ds} measurements on 11 or 12 devices on the four chips in



(a)



(b)



(c)

FIGURE 6.16: Resistance as a function of nanowire length for oxidised nanowire biosensors comprising 100 parallel nanowires measured at a back-gate bias of (a) 5 V, (b) 10 V and (c) 15 V.

the middle of the wafer. Fig. 6.17 shows the I_{ds}-V_{ds} characteristics of devices with 20 (a) and 50 (b) parallel 10 μm long nanowires, measured at a back-gate bias of 10 V. As these characteristics are not completely linear at small biases, the slopes are calculated at $V_{ds} > 3$ V. The values of resistance were extracted using a linear fit and found to be 1.4±0.2 MΩ for 20 parallel nanowires and 506±55 kΩ for 50 parallel nanowires.

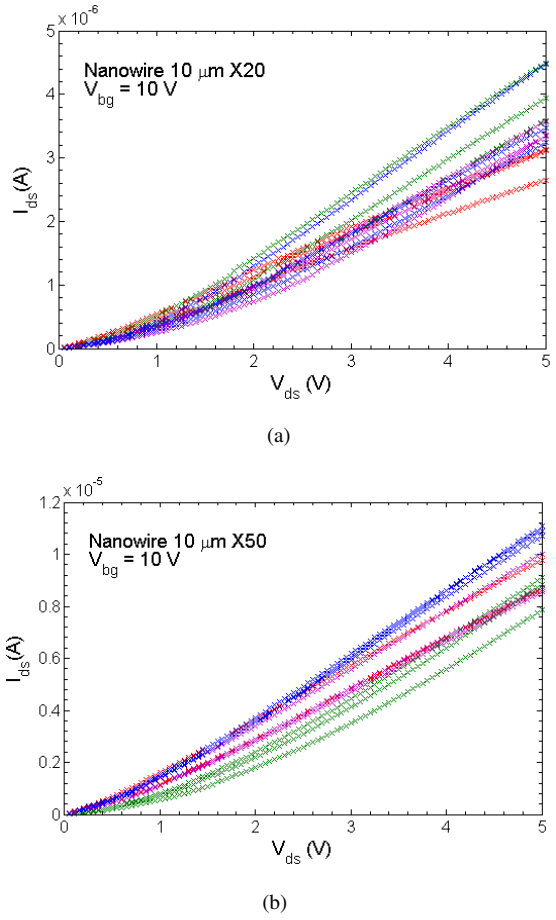


FIGURE 6.17: I_{ds}-V_{ds} characteristics of 12 oxidised nanowire biosensors comprised of (a) 20 and (b) 50 nanowires connected in parallel.

Resistances of the same devices at back-gate biases of 5 V and 15 V can be extracted from I_{ds}-V_{ds} characteristics using the same procedure above. Table 6.1 shows measured resistances of 10 μm long nanowires with 20, 50 and 100 nanowires connected in parallel. Results are shown for back-gate biases, V_{bg}, of 5 V, 10 V and 15 V. The percentage resistance spreads are presented in brackets. Interestingly, Table 6.1 shows that the standard deviation decreases significantly from 20% to 8% when the number of nanowires increases from 20 to 100 at a back-gate bias of 5 V. A similar, though less pronounced, trend can be seen at back-gate biases of 10 V and 15 V. This result will be discussed in more detail later in this chapter.

TABLE 6.1: Comparison of extracted resistances for biosensors comprising of 10 μm long oxidised nanowires connected in parallel at different back-gate biases

Num. in parallel of nanowires	×20	×50	×100
R (MΩ), at V_{bg} = 5 V	4.95±0.98 (20%)	1.66±0.15 (9%)	0.87±0.07 (8%)
R (MΩ), at V_{bg} = 10 V	1.36±0.21 (15%)	0.506±0.055 (11%)	0.253±0.025 (10%)
R (MΩ), at V_{bg} = 15 V	0.75±0.12 (15%)	0.284±0.033 (12%)	0.141±0.016 (11%)

Fig. 6.18 shows a graph of conductance as a function of the number of nanowires connected in parallel for different values of back-gate bias. For a back-gate bias of

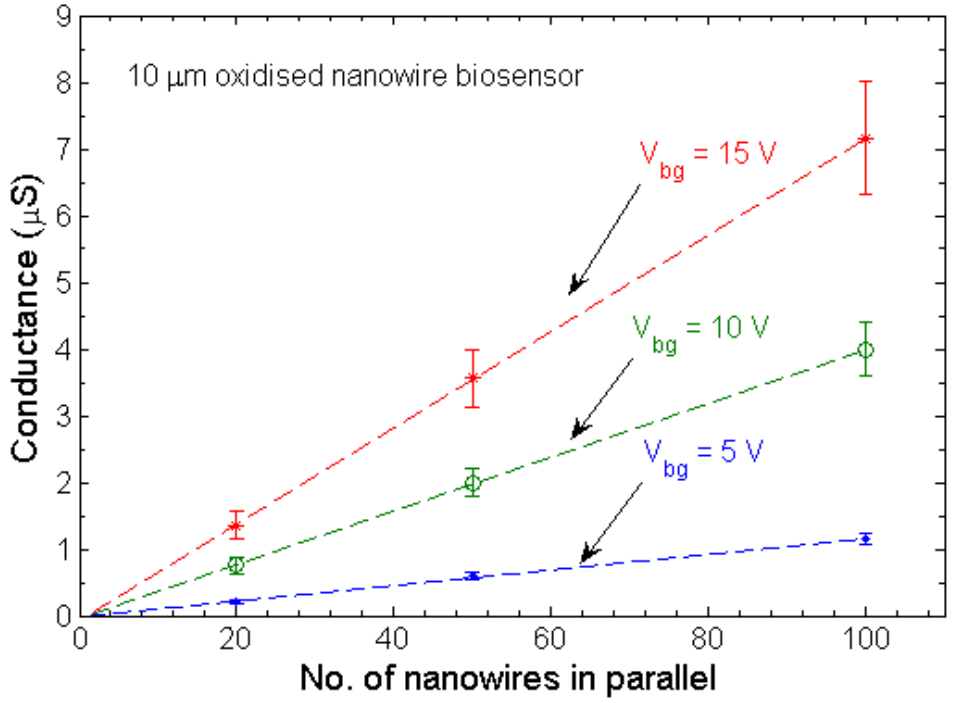


FIGURE 6.18: Conductance as a function of the number of 10 μm nanowires connected in parallel under back-gate biases of 5 V, 10 V and 15 V.

15 V, a linear relation is obtained and a conductance of 11.7 nS can be extracted for a single nanowire from the slope. This can be converted into a resistance of 85.5 MΩ for a single 10 μm long nanowire. Conductances of 40.4 nS per nanowire and 72.4 nS per nanowire can also be extracted for V_{bg} = 10 V and 15 V, respectively. The corresponding resistances are 24.8 MΩ and 13.8 MΩ. The measured conductances in Fig. 6.18 scale approximately as expected. For example, the conductance of 20 parallel nanowires at V_{bg} = 15 V is 1.36 μS. The expected value for 100 parallel nanowires should therefore be 6.80 μS, which compares with the measured value of 7.16 μS. This result implies

that few of the nanowires are broken.

6.4.7 Subthreshold characteristics

Fig. 6.19 shows sub-threshold characteristics for a 100 $\times$ 10 μm device plotted on both linear and logarithmic scales. For the linear characteristic, the transistor drain current is negligible for $V_{bg}<$ 2 V and increases with the back-gate bias for $V_{bg} >$ 2 V. Thus, the I_{gs}-V_{bg} curve unambiguously shows n-channel enhancement mode characteristics. The threshold voltage can be extracted to be about 3 V from the gate bias when the subthreshold slope starts to saturate. These results indicate that the nanowire is nearly fully depleted at zero back-gate bias. The application of back-gate biases above $\approx$ 3 V then creates an n-type accumulation layer in the n-type nanowire, leading to an increase in drain current. From the logarithmic characteristic, the device has a subthreshold slope (SS) of 1.05 V/decade and an I_{on}/I_{off} ratio of about 10^5.

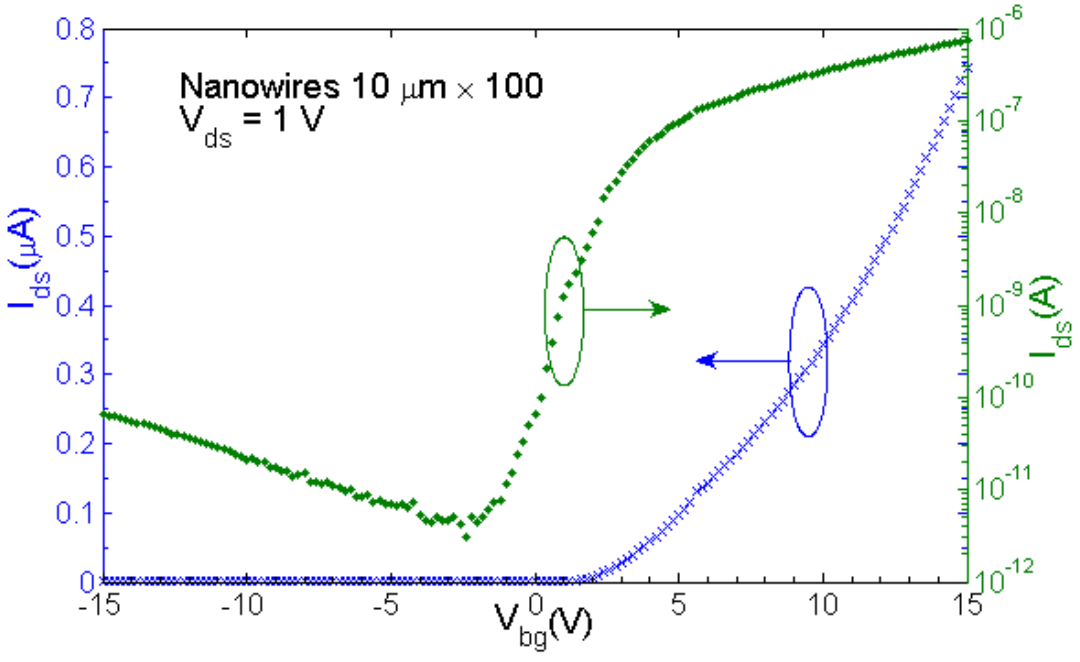


FIGURE 6.19: Subthreshold characteristic of a typical nanowire biosensor with 100 parallel nanowires of 10 μm length. The measurement was made at a drain bias of 1 V.

6.4.8 Wafer map

Device uniformity is further investigated by measuring an identical device (10 μm $\times$ 100) on each chip across the whole wafer under the same back-gate bias of 10 V, as shown in Fig. 6.20. The device resistances in the majority of the wafer are generally between 0.21 MΩ and 0.33 MΩ, whereas the resistances at the far right of the wafer are significantly lower, around 0.15 MΩ. These results are very promising, particularly when it is considered that significant resistance variations might be expected from variations of amorphous silicon deposition and the etching across the wafer.

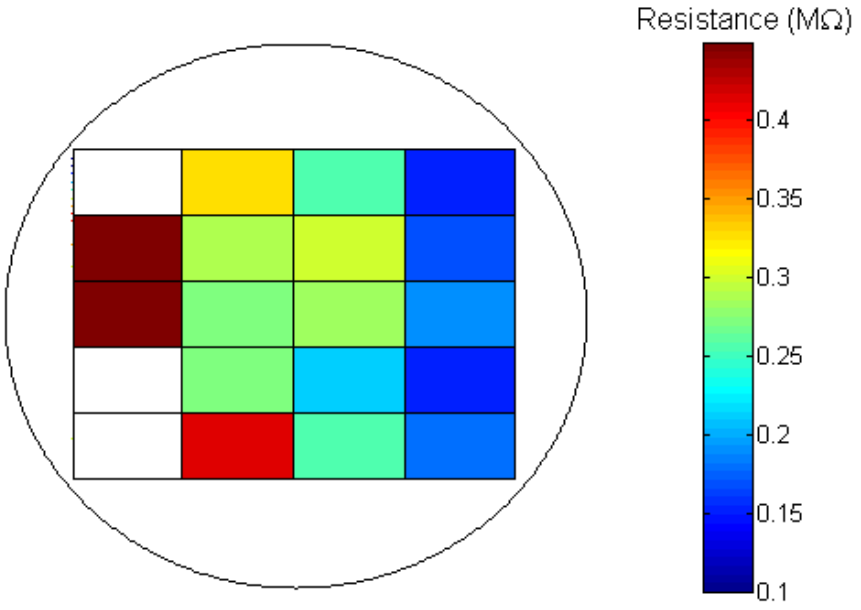


FIGURE 6.20: Wafer map of oxidised nanowire biosensor resistance measured at V_{bg} = 10 V for a device with 100 parallel 10 μm nanowires.

6.4.9 Unoxidised 100 nm nanowire biosensors

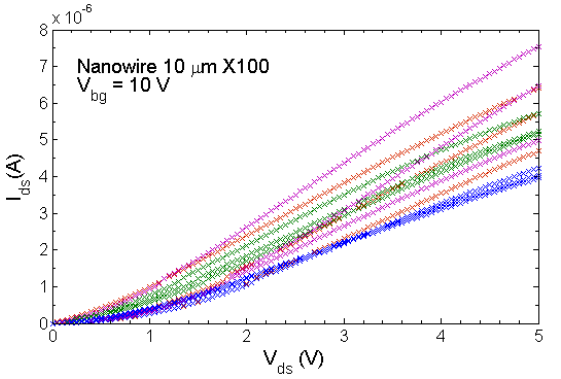
To provide some insight into the effect of the surface on the performance of the nanowire biosensor, measurements have been made on nanowire biosensors that did not have a thermal oxide layer grown on the nanowire. As discussed in section 6.3.1, these devices have been processed at a lower temperature (600°C compared with 900°C) and would be expected to have a native oxide layer on the surface of the nanowire. Fig.

6.21(a) shows I_{ds}-V_{ds} characteristics for 11 devices with 100 parallel, 10 μm unoxidised nanowires. Measurements were made at a back-gate bias of 10 V. Above a bias of about 2 V, the drain currents show approximately linear characteristics. The resistance has been extracted using linear fits ($V_{ds} > 2$ V) to be 825$\pm$151 kΩ (18 %). A comparison of this value with that for oxidised nanowires with the same dimension, (253$\pm$25 kΩ, in Fig. 6.14), shows that oxidised nanowires have a clearly significantly lower resistance and smaller spreads than unoxidised nanowires. This result is confirmed for devices with 50 and 20 parallel unoxidised nanowires, as shown in Fig. 6.21(b) and (c), respectively. The extracted resistances for 50 and 20 parallel unoxidised nanowire biosensors are 1.72$\pm$0.30 MΩ and 4.88$\pm$1.42 MΩ, respectively.

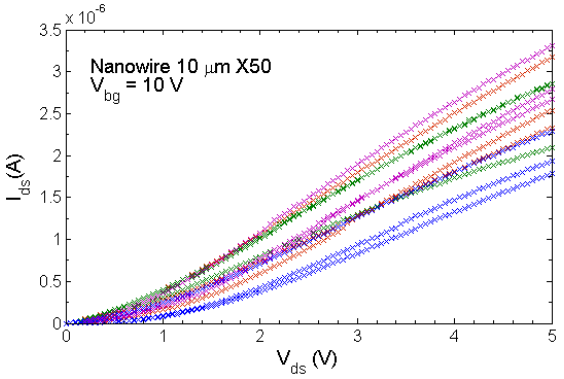
Fig. 6.22 summarises extracted values of conductance as a function of the number of unoxidised nanowires connected in parallel for different back-gate biases. Linear characteristics are obtained for all three back-gate biases of 5 V, 10 V and 15 V. The conductances for a single nanowire can be extracted from the slopes, giving 1.4 nS, 12.7 nS and 36.9 nS for back-gate biases of 5 V, 10 V and 15 V, respectively. The corresponding resistances for of a single nanowire are 713.8 MΩ, 78.8 MΩ and 27.1 MΩ for V_{bg} = 5 V, 10 V and 15 V, respectively. The measured conductances in Fig. 6.22 scale approximately as expected, as was also observed for the oxidised nanowires in Fig. 6.18. For example, the conductance of 20 parallel nanowires at V_{bg} = 15 V is 0.68 μS. The expected nanowire conductance for 100 parallel nanowires should therefore be 3.40 μS, which compares with the measured value of 3.63 μm. This result again implies that few of nanowires are broken.

Fig. 6.23 compares the values of conductance for devices with oxidised and unoxidised nanowires. The conductances of devices with the thermal oxide layer are significantly larger than those without the thermal oxide layer under the same back-gate bias. This result could be explained by the higher temperature used in the fabrication of the oxidised nanowires (maximum temperature of 900°C) compared with the unoxidised nanowires (maximum temperature of 600°C). Higher temperature process would be expected to increase α-Si crystallisation, decrease trap densities at grain boundaries and increase dopant activation in the nanowires [120]. It can also be seen that the conductance changes due to back-gate bias are more significant for devices with oxidised nanowires. This might be due to the bigger role played by surface charges in unoxidised nanowires than in oxidised nanowires, which could weaken the influence of the back-gate bias.

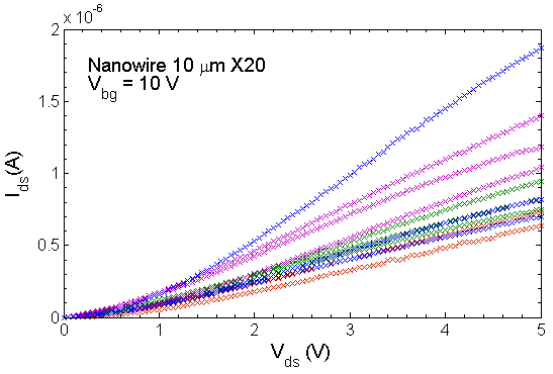
The conductance variations of the measured devices have been analysed by defining a



(a)



(b)



(c)

FIGURE 6.21: I_{ds}-V$_{ds}$ characteristics of 11 or 12 unoxidised nanowire biosensors comprising (a) 100 parallel nanowires, (b) 50 parallel nanowires and (c) 20 parallel nanowires. All devices were measured at a back-gate bias of 10 V.

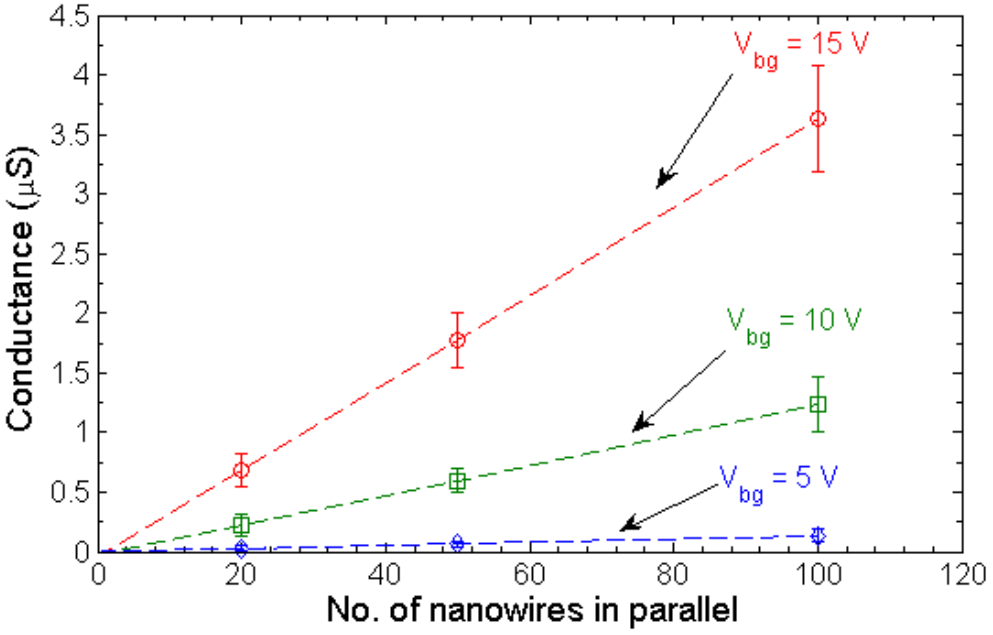


FIGURE 6.22: Conductance as a function of nanowire number in parallel of 10 μm long nanowire biosensor under back-gate biases of 5 V, 10 V and 15 V. The nanowire surface is not covered with a thermal oxide layer.

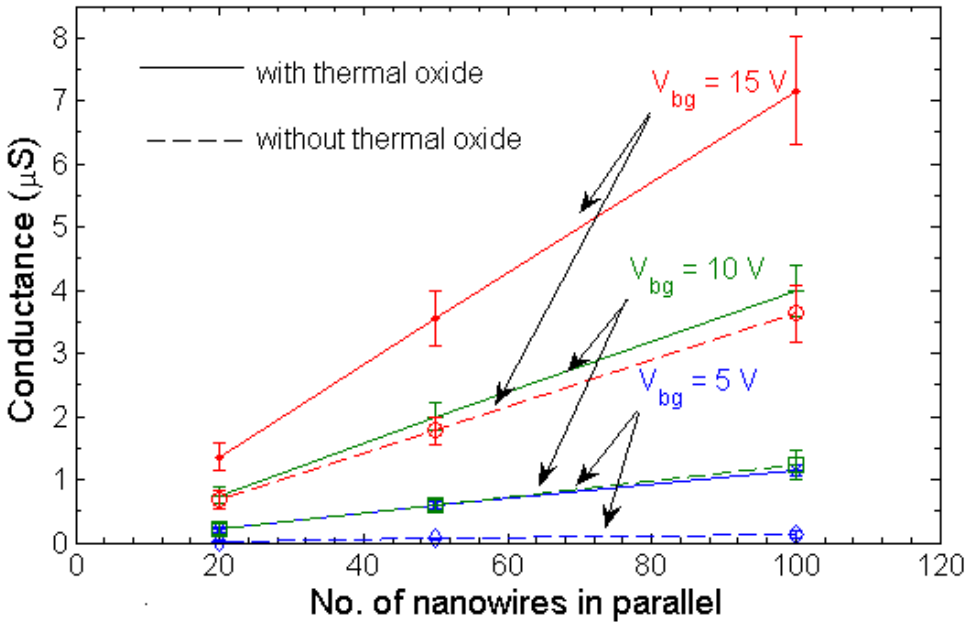


FIGURE 6.23: Comparison of conductances of oxidised and unoxidised nanowire biosensors for back-gate biases of 5 V, 10 V and 15 V.

normalised conductance variation, given by the standard deviation of the conductance divided by the mean conductance, as shown in Fig. 6.24. The conductance variations for the unoxidised nanowire biosensors are larger than for the oxidised nanowire biosensors at all values of back-gate bias. A second interesting trend can be seen in Fig. 6.24, namely that the conductance variations decrease for both types of biosensor as the number of parallel nanowires increases. This indicates that multiple nanowires in parallel are preferred for reducing the conductance variations of fabricated biosensors. A third trend is that, for the unoxidised nanowire biosensors, the conductance variation decreases significantly with increasing of back-gate bias.

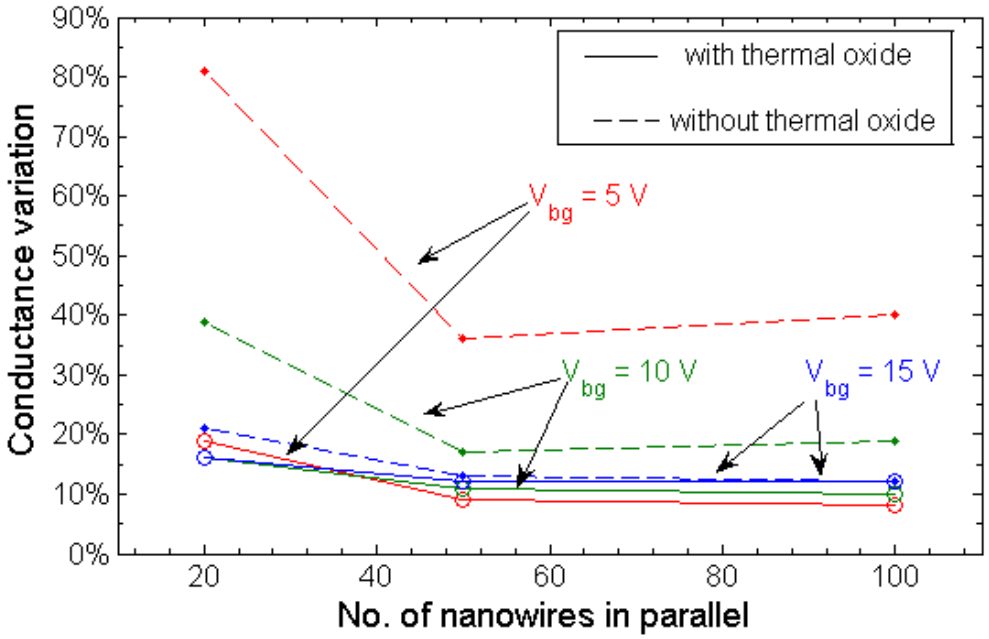


FIGURE 6.24: Normalised conductance variation (conductance standard deviation divided by conductance mean) as a function of the number of nanowires connected in parallel for oxidised and unoxidised nanowire biosensors. The nanowires were 10 μm long and measurements were made at back-gate biases of 5 V, 10 V and 15 V.

6.4.10 pH detection using fabricated Si nanowire biosensors

Fig. 6.25 shows the I_{ds}-V_{bg} characteristics of a typical fabricated nanowire biosensor under a drain bias of 10 V for different pH solutions. These nanowires (detailed in Appendix E) are different than those discussed previously and were doped using two 1×10^{13} cm^{-2} implants. The sensor consists of 100 parallel 20 μm nanowires. The results show that the drain current decreases with decreasing pH. This can be explained by

the sensing mechanism of an ion-sensitive field-effect transistor [5]. Hydroxyl groups (-OH) on the nanowire surface (SiO_2) can be protonated (OH_2^+) or deprotonated (O^-) [4], hereby changing the charge on the nanowire surface [121]. In solutions with low values of pH, the hydroxyl groups are mainly protonated, whereas in solutions with high values of pH, the hydroxyl groups are mainly deprotonated. The negative charge from the deprotonated hydroxyl groups decreases the conductance of the n-type nanowires. Therefore, the fabricated biosensor can be used for pH sensing and this demonstrates their potential for biosensing when the nanowire surface is given appropriate functionalisation.

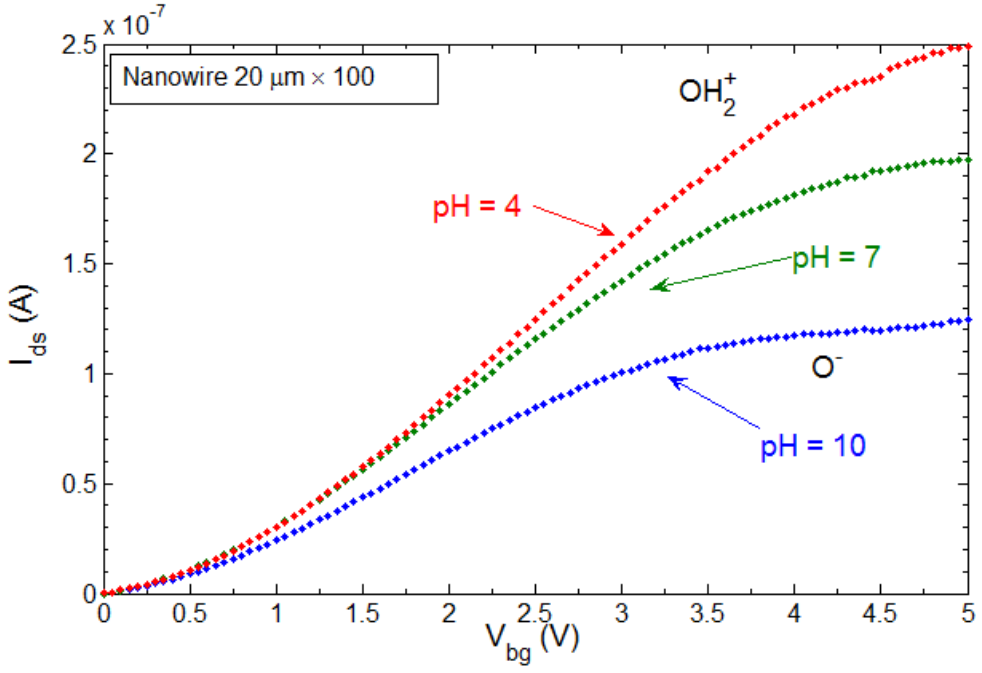


FIGURE 6.25: I_{ds}-V_{gs} characteristics of a biosensor of 20 μm $\times$100 nanowires measured in solutions with values of pH of 4, 7 or 10. The drain bias was set to 10 V.

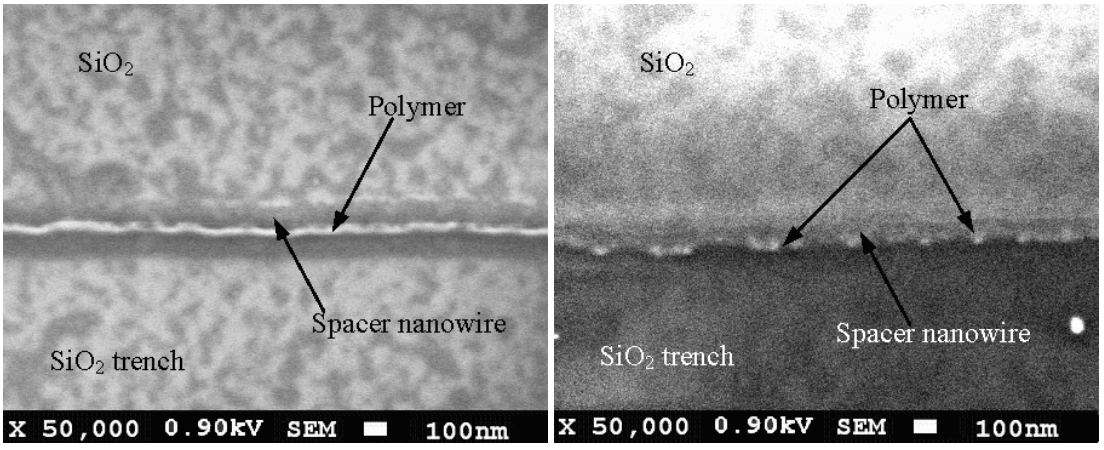
6.5 Discussion

6.5.1 Shape variability of etched nanowires

As shown in Fig. 6.7(c) and Fig. 6.12(b), different nanowire shapes were found on wafers that were fabricated using the same etching recipes. In this work, a 'Bosch' process was used for the Si nanowire etch, which uses a fluorine based plasma chemistry

for Si etch and a fluorocarbon plasma process for forming a sidewall passivation layer. The Si etch was done using sulphurhexafluoride (SF_6), which provides the necessary fluorine for silicon etching. The sidewall passivation was achieved using octofluorocyclobutane (C_4F_8), which produces CF_2 and longer chain radicals [122]. These can then form a fluorocarbon polymer layer on the etched sample. By fast plasma switching between etch and passivation formation cycles, an anisotropic Si etch can be achieved. In the literature, reported spacer nanowires [29] are triangular in shape when conventional reactive ion etch (RIE) processes are used.

To investigate the inconsistency of nanowire shapes, plan SEM inspections have been performed on wafers with 'rectangular' spacers and 'triangular' spacers. Both chips were etched in the same run and thus the etch conditions were identical. Fig. 6.26(a) shows a high magnification plan-view SEM micrograph of a 'rectangular' nanowire. The nanowire is continuous and a continuous white line can be seen on the side of the nanowire due to the deposited polymer. Fig. 6.26(b) shows an SEM micrograph of a triangular nanowire is also continuous but the polymer layer is discontinuous. Thus, polymer on square nanowires is much more uniform than that on triangular nanowires. As both samples were etched at the same time in the same run at the chamber centre,



(a) rectangular nanowire (b) triangle nanowire

FIGURE 6.26: High magnification plan SEM micrographs of etched nanowires from (a) wafer giving 'square' nanowires and (b) wafer giving 'triangle' nanowires. Both chips were etched in the same run of 20 cycles.

the polymer non-uniformity is unlikely to be caused by machine non-uniformity. Therefore, the most likely explanation is that the variability in nanowire shape is due to the photolithography for the oxide step definition.

6.5.2 Mobility and trap state density extraction

The electrical characteristics of the nanowire biosensors in this work showed field effect transistor characteristics, as shown in Figs. 6.13 and 6.19. The effective electron mobility can be extracted using MOSFET model in Chapter 3. The threshold voltage can be extracted to be 3 V from the subthreshold slope in Fig. 6.19 of a device with 100 parallel nanowires in length of 10 μm. The resistances at gate biases from 8 V to 25 V can be extracted from Fig. 6.13 using a slope fitting technique to be 338 kΩ, 237 kΩ, 184 kΩ, 138 kΩ, 114 kΩ and 102 kΩ. When V_g is much larger than $\frac{1}{2}V_{ds}$, equation (3.32) can be simplified by neglecting the second order V_{ds} term:

$$I_{ds} \approx \beta \left(V_g - V_t\right) V_{ds} \tag{6.1}$$

where $\beta = C_{ox}\mu_{ps,n,eff}\left(W/L\right)$. Thus, the nanowire channel resistance, R_{ch}, is expressed as:

$$R_{ch} = \frac{V_{ds}}{I_{ds}} = \frac{1}{\beta \left(V_g - V_t\right)} \tag{6.2}$$

As Source/Drain and contact resistance cannot be neglected, the total resistance of the device is written as;

$$R_{total} = R_{ch} + R_{ds} = \frac{1}{\beta \left(V_g - V_t\right)} + R_{ds} \tag{6.3}$$

where R_{ds} is the resistance contributed by contact, source and drain and R_{total} is the total measured resistance, which is the extracted resistance from the I-V curves in Fig. 6.13. By plotting R_{total} against $1/\left(V_g - V_t\right)$, R_{ds} and β can be extracted to be 20 kΩ and 6.46×10^{-7} F.m^2/V.s from the offset and slope, respectively. Using the expression of β above, the (poly-Si) effective mobility, $\mu_{ps,ne,ff}$ could be calculated. The value of C_{ox} is calculated from $C_{ox} = \epsilon_{ox}/t_{ox}$ using the buried oxide thickness, t_{ox}, of 580 nm, whilst W and L are 100 nm and 80 nm, respectively, from cross-section SEM measurement in Fig. 6.12. Thus, the $\mu_{ps,n,eff}$ is calculated to be 66 cm^2/V.s.

The trap state density can be extracted using the method reported in works [26] [29] [101]. In these publications, the channels were undoped and thus the channel carrier concentration is mainly modulated by the applied gate bias. Therefore, the trap state density was extracted using a modified Seto model with gate-effect [123]. However, a doped channel is used in this work and thus the gate effect is assumed to be less significant. As given in Chapter 3, a simplified model is used to extract trap state density.

Using equation (3.31) (Seto model), potential barrier height, V_b, can be calculated when $\mu_{n,eff}$ is available. The effective electron mobility ($\mu_{n,eff}$) in (111) single crystal silicon [124] is 180 cm^2/V.s. As polysilicon from solid-phase crystallisation is mainly in (111) orientation [125], the barrier height can be extracted to be 28 mV using Eq. (3.31). Assuming poly-Si grains are partially depleted, trap state density, N_t, can be extracted using Eq. (3.30). The channel doping concentration, N, is estimated to be 2×10^{18} cm^{-3} from a Silvaco Athena simulator using the implant conditions. Then the grain boundary trap state density can be calculated to be 1.7×10^{12} cm^{-2}. For typical poly-Si grains crystallised at the same condition of a 600°C anneal for 20 hours, the poly-Si grain size, L_g, is about 0.1 μm from [126] and N_t is calculated to be smaller than L_gN of 2.0×10^{13} cm^{-2}, which confirms the assumption that poly-Si grains are partially depleted.

These extracted parameters of mobility and trap state density are compared with nanowire and sheet transistors from the literature, in Table 6.2. The mobility in this work well matches those of the reported nanowire transistors but is higher than those of the sheet transistors. However, more data are needed to confirm whether this trend is universal or just due to different conditions of the deposited amorphous silicon films. The slightly higher mobility in this work than other nanowire transistors could be due to high temperature thermal oxidation at 900°C. The extracted trap state density is similar to that in [29] but significantly lower than those in Chang's works [26] [127]. The lower trap state density for devices in this work could again be due to the high temperature thermal oxidation process at 900°C. The low trap state density in Chang's work [29] could be due to the NH_3 plasma treatment, which passivates trap states at grain boundary as reported in Sheu's work [128]. For the other works, no plasma treatment or hydrogen anneal was given to the fabricated devices and the grain trap states were not passivated.

TABLE 6.2: Comparison of the fabricated poly-Si nanowire transistor with poly-Si sheet and nanowire transistors reported in the literature

	this work	Chang *et al* [26]	Chang *et al* [29]	Lin *et al* [25]	Chang *et al* [127]
Channel	100 nanowires	sheet	sheet	2 nanowires	2 nanowires
Width/length	180 nm/10 μm	10 μm/10 μm	1 μm/10 μm	21 nm/2 μm	100 nm/1 μm
Si thickness (nm)	80 nm	100 nm	50 nm	23 nm	50 nm
μ_{eff} (cm^2/V.s)	66	26	22	55	42
N_t (/cm^2)	1.7×10^{12}	6.5×10^{12}	1.4×10^{12}	NA	5.7×10^{12}

6.5.3 Comparison with the literature values of nanowire resistance

From the measured I-V curves, e.g. Fig. 6.14, it is clear that 100 nm polysilicon nanowires have been successfully fabricated using a spacer etch technology using a Bosch process. The fabricated nanowires show reasonably linear characteristics and are reasonably reproducible with uniform values of conductance. A comparison between the nanowire resistances obtained in this work and those reported in the literature [24][129][130] is given in Table 6.3. In Chen's work [129], single-crystal triangular nanowires were fabricated using SOI wafers and a Si wet etch. The extracted resistance for a single nanowire was about 63.6 kΩ/μm for a -5 V back-gate bias with a 150 nm buried oxide insulator. In Hsiao's work [24], undoped polysilicon nanowires were formed using a spacer etch technology and an RIE etch. These nanowires had width $\times$ height dimensions of 110 nm $\times$ 100 nm and were fabricated on a 50 nm silicon nitride layer. A nanowire resistance of about 1.1 MΩ/μm was reported for a 5 V back-gate bias. In Park's work [130], single-crystal nanowires were fabricated using SOI wafers by e-beam lithography and RIE etching and the extracted resistance for a single nanowire was about 0.2 MΩ/μm at an unspecified back-gate bias.

The nanowire resistance obtained in this work is a factor of 8 larger than that in Hsiao's work, a factor of 130 larger than that in Chen's work and a factor of 42 larger than that in Park's work. Chen's nanowires were fabricated in single-crystal silicon and hence a significantly lower sheet resistance would be expected for the same doping due to the effect of grain boundaries [87]. Furthermore, as nanowire conductance can be tuned by the back-gate bias, the thick gate oxide of 580 nm in this work would be much less effective than the 150 nm gate oxide in Chen's work [129]. The significantly higher resistance in this work than in Chen's work could therefore be explained by a combination of these two mechanisms.

The lower value of nanowire resistance seen in Hsiao's work [24] is very surprising, given that their nanowires were said to be undoped. There are a number of possible explanations for this surprising result. First, the thinner gate oxide in their devices would be more effective in reducing the nanowire resistance, as was the case in the work of Chen *et al* [129]. Second, the possibility of unintentional doping in Hsiao's nanowires cannot be discounted as no measurement of nanowire doping was reported in their paper. Finally, as discussed earlier that the combination of grain boundaries (trapped charges) and low doping in the nanowires has given these nanowires that are nearly fully depleted at zero bias. If this was the case, the values of resistance in these nanowires would be expected to be slightly lower than those of Hsiao *et al*. As the

resistance of these nanowires is 8 times that of Hsiao's, it casts some doubt on their claim that the nanowires are undoped.

The nanowires in Park's work [130] also gave a lower value of resistance. This can be attributed to two possible reasons. First, a higher implant dose than that in this work was used and this can significantly reduce the nanowire resistivity. Secondly, as for Chen's work, the single-crystal silicon would be expected to give a lower sheet resistance. It should be mentioned that the values of back-gate bias and buried insulator thickness were not specified in the paper by Park *et al* [130]. However, the estimated dopant concentration for their nanowires is as high as 5×10^{18} cm^{-3} [130] and this high dopant concentration would strongly limit the influence of the back-gate bias. Therefore, the influence of unspecified back-gate bias and buried insulator thickness on the nanowire resistance can be discounted. In this work, the conductance of the nanowire biosensor was found to be tuned by the back-gate substrate (Fig. 6.13). Similar results were also reported in the literature [24][79][129].

TABLE 6.3: Comparison of fabricated nanowires with nanowires reported in the literature

	this work	Chen *et al* [129]	Hsiao *et al* [24]	Park *et al* [130]
Material	polycrystalline	single-crystalline	polycrystalline	single-crystalline
Nanowire (width/height)	100 nm/80 nm	50 nm/30 nm	110 nm/100 nm	130 nm/50 nm
Nanowire (length)	10 μm	10 μm	10 μm	40 μm
Channel doping implant	P, 4×10^{13} cm^{-2}	B, 2×10^{13} cm^{-2}	undoped	B, 1.2×10^{14} cm^{-2}
Buried insulator (nm)	SiO_2, 700	SiO_2, 150	SiO_2,100+SiN_x,50	Unspecified
Resist. of Single NW	8.5 MΩ/μm	63.6 kΩ/μm	1.1 MΩ/μm	0.2 MΩ/μm
Back-gate bias	5 V	-5 V	5 V	Unspecified
I_{ds}(V_{ds} = 5 V)	0.06 μA	2.5 μA	NA	0.6 μA

6.6 Conclusions

In this work, a fabrication process has been successfully demonstrated for low-cost Si nanowire biosensors using thin film technology. A spacer nanowire etch technology using a Bosch process provides a highly anisotropic etch. This process gives rectangular nanowires when the lithography is properly optimised.

Electrical measurements show that linear I/V characteristics are generally obtained for source/drain biases greater than about 2 V. Furthermore, the nanowire conductance can be tuned by varying the back-gate bias as the applied bias. The fabricated nanowire biosensors with 50 and 100 parallel oxidised nanowires showed repeatable electrical

characteristics with about 10% variation in resistance for a back-gate bias of 10 V or 15 V. Resistances were extracted for a single nanowire and values of 8.5 MΩ/μm, 2.5 MΩ/μm and 1.4 MΩ/μm for back-gate biases of 5 V, 10 V and 15 V, respectively. Nanowires with and without a thermal oxide layer were also studied and the oxidised nanowires were found to give a superior uniformity of 10% compared with 18% for unoxidised nanowires. Conductance variations were lower in both oxidised and unoxidised nanowires when a large number of nanowires were connected in parallel. In summary, oxidised 10 μm nanowire biosensors with around 100 nanowires connected in parallel are preferred for biosensor applications.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

In this thesis, a novel technology has been reported for the fabrication of silicon nanowires for application in nanowire biosensors. The approach is based on thin film transistor (TFT) technology, which is commonly used in TVs and computer displays. Polycrystalline Si nanowires have been successfully fabricated using a mature 1 μm, top-down, microelectronic technology that is low cost and suitable for multiplexed immunoassay. The polycrystalline Si has been produced using the metal-induced lateral crystallisation, with the aim of achieving process temperatures that are low enough to satisfy the constraint of 450°C, which is imposed by the use of low-cost glass substrates. Material studies have been undertaken on the metal-induced lateral crystallisation of α-Si at low temperatures using fluorine to suppress random grain nucleation and using different deposition procedures and substrate types to increase the crystallisation length at a given temperature. It has been demonstrated that metal-induced lateral crystallisation can be achieved at anneal temperatures down to 428°C. A crystallisation length of 1.2 μm has been achieved for a lateral crystallisation anneal at 428°C, which is the lowest temperature reported for MILC. These results therefore demonstrate the feasibility of using low-cost glass as a substrate for Si nanowire biosensor fabrication. The effect of fluorine implantation dose on α-Si lateral crystallisation has been studied and an optimum dose of 2.5×10^{15} cm^{-2} has been identified. This implantation dose gives an increase in MILC length by 29% for a 10 hour MILC anneal at 550°C and by 17% for a 20 hour MILC anneal at 525°C. The action of the F is explained by the suppression of random grain nucleation at the α-Si/SiO_2 interface with higher fluorine doses giving higher

fluorine concentration at the α-Si/SiO_2 interface and hence more effective suppression of random grain nucleation. The lateral crystallisation length decreases for a higher F dose, 5×10^{15} cm^{-2}, which has been explained by the effect of implant damage (amorphisation) intersecting the α-Si/SiO_2 interface. At temperatures $\leq$ 500°C, fluorine gives a suppression in the MILC length. This result can be partially explained by the lack of F migration at these low temperatures. Another contributing factor may be difficulties in annealing the implantation damage from the F implant at such low temperatures.

Results on the lateral crystallisation of α-Si nanowires have been reported for the first time. A crystallisation length of 13 μm has been achieved in nanowires for a lateral crystallisation anneal at 550°C. This demonstrates that metal-induced lateral crystallisation can be used for polysilicon nanowire formation at a temperature that is 75°C lower than the typical polysilicon deposition temperature of 625°C . Results have also been reported on the metal-induced lateral crystallisation of micro-wide α-Si ribbons and a crystallisation length of 56 um has been achieved in 4 μm wide α-Si ribbons. The MILC length in α-Si ribbons decreases with decreasing ribbon width and the MILC length in nanowires lies below the trend line for the ribbons, indicating that lateral crystallisation is more difficult in nanowires than ribbons. Longer MILC lengths have been obtained using LPCVD α-Si than PECVD α-Si, which has been explained by the lower deposition temperature for PECVD α-Si and hence the lower degree of crystallinity. Si-on-Air structures also give significantly longer MILC lengths than Si-on-Oxide structures due to the removal of sites for random grain nucleation at the α-Si/oxide interface. Si-on-Nitride structures, which are better than Si-on-Oxide structures for functionalisation, gives only slightly shorter MILC lengths than Si-on-Oxide structures.

A top-down nanowire fabrication process has been developed using a Bosch etch process. This process gives rectangular nanowires with a well-controlled width of about 100 nm when the lithography is properly optimised. Electrical measurements show that linear I/V characteristics are generally obtained for source/drain biases greater than about 5 V. Furthermore, the nanowire conductance can be tuned by varying the back-gate bias. The fabricated nanowire biosensors showed repeatable electrical characteristics with about 10% variation in resistance for 50 or 100 parallel nanowires and a back-gate bias of 10 V or 15 V. Resistances were extracted for a single nanowire in values of 8.5 MΩ/μm, 2.5 MΩ/μm and 1.4 MΩ/μm for back-gate biases of 5 V, 10 V and 15 V, respectively. A comparison of nanowires with and without a thermal oxide layer has shown that oxidised nanowires has a uniformity of 10% compared with 18% for unoxidised nanowires. In addition, conductance variations were lower at high values of back-gate bias and decreased significantly as more nanowires were connected in paral-

lel. Therefore, biosensors comprising 100 parallel, oxidised nanowires are preferred. A comparison of measured and calculated values of nanowire current has shown that the measured currents are lower than expected. It has been tentatively proposed that this discrepancy is due to surface roughness on the etched nanowire surface.

7.2 Future Works

- **Nanowire lateral crystallisation at low temperatures**
  In this work lateral crystallisation of α-Si ribbons and sheets has been found to occur at anneal temperatures down to 428°C. In addition, lateral crystallisation in nanowires has been studied at an anneal temperature of 550°C. Further work is needed to investigate lateral crystallisation in nanowires at lower temperatures. This would give further insight into the suitability of metal-induced lateral crystallisation for the fabrication of polysilicon nanowires for biosensor applications.

- **Lateral crystallisation of suspended α-Si ribbons and nanowires**
  In this work Si-on-Air α-Si ribbons were found to give a significantly longer lateral crystallisation length than Si-on-Oxide ribbons. However, the Si-on-Air ribbons were not fully suspended and thus further work needs to be carried out to investigate the lateral crystallisation of fully suspended α-Si ribbons. HF vapour etch could be used to free ribbons from the substrates, thereby avoiding the surface tension associated with wet HF etch.

- **Poly-Si nanowire biosensor fabrication using lateral crystallisation**
  In this work a fabrication process has been developed for poly-Si nanowire biosensors made using solid-phase crystallisation. As poly-Si nanowires could also be crystallised by metal-induced lateral crystallisation, it would be sensible to investigate polysilicon nanowire biosensor fabrication using this method. A comparison of the electrical performance could then be made between biosensors fabricated by lateral crystallisation and by solid-phase crystallisation.

- **Lateral crystallisation of Ge nanowires for biosensor applications**
  In recent years, germanium has also been studied for biosensor applications [114]. As the melting point of amorphous germanium (α-Ge) is less than that of α-Si, it should be possible to achieve metal-induced lateral crystallisation at a lower temperature. Kanno *et al* [131] and Park *et al* [132] have shown that metal-induced lateral crystallisation can be used to crystallise α-Ge at a temperature

of 400°C , which is already compatible with glass substrates. As an alternative of α-Si, it would therefore be interesting to develop a top-down process for the fabrication of Ge nanowire biosensors.

- **Effect of fluorine on Ge nanowire lateral crystallisation**
  In Hakim *et al* work [31], fluorine was found to improve α-Si lateral crystallisation by suppressing random grain nucleation at the α-Si/SiO_2 interface. Park *et al* [133] have reported that random crystallisation also limits metal-induced lateral crystallisation in α-Ge. It would therefore be interesting to investigate effect of fluorine on metal-induced lateral crystallisation in α-Ge.

Appendix A

Suface Charge Derivation for an n-channel MOS device

For a MOS capacitor or MOSFET with the Source/Drain grounded, the problem can be solved by a 1-dimensional equation:

$$\frac{d^2\psi}{dy^2} = -\frac{q}{\varepsilon_{Si}}\left[p(y) - n(y) + N_D^+(y) - N_A^-(y)\right] \tag{A.1}$$

where N_D^+ and N_A^- are the concentrations of ionized donors and accepters, respectively. Here, ε_{Si} is the permittivity of silicon. In bulk region, the charge neutrality condition gives the sum of all the right terms to zero. In the surface region, the hole and electron concentrations are given in terms of ψ, defined as $\psi(y) = \psi_i - \psi_i(+\infty)$. The Poisson equation can be rewritten as:

$$\frac{d^2\psi}{dy^2} = -\frac{q}{\varepsilon_{Si}}N_A\left[\exp\left(-\frac{q\psi}{kT}\right) - 1 - \frac{n_i^2}{N_A^2}\left(\exp\left(\frac{q\psi}{kT}\right) - 1\right)\right] \tag{A.2}$$

This equation cannot be solved directly. However, the electric field, $E = -\frac{d\psi}{dy}$ can be solved by integrating Eq.(A.2). At the surface, $y = 0$, the surface charge, ψ_s, in the silicon can be obtained using Gauss's law.

$$Q_s = -\varepsilon_{Si}E_s = -\sqrt{2kTN_A\varepsilon_{Si}}\left\{\exp\left(-\frac{q\psi_s}{kT}\right) + \frac{q\psi_s}{kT} - 1 + \frac{n_i^2}{N_A^2}\left[\exp\left(\frac{q\psi_s}{kT}\right) - \frac{q\psi_s}{kT} - 1\right]\right\}^{\frac{1}{2}} \tag{A.3}$$

The negative sign means that the charge in the channel is negative whilst the charges

induced in on the gate is positive. To show the behaviour of Eq.(A.3),the surface charge against surface potential is plotted in Fig. A.1. From the plot, the surface charge in the depletion region is dominated by depleted charge, the term of $\left(\frac{q\psi_s}{kT}\right)^{\frac{1}{2}}$, whilst the inversion charge, mainly the $\exp\frac{q\psi_s}{2kT}$ term, plays a dominate role in the surface charge.

Using the surface charge equation Eq.(A.3), strong inversion can also be defined as:

$$\frac{n_i^2}{N_2^2}\exp\left(\frac{q\psi_s}{kT}\right) = 1 \tag{A.4}$$

The surface potential can be solved in the same form given in Section3.1.1.1:

$$\psi_s = \frac{kT}{q}\ln\frac{N_A^2}{n_i^2} = 2\psi_B \tag{A.5}$$

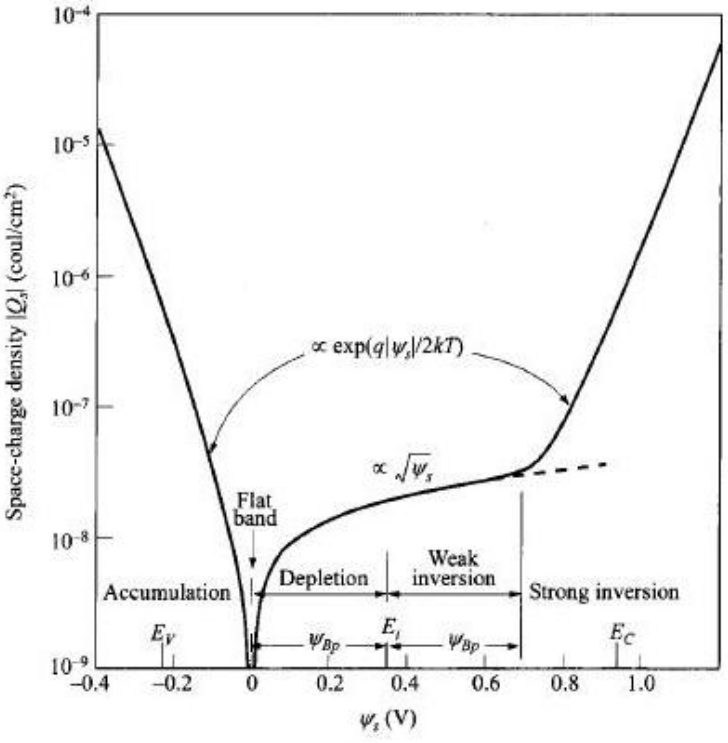


FIGURE A.1: The surface charge density in silicon as a function of surface potential, ψ_s for a p-type MOS capacitor. After Sze and Kwok [84], copyright John Wiley&Sons.

In the depletion mode ($\frac{kT}{q} < \psi_s < 2\psi_b$), the inversion charge is negligible and the surface charge is approximately as the depletion charge. The surface charge can therefore be obtained from Eq.(A.3) by keeping the dominant depleted charge term and using the

condition in Eq.(A.4).

$$Q_s \approx Q_d = -\sqrt{2qN_A\varepsilon_{Si}\psi_s} \tag{A.6}$$

In the subthreshold mode, the inversion charge cannot be neglected and can be written by keeping the inversion and depletion terms in Eq.(A.3) as:

$$Q_s = -\sqrt{2kT\varepsilon_{Si}N_A}\left(\frac{q\psi_s}{kT} + \frac{n_i^2}{N_A^2}\exp\frac{q\psi_s}{kT}\right)^{\frac{1}{2}} \tag{A.7}$$

Using Taylor series, the surface charge could be simplified into:

$$Q_s = -\sqrt{2kT\varepsilon_{Si}N_A}\left[\left(\frac{q\psi_s}{kT}\right)^{\frac{1}{2}} + \frac{1}{2}\left(\frac{q\psi_s}{kT}\right)^{-\frac{1}{2}}\frac{n_i^2}{N_A^2}\exp\frac{q\psi_s}{kT}\right] \tag{A.8}$$

As the first term in the square bracket is the depletion charge as in Eq.(A.3), the inversion charge can there be expressed as:

$$Q_i = Q_s - Q_d = -\sqrt{\frac{q\varepsilon_{Si}N_A}{2\psi_s}}\left(\frac{kT}{q}\right)\left(\frac{n_i}{N_A}\right)^2\exp\frac{q\psi_s}{kT} \tag{A.9}$$

Appendix B

Double-Gate and Surround-Gate MOSFETs

To control short channel effects, some advanced MOSFET structures have been proposed, such as Silicon-on-Insulator (SOI) [134], Silicon-on-Nothing (SON) [135], Double-gate (DG) [136], Gate-all-around (GAA)/Surround-gate (SRG) [137] and stacked / Multi-bridge [138][139]. Compared with the structure of a bulk MOSFET, these advanced structures have better gate control of the channel and thus short channel effects are suppressed and the current drive is increased [140]. This also releases the requirement for a high channel doping and thus leads to a higher carrier mobility due to the reduction of carrier scatterings in the low-doped channel. In our work, however, short channel effect suppression is not a big concern but we still need to take account of the improved channel control.

Among the above multi-gate transistors, DG and SRG transistors are the two most common types and their structures are shown in the schematic views in Fig. B.1(a) and (b), respectively. For the DG structure, there are two gates on the top and on the bottom of the channel. Here, the two gates are chosen set to be symmetrical with the same gate insulators for simplicity. For the SRG structure, the gate and gate insulator surround the Si channel. The conduction mechanism of DG transistors can be clarified by the band diagram in Fig. B.2, which is for an n-channel DG MOSFET with positive bias applied to both gates. As the gate bias increases, depletion and inversion regions are formed at both surfaces. Depending on the channel thickness, these transistors are distinguished as partially depleted (PD) or fully depleted (FD).

For partially depleted transistors, the channel thickness is larger than the sum of the

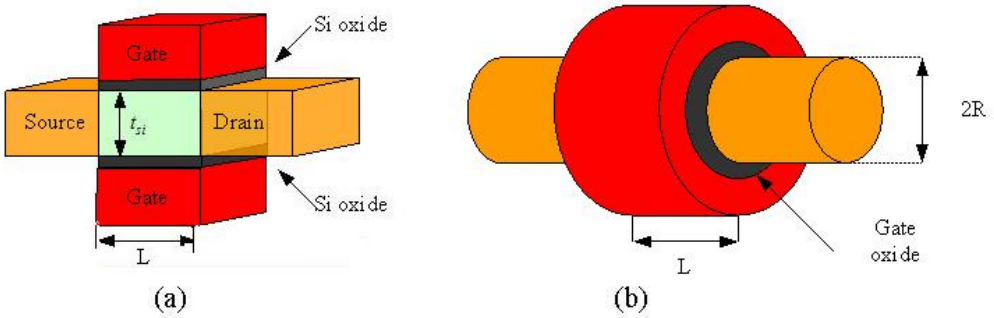


FIGURE B.1: Schematic diagrams of (a) a double-gate MOSFET and (b) a surround-gate MOSFET.

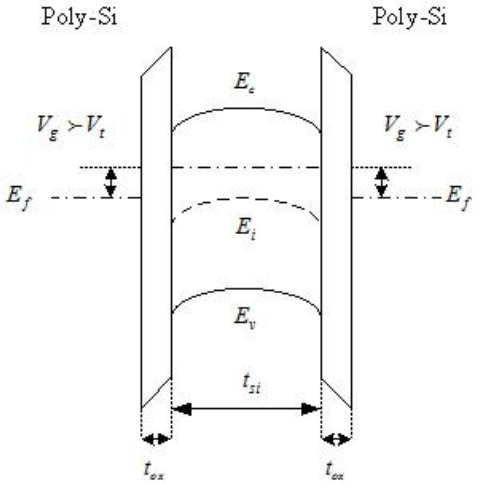


FIGURE B.2: The schematic diagram of a DG MOSFET under positive bias in volume inversion mode.

two depletion regions formed by the two gate biases and there is an undepleted region between two independent regions. The DG transistor operates as a transistor with two independent channels and thus the ON current is twice that of a single-gate transistor. A continuous analytical drain-current model for partially depleted DG SOI MOSFETs with a lightly doped channel was proposed by Taur *et al* [141]. In Taur's model, the drain-current of a DG transistor can be obtained by solving Poisson's equation without the charge sheet approximation and the drain current can be approximated as:

$$I_{ds} = 2\mu_{eff} C_{ox} \frac{W}{L} \left(V_g - V_t - \frac{1}{2} V_{ds} \right) V_{ds} \tag{B.1}$$

For a SRG MOSFET, the drain current can be approximated by [142]:

$$I_{ds} = 2\mu_{eff}\frac{\pi R}{L}C_{ox}\left(V_g - V_t - \frac{1}{2}V_{ds}\right)V_{ds} \tag{B.2}$$

For a fully depleted transistor, the channel thickness is equal to or less than the sum of the two depletion regions and the whole channel is depleted. In the central region of the channel, the depletion can be considered to be formed by the overlap of two depletion regions. Thus, this gate coupling reduces the bias, that is required to form the depletion regions, compared with the partially depleted case. This in turn reduces the threshold voltage of the transistor and thus the drain current of a fully depleted transistor is larger than twice that of a single-gate transistor under the same gate bias. This explanation also applies to SRG MOSFETs. It should be noted that Eq.(B.1) and Eq.(B.2) are still valid if the expressions for V_t take the gate coupling into consideration [141][142].

When the channel is further thinned (e.g. 50 nm in simulation [143]) and the two inversion layers merge into one inversion layer, the transistor operates in *volume inversion* [143]. Balestra *et al* [144] studied volume inversion by both simulation and experiment and found that transistors in volume inversion have excellent values of subthreshold slope, drain current and transconductance. As the double gates confine more carriers to flow in the central region of the channel, the carrier mobility is remarkably increased due to less interface scattering [143]. Therefore, the ON current of a double-gate transistor is therefore higher than twice that of a single-gate transistor at the same gate bias.

Appendix C

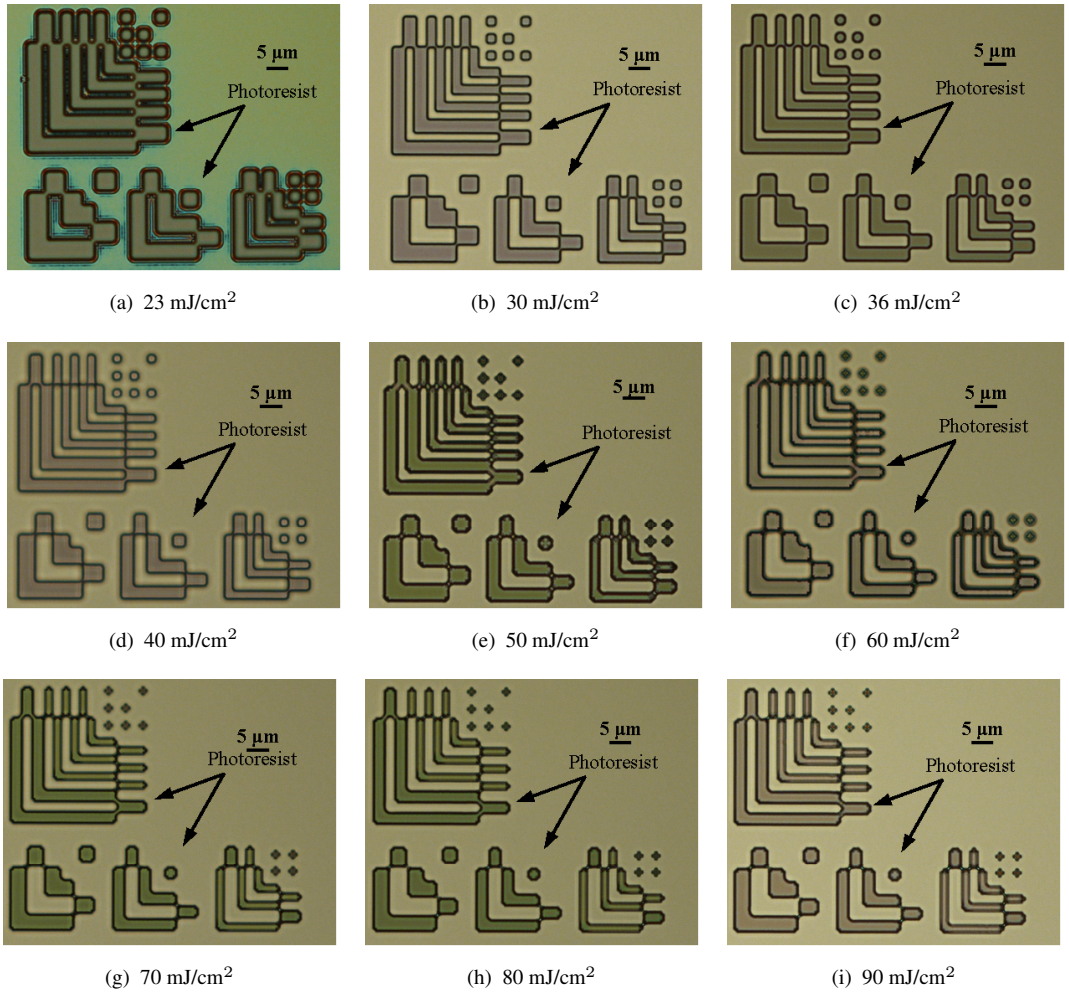
Results of Photolithography Development

C.1 Photolithography with S1813

The exposure of S1813 was investigated and calibrated using optical Nomarski microscope. Fig. C.1 shows optical Nomarski micrographs of developed photoresist features exposed at various doses ranging from 23 mJ/cm^2 to 90 mJ/cm^2. In Fig. C.1(a), photoresist given a 23 mJ/cm^2 exposure is seen as a brown colour with quite blurred edges and the background is a non-uniform colour. This non-uniform colour indicates that the photoresist was under-exposured and hence was not fully removed from the exposed area. As exposure dose is increased to 30 mJ/cm^2 in Fig. C.1(b), features become very sharp and the background is a uniform colour. As the dose increases, the smallest features (2 μm $\times$ 2 μm) change from a square to a round shape. This indicates that photoresist exposures at doses above 50 mJ/cm^2 is over exposed. Fig. C.2 shows measured photoresist ribbon widths as a function of exposure dose. These results show that the optimum dose is around 40 mJ/cm2 and 36 mJ/cm2 was used in this work to give a good uniformity over whole wafer.

C.2 Photolithography with AZ2070

The exposure of AZ2070 was similarly investigated and calibrated using optical Nomarski microscope after development. Fig. C.3 shows optical Nomarski micrographs



(a) 23 mJ/cm^2 (b) 30 mJ/cm^2 (c) 36 mJ/cm^2

(d) 40 mJ/cm^2 (e) 50 mJ/cm^2 (f) 60 mJ/cm^2

(g) 70 mJ/cm^2 (h) 80 mJ/cm^2 (i) 90 mJ/cm^2

FIGURE C.1: Nomarski micrographs of developed S1813 photoresist features using different exposure doses.

of developed photoresist features exposed in various doses ranging from 45 mJ/cm^2 to 115 mJ/cm^2. In comparison with the S1813 results in Fig. C.1, the features are less clearly defined. This is because the negative resist, AZ2070, has a higher thickness of about 4 μm (by SEM) than S1813, which is in thickness of about 1 μm. It might also be attributed to the negative sidewall slope and window features for negative photoresis. Fig. C.4 shows measured photoresist window widths as a function of exposure dose. As this photoresist is used for metal lift-off, the tolerance on feature dimensions is not critical and thus an exposure dose of 75 mJ/cm2 was used in this work.

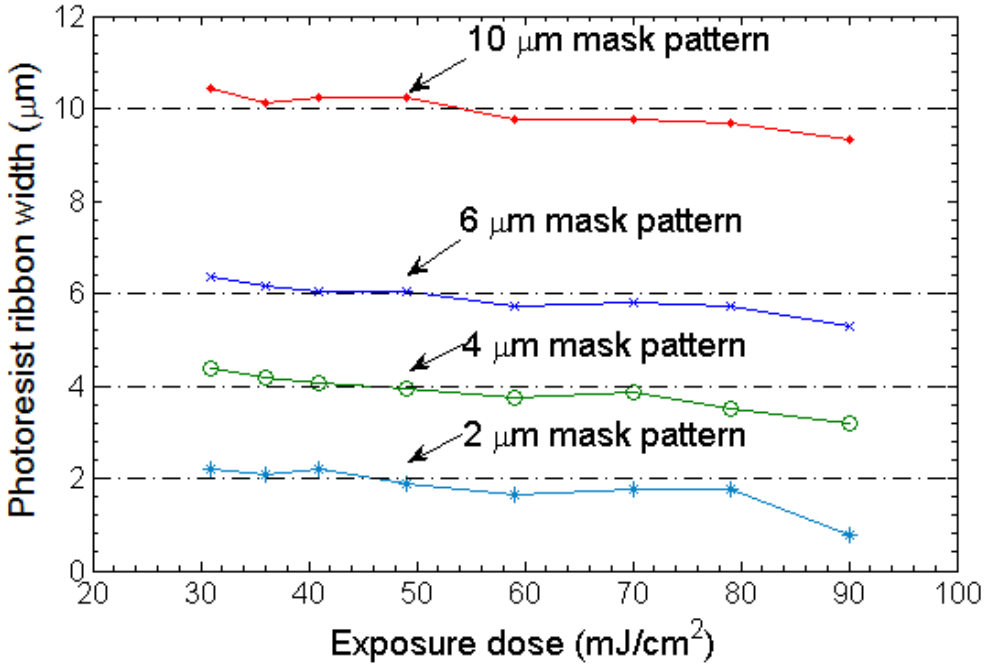


FIGURE C.2: Measured photoresist (S1813) ribbon width as a function of exposure dose for features with designed widths of 2 μm, 4 μm, 6 μm and 10 μm.

C.3 Photolithography with SU8-2

The exposure of SU8-2 was investigated and calibrated using optical Nomarski microscope. Fig. C.5 shows optical Nomarski micrographs of developed SU8-2 features exposed at various doses ranging from 42 mJ/cm^2 to 102 mJ/cm^2. These features are again less clearly defined than those in Fig. C.1 for S1813. This is also explained by the higher SU8-2 thickness of about 1.8 μm and the characteristics of negative photoresist.

Fig. C.6 shows measured photoresist ribbon window width as a function of exposure dose. As SU8-2 is used to define sensing windows, window sizes need to be very well defined to assure no direct conducting path is formed between Source and Drain region in the liquid, which can shorten nanowires. The exposure dose of 80 mJ/cm^2 was used in the device process.

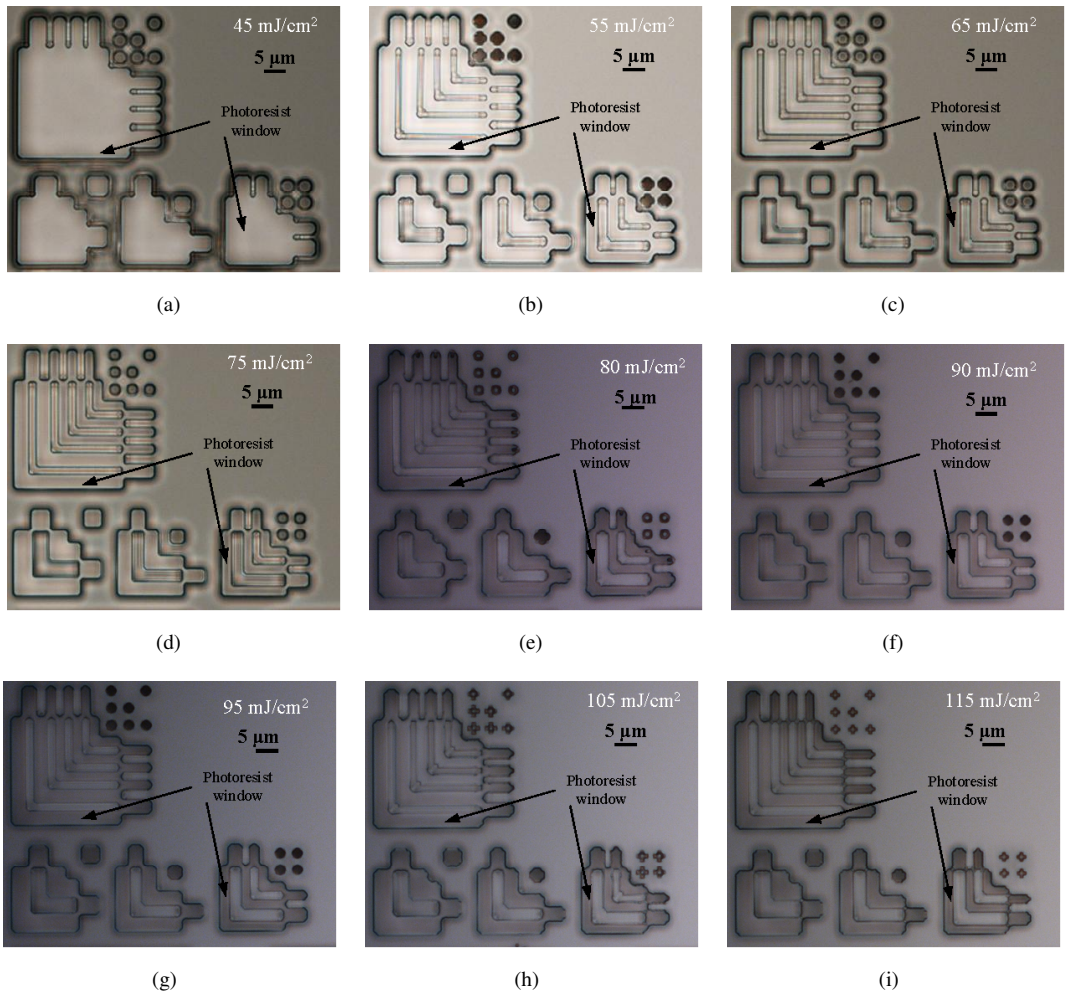


FIGURE C.3: Nomarski micrographs of developed AZ2070 photoresist features using different exposure doses.

C.4 Alignment

Fig. C.7(a) shows an optical micrograph of alignment mark on an arbitrary chip near the centre of a 4-inch wafer. Compared with the mask layout in Fig. 6.5(a), an excellent alignment has been achieved that the main and fine alignment marks are all well matched. The misalignment can be read from the misalignment measurement features from Fig. C.7(b) and found to be about 200 nm in the x-direction and $<$100 nm in the y-dimensions. This is an excellent alignment compared with the specified 0.5 μm minimum alignment tolerance in the technical manualf for the EVG 620T/620TB aligner. Typical misalignment for a chip is about 0.5 μm and thus the designed aligment features fully satisfy the alignment requirement in this work.

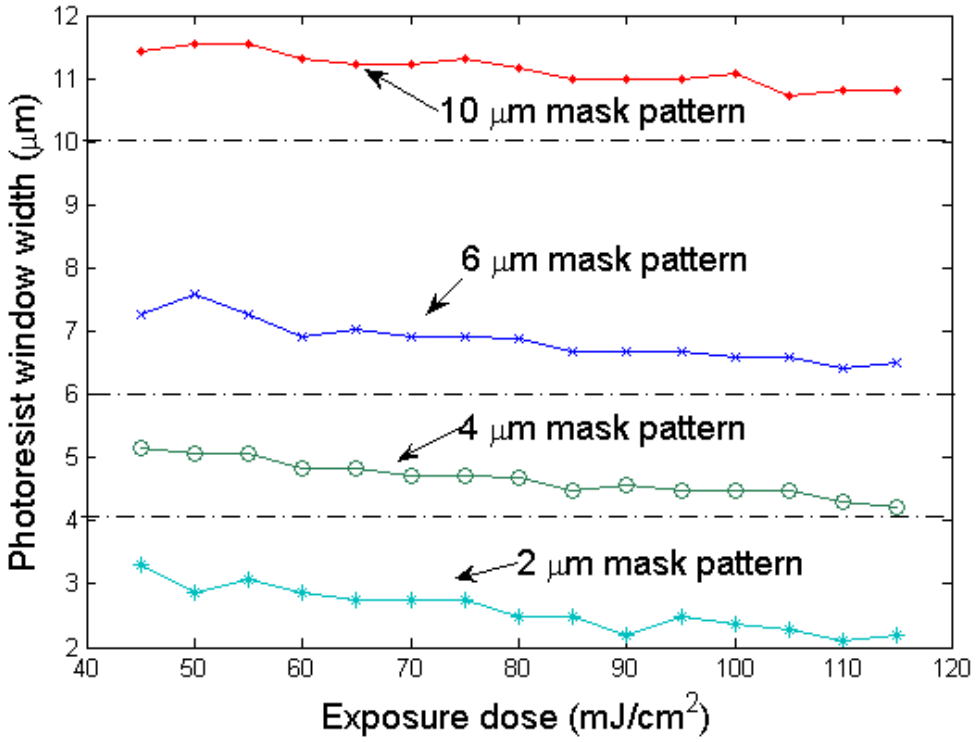


FIGURE C.4: Measured photoresist ribbon widths for AZ2070 as a function of exposure dose with mask for features with designed widths of 2 μm, 4 μm, 6 μm and 10 μm.

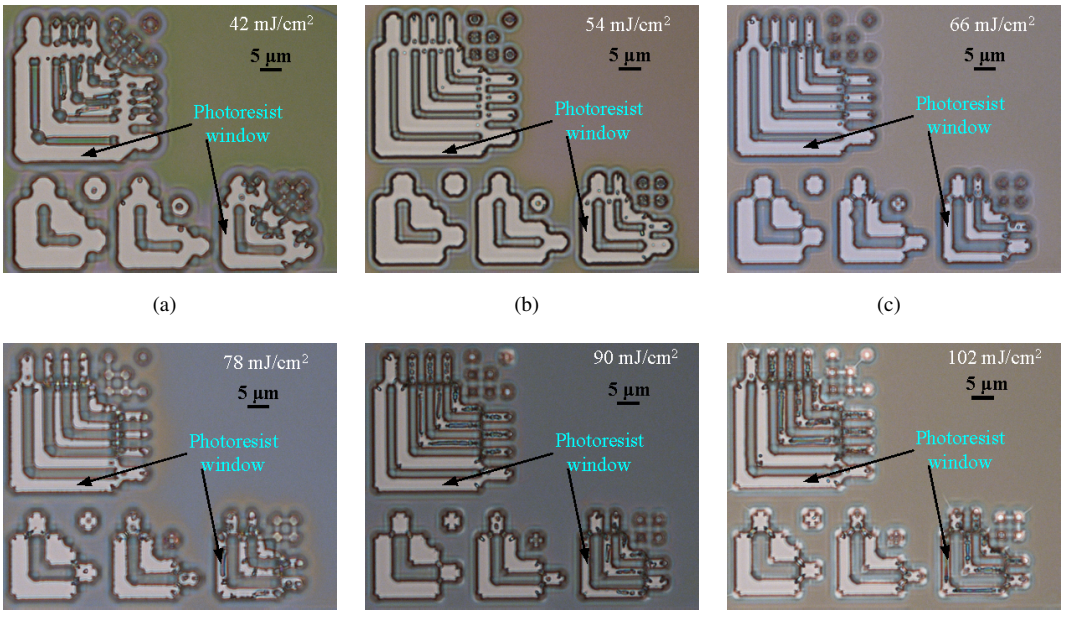


FIGURE C.5: Nomarski micrographs of developed SU8-2 photoresist features using different exposure doses.

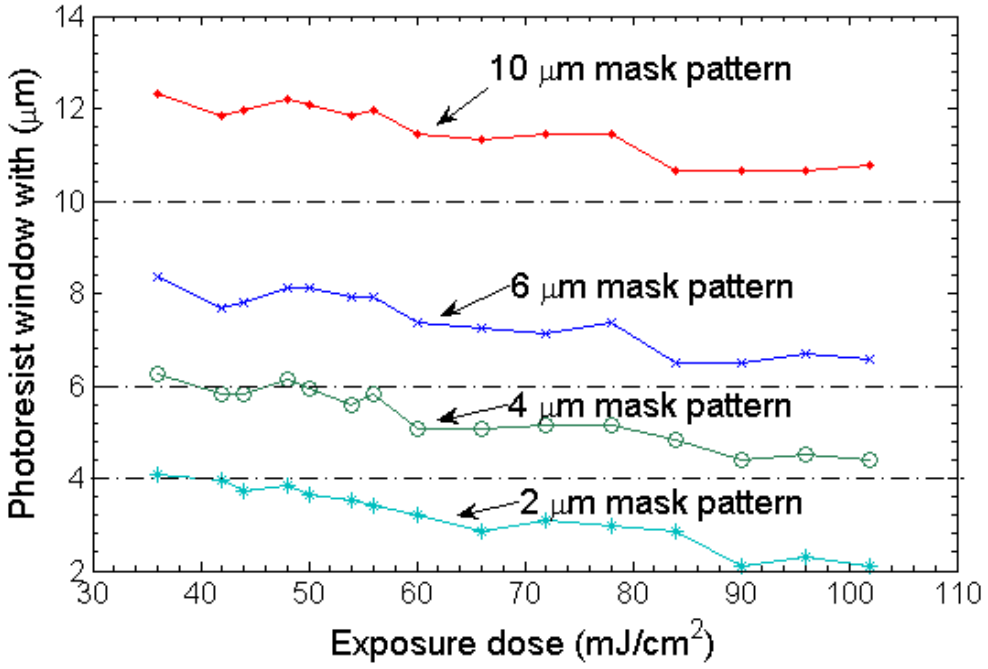
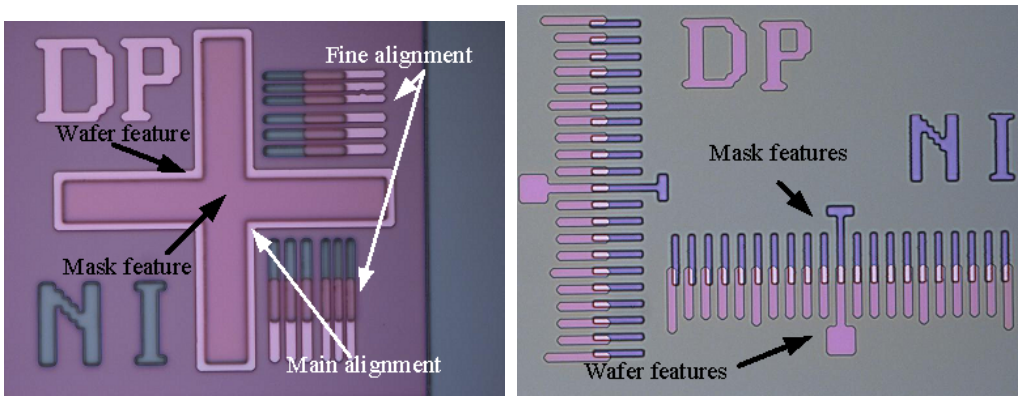


FIGURE C.6: Measured photoresist ribbon widths for SU8 as a function of exposure doses for features with designed widths of 2 μm, 4 μm, 6 μm and 10 μm.



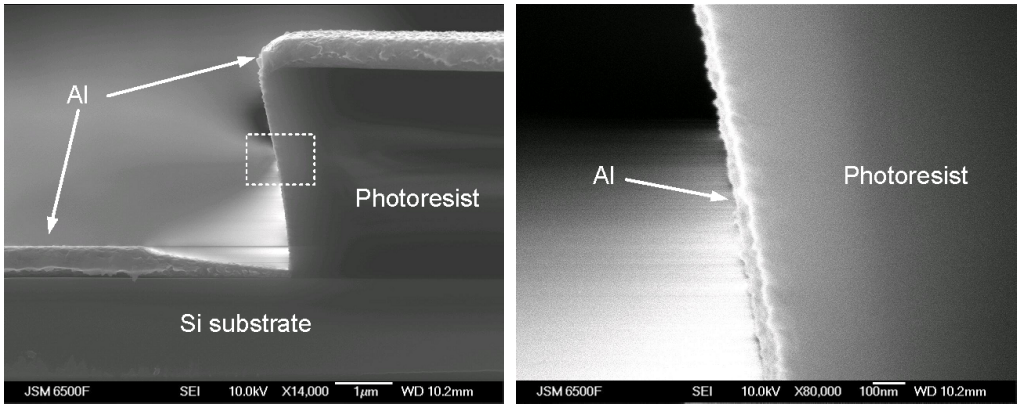
(a) (b)

FIGURE C.7: Optical Nomarski micrographs of (a) alignment marks and (b) a misalignment measurement feature. The pictures were taken at near the wafer centre after an alignment and a photoresist development.

Appendix D

Results of Metallisation

Fig. D.1(a) shows cross-section SEM micrograph of samples before the aluminium lift-off process. Photoresist was patterned on the Si substrate and measured to be 3.8 μm with an undercut slope (photoresist thicker at the top than the bottom). The thickness of the Al layer was measured to be 530 nm. The thickness of the Al on the sidewall was measured to be 20 nm (Fig. D.1(b)), which is much thinner than the thickness on top of the photoresist. This reduction of Al thickness is due to the negative photoresist profile and is important because it aids the lift-off of the Al film.

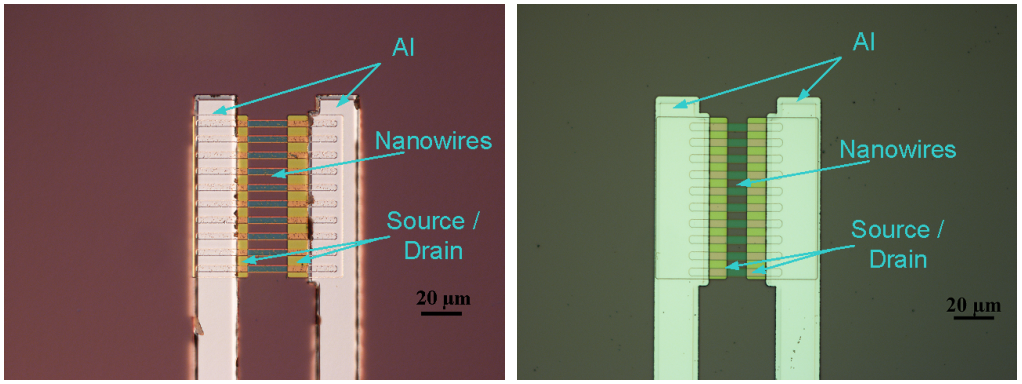


(a) (b)

FIGURE D.1: Cross-section SEM micrographs of a sample before the Al lift-off process (a) at a low magnification and (b) at a high magnification.

Fig. D.2(a) shows a DIC micrograph of a typical biosensor device after manual lift-off. The Al tracks are about 22 μm wide, which is in reasonable agreement with the as-drawn width of 20 μm. In addition, nanowires can also be clearly between the Source

and Drain, indicating that the nanowires are well preserved in the lift-off process. The automatic lift-off process gives similar results as shown in Fig. D.2(b). The Al tracks were measured to be 22 μm. The automatic lift-off process has the advantage of fewer blemishes, as can be seen by comparing Fig. D.2(a) and (b).



(a) (b)

FIGURE D.2: Nomarski micrographs of biosensor samples after Al lift-off by (a) a manual method in a beaker and (b) an antomatic methods in a lift-off machine.

Appendix E

Batch Listings

E.1 Batch Listing for Fluorine Effect on Lateral Crystallisation

Wafer List

- Wafer #1 Control wafer without fluorine
- Wafer #3 wafer with a F implant, dose: 5×10^{14} cm^{-2}
- Wafer #4 wafer with a F implant, dose: 1×10^{15} cm^{-2}
- Wafer #5 wafer with a F implant, dose: 2.5×10^{15} cm^{-2}
- Wafer #6 wafer with a F implant, dose: 5×10^{15} cm^{-2}

Process List

1. RCA clean for all wafers
2. Load in O_2, 400 nm wet oxide at 1100°C for all
3. 100 nm α-Si deposition by LPCVD at 560°C for all
4. Fluorine implant
   - F implant: 5×10^{14} cm^{-2}, 35 keV for #3

- F implant: 1×10^{15} cm^{-2}, 35 keV for #4
- F implant: 2.5×10^{15} cm^{-2}, 35 keV for #5
- F implant: 5×10^{15} cm^{-2}, 35 keV for #6

5. 300 nm low temperature oxide deposition at 400°C all

6. Photolithography with stepper
7. Hardbake for wet etch
8. Oxide wet etch by rinsing in 20:1 buffered HF for all
9. Resist strip for all
10. Fuming nitric acid clean for all
11. Native oxide removal using 100:1 HF for 20 seconds
12. Ni seed deposition for all

E.2 Batch Listing for α-Si Ribbons on Different Substrates

Wafer List

- Wafer #1 100 nm LPCVD α-Si on 100 nm Si nitride (Si-on-Nitride)
- Wafers #2 100 nm LPCVD α-Si on 500 nm Si dioxide (Si-on-Air)
- Wafers #3 100 nm LPCVD α-Si on 500 nm Si dioxide (Si-on-Oxide)
- Wafers #4 100 nm LPCVD α-Si on 500 nm Si dioxide with a 2.5×10^{15} cm^{-2} F implant
- Wafer #5 100 nm PECVD α-Si on 500 nm Si dioxide

Process List

1. RCA cleaning for all (#1-5)
2. Buried layer formation
    - 100 nm Si nitride deposition by LPCVD for #1
    - 500 nm Si dioxide deposition by LPCVD for #2,3,4
    - 500 nm Si dioxide by thermal oxidation at 1050°C for #5
3. α-Si deposition
    - 100 nm α-Si deposition by LPCVD at 560°C for #1-4
    - 100 nm α-Si deposition by PECVD at 250 °C for #5
4. photolithography for all (#1-5)
    - Fuming nitric acid cleaning for 5 minutes, DI water for 5 minutes and blow dry
    - Anneal at 210°C overnight
    - Spin photoresist, S1813, 5000 rpm for 30 seconds
    - Soft-bake at 90°C for 1 minute
    - Exposure using EVG 620TB with mask *DP* for 8 seconds
    - Development in MIF 319 for 35 seconds
    - Hard-bake at 120°C for 20 minutes
5. α-Si dry etch using OIPT RIE 80 plus for all (#1-5)
   (SF_6 20 sccm, O_2 10 sccm, Pressure 15 mTorr, Power 20 W, etch for 180 sec.)
6. Photoresist removal
    - Fuming nitric acide cleaning for 5 minutes
    - Di wafer for 5 minutes
7. Dehydrogenation anneal at 430°C for 30 minutes for #5
8. SiO_2 removal using 7:1 buffered HF for 18 minutes for #2
9. Fluorine implantation of 2.5×10^{15} cm^{-2} at 35 keV for #4
10. photolithography for all (#1-5)

- Fuming nitric acid cleaning for 5 minutes, DI water for 5 minutes and blow dry
- Anneal at 210°C overnight
- Spin photoresist, S1813, 5000 rpm for 30 seconds
- Soft-bake at 95°C for 1 minute
- Exposure using EVG 620TB with mask *NI* for 8 seconds
- Development in MIF 319 for 35 seconds

11. Remove native oxide by rinsing in 20:1 buffered HF for 10 seconds and blow dry for all (#1-5)
12. E-gun evaporation of 20 nm nickel for all (#1-5)
13. Ni lift-off in acatone for 20 minutes all (#1-5)
14. Cleave into chips for annealing in nitrogen all (#1-5)

E.3 Batch Listing for Si Nanowire Biosensor

Wafer List

- Wafer #1 Oxidised nanowires with two P implants of 2×10^{13} cm^{-2}, etched by STS for 30 cycles
- Wafer #2 Unoxidised nanowires with two P implants of 2×10^{13} cm^{-2}, etched by STS for 30 cycles
- Wafer #3 Oxidised nanowires with two P implants of 1×10^{13} cm^{-2}, etched by STS for 32 cycles

Process List

1. Grow 700 nm thermal oxide by dry oxidation for all
2. Photolithography for all
    - Fuming nitric acid cleaning

- Anneal at 210°C overnight
- Spin photoresist, S1813, 5000 rpm for 30 seconds
- Soft-bake at 95°C for 1 minute
- Exposure using EVG 620TB with mask *NW*
- Development in MIF 319 for 35 seconds
- Hard-bake at 120°C for 20 minutes

3. Si dioxide step formation for all
   (Ar 32 sccm, CHF_3 18 sccm, 200 W, 30 mTorr 190s, + O_2 100 sccm, 100W, 100 mTorr, 20 sec)

4. Remove photoresist by fuming nitric acid for all

5. 100 nm α-Si deposition by LPCVD at 560°C for all

6. Photolithography for all

   - Fuming nitric acid cleaning
   - Anneal at 210°C overnight
   - Spin photoresist, S1813, 5000 rpm for 30 seconds
   - Soft-bake at 95°C for 1 minute
   - Exposure using EVG 620T with mask *DP*
   - Development in MIF 319 for 30 seconds
   - Hard-bake at 120°C for 20 minutes

7. α-Si nanowire formation
   (deposition 3 seconds, C_4F_8 80 sccm and etch for 2 seconds, SF_6 50 sccm, O_2 5 sccm, 13.56MHz Coil=350W, 380 kHz platen 11W, T=10°C)

   - Etch for 30 cycles for #1,2
   - Etch for 32 cycles for #3

8. Photoresist strip by fuming nitric acid for all

9. Phosphors implantation

   - Two phosphors implants: 2×10^{13} cm^{-2}, 10 keV, at $\pm$45°C for #1,2
   - Two phosphors implants: 1×10^{13} cm^{-2}, 10 keV, at $\pm$45°C for #3

10. α-Si crystallsiation and dopant activation anneal at 600°C for 24 hours for all
11. 10 nm thermal oxide growth at 900°C for #1,3
12. Photolithography for all
    - Fuming nitric acid cleaning
    - Anneal at 210°C overnight
    - Spin photoresist, AZ2070, 6000 rpm for 40 seconds
    - Soft-bake at 110°C for 1 minute
    - Exposure using EVG 620T using i-line (365 nm) filter with mask *DP* (75 mJ/cm^2)
    - Development in AZ 726 MIF developer for 75 seconds
    - Plasma descum using OIPT RIE 80 plus
      (pressure 50, forward power 100W, O_2 50 sccm for 1 minute at 20°C)
13. Remove native oxide by 20:1 buffered HF for 25 seconds for all
14. 500 nm Al evaporation at 0.5 nm/sec for all
15. Lift-off using OPTI Wet ST 30 for all
16. SU8-2 passivation layer formation for #3
    - Anneal at 210°C overnight
    - Spin photoresist, SU8-2, 2000 rpm for 30 seconds
    - Soft-bake at 65°C for 1 minute and then 95°C for 3 minutes
    - Exposure using EVG 620T using i-line (365 nm) filter with mask *SU* (80 mJ/cm^2)
    - Development in SU8 developer for 45 seconds
    - Rinse in IPA and blow dry

Appendix F

The Detailed Information of the Designed Masks and Layouts

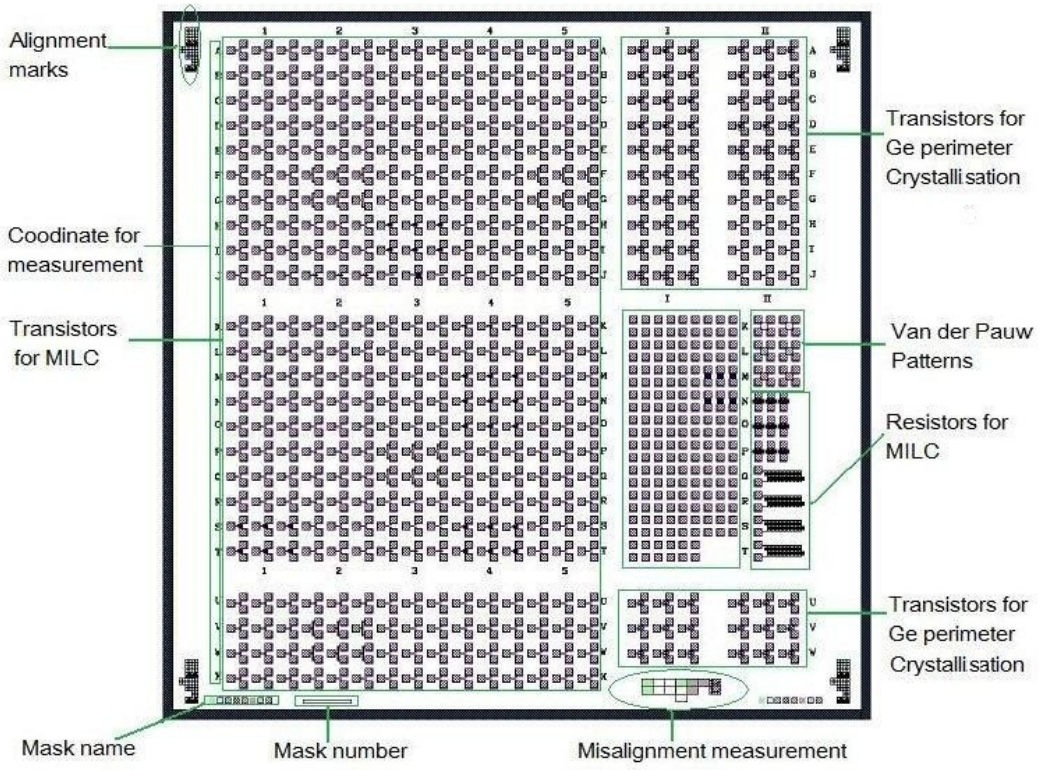
F.1 List of Designed Marks

Below is a list of the masks used in the process of Si nanowire Biosensors and crystallisation study.

- **NW** Nanowire trench definition (DF).
- **DP** n+ *in situ* doped silicon definition for source and drain (LF).
- **NI** Ni lift-off definition/Ge pattern definition (DF).
- **MT** Metal definition (LF).
- **SU** Electrode window/biosensing window definition (LF).

Note: LF=light field mask, DF=dark field mask

F.2 The Designed Chips in Mask Layouts


Alignment marks
Coodinate for measurement
Transistors for MILC
Transistors for Ge perimeter Crystallisation
Van der Pauw Patterns
Resistors for MILC
Transistors for Ge perimeter Crystallisation
Mask name
Mask number
Misalignment measurement
(a)
SEM Cells for Ge perimeter Crystallisation
100 um SIMS bars
SEM Cells for Ge perimeter Crystallisation
SEM bars for MILC
200 um SIMS bars
SEM bars and cells for MILC
SEM bars for Ge perimeter Crystallisation
Biosensor electrodes
Biosensor cells
500 um SIMS bars
Biosensor electrodes
SEM bars for TFTs
NW
DP
AA
NI
MT
SU
Mask AA is not used.
(b)

F.3 The Detailed Floor Plans on the Two Cells

F.3.1 Chip One (Transistors)

	1	2	3	4	5		I		II		
A	NW01_s	NW21_s	NW71_s	SD01_s	SD21_s	A	GN01_s		GN011_s	A	
B	NW02_s	NW22_s	NW030_s	SD02_s	SD22_s	B	GN02_s		GN012_s	B	
C	NW03_s	NW23_s	NW031_s	SD03_s	SD23_s	C	GN03_s		GN013_s	C	
D	NW04_s	NW24_s	SD71_s	SD04_s	SD24_s	D	GN11_s		GS01_s	D	
E	NW05_s	NW25_s	SD031_s	SD05_s	SD25_s	E	GN12_s		GS02_s	E	
F	NW11_s	NW41_s	NW012_i	SD11_s	NS31_s	F	GN13_s		GS03_s	F	
G	NW12_s	NW42_s	NW013_i	SD12_s	SD41_s	G	GN31_s		GN01_i	G	
H	NW13_s	NW51_s	NW015_i	SD13_s	SD42_s	H	GN32_s		GN02_i	H	
I	NW14_s	NW52_s	NW91_i	SD14_s	SD51_s	I	GN33_s		GS01_i	I	
J	NW15_s	NW61_s	NW93_i	SD15_s	SD52_s	J	GN11_i		GS02_s	J	
	1	2	3	4	5		GN12_i		GS03_i		VDP_h
K	NWX1_s	NW01_i	NW21_i	NW71_i	SD01_i	K	RN01	RN11	RN23	K	VDP_l
L	NWX2_s	NW02_i	NW22_i	NW72_i	SD02_i	L	RN02	RN13	RN24	L	VDP_g
M	NWX3_s	NW03_i	NW23_i	NW73_i	SD03_i	M	RN03	RN14	RN31	M	RS51
N	SDX01_s	NW04_i	NW24_i	NW012_i	SD04_i	N	RN04	RN21	RN32	N	RS52
O	SDX02_s	NW05_i	NW25_i	NW013_i	SD05_i	O	RN05	RN22	RN031	O	RS53
P	RT	NW11_i	NW41_i	NW015_i	SD11_i	P	RS01	RS11	RS23	P	RN51
Q	GLN11_s	NW12_i	NW42_i	NW81_i	SD12_i	Q	RS02	RS13	RS31	Q	RN51
R	GLN12_s	NW13_i	NW51_i	NW82_i	SD13_i	R	RS03	RS15	RS41	R	RN52
S	GLN15_s	NW14_i	NW52_i	NW83_i	SD14_i	S	RS04	RS21	RS031	S	RN52
T	GLN2x_s	NW15_i	NW61_i	NW85_i	SD15_i	T	RS05	RS22		T	
	1	2	3	4	5		RF52_s	RF93_i	RF11_s		
U	SD21_i	SD25_i	SD51_i	SD71_i	SDX1_i	U	RF71_i	RF72_i	RF73_i		
V	SD22_i	NS31_i	SD52_i	NWX1_i	SDX2_i	V	RF81_i	RF82_i	RF83_i		
W	SD23_i	SD41_i	SD61_i	NWX2_i	GLS11_s	W					
X	SD24_i	SD42_i	SD62_i	NWX3_i	GLS12_s	X					

F.3.2 Chip Two (Biosensors and SEM bars)

SEM_Ge1	SEM_Ge2	SEM_Ge3	H L	100 μm SIMS bar h 100 μm SIMS bar l	H L	SEM_Ge4	SEM_Ge5	SEM_Ni
A	B	C				D	E	F
				SEM bar Ni_hml				
I(H)				SEM bar Ni h				I(H)
II				SEM bar Ni m				II
III(L)				SEM bar Ni l				III(L)
A				SEM Cell bar Ni h (200 μm SIMS bar)				A
B				SEM Cell bar Ni m				B
C				SEM Cell bar Ni l (200 μm SIMS bar)				C
1				SEM Cell bar Ge h				1
2				SEM Cell bar Ge m				2
3				SEM Cell bar Ge l				3
			H	500 μm SIMS bar h	H			
BSO10_100	BSM10_100	BSF10_100	BSO15_100	BSM15_100	BSF15_100	BSO20_100	BSM20_100	BSF20_100
BSO10_50	BSM10_50	BSF10_50	BSO15_50	BSM15_50	BSF15_50	BSO20_50	BSM20_50	BSF20_50
BSO10_20	BSM10_20	BSF10_20	BSO15_20	BSM15_20	BSF15_20	BSO20_20	BSM20_20	BSF20_20
			L	500 μm SIMS bar l	L			
				SEM nanowire TFT bar for Ni				
				SEM conventional TFT bar for Ni				

'h' means n+ type doped α-Si, 'm' means p type α-Si with two pads of n+ type α-Si, and 'l' means p type doped α-Si.

F.3.3 The list of nanowire TFTs by MILC

Channel	NWs		Ni-OS	Ni-M	Ni-FO	No-Ni	Ni-BS
10 μm	1×2		• NW01	• NW02	• NW03	• NW04	• NW05
4 μm	1×2		• NW11	• NW12	• NW13	• NW14	• NW15
20 μm	1×2		• NW21	• NW22	• NW23	• NW24	• NW25
200 μm	1×2		• NS31_1	• NS31_2			
10 μm	2×2		• NW41	• NW42			
10 μm	4×2		• NW51	• NW52			
2 μm	1×2		• NW61				
10 μm	5×2		• NW81_i	• NW82_i	• NW83_i		• NW85_i
4 μm	5×2		• NW71_i	• NW72_i	• NW73_i		
2 μm	5×2		• NW91_i		• NW93_i		
10 μm	1×2		NW71_s1	funnel 4 μm width			
10 μm	1×2		NW71_s2	funnel 3 μm width			
10 μm	1×2		NW71_s3	funnel 2 μm width			
10 μm	1×2		NW012_i	2 μm gap			
10 μm	1×2		NW013_i	3 μm gap			
10 μm	1×2		NW015_i	5 μm gap			
10 μm	1×2		NW030_s	Normal trench			
10 μm	1×2		NW031_s	Ni 4 μm away from VIA			
10 μm	1×2		NWX1	NWX2	NWX3	with p layers	
4 μm	2×2		GLN11_s	GLN12_s		GLN14_s3	GLN15_s12
2 μm	2×2		GLN2x_s1			GLN2x_s2	GLN2x_s3

OS= one side, M= middle, No= without, FO= 10 μm from the junction, BS= both side.
The cell without 'i' or 's' in name means both patterns with/without a high temperature

annealing, whilst the cell with 'i' and 's' in name means pattern with and without a high temperature annealing, respectively. GLN= TFTs for Ge induced lateral crystallization

F.3.4 The list of conventional TFTs by MILC

Channel	Width		Ni-OS	Ni-M	Ni-FO	No-Ni	Ni-BS
10 μm	10 μm		• SD01	• SD02	• SD03	• SD04	• SD05
4 μm	10 μm		• SD11	• SD12	• SD13	• SD14	• SD15
20 μm	10 μm		• SD21	• SD22	• SD23	• SD24	• SD25
200 μm	10 μm			• NS31_3			
10 μm	2 μm		• SD41	SD42			
10 μm	4 μm		• SD51	• SD52			
10 μm	8 μm		• SD61	• SD62			
2 μm	2 μm		• SD71				
10 μm	10 μm		SD012_i	2 μm gap			
10 μm	10 μm		SD013_i	3 μm gap			
10 μm	10 μm		SD015_i	5 μm gap			
10 μm	10 μm		SD031_s	Ni 4 μm away from VIA			
10 μm	10 μm		SDX01	SDX02	with short p layers		
4 μm	10 μm		GLS11_s	GLS12_s	Ge-ILC TFTs		

OS= one side, M= middle, No= without, FO= 10 μm from the junction, BS= both side. The cell without 'i' or 's' in name means both patterns with/without a high temperature annealing, whilst the cell with 'i' and 's' in name means pattern with and without a high temperature annealing, respectively.

F.3.5 The list of resistors by MILC

Channel	Width	NWs		Ni-OS	Ni-M	Ni-FO	No-Ni	Ni-BS
10 μm		1×2		• RN01	• RN02	• RN03	• RN04	• RN05
2 μm		1×2		• RN11		• RN13	• RN14	
20 μm		1×2		• RN21	• RN22	• RN23	• RN24	
10 μm		8×2		• RN31	• RN32	• RN33		
10 μm		8×2×10		• RN51	• RN52			
10 μm	1×2			RN031	Ni 4 μm away from VIA			
10 μm	10 μm			• RS01	• RS02	• RS03	• RS04	• RS05
5 μm	10 μm			• RS11		• RS13		• RS14
20 μm	10 μm			• RS21	• RS22	• RS23		
10 μm	4 μm			• RS31				
10 μm	2 μm			• RS41				
10 μm	10 μm	×10		• RS51	• RS52	• RS53	for p-type	
10 μm	10 μm			RS031	Ni 4 μm away from VIA			
5+10 μm		1×2		RT_1				
5+10 μm		8×2		RT_1				
5+10 μm	10 μm			RT_1				

OS= one side, M= middle, No= without, FO= 10 μm from the junction, BS= both side. The width column is applied to conventional resistors, whilst the NWs (nanowire number) column is applied to nanowire resistors.

F.3.6 The nanowire biosensors by MILC

NWs	Channel length	Ni-OS	Ni-M	Ni-FO
×100	10 μm	• BSO10_100	• BSM10_100	• BSF10_100
×100	15 μm	• BSO15_100	• BSM15_100	• BSF15_100
×100	20 μm	• BSO20_100	• BSM20_100	• BSF20_100
×50	10 μm	• BSO10_50	• BSM10_50	• BSF10_50
×50	15 μm	• BSO15_50	• BSM15_50	• BSF15_50
×50	20 μm	• BSO20_50	• BSM20_50	• BSF20_50
×20	10 μm	• BSO10_20	• BSM10_20	• BSF10_20
×20	15 μm	• BSO15_20	• BSM15_20	• BSF15_20
×20	20 μm	• BSO20_20	• BSM20_20	• BSF20_20

OS= one side, M= middle, NFO= 10 μm from the junction.

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