Analysis of Si:Ge Heterojunction Integrated Injection Logic (I^2L) Structures Using a Stored Charge Model

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***Abstract*— A quasi-two-dimensional stored charge model is developed as an aid to the optimization of SiGe integrated injection logic (I^2L) circuits. The model is structure-based and partitions the stored charge between the different regions of the I^2L gate. Both the NpN switching transistor and the PNp load transistor are correctly modeled and the effects of series resistances on the gate operation are taken into account. The model is applied to surface-fed and substrate-fed variants of SiGe I^2L and the Ge and doping concentrations varied to determine the important tradeoffs in the gate design. At low injector currents, the substrate-fed variant is found to be faster because of lower values of critical depletion capacitances. At high injector currents, the performance of both variants is limited by series resistances, particularly in the NpN emitter layer. The inclusion of 16% Ge in the substrate-fed I^2L gate leads to a decrease in the dominant stored charge by a factor of more than ten, which suggests that gate delays well below 100 ps should be achievable in SiGe I^2L even at a geometry of 3 μm. The model is applied to a realistic, self-aligned structure and a delay of 34 ps is predicted. It is expected that this performance can be improved with a fully optimized, scaled structure.**

NOMENCLATURE

$N_{\rm SUB}$	N-type Si doping concentration in the substrate (used exclusively in C-I^2L).
$N_{\rm SE}$	N-type Si doping concentration in the switch emitter (used exclusively in C-I^2L).
$N_{\rm IB}$	N-type Si doping concentration in the injector base (used exclusively in C-I^2L).
$N_{\rm IE}$	P-type Si doping concentration in the injector emitter (used in both C-I^2L and SF-I^2L).
$N_{\rm ICSB}$	p-type SiGe doping concentration in the injector collector/switch base (used in both C-I^2L and SF-I^2L).
$N_{\rm SC}$	N-type Si doping concentration in the switch collector (used in both C-I^2L and SF-I^2L).
$N_{\rm IBSE}$	N-type Si doping concentration in the injector base/switch emitter (used exclusively in SF-I^2L).
$W_{\rm SE}$	Width of the switch emitter (used exclusively in C-I^2L).
$W_{\rm IB}$	Width of the injector base (used exclusively in C-I^2L).
$W_{\rm ICSB}$	Width of the injector collector/switch base (used in both C-I^2L and SF-I^2L).
$W_{\rm SC}$	Width of the switch collector (used in both C-I^2L and SF-I^2L).
$W_{\rm IBSE}$	Width of the injector base/switch emitter (used exclusively in SF-I^2L).
d	Depth of the intrinsic structures (into the page).
$d_{\rm br}$	Depth of the extrinsic base rails (into the page).
β_{uN}	Upward current gain of the N-p-N switch transistor.
β_{uP}	Upward current gain of the P-N-p injector transistor.
I_{SN}	N-p-N (switch) Gummel-Poon forward transport coefficient.
I_{SN}	P-N-p (injector) Gummel-Poon forward transport coefficient.
α_{FN}	Forward common base current gain of switch.
α_{FP}	Forward common base current gain of injector.
α_{RN}	Reverse common base current gain of switch.
α_{RP}	Reverse common base current gain of injector.

Substrate-Fed I^2L *Parameters*

l_1	Length of injector base/switch emitter contact.
l_2	Spacing between injector base/switch emitter contact and edge of switch base/injector collector implantion.
l_3	Length of switch base/injector collector implantation.
l_4	Spacing between edge of switch base/injector collector implantation and switch collector contact.
l_5	Length of switch collector contact.
l_6	Spacing between switch collector contact and edge of switch base/injector collector implantation.
l_7	Length of switch base/injector collector contact.
l_C	Length of switch collector $(=l_4+l_5+l_6)$.
l_A	Length of active area $(=l_3+l_C+l_7)$.
l_T	Length of total area $(=l_1+l_2+l_A)$.
$\Delta Q_{\rm eS}$	Electron stored charge in the substrate. (injector emitter).

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ΔQ_{hB} Hole stored charge in the injector base/switch emitter.
ΔQ_{eB} Electron stored charge in the switch base/injector collector.
ΔQ_{hC} Hole stored charge in the switch collector.
$\Delta Q_{h\mathrm{ext}}$ Hole stored charge in the switch collector injected from the extrinsic base rails.
$\Delta Q_{e\mathrm{ext}}$ Electron stored charge in the extrinsic base rails.
ΔQ_{DE} Switch emitter/base (injector base/collector) depletion charge.
ΔQ_{DC} Switch collector/base depletion charge.
ΔQ_{DCS} Switch collector/base sidewall depletion. charge

Conventional (Surface-Fed) I^2L *Parameters*

x_1 Length of switch emitter contact and isolation to edge of switch base/injector collector implantion.
x_2 Length of switch base/injector collector implantion.
x_3 Length of injector base region.
x_4 Length of isolation implantation between injector base and switch collector.
x_5 Length of switch collector region.
x_6 Length of switch base/injector collector implantation.
x_C Length of switch base/injector collector region $(=x_3+x_4+x_5)$.
x_A Length of active area $(=x_2+x_C+x_5)$.
x_T Length of total area $(=x_1+x_A)$.

ΔQ_{hS} Hole stored charge in the substrate.
ΔQ_{hN} Hole stored charge in the switch emitter.
ΔQ_{eB} Electron stored charge in the switch base/injector collector.
ΔQ_{hB} Hole stored charge in the injector base.
ΔQ_{hC} Hole stored charge in the switch collector.
$\Delta Q_{\mathrm{hCext}}$ Hole stored charge in the switch collector injected from the extrinsic base rails.
$\Delta Q_{\mathrm{hBext}}$ Hole stored charge in the injector base injected from the extrinsic base rails.
$\Delta Q_{e\,\mathrm{ext}}$ Electron stored charge in the extrinsic base rails.
ΔQ_{DE} Switch emitter/base depletion charge.
ΔQ_{DC} Switch collector/base depletion charge.
ΔQ_{DI} Injector collector/base depletion charge.
ΔQ_{DCSI} Injector collector/base sidewall depletion charge.
ΔQ_{DCSS} Switch collector/base sidewall depletion charge.

I. Introduction

HIGH-performance bipolar logic circuits are usually realized using emitter coupled logic (ECL) but that technology features relatively low packing density and high power dissipation. Integrated injection logic or I^2L [1], [2] is a low power bipolar technology suitable for VLSI which traditionally has suffered from a relatively poor dynamic performance. The minimum gate delay of Si I^2L [3] is primarily determined by stored charge in parasitic diodes associated with the extrinsic base regions of the I^2L gate. Self-aligned collector-base structures have been reported [4] which minimize the area of these parasitic diodes and deliver a gate delay of 0.8 ns for a layout geometry of 2.5 μm and a fan-out of 3. Other parasitics that can influence the gate delay are series resistance effects in the base and charge storage in the intrinsic base of the pnp transistor.

Recently there has been renewed interest in I^2L, motivated by the impressive performance reported for SiGe heterojunction bipolar transistors. In the context of I^2L, SiGe technology offers the prospect of using bandgap engineering to minimize the stored charge in the parasitic diodes associated with the I^2L gate. Modeling of SiGe I^2L has been reported recently [5], [6] but with considerable compromise in the treatment of the pnp load structure and hence the omission of important parasitic elements in the models. The work of Mazhari *et al.* [5] represented the load as a current source, implemented by a voltage source and resistor, whereas Karlsteen *et al.* [6] represented the load with an ideal current source. These approximations therefore preclude consideration of the charge storage associated with the load and also predict incorrectly the current delivered by the load; the latter because the load transistor is either in the active or saturated regime, depending on the prevailing logic condition. Moreover, these approaches do not consider the inherent tradeoffs in the design of the merged n-p-n/p-n-p devices, which place severe constraints on the relative doping levels of the semiconductor regions and the Ge concentration of the n-p-n base layer, as outlined in Section II. Furthermore the work presented in [5] only considers the *intrinsic* gate delay of circuits which, although being a key part in the total delay, neglects components of capacitance and lateral series 'access' resistances.

The approach used here is based on the model of Hendrickson and Huang [7] and involves dividing the structure into discrete regions for each of which the charge injection conditions can be calculated. Thus the stored charge can be ascertained throughout the structure and for a given injector current, the propagation delay of the inverter can be calculated. The model is extended from that described in [7] in that junction voltages are calculated for a given injector current and load gate. Thus all terminal currents are known and a quasi-two-dimensional approach is then employed to calculate terminal voltages using simple spreading resistances calculated from the semiconductor layer parameters, assuming the depletion approximation. The model is therefore quasi-two-dimensional. We have chosen to apply the model to three specific SiGe I^2L designs, one a conventional surface-fed approach, the second substrate-fed [8] and the third a variant which is specifically optimized for SiGe I^2L and features a high degree of self-alignment. The latter serves to demonstrate the flexibility of the method and also predicts a gate delay of 34 ps. Thus the use of heterojunctions can add high speed to the other well known advantages of I^2L technology, namely high packing density, low voltage and low power dissipation.

II. I^2L Gate Design

A schematic diagram of an I^2L inverter is shown in Fig. 1. We are concerned here with two forms of I^2L: substrate fed logic (SF-I^2L) and conventional surface fed logic (C-I^2L) of

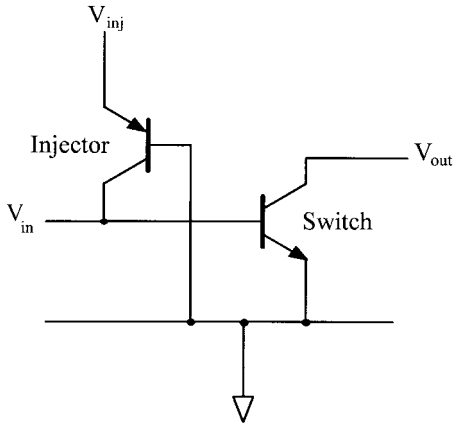

Fig. 1. Circuit diagram of an integrated injection logic inverter.

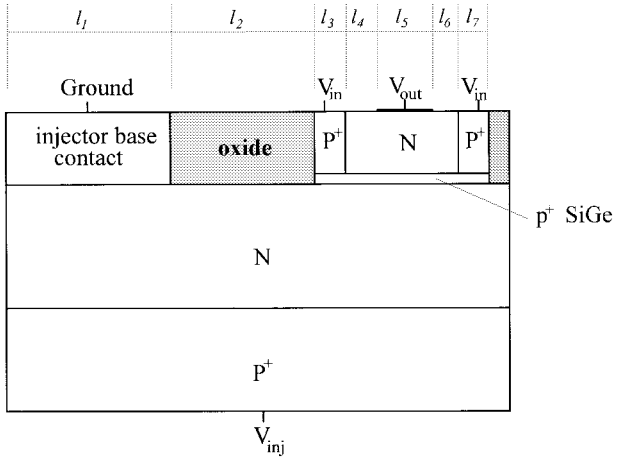

Fig. 2. Schematic cross-sectional view of the substrate-fed integrated injection logic (SF-I^{2}L) gate. Dimensions (μm) are, lateral: $l_1 = 10$, $l_2 = 15$, $l_3 = 2.5$, $l_4 = 2.5$, $l_5 = 5$, $l_6 = 2.5$, $l_7 = 2.5$. Intrinsic device width, $d = 12.5$ and width of extrinsic base rails, $d_{\rm br} = 3.3$.

which the simplified cross sections are shown in Figs. 2 and 3. These structures have been designed to be consistent with the epitaxial base and collector processes that are needed for a SiGe technology. The original conventional surface fed I^{2}L circuits reported in [1], [2] featured a lateral P-N-P injector transistor which was inefficient in delivering the base current for the vertical switching transistor. The lateral P-N-P also led to the poor dynamic performance of the original C-I^{2}L circuits as a result of excessive charge storage in the vicinity of the emitter of the switching transistor which is merged with the base of the injector transistor. The SiGe version of C-I^{2}L shown in Fig. 3 has a vertical P-N-p (upper-case denotes Si, lower-case SiGe), which has the potential to overcome the problem of poor dynamic performance because the heterojunction can limit the hole injection back into the base of the P-N-p injector transistor and also into the N-substrate. The SiGe collector of the injector transistor is merged with the base of the N-p-N switching transistor and the N-substrate forms the emitter of the switching transistor. In the SF-I^{2}L variant [8], shown in Fig. 2, the emitter of the injector transistor is assigned to the substrate, thereby ensuring an efficient supply of base current for the switching transistor.

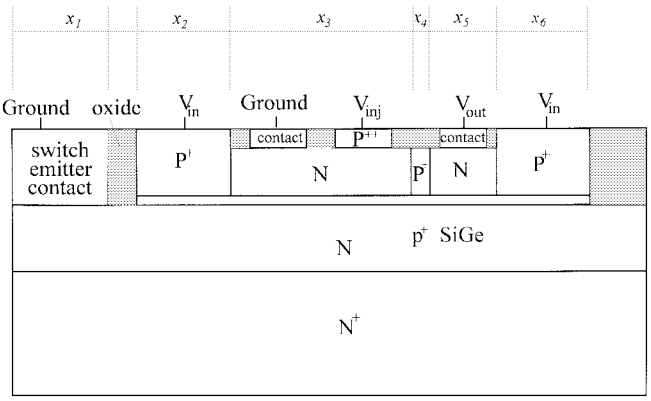

Fig. 3. Schematic cross-sectional view of the surface-fed integrated injection logic (C-I^{2}L) gate. Dimensions (μm) are, lateral: $x_1 = 15$, $x_2 = 10$, $x_3 = 30$, $x_4 = 2.5$, $x_5 = 10$, $x_6 = 10$. Intrinsic device width, $d = 15$ and width of extrinsic base rails, $d_{\rm br} = 2.5$.

Clearly, the substrate fed version has higher packing density and inherently lower capacitance than the surface fed, but at the expense of more complex device design tradeoffs.

The inherent advantages of the designs shown in Figs. 2 and 3 are firstly that the heterojunction emitter/base structure of the N-p-N switching transistor produces high β for improved dynamic fan-out. Secondly the heterojunction collector/base structure for the injector transistor reduces hole injection into the base of the injector (also the emitter of the switch in SF-I^{2}L) reducing charge storage in that region. Thirdly modern low temperature growth techniques (MBE or LPCVD) ensure excellent control of epitaxial layer thicknesses. This is especially important for the SF-I^{2}L N-p-N emitter layer which has a strong influence on dynamic performance and was a major drawback of the original technology. Finally, epitaxial SiGe bases are more readily scalable, which is an important advantage over Si I^{2}L.

A. Design Constraints

An analytical model of the I^{2}L inverter has been presented by Klaassen [9] which allows the conditions for achieving inverter action to be defined. Referring to Fig. 1, physically, the requirement is that the merged P-N-p (injector) and N-p-N (switch) transistors should be designed such that the voltage associated with a logic 1 on the base of the N-p-N ($V_{\rm in}$) should be sufficiently lower than the power rail voltage, $V_{\rm inj}$, so that the P-N-p injector is able to supply sufficient current, that is to say, the P-N-p must not totally saturate. There is also a limit to the "upward" gain, β_{uN}, of the N-p-N switch transistor. These two conditions can be summarized as

$$\frac{I_{SN}}{I_{SP}} > 1 \tag{1}$$

$$\beta_{uN} > \frac{1}{1 - I_{SP}/I_{SN}} \tag{2}$$

where I_S is the Gummel-Poon forward saturation current, the subscripts "N" and "P" refer to the N-p-N and P-N-p devices respectively and

$$I_S = \frac{qAD_b(N_b)n_{ib}^2(\Delta E_{g(\rm SiGe)}, \Delta E_{g(\rm BGN)})}{N_b W_b(N_b)} \tag{3}$$

where

- q electronic charge;
- A emitter-base junction area;
- D_b diffusion coefficient of minority carriers in the base;
- n_i intrinsic carrier concentration, dependent on both the Ge concentration and band-gap narrowing in the heavily doped base;
- W_b base width;
- N_b doping concentration of the base, which is assumed constant.

Referring to (3), we now list the important design tradeoffs associated with the ratio of I_{SN}/I_{SP} which figures in (1) and (2).

1) Increasing the Ge concentration increases I_{SN} due to a reduction in bandgap and has the added advantage of deferring the high injection condition in the base of the N-p-N switching transistor to a higher bias value. However the excess charge storage in the base of the N-p-N switching transistor is increased which affects the dynamic performance.
2) Reducing the SiGe doping causes a net increase in I_{SN}, as the band gap narrowing and other dependencies are weaker, in (3) than that of N_b. Reducing N_b however has the adverse effects of increasing the series resistance and charge storage in the base of the N-p-N switching transistor as well as reducing the bias level for the onset of high injection.
3) Increasing W_{bP} (P-N-p basewidth) directly decreases I_{SP} but also adversely increases the charge storage in the injector base. A larger W_{bP} has the advantage of reducing the series resistance in the base of the P-N-p and also, for the SF variant, in the emitter of the N-p-N device. This is an important advantage, as the current is this layer will be high with a logic 1 at the input.
4) Increasing the injector base doping reduces I_{SP} which decreases series resistance and increases the bias level for the onset of high level injection. There is also a disadvantage for the SF-I^{2}L variant, as it also increases the base-emitter capacitance for the switching transistor which limits switching speeds.

These important design tradeoffs place severe constraints on the Ge concentration and doping levels but are vital to take into account in a realistic appraisal of I^{2}L. In particular, spreading resistance, especially in the N-p-N emitter layer can prevent inverter action [10]. Further comment is deferred to the discussion in Section V.

III. The Charge Control Model

In this section and the associated appendix, we describe the model which allows calculation of the average time to switch charge between two logic levels, as a function of injector current. The device is divided into discrete charge storage regions associated with quasineutral and depleted regions. The detailed expressions for the charge storage in each region considered are presented in the appendix and can be understood by referring to the list of symbols and the regional definitions in Figs. 2 and 3. The principle is demonstrated by consideration of the following two equations which describe the switched (free) charge associated with a quasi-neutral region bounded by injecting and collecting junctions:

$$\Delta Q_{\text{neut}} = \frac{q(A \cdot W) n_i^2}{2 \cdot N} \cdot \Delta \exp\left(\frac{V_j}{v_t}\right) \tag{4}$$

and that for the switched charge associated with a depletion region

$$\Delta Q_{\text{dep}} = q \cdot A \sqrt{\frac{2 \cdot \varepsilon \cdot N}{q}} \cdot \Delta \sqrt{V_j + V_{\text{bi}}} \tag{5}$$

where

- q electronic charge;
- A area;
- n_i intrinsic carrier concentration of the semiconductor;
- N doping concentration of the region;
- W thickness of the epitaxial layer (or the diffusion length if necessary);
- V_j applied junction voltage;
- V_{bi} built-in junction voltage;
- v_t thermal voltage.

The voltage terms in expressions (4) and (5) account for the difference in junction voltage at logic "1" and logic "0" and are defined as:

$$\Delta \exp\left(\frac{V_j}{v_t}\right) = \exp\left(\frac{V_{j1}}{v_t}\right) - \exp\left(\frac{V_{j0}}{v_t}\right) \tag{6}$$

$$\Delta \sqrt{(V_j + V_{\text{bi}})} = \sqrt{(V_{j1} + V_{\text{bi}})} - \sqrt{(V_{j0} + V_{\text{bi}})} \tag{7}$$

where the subscripts "1" and "0" relate to high and low logic conditions respectively. The average time to switch between the two logic levels as a function of injector current is found from

$$\tau_d = \frac{1}{2 \cdot I_{\text{inj}}} \sum_i \Delta Q_i \tag{8}$$

Also included in the model are the spreading resistances of each region which when combined with the Ebers-Moll models can be used to calculate the terminal voltages as follows.

The operating conditions (V_{BE1}, V_{BE0}, V_{CB1}, V_{CB0}), for a given injector current, are determined by the following iterative procedure. First, the common emitter (β) and common base (α) current gains and the spreading resistances of the different layers, are calculated from the doping levels and thicknesses of the various regions, ignoring depletion regions. Both reverse injection and neutral base recombination are considered as mechanisms for base current. Doping dependent diffusion coefficients and band-gap narrowing are taken into account using the empirical expressions included in [11] and [12]. The effect of Ge concentration on the intrinsic carrier concentration is taken from [13]. Junction voltages and currents are then calculated using the Ebers-Moll transport model to give the emitter-base voltage of the switch transistor, as

$$V_{\text{BE}N} = V_t \cdot \ell n \left[\frac{I_{CN} + I_{SN} + (I_{EN}/\alpha_{RN}) - (I_{SN}/\alpha_{RN}\alpha_{FN})}{I_{SN} - (I_{SN}/\alpha_{RN}\alpha_{FN})} \right] \tag{9}$$

and the base-collector voltage of the injector transistor as:

$$V_{\mathrm{CB}\,P} = V_t \cdot \ell n\left[\frac{I_{EP} - I_{SP} + \left(I_{CP}/\alpha_{FP}\right) + \left(I_{SP}/\alpha_{RP}\alpha_{FP}\right)}{\left(I_{SP}/\alpha_{RP}\alpha_{FP}\right) - I_{SP}}\right]. \tag{10}$$

Referring to Fig. 2, the emitter current for the injector transistor of the SF-I^{2}L version only is

$$I_{EP} = \frac{l_A}{l_T} \cdot I_{\mathrm{inj}}. \tag{11}$$

The factor "l_A/l_T" in (11) is an estimate of the fraction of the emitter current that is collected in the base of the switch transistor. The collector currents of the N-p-N switch transistor of the gate under consideration and the P-N-p injector transistor of the following inverter are equal ($I_{CP} = I_{CN}$), and so we can write

$$I_{CN} = \frac{I_{EP}}{\alpha_{FP}}. \tag{12}$$

The active value for α_{FP} is used in (12) because the injector transistor of the loading gate is unsaturated with a logic zero on the output of the test gate. We can also write

$$I_{EN} = I_{CN} + I_{CP}. \tag{13}$$

Now, recognising that $V_{\mathrm{BE}\,N} = V_{\mathrm{CB}\,P}$, (9) and (10) are equated and rearranged to allow calculation of I_{CP} $(=I_{BN})$ of the first inverter and hence $V_{\mathrm{BE}\,N}$ can be found. The junction voltage $V_{\mathrm{CB}\,N}$ can also be found from the appropriate equation of the form of (10). All currents can thus be determined in the "intrinsic" inverter and hence the voltage drop across the switch emitter layer with series resistance, R_{ES}, can be calculated as

$$V_{\mathrm{RES}} = (I_{EN} + I_{BP}) \cdot R_{\mathrm{ES}} \quad \text{for the SF-I}^2\text{L structure} \tag{14a}$$

$$V_{\mathrm{RES}} = I_{EN} \cdot R_{\mathrm{ES}} \quad \text{for the C-I}^2\text{L structure.} \tag{14b}$$

Similarly the voltage drop across the collector series resistance, R_{CS}, can be calculated using the following expressions:

$$V_{\mathrm{RCS}} = I_{CN} \cdot R_{\mathrm{CS}}. \tag{15}$$

This enables the *terminal* voltages to be found. These values for terminal voltage are then used to give "worst case" estimates of depletion region widths and dependent parameters and the terminal voltages are re-calculated using adjusted values of quasineutral regions. Finally the various charge components (ΔQ_i) are calculated using (A1)–(A13) or (A14)–(A28) and the propagation delay τ_d, for the inverter switching between the two logic levels, for a given injector current is calculated from (8).

The injector rail voltage can be calculated from

$$V_{\mathrm{inj}} = V_{\mathrm{BE}\,P} + R_{EP} \cdot I_{EP} \tag{16}$$

where R_{EP} is the series resistance associated with the emitter of the injector transistor. The value of injector voltage obtained from (16) allows the calculation of the average power dissipation.

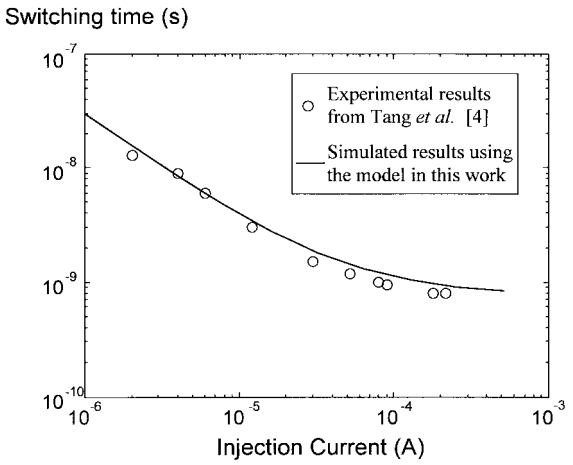

Fig. 4. Validation of the charge storage model by a comparison of the predicted switching time as a function of injection current with the measured results of Tang *et al*. [4].

IV. Results

A. Validation of the Modeling Technique

The self-aligned Si I^{2}L structure of Tang *et al*. [4] was implemented in the model to provide experimental validation of the analysis method. Average values for impurity levels of diffused regions were used, deduced from the sheet resistance values given and taking into account doping dependence of mobility based on the average values. The reported, measured values for transistor current gains (α, β) were used. The results are shown in Fig. 4 and despite the approximations made, very good agreement is obtained between the experimental data points and the simulated switching time, which provides confidence in the modeling technique used here for predictive simulations. It is worth noting that the assumption of constant, average doping concentration is more appropriate for the case of the epitaxial SiGe structures considered next.

B. SiGe I^{2}L Simulations

There are two aspects of I^{2}L operation that must be considered; firstly the fact that dimensions and doping concentrations should satisfy the conditions for inverting action, and secondly, within those restrictions, that the relative parameters should be optimized to obtain the best possible transient performance. The parameters needed to satisfy the inverting action conditions were determined by two-dimensional (2-D) simulation (MEDICI) from which the SPICE dc model parameters were extracted. The results of this process [10] identified the importance of minimizing spreading resistance, particularly in the switch emitter, in addition to the requirements set by (2) and (3). The material parameters that are required to allow inverting action are given in Table I. Using the doping concentrations in Table I it was found that a 16% mole fraction of Ge was required to ensure inverting action. The values for switch emitter doping concentrations, N_{SE} and N_{IBSE}, need to be high in order to reduce spreading resistances.

Using these preliminary results the charge storage model can be utilized to determine the switching delay time, the power-

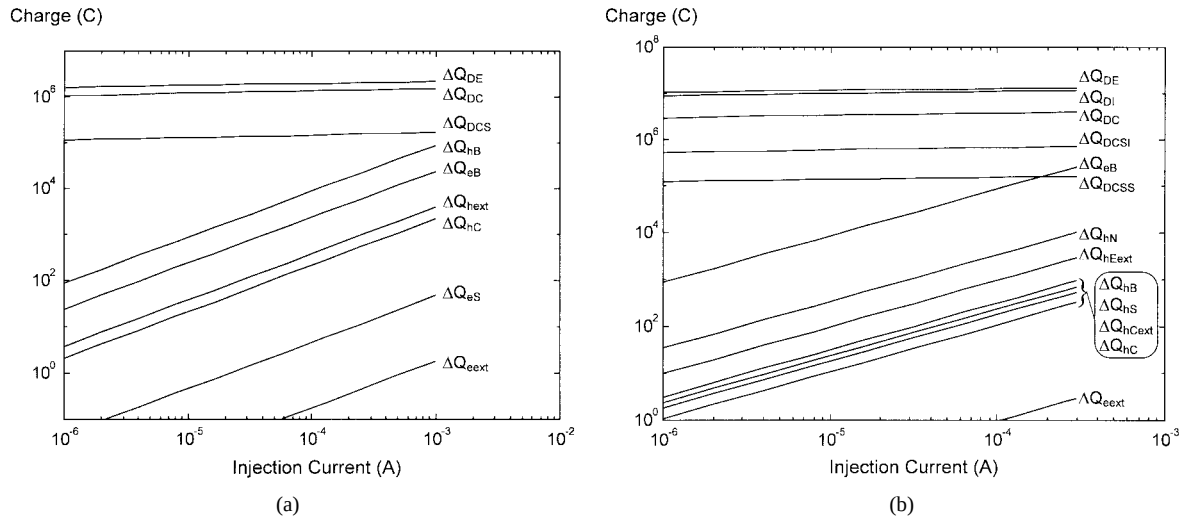

Fig. 5. Calculated components of stored charge as a function of as a function of injection current: (a) substrate-fed Integrated Injection Logic (SF-I^{2}L) and (b) surface-fed integrated injection logic (C-I^{2}L).

TABLE I
SUMMARY OF THE MATERIAL AND DEVICE PARAMETERS USED IN THE CALCULATIONS

C - I^{2}L		SF - I^{2}L	
N_{SUB}	8 x 10^{18} cm^{-3}	N_{IE}	8 x 10^{18} cm^{-3}
N_{SE}	1 x 10^{18} cm^{-3}	N_{IBSE}	5 x 10^{17} cm^{-3}
W_{SE}	600 nm	W_{IBSE}	5 μm
N_{ICSB}	2 x 10^{19} cm^{-3}	N_{ICSB}	2 x 10^{19} cm^{-3}
W_{ICSB}	25 nm + 20nm of intrinsic spacers	W_{ICSB}	25 nm + 20nm of intrinsic spacers
Ge mole percentage	16%	Ge mole percentage	16%
N_{IB}	1 x 10^{18} cm^{-3}	N_{SC}	2 x 10^{17} cm^{-3}
W_{IB}	300 nm	W_{SC}	300 nm
N_{SC}	1 x 10^{18} cm^{-3}		
W_{SC}	300 nm		

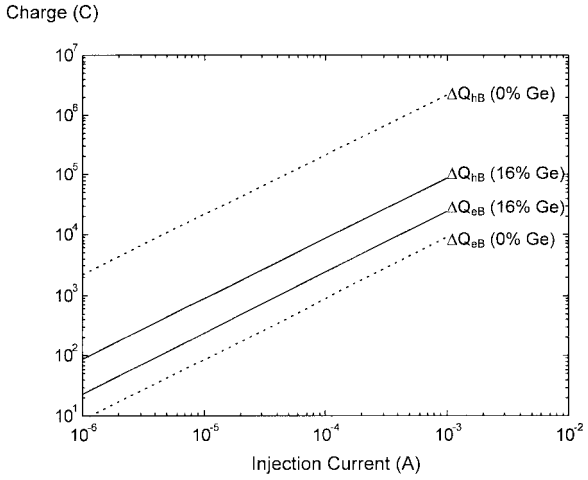

Fig. 6. Stored hole charge in the switch emitter ($\Delta Q_{\rm hB}$) and stored electron charge in the switch base ($\Delta Q_{\rm eB}$) as a function of injection current for substrate-fed integrated injection logic gates (SF-I^{2}L) with 0% Ge and 16% Ge.

delay characteristics and to identify which charge storage region limits performance. We present results for 2.5 μm design rules, unless otherwise stated, in order to allow easy comparison with the literature. Fig. 5 shows the magnitude of the charge components as a function of injector current, $I_{\rm inj}$, for each structure using the parameters in Table I. It can be seen that in both substrate fed [Fig. 5(a)] and surface fed [Fig. 5(b)] variants the most significant elements of charge are those associated with the depletion regions (the ΔQ_D terms). To reduce these charge elements the structural dimensions and/or the doping concentrations of these regions have to be reduced. Unfortunately this latter modification will cause an increase in critical series resistances in the associated regions and as a result there is tradeoff between depletion capacitance and series resistance, as will be discussed later.

The effect of introducing SiGe into the base of the switch transistor is illustrated using the specific example of the two largest excess charge terms in the substrate fed structure, namely $\Delta Q_{\rm hB}$ (holes stored in the switch emitter) and $\Delta Q_{\rm eB}$ (electrons stored in the switch base). The results are shown in Fig. 6 for a SiGe (16% Ge) base and a pure Si base (0% Ge). It is observed that the inclusion of SiGe (16% Ge) in the base of the switch transistor effectively reduces, for a given current level, the reverse injection of holes from the base to the emitter $(\Delta Q_{\rm hB})$ by more than an order of magnitude by virtue of the heterojunction action. A disadvantage of introducing SiGe is the increase in electron storage in the switch base $(\Delta Q_{\rm eB})$ due to the increase in intrinsic carrier concentration in the reduced bandgap SiGe base. The benefits of SiGe clearly overcome the disadvantages in a structure with adequate dimensions, as the increase in electron storage in the base is little more than a factor of three. The difference in size, doping levels and spreading resistances between the two structures explains the fact that this stored electron charge is greater in the C-I^{2}L than in the SF-I^{2}L. These results imply that a properly optimized SiGe I^{2}L technology could potentially deliver a switching time that was more than ten times faster than its Si equivalent.

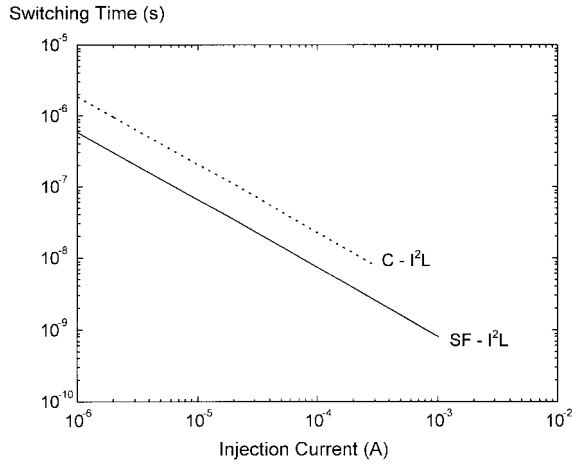

Fig. 7. Calculated switching time as a function of injection current for the substrate-fed (SF-I^2L) and surface-fed (C-I^2L) integrated injection logic gates.

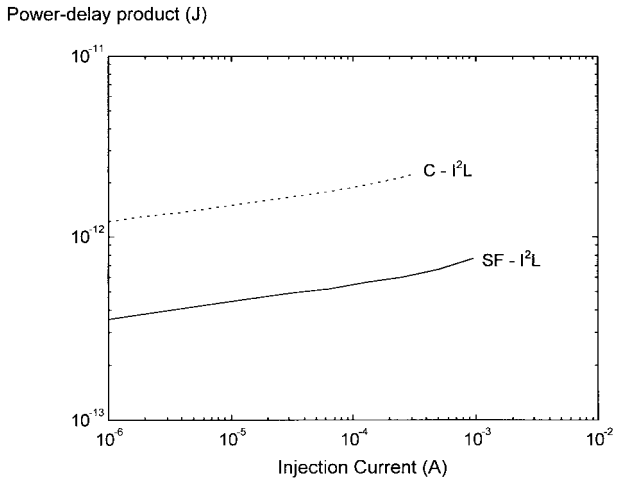

Fig. 8. Calculated power-delay product as a function of injection current for the substrate-fed (SF-I^2L) and surface-fed (C-I^2L) Integrated Injection Logic gates.

The switching delay times, power delay product and intrinsic and terminal voltage (logic) levels can be seen in Figs. 7–9, respectively. The linear nature of the delay time curve observed in Fig. 7 confirms that the switching at these injection current levels is limited by depletion charge. The power delay-product of SF-I^2L can be seen, in Fig. 8, to be approximately a factor of three lower than that of C-I^2L which is consistent with the switching delay times shown in Fig. 7. The predicted logic levels of the substrate fed version are shown as a function of injection current in Fig. 9. The terminal voltage levels can be seen to depart from the intrinsic potentials at higher injection currents due to parasitic potential drops across the series resistances. The most important component of series resistance is that associated with the N epitaxial layer that forms the emitter of the switch (NpN) and the base of the injector (PNp). The magnitude of this access resistance causes debiasing of the NpN transistor at high current levels which eventually prohibits circuit action. The cessation of circuit functionality can be seen in this case to occur at an injection current of 1 mA.

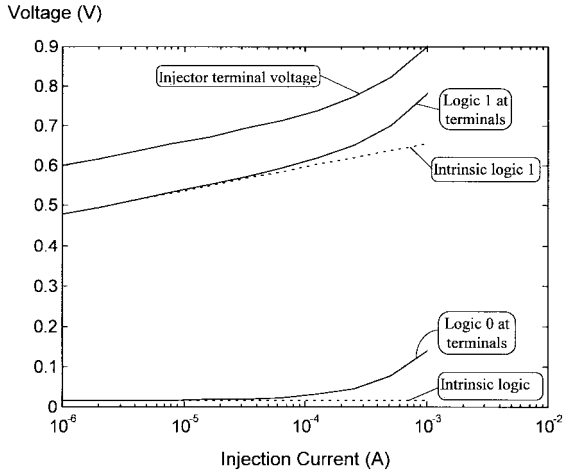

Fig. 9. Predicted logic level as a function of injection current for the substrate-fed (SF-I^2L) integrated injection logic gate. Also shown are the intrinsic logic levels which are the logic levels at the terminals of the intrinsic device (i.e. logic levels in the absence of series resistances).

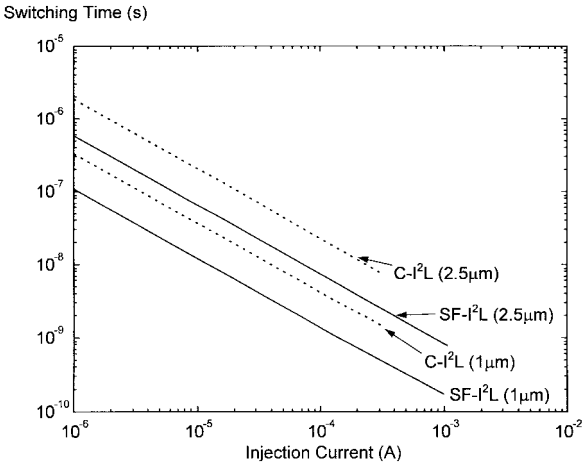

Fig. 10. Calculated switching time as a function of injection current for a substrate-fed (SF-I^2L) and a surface-fed (C-I^2L) integrated injection logic gate designed with a gate design rule of 1 um. Also shown for comparison are the gates that were designed with a design rule of 2.5 um.

V. Discussion

The results in Figs. 5–9 indicate that a number of tradeoffs are involved in the design of SiGe I^2L gates. We will begin by considering the tradeoffs at low injection currents where the charges in the depletion regions (ΔQ_D) dominate the gate behavior. It is clear that to improve the switching time at low injection currents, the dominant depletion charge should be reduced. For the SF-I^2L structure, the switch collector doping consideration should be decreased until the switch collector/base depletion charge ΔQ_{DC} is lower than the switch emitter/base depletion charge ΔQ_{DE} [Fig. 5(a)]. It is not possible to reduce the switch emitter doping in order to reduce ΔQ_{DE}, because of limitations imposed by series resistance in the switch emitter. For the C-I^2L structure in Fig. 5(b), the charges that need to be minimized are the charge in the injector collector/base depletion region ΔQ_{DI} and in the switch collector/base depletion region, ΔQ_{DC}. This can be achieved by reducing the doping in the collectors of the

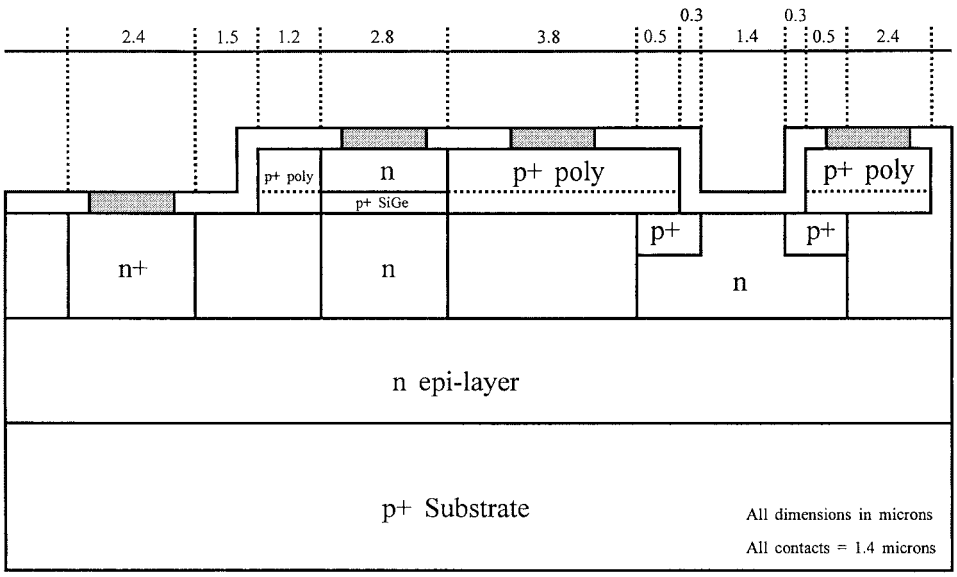

Fig. 11. Schematic cross-sectional view of the second generation surface-fed integrated injection logic gate. Layer widths (μm) are, n epi-layer = 3, selective epi (in oxide windows) = 0.25, p^+ implants = 0.1, p^+ SiGe = 0.045, p^+ poly-silicon 0.195, selective epi = 0.15. Components ΔQ_{DEP}, $\Delta Q_{e\,\mathrm{EP}}$, $\Delta Q_{e\,\mathrm{CP}}$, ΔQ_{BL} are specific to this structure but are calculated using the same form of equations.

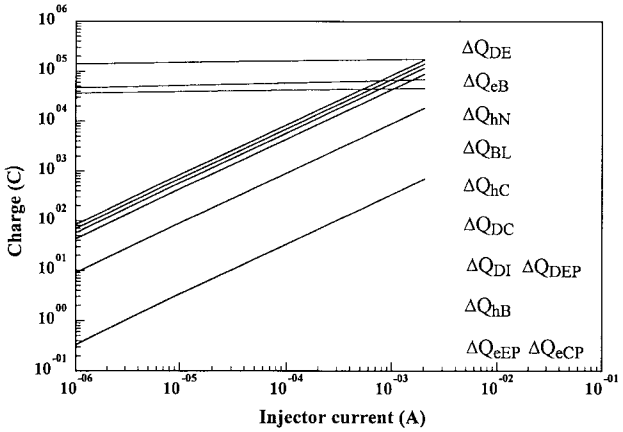

Fig. 12. Calculated components of stored charge as a function of injector current for the self-aligned structure of Fig. 11.

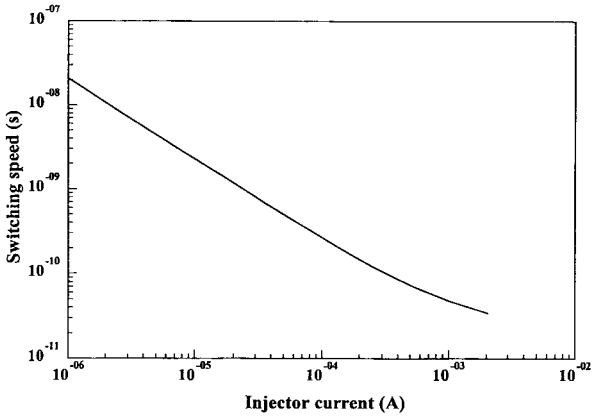

Fig. 13. Calculated switching time as a function of injector current for the self-aligned structure of Fig. 11.

injector and switch transistors. In the case of the former, there is a tradeoff with series resistance, because the collector of the injector transistor is also the base of the switch transistor. Once again, it is not desirable to reduce the switch emitter doping concentration due to limitations imposed by series resistance.

The above considerations suggest that, at low injection currents the direct benefits of SiGe are marginal due to the dominance of the depletion charge. A small benefit is obtained, which is mainly due to the decreased charge in the switch emitter/base and collector/base depletion regions. At low injection currents, the most effective way of reducing the propagation delay is to reduce the area of the depletion regions, either by reducing the gate geometry or by employing self-aligned fabrication schemes to reduce the extrinsic areas of the gate. In scaling the device geometry, SiGe is likely to be of indirect benefit, since the increased gain of the SiGe switch transistor would allow scaling to smaller geometries than could be achieved using a pure Si I^2L technology. Fig. 10 illustrates the effects of scaling the gate geometry on the switching time. A reduction of the gate design rules from 2.5 μm to 1.0 leads to a decrease in the switching time by a factor of approximately 6 for both C-I^2L and SF-I^2L. The benefits of reducing the extrinsic areas of the gate can be seen in the difference in performance of C-I^2L and SF-I^2L gates. The overall area of the SF-I^2L gate is smaller than that of the C-I^2L gate because of the use of an injector in the substrate (Fig. 2). As a result, the critical depletion capacitors in the SF-I^2L gate are smaller than those in the C-I^2L gate. Even further benefits would be obtained if self-aligned fabrication schemes were used to reduce depletion charge and eliminate the excess charge associated with the extrinsic base rails [4]. Such a strategy has achieved a switching time of 290 ps in a pure Si I^2L gate [14] at a gate geometry of 3 μm and one for SiGe I^2L is presented in the next section.

VI. A Self-Aligned SiGe I^2L Technology

We have seen that the biggest benefits of SiGe are to be found at high injection currents where the stored charges ΔQ_h and ΔQ_e dominate the switching time. Minority carrier stored

charge increases with injection current (Fig. 5) and hence dominates the gate switching time at the high speed end of the speed-power characteristic. Another factor which has to be taken into account in this region of operation is series resistances, which limit the achievable switching speeds. A careful optimization of the gate layout and architecture is needed to optimize the switching speed, and this is addressed in the structure of Fig. 11. The structure features a self-aligned SiGe HBT which minimizes the area of the extrinsic base rails, and a lateral pnp injector for compatibility with mainstream SiGe technology. Series resistances are minimized by including an n^+ buried layer with a sheet resistance of 20 Ωsq. and a p^+ polysilicon extrinsic base which is silicided with a sheet resistance of 2 Ω/sq. The charge components from application of the stored charge model are shown in Fig. 12 and delay characteristic in Fig. 13, where a maximum delay of 34 ps is predicted using 1.4 micron design rules. In calculating these curves, a Ge concentration of 16% was used and base, emitter and collector doping concentrations of 4×10^{19} cm^{-3}, 3×10^{18} cm^{-3} and 1×10^{17} cm^{-3} respectively. Optimum performance at the highest achievable current level was achieved by ensuring that the depletion and stored charge components in the vicinity of the NpN base are equal. The predicted gate delay of 34 ps is 8.5 times lower than the reported experimental value of 290 ps for 3 micron pure Si I^2L gates [14], which clearly demonstrates the potential of SiGe I^2L. In addition, there is undoubtedly scope for improving on the gate delay by scaling the device geometry and further optimising the gate layout.

VII. Conclusion

The paper has presented a modified charge storage model for use in the investigation and design of SiGe I^2L gates, taking account of the detailed architecture of the gate. The modified charge storage model allows identification of the dominant charge storage regions in the I^2L gate and represents a powerful aid in optimization. The model is structure-based, includes both switch and load devices and allows for appropriate loading of input and output of a given inverter. The importance of d.c. design constraints has been emphasised so that realistic values for parameters are used. Furthermore, the effects of series resistances which preclude operation to higher injector currents, is inherent in the model and is shown to be a very important aspect of I^2L gate design.

At low injector currents, the use of SiGe has been shown to offer only marginal benefits, since the switching speed is dominated by depletion region charge. The most important advantage of SiGe at these current levels is likely to be improved scalability of I^2L technology. At high injector currents, where the switching speed is dominated by stored minority carrier charge, the use of SiGe in I^2L technology has been shown to have important benefits. A reduction by a factor of more than ten in the stored charge is obtained when 16% Ge is incorporated into the base of the npn switch resistor. The model has been applied to a self-aligned structure which is specifically optimized for SiGe I^2L and a switching speed of 34 ps is predicted even at a geometry of 1.4 micron. This delay will be further reduced with a fully optimized, scaled design.

Appendix
Charge Storage Equations

Following the approach in [7], one-dimensional (1-D) expressions can be written for the excess stored charge switched between the two logic levels set by the injector current, in each of the individual regions. Reference should be made to the list of symbols and the regional definitions in Figs. 2 and 3.

SUBSTRATE FED I^2L

1) **Electron charge stored in the substrate (injector emitter)**

$$\Delta Q_{\mathrm{eS}} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot L_{e\,\mathrm{IE}}}{2 \cdot N_{\mathrm{IE}}} (l_T \cdot (d + d_{\mathrm{br}})) \Delta \exp\left(\frac{V_{\mathrm{inj}}}{v_t}\right) \tag{A1}$$

which consists of excess electrons in the injector emitter.

2) **Hole charge stored in the injector base/switch emitter**

$$\Delta Q_{\mathrm{hB}} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot W_{\mathrm{IBSE}}}{2 \cdot N_{\mathrm{IBSE}}} (l_T \cdot (d + d_{\mathrm{br}})) \Delta \exp\left(\frac{V_{\mathrm{BE}}}{v_t}\right) \tag{A2}$$

which consists of holes from the injector emitter (substrate) and the switch base (SiGe). The latter is suppressed by the heterojunction action.

3) **Electron charge stored in the switch base/injector collector**

$$\Delta Q_{\mathrm{eB}} = \frac{q \cdot n_{i(\mathrm{SiGe})}^2 \cdot W_{\mathrm{ICSB}}}{2 \cdot N_{\mathrm{ICSB}}} (l_A \cdot (d + d_{\mathrm{br}})) \Delta \times \exp\left(\frac{V_{\mathrm{BE}}}{v_t}\right) \tag{A3}$$

which consists of electrons from the switch emitter (injector base) and switch collector when saturated.

4) **Hole charge stored in the intrinsic switch collector**

$$\Delta Q_{\mathrm{hC}} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot W_{\mathrm{SC}}}{2 \cdot N_{\mathrm{SC}}} (l_C \cdot d) \Delta \exp\left(\frac{V_{\mathrm{BE}}}{v_t}\right) \tag{A4}$$

which consists of holes from the SiGe base when the switch is saturated. This component of stored charge is suppressed by the heterojunction action.

5) **Hole charge stored in the switch collector injected from the extrinsic base rails**

$$\Delta Q_{h\,\mathrm{ext}} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot L_{\mathrm{hSC}}}{2 \cdot N_{\mathrm{SC}}} (2 \cdot (l_C + d) \cdot W_{\mathrm{SC}}) \Delta \exp\left(\frac{V_{\mathrm{BC}}}{v_t}\right) \tag{A5}$$

which consists of holes injected from the extrinsic base rails into the switch collector.

6) **Electrons in the extrinsic base rails**

$$\Delta Q_{e\,\mathrm{ext}} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot L_{\mathrm{eSB}}}{2 \cdot N_{\mathrm{SC}}} (2 \cdot (l_C + d) \cdot W_{\mathrm{SC}}) \Delta \exp\left(\frac{V_{\mathrm{BC}}}{v_t}\right) \tag{A6}$$

which consists of holes injected from the extrinsic base rails into the switch collector.

7) **Switch emitter/base (injector base/collector) depletion charge**

$$\Delta Q_{\mathrm{DE}} = q \cdot \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_s \cdot N_{\mathrm{IBSE}}}{q}} (l_A \cdot (d + d_{\mathrm{br}})) \times \Delta\sqrt{V_{\mathrm{BE}} + V_{\mathrm{bi}}}. \quad \text{(A7)}$$

This element of charge is defined by the active area.

8) **Switch collector/base depletion charge**

$$\Delta Q_{\mathrm{DC}} = q \cdot \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_s \cdot N_{\mathrm{SC}}}{q}} (l_C \cdot d) \Delta\sqrt{V_{\mathrm{CB}} + V_{\mathrm{bi}}}. \quad \text{(A8)}$$

This element of charge is defined by the switch collector area.

9) **Switch collector/base sidewall depletion charge**

$$\Delta Q_{\mathrm{DCS}} = q \cdot \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_s \cdot N_{\mathrm{SC}}}{q}} 2 \cdot W_{\mathrm{SC}} \cdot (l_C + d) \times \Delta\sqrt{V_{\mathrm{BE}} + V_{\mathrm{bi}}}. \quad \text{(A9)}$$

This element of charge accounts for the vertical sidewalls formed by the P^+ implantations down to the SiGe layer.

The depletion charge in the emitter/base junction of the injector transistor was assumed to be negligible. The voltage terms included in each charge difference expression account for the difference in voltages at logic "1" and logic "0." The full expressions used are given below:

$$\Delta \exp\left(\frac{V_{\mathrm{BE}}}{v_t}\right) = \exp\left(\frac{V_{\mathrm{BE1}}}{v_t}\right) - \exp\left(\frac{V_{\mathrm{BE0}}}{v_t}\right) \quad \text{(A10)}$$

$$\Delta \exp\left(\frac{V_{\mathrm{inj}}}{v_t}\right) = \exp\left(\frac{V_{\mathrm{inj1}}}{v_t}\right) - \exp\left(\frac{V_{\mathrm{inj0}}}{v_t}\right) \quad \text{(A11)}$$

$$\Delta\sqrt{(V_{\mathrm{BE}} + V_{\mathrm{bi}})} = \sqrt{(V_{\mathrm{BE1}} + V_{\mathrm{bi}})} - \sqrt{(V_{\mathrm{BE0}} + V_{\mathrm{bi}})} \quad \text{(A12)}$$

$$\Delta\sqrt{(V_{\mathrm{CB}} + V_{\mathrm{bi}})} = \sqrt{(V_{\mathrm{CB1}} + V_{\mathrm{bi}})} - \sqrt{(V_{\mathrm{CB0}} + V_{\mathrm{bi}})}. \quad \text{(A13)}$$

The terms V_{BE1}, V_{BE0}, V_{CB1}, V_{CB0} relate to high (1) and low (0) logic conditions and V_{bi} is the appropriate junction built-in voltage.

SURFACE FED I^2L

1) **Hole charge stored in the N^+ substrate**

$$\Delta Q_{\mathrm{hS}} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot L_{\mathrm{hSub}}}{2 \cdot N_{\mathrm{SUB}}} \cdot \delta \cdot x_A \cdot (d + d_{\mathrm{br}}) \cdot \Delta\left(\exp\frac{V_{\mathrm{BE}}}{v_t}\right). \quad \text{(A14)}$$

2) **Hole charge stored in the switch emitter**

$$\Delta Q_{hN} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot W_{\mathrm{SE}}}{2 \cdot N_{\mathrm{SE}}} \cdot (1 + \delta) \cdot x_A \cdot (d + d_{\mathrm{br}}) \cdot \Delta\left(\exp\frac{V_{\mathrm{BE}}}{v_t}\right). \quad \text{(A15)}$$

3) **Electrons stored in the switch base/injector collector**

$$\Delta Q_{\mathrm{eB}} = \frac{q \cdot n_{i(\mathrm{SiGe})}^2 \cdot W_{\mathrm{ICSB}}}{2 \cdot N_{\mathrm{ICSB}}} x_C \cdot d \cdot \Delta\left(\exp\frac{V_{\mathrm{BE}}}{v_t}\right). \quad \text{(A16)}$$

4) **Holes stored in the injector base**

$$\Delta Q_{\mathrm{hB}} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot W_{\mathrm{IB}}}{2 \cdot N_{\mathrm{IB}}} \cdot x_3 \cdot d \cdot \Delta\left(\exp\frac{V_{\mathrm{inj}}}{v_t}\right). \quad \text{(A17)}$$

5) **Holes stored in the intrinsic switch collector**

$$\Delta Q_{\mathrm{hC}} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot W_{\mathrm{SC}}}{2 \cdot N_{\mathrm{SC}}} \cdot x_5 \cdot d \cdot \Delta\left(\exp\frac{V_{\mathrm{BE}}}{v_t}\right). \quad \text{(A18)}$$

6) **Holes stored in the switch collector injected from the extrinsic base rails**

$$\Delta Q_{\mathrm{hCext}} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot L_{\mathrm{hSC}}}{2 \cdot N_{\mathrm{SC}}} \cdot (2 \cdot W_{\mathrm{SC}} \cdot (x_5 + d)) \cdot \Delta\left(\exp\frac{V_{\mathrm{BC}}}{v_t}\right). \quad \text{(A19)}$$

7) **Holes stored in the injector base injected from the extrinsic base rails**

$$\Delta Q_{\mathrm{hBext}} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot L_{\mathrm{hIB}}}{2 \cdot N_{\mathrm{SC}}} \cdot (2 \cdot W_{\mathrm{IB}} \cdot (x_3 + d)) \cdot \Delta\left(\exp\frac{V_{\mathrm{BE}}}{v_t}\right). \quad \text{(A20)}$$

8) **Electrons stored in the extrinsic base rails**

$$\Delta Q_{e\,\mathrm{ext}} = \frac{q \cdot n_{i(\mathrm{Si})}^2 \cdot L_{\mathrm{eSB}}}{2 \cdot N_{\mathrm{SC}}} \cdot (2 \cdot W_{\mathrm{SC}} \cdot (x_C + d)) \cdot \Delta\left(\exp\frac{V_{\mathrm{BC}}}{v_t}\right). \quad \text{(A21)}$$

9) **Switch emitter/base depletion charge**

$$\Delta Q_{\mathrm{DE}} = q \cdot \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_s \cdot N_{\mathrm{SE}}}{q}} x_A \cdot (d + d_{\mathrm{br}}) \cdot \Delta\sqrt{V_{\mathrm{BE}} + V_{\mathrm{bi}}}. \quad \text{(A22)}$$

10) **Switch collector/base depletion charge**

$$\Delta Q_{\mathrm{DC}} = q \cdot \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_s \cdot N_{\mathrm{SC}}}{q}} x_5 \cdot d \cdot \Delta\sqrt{V_{\mathrm{BC}} + V_{\mathrm{bi}}}. \quad \text{(A23)}$$

11) **Injector collector/base depletion charge**

$$\Delta Q_{\mathrm{DI}} = q \cdot \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_s \cdot N_{\mathrm{IB}}}{q}} x_3 \cdot d \cdot \Delta\sqrt{V_{\mathrm{BC}} + V_{\mathrm{bi}}}. \quad \text{(A24)}$$

12) **Injector collector/base sidewall depletion charge**

$$\Delta Q_{\mathrm{DCSI}} = q \cdot \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_s \cdot N_{\mathrm{IB}}}{q}} 2 \cdot W_{\mathrm{IB}} (x_3 + d) \cdot \Delta\sqrt{V_{\mathrm{BE}} + V_{\mathrm{bi}}}. \quad \text{(A25)}$$

13) **Switch collector/base sidewall depletion charge**

$$\Delta Q_{\mathrm{DCSS}} = q \cdot \sqrt{\frac{2 \cdot \varepsilon_o \cdot \varepsilon_s \cdot N_{\mathrm{SC}}}{q}} 2 \cdot W_{\mathrm{SC}} \cdot (x_5 + d) \cdot \Delta \sqrt{V_{\mathrm{BC}} + V_{\mathrm{bi}}}. \quad \text{(A26)}$$

The high-low junction that results if the substrate doping, N_{SUB}, is different from the switch emitter doping, N_{SE}, has been treated using a simplified version of the analysis presented by Dutton and Whittier [16] who define a blocking parameter, α, as:

$$\alpha = \frac{N_{\mathrm{SE}} \cdot D_{h\,\mathrm{SUB}} \cdot W_{\mathrm{SE}}}{N_{\mathrm{SUB}} \cdot D_{h\,\mathrm{SE}} \cdot L_{h\,\mathrm{SUB}}}. \quad \text{(A27)}$$

The parameter δ [see (A2)] is then written as

$$\delta = \frac{1}{1+\alpha}. \quad \text{(A28)}$$

Physically, this implies that for a larger switch emitter doping concentration ($N_{\mathrm{SE}} > N_{\mathrm{SUB}}$) that the junction is "collecting" and for a smaller switch emitter doping concentration ($N_{\mathrm{SE}} < N_{\mathrm{SUB}}$) that the junction is "reflecting."

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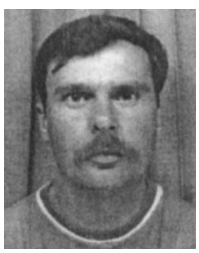
He then joined the lecturing staff, University of Liverpool, where he began work on SOI materials characterization and device physics and subsequently obtained funding to work in these areas on the SIMOX and oxidised porous Si systems, with U.K. university and industrial collaborators. Other areas of activity concerned fabrication and electrical assessment of cobalt disilicide Schottky diodes together with silicon-germanium materials characterization and device physics for bipolar transistor and MOSFET appplication. The SiGe work currently concerns high performance analogue bipolar and new forms of integrated injection logic with particular interest in modeling and associated materials characterization. Current SOI work is in the area of low voltage/low power integrated circuits which aims to address this topic from devices and technology through logic circuit styles to architectures and algorithms, in collaboration with other U.K. universities and industry.

Peter Ashburn (M'89) was born in Rotherham, U.K., in 1950. He received the B.Sc. degree in electrical and electronic engineering in 1971, and the Ph.D. degree in 1974, both from the University of Leeds, U.K. His dissertation topic was an experimental and theoretical study of radiation damage in silicon p-n junctions.

In 1974, he joined the technical staff of Philips Research Laboratories, Redhill, U.K., and worked initially on ion-implanted integrated circuit bipolar transistors, and then on electron lithography for submicron integrated circuits. In 1978, he joined the academic staff of the Department of Electronics and Computer Science, University of Southampton, Southampton, U.K., as a Lecturer. Currently, he is a Professor at the same university, where his present areas of research are npn and pnp polysilicon emitter bipolar transistors, Si/SiGe heterojunction bipolar transistors, high speed bipolar and BiCMOS processes, and silicon on insulator technology. He has authored and coauthored over 100 papers in the technical literature and has authored a book on bipolar transistors.



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