

# Determination of Bandgap Narrowing and Parasitic Energy Barriers in SiGe HBT's Integrated in a Bipolar Technology

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**Abstract**—This paper describes a method for characterizing the bandgap narrowing and parasitic energy barrier in SiGe heterojunction bipolar transistors (HBT's), fabricated using a single-polysilicon self-aligned bipolar process. From a comprehensive study of the temperature dependence of the collector current, the bandgap narrowing in the base due to germanium has been dissociated from that due to the heavy dopant concentration. The same approach has been used to characterize the height and width of parasitic energy barriers which appear when boron out-diffusion from the SiGe base is present. The method has been applied to SiGe heterojunction bipolar transistors fabricated using a single polysilicon, self aligned, bipolar process, as well as mesa transistors. The experimental results show that small geometry transistors have degraded collector currents due to boron out-diffusion around the perimeter of the emitter. This behavior has been explained by accelerated boron diffusion due to point defect generated during the extrinsic base implant. The values of undoped SiGe spacer thickness needed to suppress the parasitic energy barrier are described. Finally, high-frequency results are reported, which correlate the frequency transition to these parasitic energy barriers.

## I. INTRODUCTION

THE introduction of SiGe into the base of a Si bipolar transistor allows a significant enhancement of transistor performance. Thanks to the heterojunction effect, thin, heavily doped base can be used to reduce the transit time in the base without compromising the base resistance or the emitter injection efficiency [1], [2]. Over the last ten years, SiGe technology and heterojunction bipolar transistor (HBT) design has progressed considerably, and has reached the point of record cut-off frequencies above 100 GHz [3], [4] and record ECL gate delays down to 11 ps [5], [6].

Parallel with these developments in high-speed technology, there has also been interest in the development of BiCMOS processes for operation at liquid nitrogen temperature [7], [8]. The well known difficulty with the low-temperature operation of bipolar transistors is the exponential decrease in current gain with decreasing temperature. In a conventional Si bipolar transistor, this occurs because the band gap in the heavily doped emitter is smaller than that in the more lightly doped

base due to doping-induced bandgap narrowing. The SiGe HBT offers a solution to this problem because the introduction of SiGe into the base reduces the band gap in the base. In addition, a low-doped emitter is generally used in a SiGe HBT to separate the highly doped base from the highly doped emitter contact and hence avoid emitter/base tunnelling leakage. As a result, the doping-induced bandgap narrowing in the emitter of a SiGe HBT is generally less than that in a conventional Si bipolar transistor. These two features of the SiGe HBT make it possible to design devices with high values of gain, even at liquid nitrogen temperature.

The analysis of bipolar transistor behavior at low temperature is also important as a method of providing detailed understanding of the physics of device operation. Analysis of the base current as a function of temperature can highlight mechanisms responsible for leakage current [9] and analysis of the collector current can provide important information on the base doping profile. In an earlier paper [10], an analysis method was described for determining the apparent bandgap narrowing in the base of a Si homojunction or SiGe heterojunction bipolar transistor from the temperature dependence of the collector current. This method was shown to be highly sensitive to the presence of tails on the base doping profile, and hence would be well suited to the study of anomalous diffusion of boron in the very thin, highly doped bases that are needed for SiGe HBT's.

Boron out-diffusion from the base of a SiGe HBT can severely degrade the device performance due to the formation of parasitic energy barriers at the collector/base and emitter/base junctions [11]–[13]. Even very small amounts of out-diffusion (a few nanometers) from the SiGe base can dramatically degrade the collector current [14] and hence the current gain. Transient enhanced diffusion due to implantation-induced point defects has been shown to cause severe out-diffusion of boron when an emitter contact implant is included immediately above the SiGe base [15], [16]. Although this problem can be avoided by the use of a polysilicon emitter contact, similar transient enhanced diffusion phenomena may be seen due to the implantation of an extrinsic base contact [17], [18].

In this paper, the analysis method described earlier [10], [11], [13] are further developed to take into account out-diffusion from the heavily doped bases of SiGe HBT's. This modified analysis method is then used to study how the major processing variables influence the device electrical characteristics when a SiGe epitaxial base is inserted into an existing CMOS-derived, single polysilicon, self-aligned bipolar process. The analysis method is applied to transistors with

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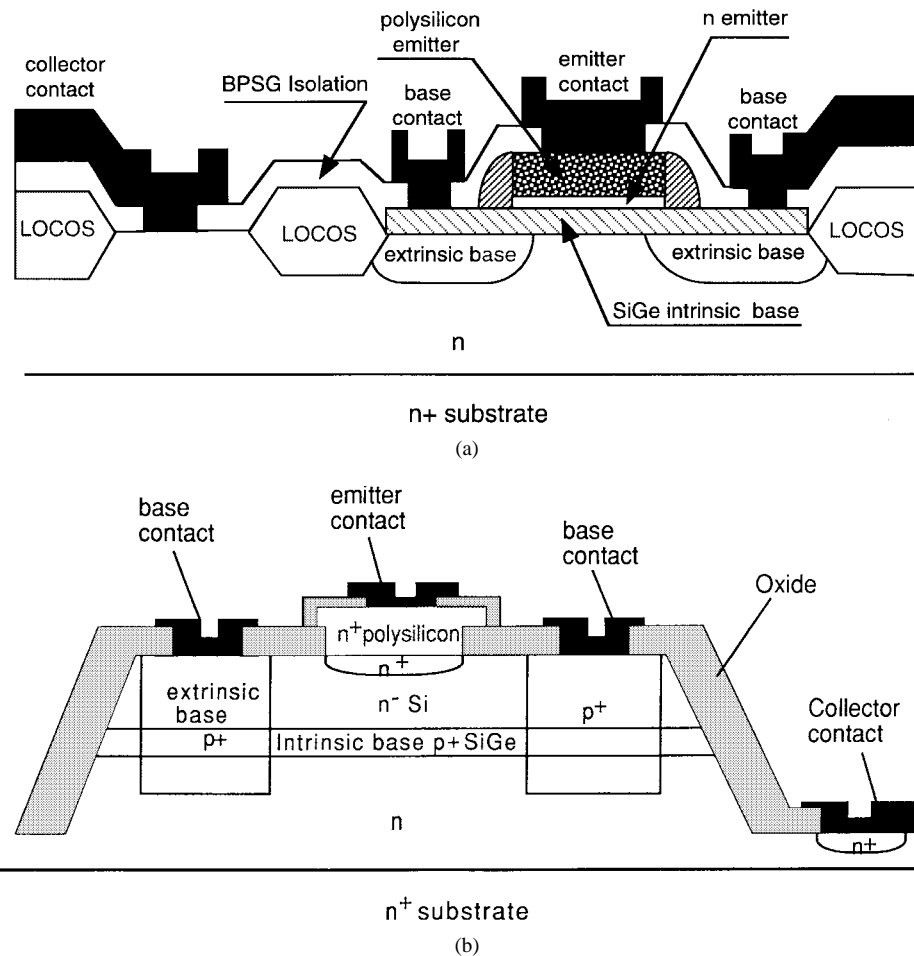


Fig. 1. Schematic cross section of (a) a LOCOS isolated and (b) a mesa-isolated HBT.

different emitter geometries, and the results obtained are used to study how the extrinsic base implant influences boron out-diffusion from the intrinsic SiGe base.

## II. DEVICE STRUCTURE AND TECHNOLOGY

The HBT structure under investigation was fabricated by inserting a  $\text{Si}_{1-x}\text{Ge}_x$  epitaxial layer, into an existing CMOS-derived, single-polysilicon, self-aligned bipolar process [9]. After the field oxide (LOCOS) isolation, and gate oxide removal, the  $\text{p}^+$  base and  $\text{n}^-$  emitter were grown using rapid thermal, chemical vapor deposition (RT-CVD). The basic targeted vertical stack consisted of a 300-Å thick,  $5 \cdot 10^{18} \text{ cm}^{-3}$  boron-doped  $\text{Si}_{0.92}\text{Ge}_{0.08}$  base, followed by a 1000-Å thick,  $10^{18} \text{ cm}^{-3}$  phosphorus-doped silicon emitter. To prevent boron out-diffusion, 100-Å or 50-Å thick undoped SiGe spacer layers were introduced on both sides of the doped SiGe base. The emitter was fabricated by depositing a polysilicon emitter and then etching through the polysilicon, the low-doped silicon emitter to produce the structure shown in Fig. 1(a). A link base was then produced using a 30 keV,  $1 \cdot 10^{13} \text{ cm}^{-2}$  boron implant, followed by the formation of sidewall spacers using PECVD  $\text{SiO}_2$ . The extrinsic base was fabricated using a 10 keV,  $8 \cdot 10^{14} \text{ cm}^{-2}$  boron implant and was self-aligned to the etched polysilicon emitter, as shown in Fig. 1(a). The thermal budget used in the process consisted of a dopant activation

anneal at 800 °C for 20 min after polysilicon implantation and a rapid thermal anneal at 900 °C for 20 s before contacts and metallization.

For comparison purposes, mesa transistors were also fabricated using a previously described process [19]. In this case, the extrinsic base was fabricated using a dual implant of 35 keV,  $2 \cdot 10^{15} \text{ cm}^{-2} \text{BF}_2$ , and 120 keV,  $2 \cdot 10^{15} \text{ cm}^{-2} \text{B}$  into the low-doped silicon emitter to produce the structure shown in Fig. 1(b). The thermal budget used in this process was a rapid thermal anneal at 900 °C for 30 s. Some of the epitaxial layers for the mesa transistors were grown under the same conditions as those for the LOCOS transistors, while others were grown under different conditions. Full details of the epitaxial layers for both the LOCOS and mesa transistors are given in Table I.

Some of the electrical measurements were performed on large geometry devices (up to  $100 \times 100 \mu\text{m}^2$ ), in order to characterize the intrinsic transistor only, and to eliminate edge effects and technological problems linked to small geometry devices. The values of base doping concentration, undoped SiGe spacer width and emitter dimensions are summarized in Table I, for both types of device.

## III. THE ANALYSIS METHOD

This analysis method gives the bandgap narrowing in the base from the temperature dependence of the collector current. For a constant and uniform Si base doping, the collector

TABLE I  
TECHNOLOGICAL PARAMETERS FOR LOCOS AND MESA-ISOLATED TRANSISTORS

Transistor	Isolation type	Base doping cm <sup>-3</sup>	Spacer thickness Å	Ge content %	Emitter width*length μm*μm
T1	LOCOS	5.10 <sup>18</sup>	100	8	100*100
T2	LOCOS	5.10 <sup>18</sup>	50	8	100*100
T3	LOCOS	5.10 <sup>18</sup>	100	8	1.4*10
T5	mesa	6.10 <sup>18</sup>	50	16	66*66
T6	mesa	5.10 <sup>18</sup>	150	16	66*66
T7	mesa	6.10 <sup>18</sup>	50	16	(9)*22*22
T8	mesa	5.10 <sup>18</sup>	150	16	(9)*22*22

current density can be expressed as [10]

$$J_{C(\text{Si})}(T) = \frac{kTn_{i0}^2\mu_{nB}(T)}{W_B(T) \cdot p(T)} \exp \frac{\Delta E_{gB}}{kT} \exp \frac{qV_{BE}}{kT} \quad (1)$$

where  $k$  is the Boltzmann constant,  $T$  the temperature,  $\mu_{nB}(T)$  the minority carrier electron mobility in the base given by the Klaassen model [20],  $\Delta E_{gB}$  the bandgap narrowing in the base induced by high doping effects, and  $V_{BE}$  the base-emitter voltage.

The temperature dependence of the intrinsic carrier concentration for undoped silicon,  $n_{i0}(T)$ , is given by the following expression:

$$n_{i0}^2(T) = 4 \left( \frac{2\pi k}{h^2} \right)^3 (m_n m_p)^{3/2} T^3 \exp \frac{-E_G(T)}{kT} \quad (2)$$

where  $m_n$  and  $m_p$  are the effective masses for electrons,  $1.08m_o$ , and for holes,  $0.97m_o$  [21]. The silicon bandgap variation with temperature  $E_G(T)$  is described by the Thurmond model [22]. The product of the neutral base width  $W_B$  with the free carrier concentration in the base  $p$ , can vary with temperature as a result of freeze-out of carriers in the base. This can be measured from the temperature variation of the intrinsic base sheet resistance  $R_B(T)$

$$W_B(T) \cdot p(T) = \frac{1}{q\mu_{pB}R_B(T)} \quad (3)$$

where  $\mu_{pB}(T)$  is the majority carrier mobility in the base, given by the Klaassen model [20].

If the Si base is replaced by a SiGe base, the collector current expression (1) becomes

$$J_{C(\text{SiGe})}(T) = J_{C(\text{Si})}(T) \frac{NcNv(\text{SiGe})}{NcNv(\text{Si})}(T) \cdot \frac{\mu_{nB(\text{SiGe})}(T)}{\mu_{nB(\text{Si})}(T)} \exp \frac{\Delta E_G}{kT} \quad (4)$$

where  $\Delta E_G$  is the bandgap narrowing in the base due to the presence of the germanium. There is little data in the literature concerning the effective density of states and the carrier mobilities in SiGe. In this article, we have used the data of Manku and Poortmans [23], [24]. The density of states ratio has a value of 0.3 for 8% Ge at 300 K, and  $\mu_{nB}(\text{SiGe}) = 1.3 \mu_{nB}(\text{Si})$ . There is no data concerning majority carrier mobility  $\mu_{pB}(T)$  in SiGe so it has been assumed that it is the same as that in Si.

A factor  $C_{(\text{SiGe})}$  can be defined to take the SiGe alloy into account, which is expressed as

$$C_{(\text{SiGe})} = \frac{NcNv(\text{SiGe})(T)}{NcNv(\text{Si})(T)} \frac{\mu_{nB(\text{SiGe})}(T)}{\mu_{nB(\text{Si})}(T)} = 0.39 \text{ for } 8\% \text{Ge and } 0.21 \text{ for } 16\% \text{Ge.} \quad (5)$$

This factor  $C$  is assumed not to vary strongly with temperature and will be considered as a constant in the following analysis.

Combining (1)–(5), we can describe the temperature dependence of the collector current density for a SiGe HBT as follows:

$$\frac{J_{C(\text{SiGe})}(T)}{J_0(T)} = \exp \frac{\Delta E_G + \Delta E_{gB}}{kT} \quad (6)$$

where

$$J_0(T) = C_{(\text{SiGe})} 4q \left( \frac{2\pi}{h^2} \right)^3 (m_n m_p)^{3/2} (kT)^4 \mu_{nB(\text{Si})}(T) \mu_{pB(\text{Si})}(T) R_B(T) \exp \frac{qV_{BE} - E_G(T)}{kT} \quad (7)$$

$J_0(T)$  can be determined by measuring the intrinsic base sheet resistance  $R_B(T)$  for several temperatures, and by using the described models for the temperature dependences of the mobilities and the silicon bandgap. The mobilities are calculated at the mean base doping level, which is determined in an iterative way by fitting to the measured intrinsic base sheet resistance. Then, the total bandgap narrowing  $\Delta E_G + \Delta E_{gB}$  can be obtained from the slope of a graph of  $\ln(J_{C(\text{SiGe})}(T)/J_0(T))$  versus the reciprocal temperature. We can notice that the intercept with the vertical axis should be equal to unity.

## IV. RESULTS AND DISCUSSION

### A. Effect of the Undoped SiGe Spacer Thickness

The SIMS doping profiles for a typical SiGe HBT analyzed in this paper are shown in Fig. 2. The as-grown  $\text{Si}_{0.92}\text{Ge}_{0.08}$  base was 550 Å thick, with a boron doping concentration of  $5.10^{18} \text{ cm}^{-3}$ , and was bounded by 100-Å thick undoped SiGe spacer layers (transistor T1 in Table I). After processing, and mostly due to the non negligible thermal budget used in the device processing, the mean calculated base doping concentration became  $1.7 \cdot 10^{18} \text{ cm}^{-3}$  for a measured metallurgical base width of 900 Å. It can be noticed however that the base profile remains rather abrupt and hence the assumption of uniform doping in the analysis method is reasonable.

Fig. 3 shows graphs of  $J_{C(\text{SiGe})}(T)$  versus reciprocal temperature (band gap narrowing plot) for a large geometry LOCOS transistor with an undoped SiGe spacer layer of 100 Å (transistor T1). The  $I_C(V_{BE})$  characteristics were measured at temperatures between 340 K and 40 K and found to be ideal over the whole temperature range. The characteristic shown in Fig. 3 is extremely linear and the extracted slope gives a value for the total band gap narrowing in the base ( $\Delta E_G + \Delta E_{gB}$ ) of 109 meV. Measurements were also made on a comparable Si bipolar transistor with 0% Ge in the base, in order to determine the band gap narrowing in the base in the absence of Ge (the so-called doping-induced band gap narrowing). For a transistor having a 1050-Å thick Si base, with a mean base doping concentration of  $2 \cdot 10^{18} \text{ cm}^{-3}$ , a doping-induced bandgap narrowing in the base  $\Delta E_{gB}$  of 39

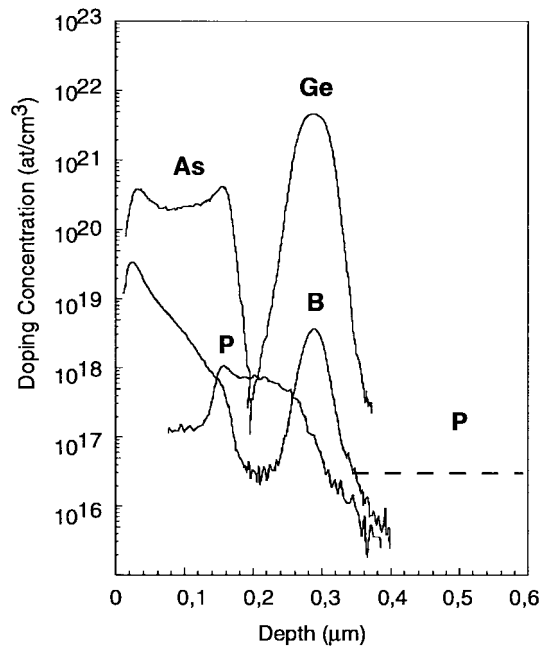


Fig. 2. SIMS doping profile of a 300-Å thick,  $5.10^{18} \text{ cm}^{-3}$  boron-doped  $\text{Si}_{0.92}\text{Ge}_{0.08}$  base, bounded by 100-Å thick undoped SiGe spacer layers (transistor T1).

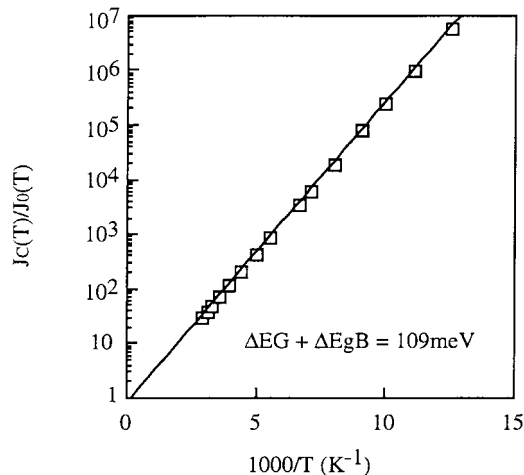


Fig. 3.  $J_C/J_0$  versus  $(1/T)$  characteristic for a typical LOCOS isolated  $\text{Si}_{0.92}\text{Ge}_{0.08}$  HBT (transistor T1, 100-Å spacers) in the 340 K–80 K temperature range. The extracted slope (total bandgap narrowing in the base) and intercept are 109 meV and 0.9.

meV was measured [25] which is also the expected value from literature [26]. Subtracting this value from the total band gap narrowing in the base, gives a band gap narrowing of 70 meV due to 8% Ge. This result is in reasonable agreement with the theoretical values of 75 meV [27] and 74 meV [28], given in the literature. The value of intercept in Fig. 3 is 0.9, which compare well with the expected value of 1.0. This demonstrates that the theoretical models and chosen constants are good and that the temperature measurements are well controlled. On a similar transistor, with a mesa structure, we obtained the same band gap narrowing (109 meV), and an intercept of 0.8.

Fig. 4 shows a bandgap narrowing plot for a large geometry LOCOS transistor (T2), with a thinner undoped SiGe spacer

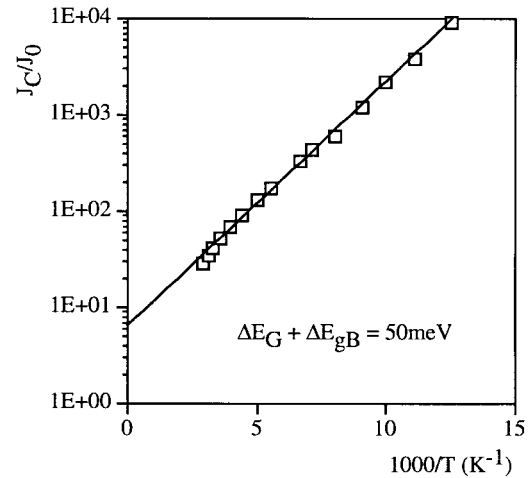


Fig. 4.  $J_C/J_0$  versus  $(1/T)$  characteristic of the LOCOS isolated  $\text{Si}_{0.92}\text{Ge}_{0.08}$  HBT (transistor T2, 50-Å spacers), for the 340 K–80 K temperature range. The measured slope equals 50 meV and the intercept 7.

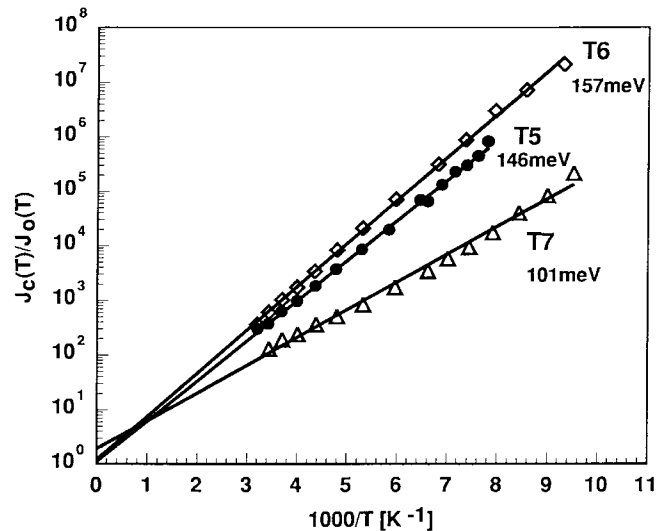


Fig. 5.  $J_C/J_0$  versus  $(1/T)$  characteristic of the mesa-isolated  $\text{Si}_{0.84}\text{Ge}_{0.16}$  HBT's T5 (50-Å spacers), T6 (100-Å spacers) and T7 (50-Å spacers, long perimeter), for the 340 K–80 K temperature range.

of 50 Å (instead of 100 Å on Fig. 3). On the  $I_C(V_{BE})$  characteristic, we measured a non ideality which appeared for temperatures lower than 225 K and a significant leakage current for temperature below 180 K. When we plot the  $J_C/J_0$  versus  $1/T$  characteristic for this sample (Fig. 4), the characteristic is less linear than that shown in Fig. 3, with the slope at high temperatures being higher than that at low temperatures. The measured slope of 50 meV is much lower than that observed in Fig. 3 and the intercept diverges from the expected value of unity to a value of 7. Earlier work [10] has shown that non linear characteristics can be indicative of the presence of a tail on the base doping profile, and that in this case the slope of the characteristic at high temperature gives a more reliable value for the band gap narrowing. If the data for  $1000/T < 5 \text{ K}^{-1}$  is taken in Fig. 4, the slope increases to 60 meV and the intercept decreases to 3.8. These values are still considerably different than those seen in Fig. 3.

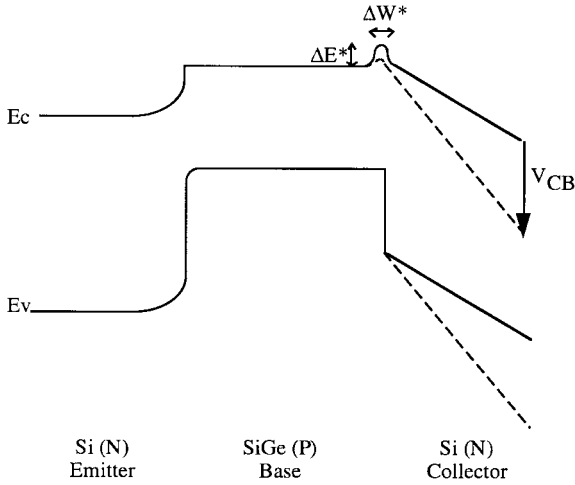


Fig. 6. Schematic band diagram showing the base-collector parasitic barrier dimensions (its width  $\Delta W^*$ , and its height  $\Delta E^*$ ), as well as the effect of the base-collector junction reverse bias on the parasitic barrier.

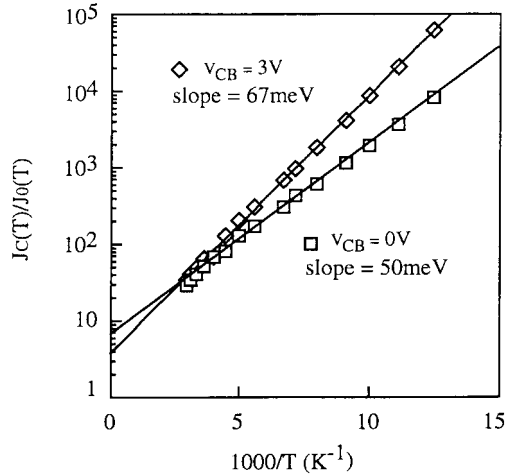


Fig. 7.  $J_C/J_0$  versus  $(1/T)$  characteristic showing the effect of a collector-base reverse bias for the LOCOS isolated  $\text{Si}_{0.92}\text{Ge}_{0.08}$  HBT T2 (50-Å spacers), for the 340 K–80 K temperature range. The measured slope equals 50 meV at  $V_{BC} = 0$  V and 67 meV at  $V_{BC} = 3$  V.

Similar behavior is also observed on mesa devices, as illustrated on the bandgap narrowing plots in Fig. 5. The slope of 146 meV obtained for the  $\text{Si}/\text{Si}_{0.84}\text{Ge}_{0.16}$  HBT with a 50-Å undoped SiGe spacer (transistor T5) is less than the slope of 157 meV obtained for the device with a 150-Å spacer (transistor T6). Also shown for comparison is the characteristic of a transistor (T7) with the same area as transistor T5, but a longer perimeter. In this case, a slope of 101 meV is obtained, which is significantly less than the value of 146 meV obtained for transistor T5. The results in Figs. 4 and 5 show anomalous behavior on both LOCOS and mesa devices when the undoped SiGe spacer is very thin. This suggests that the explanation for the anomalous behavior may be out-diffusion of boron from the SiGe base, which leads to the formation of parasitic energy barriers at the emitter/base and collector/base junctions [11]–[13], and consequently to a reduction of the collector current. The perimeter dependence of the slope seen in Fig. 5 suggests that the out-diffusion is greater around the perimeter of the emitter than in the centre.

A simple way to highlight the existence of a parasitic energy barrier at the base-collector junction, is to reverse bias the base-collector junction, in order to widen the depletion layer and to reduce the barrier height, as illustrated schematically in Fig. 6. If we now plot the  $J_C/J_0$  versus  $1/T$  characteristic for a 3 V reverse bias, as shown in Fig. 7, we see that the slope increases to 67 meV, and becomes closer to the expected bandgap narrowing of 109 meV. In addition the intercept decreases to 1.5 and becomes closer to the expected value of unity. These results confirm the existence of a parasitic barrier at the base-collector junction.

The Slotboom parasitic energy barrier model [13], [28] can be adapted to obtain an expression for the collector current density as a function of the barrier characteristics. If a barrier width  $\Delta W^*$  and a barrier height  $\Delta E^*$  are defined (Fig. 6), then the  $\exp(qV_{BE}/kT)$  term in (6) can be replaced by a term

$$\frac{\exp\left(\frac{qV_{BE}}{kT}\right)}{1 + \left(\frac{\Delta W^*}{W_B}\right) * \left(\exp\left(\frac{\Delta E^*}{kT}\right) - 1\right)}.$$

For a large barrier ( $\Delta E^* \gg kT$ ),  $J_C/J_0$  can be approximated by

$$\frac{J_C}{J_0} \approx \frac{W_B}{\Delta W^*} \exp\left(\frac{\Delta E_G + \Delta E_{gB} - \Delta E^*}{kT}\right).$$

In this case, the slope of a graph of  $\ln(J_C/J_0)$  versus  $1/T$  gives  $\Delta E_G + \Delta E_{gB} - \Delta E^*$  and the intercept gives  $W_B/\Delta W^*$ . We can estimate the width and height of the parasitic energy barrier in transistor T2 (with 50-Å spacers) if we assume that the measurement on transistor T1 (with 100-Å spacers) gives a value of  $\Delta E_G + \Delta E_{gB}$ . In this case, the barrier height  $\Delta E^*$  can be obtained by subtracting the slope of 50 meV in Fig. 4 from the value of 109 meV in Fig. 3 to give 58 meV. Similarly, the barrier width  $\Delta W^*$  can be obtained from the intercept in Fig. 4 (7.0) and the measured base width (1100 Å) to give 150 Å. These are reasonable and realistic values, considering that the barrier height should be lower than the band gap difference between silicon and the SiGe alloy ( $\Delta E_G = 70$  meV).

It is much more difficult to characterize the effect of the parasitic energy barrier at the emitter base junction. Reversing the emitter and collector role and operating the transistor in the inverse active mode is not conclusive; the collector is the n-on-n<sup>+</sup> wafer substrate and parasitic currents originating in the extrinsic regions disturb the collected current in the emitter. Another possible approach would be to use the conclusions of Gruhle [29] who showed that the collector current ideality factor was sensitive to the presence of parasitic energy barriers at the emitter-base junction. This ideality factor  $\eta$  can be introduced into the analysis method by replacing the  $(qV_{BE}/kT)$  term in (7) by  $(qV_{BE}/\eta kT)$ . The ideality factor  $\eta$  has been carefully measured on  $I_c(V_{BE})$  characteristics, for each temperature, with a precision better than 1%. Fig. 8 shows the corrected characteristic for the 340 K–125 K temperature range and zero collector/base voltage. In this case, we obtain a slope of 103 meV, which is very close to the expected value of 109 meV.

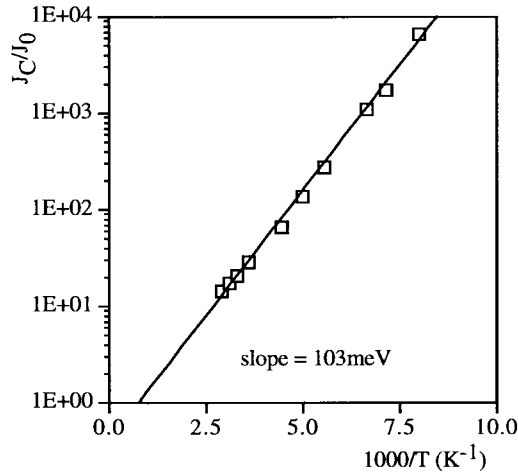


Fig. 8.  $J_C/J_0$  versus  $(1/T)$  characteristic of the LOCOS isolated  $\text{Si}_{0.92}\text{Ge}_{0.08}$  HBT T2, corrected for the nonideality, for the 340 K–125 K temperature range.

### B. Small Geometry Effects: Transient Enhanced Base Diffusion

So far, we have only tested large area transistors ( $A = 100 \times 100$  or  $66 \times 66 \mu\text{m}^2$ ). In this section, we analyze a small geometry transistor (Transistor T3,  $A = 1.4 \times 10 \mu\text{m}^2$ ), originating from the same chip as the large geometry transistor T1, with doping profiles shown on Fig. 2. Consequently, we can assume that the doping profiles of the two devices are the same.

Fig. 9 shows a band gap narrowing plot for transistor T3, measured at zero collector/base voltage. The measured slope of 45 meV is much lower than the expected value of 109 meV extracted previously in Fig. 3 on the large geometry transistor. This indicates that the boron out-diffusion from the SiGe base is greater in small geometry devices, and implies a perimeter dependence to the out-diffusion. When we reverse bias the base-collector junction, the slope increases to 58 meV for a 2 V bias, and to 72 meV for a 4 V reverse bias (Fig. 9). We conclude therefore that, at zero collector/base voltage, a base-collector parasitic barrier is present in the small geometry devices with a height  $\Delta E^*$  estimated at 63 meV and a width  $\Delta W^*$  at 250 Å using the previously described method.

The results on LOCOS devices in Fig. 9, taken together with the results on mesa devices in Fig. 5, indicate that the boron out-diffusion from the SiGe base is greater around the perimeter of the emitter than in the centre. In both types of device, an extrinsic base implant is carried out immediately adjacent to the active emitter area. The above results could therefore be explained by transient enhanced diffusion of the boron around the perimeter of the emitter due to point defects created during the extrinsic base implantation. The results suggest that, in small geometry devices, these point defects are able to migrate across the whole of the intrinsic base and cause enhanced boron out-diffusion across the whole area of the emitter. In large geometry devices, however, the point defects are unable to migrate as far as the centre of the intrinsic base, and hence enhanced boron out-diffusion is only obtained around the perimeter of the emitter. Similar transient enhanced diffusion has been observed in silicon bipolar transistors when an ion implanted emitter contact was introduced above a buried

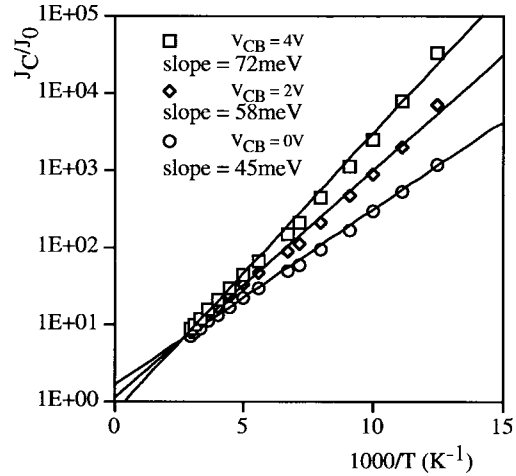


Fig. 9.  $J_C/J_0$  versus  $(1/T)$  showing the effect of a collector-base reverse bias, for a small geometry LOCOS isolated  $\text{Si}_{0.92}\text{Ge}_{0.08}$  HBT T3 (Table I), for the 340 K–80 K temperature range. The measured slope equals 45 meV at  $V_{BC} = 0$  V, 58 meV at  $V_{BC} = 2$  V and 72 meV at  $V_{BC} = 4$  V.

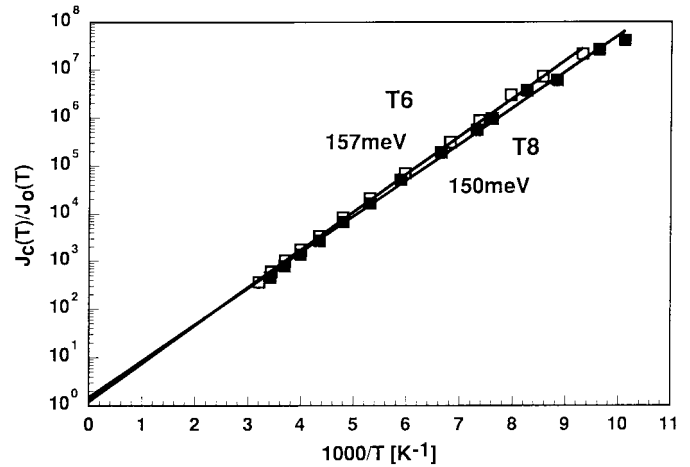


Fig. 10.  $J_C(T)/J_0(T)$  versus  $(1/T)$  characteristic for the mesa-isolated  $\text{Si}_{0.84}\text{Ge}_{0.16}$  HBT's T6 (150-Å spacers) and T8 (150-Å spacers, longer perimeter).

Si epitaxial base [15], [16]. In this case, point defects generated by the emitter implant dramatically enhanced the diffusivity of the boron in the underlying base.

The results presented in this paper clearly demonstrate the hazards of using ion implantation in the fabrication of SiGe HBT's. The question posed by these results is whether ion implantation should be completely avoided in SiGe processes. In order to address this question, mesa devices were fabricated with thicker undoped SiGe spacers in an attempt to eliminate the parasitic energy barriers around the perimeter of the emitter. The resulting bandgap narrowing plots are shown in Fig. 10 for HBT's with 150-Å spacers and for zero collector/base voltage. A slope of 157 meV is obtained for the device with a short perimeter, and 150 meV for the device with a long perimeter. On the application of a 5 V reverse bias to modulate any residual potential barrier at the collector/base junction, these slopes increased to 159 meV and 156 meV, respectively. It can therefore be concluded that increasing the spacer thickness to 150 Å has eliminated the majority of the parasitic energy barrier at the perimeter of the emitter, as can be seen by comparing the slope of 101 meV in Fig. 5 with

the slope of 150 meV in Fig. 10. However a small residual energy barrier may still be present, even for a spacer thickness of 150 Å, as can be seen from the increase in slope from 150 to 156 meV on the application of a reverse collector bias. These results demonstrate that a careful choice of undoped SiGe spacer thickness must be made when an ion implanted extrinsic base is incorporated into a SiGe HBT process.

As small geometry devices are used in high-frequency circuits, the previous results are of great importance. We have tried to correlate the existence of parasitic barriers to the dynamic performance, in particular, to the cut-off frequency. For the 900-Å thick,  $2.10^{18}$  cm<sup>-3</sup> boron-doped transistor, we have estimated a transit time in the base,  $\tau_B$ , of 6.3 ps, leading to a cut-off frequency,  $f_T$ , of 19.4 GHz (this simple calculation does not consider the extrinsic elements). The Slotboom model [13] gives an expression of the base transit time  $\tau_B^*$  in the presence of barriers

$$\frac{\tau_B^*}{\tau_B} \approx 1 + 2 \frac{\Delta W^*}{W_B} \left( 1 - \frac{\Delta W^*}{W_B} \right) \left( \exp \frac{\Delta E^*}{kT} - 1 \right).$$

If we use the measured barrier characteristics with the previously calculated base transit time  $\tau_B$ , we can estimate a new base transit time  $\tau_B^*$  of 32.6 ps, and a drop of the cut-off frequency to 4.6 GHz. We have measured on equivalent devices a cut-off frequency of approximately 6.3 GHz, which is much lower than to the original estimate of 19.4 GHz, and comparable to the value of 4.6 GHz obtained by taking into account parasitic barriers.

## V. CONCLUSION

We have presented an analysis method for measuring the bandgap narrowing in the SiGe base of heterojunction bipolar transistors from the temperature dependence of the collector current. This method has been shown to be very accurate, and has been applied to LOCOS isolated, self aligned transistors, as well as mesa transistors. We have dissociated the bandgap narrowing contribution of the germanium from that of high doping effects. The values obtained are very comparable with the theoretical results given by the literature.

The application of this method to HBT's with thinner undoped SiGe spacers and to small-geometry devices has highlighted the formation of parasitic potential barriers around the perimeter of the emitter. The analysis method has been used to calculate the heights and widths of these energy barriers. The formation of the energy barriers has been explained by boron out-diffusion from the SiGe base due to point defects.

Results on devices with thicker spacers indicate that the parasitic energy barriers generated during the implantation of the extrinsic base can be suppressed by a suitable choice of spacer thickness. In order to avoid a degradation of collector current and cut-off frequencies, the thickness of the SiGe base and undoped SiGe spacer (critical layer thickness) must be carefully optimized to be compatible with the use of an ion implanted extrinsic base.

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