Testing Analog Circuits by Supply Voltage Variation and Supply Current Monitoring

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Abstract

A technique for sensitizing faults in analog circuits by varying the supply voltage is discussed. Unlike previous work, the technique is applied to the detection of short circuit faults. The validity of the technique is demonstrated with a simple CMOS circuit. The technique is applied to a larger analog circuit and significantly improved fault cover results are obtained.

Introduction

Testing of digital circuits has traditionally been based on the single-stuck fault model (although, of course, other fault models have been used). Test pattern generation algorithms based on this model attempt to force the node under consideration to the value opposite to that at which it might be stuck. The principle of *toggle testing* was proposed in which each node of a circuit is toggled between logic 0 and logic 1. IDDQ testing refined this idea such that the nodes of a circuit are switched to a logic value and under fault-free conditions the quiescent current is ideally negligible. Underlying all these techniques is the idea that individual transistors can be switched between conducting and non-conducting states.

Analog circuit testing, on the other hand, is much less structured. It is generally accepted that faults in analog circuits can be characterized by open and short circuits. The effects of such faults can be observed through the output voltages and supply currents, using DC, AC and other computed values and determining the deviation of such values from the nominal values. These measurements are made more difficult by the fact that parametric variations may cause the behavior of fault-free circuits to deviate significantly from nominal values. Hence the effect of a fault may be masked by its falling within the normal range.

In a manner analogous to that of digital circuits, the testability of analog circuits could theoretically be much improved if it were possible to cause transistors in the circuit to switch between different regions of operation. Under normal operating conditions, most of the transistors in a CMOS analog circuit are likely to be in saturation. If it were possible to switch some or all of the transistors to operate in the cutoff or triode regions, the difference between the fault-free and faulty behaviors would be likely to be very marked.

It is possible to incorporate Design for Test structures that would give greater control over an analog block, but it is likely that such structures would be as complex as the original circuit.

Some control over the behavior of transistors within an analog circuit can be achieved by varying the supply voltage in conjunction with the inputs. Bruls used this idea to test a class AB amplifier at various supply voltage levels (1). He used the inductive fault analysis technique to insert processing defects into the layout of the IC in a random manner. A.K.B. A'ain, A.H.Bratt and A.P. Dorey applied a ramped power supply voltage to test small opamp circuits, and for exposing floating gate defects in analog CMOS circuits (2,3). The same authors applied an AC supply voltage to analog CMOS circuits (4). They achieved high fault covers with these tests, although the sizes of the circuits and the numbers of faults were small.

In this paper we show how varying the supply voltage of an analog circuit block can increase the fault cover of that block. Unlike the work described previously, we use a larger circuit element – a phase locked loop – and we model short circuit faults, which are much more likely to occur than open faults.

Transistor Switching

A typical, if simple, analog CMOS circuit is shown in Fig. 1. Under normal operating conditions, all of the transistors are in saturation all of the time. Therefore the quiescent current is naturally large (e.g. 300μA). Hence the fault cover obtained by simply measuring the DC supply current is low. Other supply current measurements – the RMS value of the AC component and transient measurements can give a significantly higher fault cover, but such measurements must take into account the process parameter variations, which can make the distinguishing of faulty from fault-free behavior difficult.

When the opamp circuit of Fig. 1 is connected as an inverting amplifier, and operating linearly, all the transistors are in the saturation region, as noted. As the amplitude of the input is increased, various transistors start to operate in the MOS linear region. In particular as the input (in1) becomes more positive, M7 and M4 operate in the linear region. Similarly
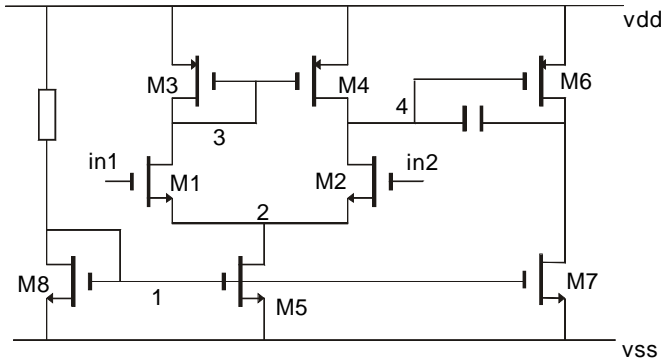
Figure 1 CMOS Opamp Circuit

Figure 2 Phased-Locked Loop

as in1 becomes more negative, M6 operates in the linear region. With still larger negative amplitudes, M2 also starts to operate in the linear region. Finally with a very large negative input, both M6 and M2 move into the cutoff region.

The same effect can be achieved by varying the supply voltage. If VDD is reduced from the normal operating range of 5V to 4V or even 3V, M7 and M4 operate in the linear region and M6 can be forced into the cutoff region. A similar, but less pronounced effect can be achieved by varying VSS. Under these conditions, the opamp is itself in saturation. Hence the supply current is also saturated.

Under fault conditions, the advantages of varying the supply voltage become much more marked. A short circuit between the gate and drain of M4 was modeled by a 100Ω resistance between nodes 3 and 4. With this fault, the opamp does not amplify nor invert – the output tracks the input, albeit with an offset of about 0.3V. With a low-frequency sinusoidal input with amplitude 0.3 V, the DC current was found to be 291µA with an AC ripple of 500nA amplitude. The fault-free DC current was 288µA with an 35µA AC component. Even in the presence of the fault, all the transistors continued to operate in the saturation region. This fault cannot be considered detectable if only the DC current were to be measured, but an RMS measurement of the AC component is probably sufficient.

When the input amplitude was increased to 2.0V, transistors M1 and M2 were forced into cutoff for part of the cycle, but the DC current remained almost unchanged at 292µA. Again this is not significantly different from the fault-free case. The AC component had an amplitude of 3µA. The apparently equivalent technique of varying the supply voltage had a much more significant effect. With the supply voltage, VDD at 3V and an input stimulus of 0.4V amplitude, again M1 and M2 operate for part of the time in cutoff, but now the DC current is 221µA, which is over 20% below the fault-free value and the fault must therefore be considered detectable.

It can therefore be seen that the basic hypothesis that causing transistors to switch between regions of operation is likely to increase the fault coverage is valid. This can be achieved by applying large input signals or by varying the supply voltage.
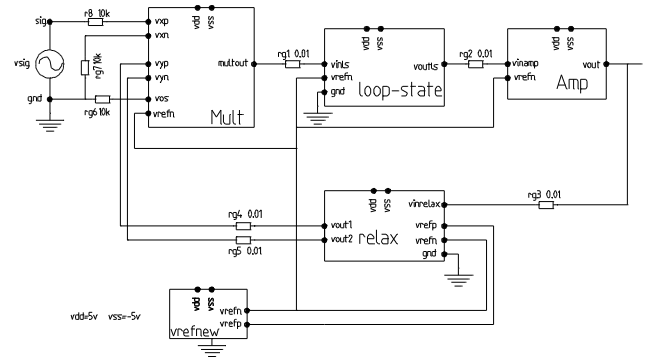
In this example, varying the supply voltage had a much more significant effect than simply increasing the input signal amplitude.

The remainder of this paper is concerned with the application of this technique to a larger circuit.

Variable Supply Voltage Testing
A CMOS Phase-Locked Loop, Fig. 2, was used to test the application of the technique to a larger circuit. The circuit was designed using the MIETEC 2.4µm CMOS technology. The repeated insertion of circuit faults by hand is tedious, so the ANTICS fault simulator was used to inject faults into a SPICE netlist and to analyse the simulation results (5). Gate-source and gate-drain short fault models only were used. This is distinct from the open-gate fault model used in previously reported work. The total number of faults injected was 190, of which 28 were redundant (the short circuits already existed as part of the circuit configuration) and 33 were equivalent (the same inter-nodal short was injected at two separate transistors) Hence, 129 distinct faults were simulated. Monte Carlo simulations were performed for each of these 129 faults and the RMS value of the AC component of the supply current and the DC supply current were measured. The PLL was simulated as a whole, thus the input stimulus was a sinusoidal input within the locking frequency range.

The fault cover was then evaluated such that a fault was considered detectable if the 3σ points of the faulty and fault-free current distributions did not overlap. This separation or gap between two distributions is defined in (6) as:

$$gap = \left(\mu_f - 3\sigma_f\right) - \left(\mu + 3\sigma\right) \quad (1)$$

where μ_f is the mean value of the faulty circuit response and μ is the mean value of the fault-free circuit response.
The fault covers were evaluated at different supply voltages using the DC and AC RMS values individually and combined.

A. VDD Change for whole PLL

Table I shows the fault cover for the PLL as the supply voltage was varied between 4.0V and 5.3V. As can be seen from Table 1, the fault cover changes very little for different supply voltages. The three figures given for each supply voltage value are the fault covers found by measuring the RMS value of the AC component of the supply voltage; the DC supply and the cumulative total of the two measures. A number of faults are detected by both measurements, which is why the sum is only around 10% higher than the RMS value alone.

Table II shows the cover obtained by combining two or more of the tests from Table I. All three given figures are fractionally above those of Table I. This means that a large common subset of faults is found by all the tests, with a small number of extra faults found by each test individually.

In other words, it appears that very few faults are sensitized, with respect to the supply current, by varying the supply voltage of the PLL as a whole.

B. Change in VDD of one subcircuit

Most of the undetected faults occured within the VCO, (relax in Fig. 2) therefore the exercise was repeated, with the supply voltage of the VCO subcircuit being changed to 4.5V while the supply voltage of the other subcircuits was held at 5.0V. The combined fault covers of this test and the previous tests are shown in Table III. The DC fault cover quoted here is that obtained using the first VDD value in the table. The cumulative totals for the single DC test and the two or three AC supply current tests are given.
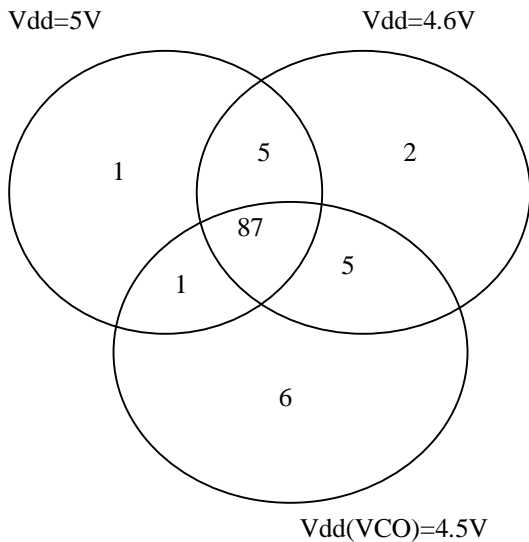
Figure 3 Venn diagram of fault covers of different tests.

Fig. 3 shows a Venn diagram for the fourth test in Table III. Again, it can be seen that most faults are detectable by all three tests. Six extra faults are detected by changing only the supply voltage of the VCO. While this only increases the overall fault cover by around 4%, these faults would not otherwise be detectable. Note that for all these tests the PLL continued to work as a PLL. (To be precise, for VDD=5V, and a 1MHz input sinusoid of 2V amplitude, the output of VCO is a square wave that varies between +1.96V and -2.3V, for VDD 4.5V and the same input the output value varies between +1.52V and -2.3V.)

C. VSS Change

Even by changing the supply voltage for just the VCO, a number of faults remained undetected. In addition, therefore VSS of the VCO was changed. Now, for VSS=-4.7V (instead of -5.0V) the fault coverage was 66% compared with a fault cover of 70% when VDD=4.7. Therefore monitoring the current from VSS seems to be better in terms of fault coverage.

For various VSS values of the VCO part (-4.6V, -4.65V, -4.7V, -4.75V, -4.8V) it was still not possible to detect any of those faults that couldn't be detected before.

TABLE I PLL FAULT COVER FOR VARYING SUPPLY VOLTAGE

VDD [V]	Fault Cover [%] RMS	Fault Cover [%] DC	Fault Cover [%] RMS + DC
5.3	67	38	74
5.0	64	40	73
4.8	67	39	77
4.7	69	39	77
4.6	68	44	77
4.5	67	40	77
4.0	65	41	76

TABLE II PLL FAULT COVER FOR COMBINED TESTS

Multiple VDDs [V]	Fault Coverage [%] RMS + DC
5 + 4.7 + 4.6	79
5.3 + 4.8 + 4.7 + 4.6	80
4.6 + 4.7	78

TABLE III CUMULATIVE FAULT COVER WITH VDD VARIED FOR ONE SUBCIRCUIT.

Multiple VDD [V]	Fault Cover [%] RMS + DC
5 + 4.7 + 4.6 + 4.5(VCO)	81
5.3 + 4.8 + 4.7 + 4.6 + 4.5(VCO)	82
4.6 + 4.7 + 4.5(VCO)	80
5 + 4.6 + 4.5(VCO)	83
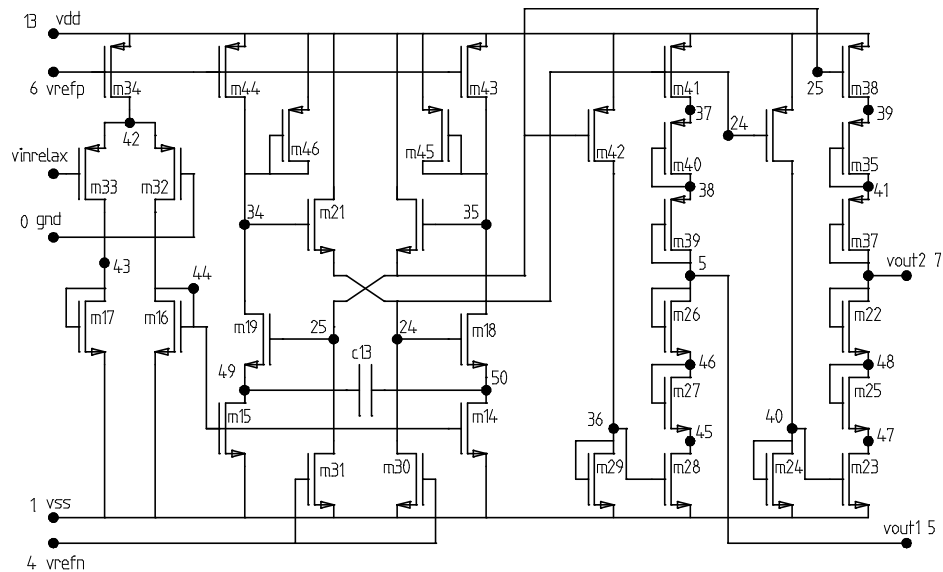
Figure 4 Voltage Controlled Oscillator

Undetected Faults

The fault cover using the DC and AC supply current tests was increased from 73% to 83% by using three different supply voltages. Nevertheless, 17% or 22 faults remain undetected. The reason why these faults remain undetected will be discussed here. 13 of the 22 undetected faults occur in the VCO. Fig. 4 shows the circuit diagram of the VCO. Of these 13 faults, 8 occur in the voltage divider chains on the right of the circuit in Fig. 4.These undetectable faults include the gate-source shorts on M26, M27 and M28. Although these faults would affect the functioning of the circuit, effect in terms of the supply current would be negligible, unless they were to force the PLL as a whole to cease to function. Therefore it is not surprising that a supply current test is unable to find them. More significantly, it should be noted that the original premise – that stimuli that would cause transistors to change their region of operation are ideal for supply current testing – cannot be satisfied for such circuit configurations. M26 and M27 are connected so as to be in permanent saturation.

Other undetectable faults include the gate to source shorts of M18 and M21 in Fig. 4. Again, from the circuit configuration, it would be almost impossible to apply any stimulus that would cause these transistors to switch their mode of operation. It is reasonable to suppose that this test technique cannot provide a significantly higher fault cover than that found here for voltage-mode circuits operating with ±5V supplies.

Conclusions

A testing technique for analog CMOS circuits has been discussed. This technique aims to sensitize faults by causing transistors to switch from their normal saturation mode of operation. Hence, the supply current, in both DC and AC domains is changed sufficiently to give a clear indication of the presence or absence of a fault. This technique has been shown to increase the fault cover of a complex analog CMOS circuit by 10% to 83%. This technique may be even more successful with lower voltage, current mode circuits. It is intended that the technique will form the basis of a mixed-signal Built-In Self-Test (BIST) methodology.

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