Minimisation of Power Dissipation During Test Application in Full Scan Sequential Circuits Using Primary Input Freezing

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Abstract

This paper describes a new technique for minimising power dissipation in full scan sequential circuits during test application. The technique increases the correlation between successive states during shifting in test vectors and shifting out test responses by reducing spurious transitions during test application. The reduction is achieved by freezing the primary input part of the test vector until the smallest transition count is obtained which leads to lower power dissipation. This paper presents a new algorithm which determines the primary input change time such that maximum saving in transition count is achieved with respect to a given test vector and scan latch order. It is shown how combining the proposed technique with the recently reported scan latch and test vector ordering yields further reductions in power dissipation during test application. Exhaustive experimental results using compact and non compact test sets demonstrate substantial savings in power dissipation using a simulated annealing-based design space exploration. As an example saving of 34% in power dissipation for benchmark circuit *s713* is achieved.

1 Introduction

Performance, cost and testability are the main parameters targeted during the synthesis and optimisation phase of integrated circuits. Recently the issue of low power dissipation has emerged as an important parameter in the design flow [1] and has been investigated at different design hierarchy levels. High level power minimisation techniques [2, 3, 4] trade-off throughput, area and power dissipation during scheduling, allocation and binding. At the logic level, two successful power management techniques, based on precomputation [5, 6] and guarded evaluation [7] have been presented. While the above research has outlined solutions for minimising power dissipation during the normal (functional) mode of operation, it is essential to examine the power dissipation during the test mode of operation. It was outlined in [8] that power dissipated during test application is substantially higher than power dissipated during functional operation, which can lead to loss of yield and decrease the reliability of the circuit under test. High power dissipation during test application is due to the following two problems:

- correlation between consecutive test vectors generated by an automatic test pattern generator (ATPG) is very low since a test vector is generated for a given target fault without any consideration of the previous test vector in the test sequence.
- use of scan design for testability (DFT) technique destroys the correlation that typically exists between successive states of the sequential circuit by allowing the application of any desired values to the state latches.

To overcome the problem of high power dissipation during test application, a power-constrained test scheduling algorithm has been proposed for high performance memories and multichip modules [9]. The algorithm is based on a resource graph formulation for the test problem and tests are scheduled concurrently without exceeding their power ratings during test application. A new ATPG tool [10] was proposed to overcome the low correlation between consecutive test vectors during test application. Despite achieving the objectives of safe and inexpensive testing of low power circuits the approach in [10] increased the test application time. Furthermore, in the case of sequential circuits, only the combinational part assuming parallel scan is considered to contribute to power dissipation. However, recently Dabholkar et al. [11] showed that the power dissipation in full scan sequential circuits depends not only on the combinational part but also on the sequential part of the circuit. Here the two above mentioned problems associated with low power testing are solved as follows. Test vector ordering was used to solve the low correlation between consecutive test vectors, while scan latch ordering was employed to

introduce correlation between consecutive states during test application. Further benefit of the technique proposed in [11] is that minimisation of power dissipation during test application has been achieved without any increase in test application time unlike [9, 10]. The techniques in [11] did not consider the effect of the timing of the primary input part of the test vector on the power dissipation during test application.

The aim of this paper is to analyse and exploit the influence of primary input freezing on minimisation of power dissipation during test application. Furthermore, the effect of combining the primary input freezing with test vector and scan latch ordering on power dissipation is investigated. In section 2, the power dissipation model and the parameters which are accountable for power dissipation in full scan circuits during test application are described. Section 3 outlines that primary input freezing has profound impact on reducing spurious transitions during test application. New algorithms for exploiting all the parameters which lead to substantial savings are introduced in section 4. Experimental results and conclusions are presented in sections 5 and 6 respectively.

2 Power Dissipation During Test Application

Power dissipation in CMOS circuits can be divided into static, short circuit, leakage and dynamic power dissipation. The static power dissipation is negligible for correctly designed circuit, short circuit power dissipation caused by short circuit current during switching and power dissipated by leakage currents contribute up to 20% of the total power dissipation. The remaining 80% is attributed to dynamic power dissipation caused by switching of the gate outputs [12]. If the gate is part of a synchronous digital circuit controlled by global clock, it follows that the dynamic power P_d required to charge and discharge the output capacitance load of every gate is:

$$P_d = 0.5 \times C_{load} \times (V_{DD}^2 / T_{cyc}) \times N_G \tag{1}$$

where C_{load} is the load capacitance, V_{DD} is the supply voltage, T_{cyc} is the global clock period, and N_G is the total number of gate output transitions ($0 \rightarrow 1$ or $1 \rightarrow 0$). The vast majority of power reduction techniques concentrate on minimising the dynamic power dissipation by reducing one or more variables of P_d. The supply voltage V_{DD} is usually not under designer control and global clock period T_{cyc}, or more generally, the system throughput is a constraint rather than a design variable. Thus, *node transition count*

$$NTC = \sum_{for\ all\ gates\ G} N_G \times C_{load} \tag{2}$$

is used as quantitative measure for power dissipation throughout the paper. It has been assumed that load capacitance for each gate is equal to the number of fan-outs. The node transition count in scan latches N_{SL} is considered as in [11], where it was shown that for input changes $0 \rightarrow 0$ and $1 \rightarrow 1$, $N_{SL_{min}} = 2$, whilst for input changes $0 \rightarrow 1$ and $1 \rightarrow 0$, $N_{SL_{max}} = 6$. Previous research has established that node transition count depends on two factors, test vector ordering and scan latch ordering, when circuit is in the test mode [11].

To illustrate the factors accountable for power dissipation consider the *s27* circuit (Figure 1) from the commonly accepted ISCAS89 benchmark set [13]. The $\{x_0, x_1, x_2, x_3\}$ are primary inputs, $\{S_0, S_1, S_2\}$ are the scan latches, $\{y_0, y_1, y_2\}$ are the present state lines, and $\{z_0\}$ is the circuit output. The transitions on circuit data lines are described later in the paper. Using the GATEST [14] ATPG tool, it has been shown that 5 test vectors are needed to achieve 100% fault coverage. The test vectors are $\{1101011, 0000000, 0010010, 0111111, 1100010\}$. For easy reference they are labelled as $\{V_0, V_1, V_2, V_3, V_4\}$. Each test vector consists of primary inputs and pseudoinputs (present state lines) in the following order $x_0x_1x_2x_3y_0y_1y_2$. Assume initially all the primary and pseudoinputs are set to 0 and using Eqn. 2 the node transition count is calculated as $NTC = 372$. A detailed description for calculating NTC over the entire test application period is outlined in section 3. By reordering the test vectors as such $\{V_0, V_2, V_4, V_3, V_1\}$ a new lower value for node transition count is obtained $NTC = 352$. This shows that reordering of test vectors reduces power dissipation during test application by increasing the correlation between consecutive test vectors. Note that node transition count is computed for the entire test application period of $n \times (m+1) + m$ clock cycles, where n is the number of test vectors and m is the number of scan latches. Now the effect of scan latch ordering on power savings is examined. Consider the reordered test vector set $\{V_0, V_2, V_4, V_3, V_1\}$ and reordering scan latces as such $\{S_0, S_2, S_1\}$ the value of node transition count is reduced further to $NTC = 328$. This reduction is due to higher correlation between succesive states during shifting in test vectors and shifting out test responses. If test vector ordering and scan latch ordering are done simultaneously further reduction in node transition count is achieved $NTC = 296$, for the following test vector order $\{V_0, V_2, V_3, V_4, V_1\}$ and scan latch order $\{S_2, S_1, S_0\}$. This shows that these two parameters (scan latch ordering and test vector ordering) are interrelated which leads to higher reductions than when each parameter is considered separetely.

3 New Technique for Minimisation of Power Dissipation During Test Application Using Primary Input Freezing

In this section the motivation for the research is outlined and key ideas are presented. The influence of primary input freezing on the reduction of spurious transitions and hence savings in the total number of transitions is demonstrated through detailed examples.

For a full scan sequential circuit with m scan latches the pseudoinput part of the test vector is scanned in m clock cycles t_0 to t_{m-1}. In the next clock cycle t_m the entire test vector is applied to the combinational logic and the test response is loaded in scan latches. During the next m clock cycle the test response is scanned out simultaneously with scanning in the next test vector. So far we have assumed that the changing of the primary inputs $x_0x_1x_2x_3$ occurs at time t_0 which is the beginning of scanning out the response of the previous test vector and scanning in the pseudoinputs of the new test vector. From now onwards the test application strategy where primary inputs change at t_0 is called *as soon as possible* (ASAP). For the particular example in Figure 1, where the number of scan latches is 3, at times t_0, t_1, and t_2 the scan latches are in the shift mode and the values on the input lines of the combinational part of the circuit are irrelevant. The value of primary inputs is important only at t_3 when the entire test vector is applied to the combinational part of the circuit. Therefore the primary inputs can be frozen (keep the value of the previous test vector) during t_0 to t_2 without affecting the testing process. To illustrate the importance of primary input freezing consider the application of test vector $\{0000000\}$ followed by test vector $\{1101011\}$. The circuit data lines are described in terms of three values. For example in Figure 1(a), in the case of primary input x_0 the value $0/1/1$ denotes value 0 at t_3 when applying $\{0000000\}$ and value 1 at t_0 and t_1 when shifting in the second test vector $\{1101011\}$. When primary inputs $x_0x_1x_2x_3$ change at t_0 as shown in Figure 1(a) the two marked boxes illustrate spurious transitions $0/1/0$ and $1/0/1$ at the output of the marked NOR and NOT gate respectively. A spurious transition during test application in full scan sequential circuits is a transition which occurs in the combinational part of the circuit under test while shifting out the test response and shifting in the pseudoinput part of the next test vector. Spurious transitions do not have any influence on test efficiency since the value at the input and output of the combinational part of the circuit is not useful test data. Furthermore, the value of primary inputs is irrelevant during shifting out the test response. Therefore if the primary inputs are frozen until t_1 the controlling value 1 at the input of the marked NOR gate is preserved at t_1 and no spurious transitions at the output of the marked NOR and NOT gates will occur, as shown in Figure 1(b). The primary inputs can be frozen until t_3 when test vector $\{1101011\}$ is applied to the combinational part of the circuit. The test application strategy where primary

inputs change at time t_m is called *as late as possible* (ALAP). However freezing the primary inputs until t_m will not yield the minimal number of node transition count as demonstrated in Figures 1(c) and 1(d) using the same test vectors. In Figure 1(c), in the case of primary input x_0 the value $0/0/1$ denotes value 0 at t_1 and t_2 when shifting in $\{1101011\}$ and value 1 at t_3 when applying $\{1101011\}$. When primary inputs $x_0x_1x_2x_3$ are frozen until t_3 as shown in Figure 1(c) the marked box illustrates a spurious transition $0/1/0$ at the output of the marked AND gate. However if the primary inputs are changed earlier at t_2 the controlling value 0 at the input of the marked AND gate is preserved at t_2 and no spurious transitions at the output of the marked AND gate will occur as shown in Figure 1(d). So far it was shown that both ASAP or ALAP test application strategies lead to spurious transitions during shifting in test vectors and shifting out test responses. Now the question is when should the primary inputs change such that the smallest number of spurious transitions occur which leads to lower power dissipation? The best primary input change time is the time when the primary inputs of the previous test vector are unfrozen and changed to the values of the actual test vector, leading to the smallest value in node transition count *NTC*. Thus, finding the optimal primary input change time will lead to higher correlation between consecutive values on the input lines of the combinational part of the circuit and hence to lower power dissipation during test application.

Figures 1(a) to 1(d) have illustrated the reduction of spurious transitions over a three clock cycles period. To give insight of the proposed technique for power dissipation minimisation during the entire test application period, Tables 1(a) and 1(b) show the flow of test data for the benchmark circuit *s27* of Figure 1 for ASAP and the proposed test application strategy respectively. In Table 1(a) consider the scan latch order $\{S_2, S_1, S_0\}$ and test vector order $\{V_0, V_2, V_3, V_4, V_1\}$ after simultaneous test vector ordering and scan latch ordering was carried out as shown in section 2. The first column shows the clock cycle index and the second column outlines the test vector which is scanned in during t_0, t_1, t_2 and applied at t_3. The operation type (**S**can or **L**oad) is shown in column 3. In the case of a **S**can operation the fourth column gives the *ScanIn* value. Columns 5-8 show the values of primary inputs $x_0x_1x_2x_3$ and the columns 9-11 show the next state values $y'_2y'_1y'_0$. The last column shows the value of node transition count *NTC* for each clock cycle. The node transition count is calculated as follows. In clock cycle *i* the number of transitions in combinational part is computed by considering the primary inputs of clock cycle *i* and the next state values of clock cycle $(i-1)$. The node transition count in sequential part is the sum of node transition count of each scan latch by scanning/loading the next state values $y'_2y'_1y'_0$ in clock cycle *i*, using the values of $N_{SL_{min}}$ and $N_{SL_{max}}$ outlined in section 2. Initially all the primary and scan inputs are set to 0 and the node transition count

over the entire test application period under the ASAP test application strategy is $NTC = 296$. This value can be reduced if spurious transitions during shifting in test vectors and shifting out responses are avoided by primary input freezing. Test application strategy where primary input change time is determined such that maximum saving in transition count is achieved is refered to as *best primary input change* (BPIC) test application strategy. The change of primary input part of test vector V_i at time t_j is indicated by $t_{V_i} = t_j$. If the primary input change times are set to $t_{V_0} = t_2$, $t_{V_2} = t_0$, $t_{V_3} = t_0$, $t_{V_4} = t_3$, and $t_{V_1} = t_1$ as shown in the marked boxes of Table 1(b), the node transition count reduces to $NTC = 266$. The reason for reducing the number of transitions is the increased correlation between consecutive values of primary and pseudoinput inputs during t_0, t_1, t_2, when test vectors are scanned in and test responses are scanned out. For example by freezing t_{V_4} until t_3 the NTC in clock cycles 12 and 14 reduces from 16 and 24 respectively in the case of ASAP (Table 1(a)) to 10 and 14 respectively in the case of BPIC (Table 1(b)). Note that in clock cycles when test responses are loaded in scan latches (**L** in column 3), the correct test response values from Table 1(a) are preserved. When combining primary input freezing with simultaneous scan latch ordering and test vector ordering further improvements are achieved. For test vector order $\{V_1, V_0, V_4, V_3, V_2\}$, scan latch order $\{S_1, S_2, S_0\}$ and primary input change times set at $t_{V_1} = t_0$, $t_{V_0} = t_0$, $t_{V_4} = t_1$, $t_{V_3} = t_1$, and $t_{V_2} = t_3$, it is shown that the new value of node transition count is reduced further to $NTC = 251$ (Table 1(c)). This highlights the importance of combining primary input freezing with simultaneous scan latch and test vector ordering for NTC reduction and hence savings in power dissipation. Note that the proposed BPIC test application strategy depends only on controlling primary input change time, and hence does not require extra design for test hardware. This means that power dissipation is minimized without an increase in gate count or performance. Furthermore, since no extra test data is necessary and the complete test vector computed by the ATPG tool is applied to the circuit under test irrespective of the primary input change time, the proposed test application strategy does not decrease test efficiency and no penalty in test application time or volume of test data is added.

4 Proposed Algorithms for Minimising Power Dissipation During Test Application

In section 4.1 a new algorithm which computes best primary input change time for each test vector with respect to a given test vector and scan latch order is given. Section 4.2 shows how combining the proposed technique with the recently introduced scan latch and test vector ordering using a simulated annealing-based design space exploration leads to further reductions in power dissipation during test application.

4.1 Best Primary Input Change (*BPIC*) Algorithm

Spurious transitions induced by fixed primary input changes as outlined in section 3 are solved by freezing the primary inputs for each test vector until the minimum number of transitions is achieved. For a given scan latch order with m scan latches, the total number of primary input change times is $(m+1)$. Considering n test vectors, in a given test vector order, the total number of configurations of primary input changing for all the test vectors is $(m+1)^n$. Best Primary Input Change (*BPIC*) algorithm computes the best primary input change time for each test vector for a given scan latch order and test vector order. Figure 2 illustrates the pseudocode of the proposed (*BPIC*) algorithm. The function accepts as input, a test set **S** and a circuit **C**. The outer loop represents the traversal of all the test vectors from test set **S**. All the $m+1$ primary input change times for test vector V_i are then considered in the inner loop. For each primary input change time t_j, circuit **C** is simulated and the node transition count $NTC_{i,j}$ is registered. After the completion of the inner loop the best primary input change time t_{j_i}, for which NTC_{i,j_i} is minimum, is retained and the outer loop continues until the entire test set is examined. The algorithm computes the best solution in a computational time which is polynomial in the number of test vectors n, the number of scan latches m, and the circuit size $|\mathbf{C}|$. Despite the reductions which are achieved by the *BPIC* algorithm as shown in section 5, all the factors accountable for power dissipation during test application must be combined for achieving best results, which is described next.

4.2 Simulated Annealing Design Space Exploration for Simultaneous Test Vector Ordering, Scan Latch Ordering and Primary Input Freezing

High power dissipation problems caused by an inadequate test vector ordering and scan latch ordering are solved by an simulated annealing algorithm which can escape local minima. For a test test which consists of n test vectors there are $n!$ test vector orderings. Furthermore for each

test vector ordering there are $m!$ scan latch orderings, where m is the number of scan latches. Finding the optimal test vector and scan latch order is NP-hard [11]. The total complexity of the design space is $n! \times m!$ which even for small design problems with 15 test vectors and 15 scan latches is computationally expensive. We need to use efficient design space exploration techniques which should take account of the discrete, degenerate and highly irregular design space.

Figure 3 illustrates the basic steps of simulated annealing-based optimisation. The optimisation function accepts as input a test set **S** and a circuit **C** which are set to initial configuration S_{INIT} and C_{INIT} respectively. The calculation of the initial control parameter value [15] is based on the assumption that a sufficiently large number of generated solutions (for example 95%) should be accepted at the beginning of the annealing process. The outer loop modifies the control parameter of the simulated annealing algorithm which is gradually lowered as the annealing process proceeds. Within the inner loop a new sequence of solutions is generated at a constant control parameter value. The length of a sequence of solutions is set to 20. The control parameter is decreased in such a way that the stationary distributions at the end of the sequences of solutions are close to each other. By evaluating information about the cost distribution within each sequence of solutions, a fast decrease of the control parameter is given according to the cooling schedule from [15]. Each new solution is generated using one of the following:

- randomly choose two scan latches S_i and S_j from the actual scan latch order $\{S_0, \ldots, S_i, \ldots, S_j, \ldots, S_{m-1}\}$ and exchange their position generating a new scan latch order $\{S_0, \ldots, S_j, \ldots, S_i, \ldots, S_{m-1}\}$, where m is the number of scan latches in the circuit.

- randomly choose two test vectors V_a and V_b from the actual test vector order $\{V_0, \ldots, V_a, \ldots, V_b, \ldots, V_{n-1}\}$ and exchange their position generating a new test vector order $\{V_0, \ldots, V_b, \ldots, V_a, \ldots, V_{n-1}\}$, where n is the number of test vectors in the test set.

The alternative application of exchanges between randomly chosen test vectors and scan latches proves to be efficient in exploring the discrete design space. For each new solution the proposed best primary input change algorithm $BPIC(S_{NEW}, C_{NEW})$ is called to determine the best primary input change times for all the test vectors from S_{NEW} according to the scan latch order in C_{NEW}. New solutions are either accepted or rejected depending on the acceptance criterion defined in the simulated annealing algorithm [16]. If the best solution so far is reached then it is saved in $\{S_{BEST}, C_{BEST}\}$ which is returned at the end of the optimisation process. The optimisation process is terminated after the variation in the average cost over a selected number of sequences of solutions falls bellow a given value as described in [15]. It is important to

note that all the factors accountable for power dissipation during test application as described in sections 2 and 3 are included in the optimisation process. This leads to high savings in power dissipation as outlined in the experimental results section.

5 Experimental Results

This section demonstrates through a set of benchmark examples that the proposed best primary input change (*BPIC*) algorithm outlined in section 4.1 yields savings in power dissipation during test application. Furthermore the savings can be substantially improved when *BPIC* is integrated with test vector ordering and scan latch ordering as described in the algorithm in section 4.2. These algorithms have been implemented within the framework of a low power testing system on a 350 MHz Pentium II PC with 64 MB RAM running Linux and using GNU CC version 2.7.

Table 2 shows the results when the *BPIC* algorithm is applied by itself (i.e. without scan latch and test vector ordering) for 24 commonly accepted ISCAS89 benchmark circuits [13]. The first and second columns give the circuit name and the number of scan latches (SL) respectively. The third column gives the number of test vectors (TV) generated by the ATPG tool ATOM [17]. The average value of node transition count (*NTC*), which is the total value of *NTC* divided by the total number of clock cycles, for as soon as possible (ASAP), as late as possible (ALAP), and the proposed best primary input change (BPIC) test application strategies outlined in section 3, are given in columns 4, 5 and 6 respectively. The average value of *NTC* is calculated under the assumption of the zero delay model. The power minimisation techniques described in this paper also apply to other delay models, such as unit delay model [18] and variable delay model [19]. It can been clearly seen from Table 2 that BPIC test application strategy has the least average value of *NTC* for all the benchmark circuits when compared to ASAP and ALAP test application strategies. To give an indication of the reductions in average value of *NTC*, columns 7 and 8 show the percentage reduction of BPIC over ASAP and ALAP test application strategies. The reduction varies from approximately 10% as in the case of *s641* down to under 1% as in the case of *s526*. Table 2 has shown the reductions in node transition count using a non compact test set. In order to reduce test application time while maintaining the same test quality, compact test sets are used. Compact test sets may lead to higher power dissipation because of an increased number of sensitised paths by each test vector. However, using the proposed *BPIC* algorithm similar average values of *NTC* are achieved for all the benchmark circuits when comparing compact test sets to non compact test sets. Table 3 shows experimental results for compact test set generated by MINTEST [20] when applying the proposed *BPIC* algorithm without scan latch and test vector ordering. For example, in the

case of *s298* the average value of *NTC* for non compact test set is 114.73 (Table 2), whereas for compact test set the average value of *NTC* is 107.85 (Table 3) despite a considerable reduction in the number of test vectors from 52 as in the case of non compact test set to 23 as in the case of the compact test set. The similar values of *NTC* are due to finding the best primary input change time for reducing spurious transitions during shifting in test vectors and shifting out responses. This clearly shows that using compact test sets and hence decreasing the test application time will *not* increase the power dissipation during test application in full scan sequential circuits.

While the application of the *BPIC* algorithm reduces average value of *NTC* when compared to ASAP and ALAP test application strategies, as shown in Tables 2 and 3 for non compact and compact test sets respectively, further savings can be achieved when *BPIC* is combined with test vector ordering and scan latch ordering. The results of the proposed simulated annealing-based design space exploration (section 4.2) for solving simultaneous test vector ordering, scan latch ordering and primary input freezing for non compact test set is shown in Table 4. In order to asses the impact of all the factors accountable for power dissipation the following three experiments were carried out. In the first experiment the average value of *NTC* is computed using scan latch and test vector ordering under ASAP test application strategy. The results are given in columns 2 and 3. The reduction in column 3 is computed over the node transition count of the initial scan latch and test vector. In the second experiment the test application strategy has been changed to ALAP, and the results are shown in columns 4 and 5. In the third experiment the proposed BPIC test application strategy is combined with scan latch and test vector ordering and the results are given in columns 6 and 7. Note that BPIC always produces better results than ASAP and ALAP due to higher correlation between successive states during shifting in test vectors and shifting out test responses. This clearly shows the importance of integrating *all* the factors accountable for power dissipation in the optimisation process. The reduction value depends on the type of the circuit and the average value of *NTC* for the initial scan latch and test vector order. For example in the case of *s713* the reduction is 34% and it goes down to 4% as in the case of *s838*. However, this still presents an improvement when compared to ASAP and ALAP which yield reductions only of 3%. Table 5 shows the results for ASAP, ALAP and BPIC test application strategies when using compact test sets. Again the proposed BPIC provides better results than ASAP and ALAP, for all the circuits from the benchmark set. It is interesting to note that *NTC* values for BPIC test application strategy when using non-compact and compact test sets are similar. This indicates that test set size has no influence on the average value of *NTC* confirming that the only three accountable factors for power dissipation during test application in full scan circuits are test vector ordering, scan latch ordering and

primary input freezing. For some of the examples the computational time for completing the optimisation may increase over 40,000s using a Pentium II processor at 350 MHz, as shown in Table 4. This is due to the huge size of the design space and the low number of solutions with identical *NTC* which clearly leads to longer times for exploration and convergence of the simulated annealing algorithm. However, when using compact tests as shown in Table 5, due to smaller number of test vector vectors and consequently the size design space, lower time for completion is required which leads to the conclusion that compact test sets have benefits in both test application time as well as in computational time with similar reductions in power dissipation.

6 Conclusions

This paper has proposed a new technique for minimising power dissipation in full scan sequential circuits during test application. The technique is based on increasing the correlation between successive states during shifting in test vectors and shifting out test responses by freezing the primary inputs until the smallest number of transitions is achieved. A new algorithm which computes best primary input change (BPIC) time for each test vector has been presented. It has been shown that combining the described technique with the recently reported scan latch and test vector ordering using a simulated annealing-based design space exploration yields substantial reductions in power dissipation during test application. Exhaustive experimental results using both compact and non compact test sets have shown that compact test sets have similar power dissipation during test application with substantial reduction in test application time and computational time when compared to non compact test sets.

While this paper has shown how BPIC minimises power dissipation in full scan sequential circuits, current research underway by the authors investigates the applicability of BPIC to partial scan and the identification of the best design for test method in terms of power dissipation during test application.

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Tables

Cycle	Vector	Op	SI	x_0	x_1	x_2	x_3	y'_2	y'_1	y'_0	NTC
0 (t_0)	V_0	S	0	1	1	0	1	0	0	0	14
1 (t_1)	V_0	S	1	1	1	0	1	1	0	0	10
2 (t_2)	V_0	S	1	1	1	0	1	1	1	0	19
3 (t_3)	V_0	L	-	1	1	0	1	0	0	1	18
4 (t_0)	V_2	S	0	0	0	1	0	0	0	0	15
5 (t_1)	V_2	S	1	0	0	1	0	1	0	0	10
6 (t_2)	V_2	S	0	0	0	1	0	0	1	0	14
7 (t_3)	V_2	L	-	0	0	1	0	1	1	0	19
8 (t_0)	V_3	S	1	0	1	1	1	1	1	1	11
9 (t_1)	V_3	S	1	0	1	1	1	1	1	1	10
10 (t_2)	V_3	S	1	0	1	1	1	1	1	1	6
11 (t_3)	V_3	L	-	0	1	1	1	0	0	0	18
12 (t_0)	V_4	S	0	1	1	0	0	0	0	0	16
13 (t_1)	V_4	S	1	1	1	0	0	1	0	0	10
14 (t_2)	V_4	S	0	1	1	0	0	0	1	0	24
15 (t_3)	V_4	L	-	1	1	0	0	0	1	0	16
16 (t_0)	V_1	S	0	0	0	0	0	0	0	1	18
17 (t_1)	V_1	S	0	0	0	0	0	0	0	0	18
18 (t_2)	V_1	S	0	0	0	0	0	0	0	0	6
19 (t_3)	V_1	L	-	0	0	0	0	0	0	0	6
20 (t_0)	-	S	0	0	0	0	0	0	0	0	6
21 (t_1)	-	S	0	0	0	0	0	0	0	0	6
22 (t_2)	-	S	0	0	0	0	0	0	0	0	6
TOTAL											296

(a) As Soon As Possible (ASAP) test application strategy

Table 1: The flow of test data for the circuit in Figure 1 during the entire test application period

Cycle	Vector	Op	SI	x_0	x_1	x_2	x_3	y'_2	y'_1	y'_0	NTC
0 (t_0)	V_0	S	0	0	0	0	0	0	0	0	6
1 (t_1)	V_0	S	1	0	0	0	0	1	0	0	10
2 (t_2)	V_0	S	1	**1**	**1**	**0**	**1**	1	1	0	17
3 (t_3)	V_0	L	-	1	1	0	1	0	0	1	18
4 (t_0)	V_2	S	0	**0**	**0**	**1**	**0**	0	0	0	15
5 (t_1)	V_2	S	1	0	0	1	0	1	0	0	10
6 (t_2)	V_2	S	0	0	0	1	0	0	1	0	14
7 (t_3)	V_2	L	-	0	0	1	0	1	1	0	19
8 (t_0)	V_3	S	1	**0**	**1**	**1**	**1**	1	1	1	11
9 (t_1)	V_3	S	1	0	1	1	1	1	1	1	10
10 (t_2)	V_3	S	1	0	1	1	1	1	1	1	6
11 (t_3)	V_3	L	-	0	1	1	1	0	0	0	18
12 (t_0)	V_4	S	0	0	1	1	1	0	0	0	10
13 (t_1)	V_4	S	1	0	1	1	1	1	0	0	10
14 (t_2)	V_4	S	0	0	1	1	1	0	1	0	14
15 (t_3)	V_4	L	-	**1**	**1**	**0**	**0**	0	1	0	16
16 (t_0)	V_1	S	0	1	1	0	0	0	0	1	14
17 (t_1)	V_1	S	0	**0**	**0**	**0**	**0**	0	0	0	18
18 (t_2)	V_1	S	0	0	0	0	0	0	0	0	6
19 (t_3)	V_1	L	-	0	0	0	0	0	0	0	6
20 (t_0)	-	S	0	0	0	0	0	0	0	0	6
21 (t_1)	-	S	0	0	0	0	0	0	0	0	6
22 (t_2)	-	S	0	0	0	0	0	0	0	0	6
TOTAL											266

(b) Proposed Best Primary Input Change (BPIC) test application strategy

Table 1: The flow of test data for the circuit in Figure 1 during the entire test application period

Cycle	Vector	Op	SI	x_0	x_1	x_2	x_3	y'_1	y'_2	y'_0	NTC
0 (t_0)	V_1	S	0	**0**	**0**	**0**	**0**	0	0	0	6
1 (t_1)	V_1	S	0	0	0	0	0	0	0	0	6
2 (t_2)	V_1	S	0	0	0	0	0	0	0	0	6
3 (t_3)	V_1	L	-	0	0	0	0	0	0	0	6
4 (t_0)	V_0	S	0	**1**	**1**	**0**	**1**	0	0	0	14
5 (t_1)	V_0	S	1	1	1	0	1	1	0	0	10
6 (t_2)	V_0	S	1	1	1	0	1	1	1	0	10
7 (t_3)	V_0	L	-	1	1	0	1	0	0	1	27
8 (t_0)	V_4	S	0	1	1	0	1	0	0	0	14
9 (t_1)	V_4	S	0	**1**	**1**	**0**	**0**	0	0	0	11
10 (t_2)	V_4	S	1	1	1	0	0	1	0	0	10
11 (t_3)	V_4	L	-	1	1	0	0	1	0	0	6
12 (t_0)	V_3	S	1	1	1	0	0	1	1	0	10
13 (t_1)	V_3	S	1	**0**	**1**	**1**	**1**	1	1	1	16
14 (t_2)	V_3	S	1	0	1	1	1	1	1	1	10
15 (t_3)	V_3	L	-	0	1	1	1	0	0	0	18
16 (t_0)	V_2	S	0	0	1	1	1	0	0	0	10
17 (t_1)	V_2	S	0	0	1	1	1	0	0	0	6
18 (t_2)	V_2	S	1	0	1	1	1	1	0	0	10
19 (t_3)	V_2	L	-	**0**	**0**	**1**	**0**	1	1	0	19
20 (t_0)	-	S	1	0	0	1	0	1	1	1	10
21 (t_1)	-	S	1	0	0	1	0	1	1	1	10
22 (t_2)	-	S	1	0	0	1	0	1	1	1	6
TOTAL											251

(c) Proposed Best Primary Input Change (BPIC) test application strategy combined with simultaneous scan latch and test vector ordering

Table 1: The flow of test data for the circuit in Figure 1 during the entire test application period

circuit	SL	TV	ASAP NTC	ALAP NTC	proposed BPIC NTC	**%reduction over ASAP**	**%reduction over ALAP**	CPU time (s)
s208	8	65	55.39	55.73	53.48	**3.45**	**4.03**	0.17
s298	14	52	115.39	115.59	114.73	**0.56**	**0.74**	0.28
s344	15	62	131.43	131.45	130.54	**0.67**	**0.69**	0.48
s349	15	65	132.46	132.45	131.47	**0.75**	**0.74**	0.50
s382	21	72	145.12	145.54	143.91	**0.83**	**1.12**	0.80
s386	6	109	86.61	86.20	84.22	**2.76**	**2.29**	0.38
s400	21	71	146.32	146.35	144.78	**1.05**	**1.07**	0.81
s420	16	98	107.19	107.17	104.46	**2.53**	**2.52**	1.00
s444	21	77	149.08	149.93	148.05	**0.69**	**1.25**	0.97
s510	6	90	115.50	115.04	114.13	**1.17**	**0.79**	0.40
s526	21	107	185.83	186.17	184.79	**0.55**	**0.73**	1.45
s641	19	99	186.74	184.03	168.71	**9.65**	**8.32**	2.19
s713	19	100	198.88	196.83	180.42	**9.28**	**8.33**	2.29
s820	5	190	139.22	138.89	136.79	**1.74**	**1.51**	1.02
s832	5	200	138.46	137.96	136.05	**1.73**	**1.37**	1.07
s838	32	183	199.81	199.84	195.00	**2.40**	**2.42**	14.72
s953	29	138	169.93	169.66	167.20	**1.60**	**1.44**	4.71
s1196	18	227	105.18	105.35	100.43	**4.51**	**4.67**	6.38
s1238	18	240	106.85	107.43	102.06	**4.48**	**5.00**	6.69
s1423	74	135	508.09	509.91	502.78	**1.04**	**1.39**	56.48
s1488	6	196	346.62	346.92	342.76	**1.11**	**1.19**	2.68
s1494	6	191	351.92	352.85	348.54	**0.95**	**1.22**	2.62
s5378	179	358	1786.44	1786.58	1774.36	**0.67**	**0.68**	3113.87
s9234	211	660	3123.16	3123.33	3098.91	**0.77**	**0.78**	16395.37

Table 2: Experimental results for non compact test set generated by ATOM [17] when applying the proposed *BPIC* algorithm without scan latch and test vector ordering

circuit	SL	TV	ASAP NTC	ALAP NTC	proposed BPIC NTC	**%reduction over ASAP**	**%reduction over ALAP**	CPU time (s)
s208	8	27	54.80	54.72	52.42	**4.35**	**4.20**	0.07
s298	14	23	108.25	108.57	107.85	**0.36**	**0.66**	0.12
s344	15	13	124.36	124.21	123.48	**0.70**	**0.58**	0.10
s349	15	13	128.35	128.33	127.62	**0.57**	**0.55**	0.10
s382	21	25	147.91	148.14	146.75	**0.78**	**0.93**	0.28
s386	6	63	85.77	85.26	83.38	**2.78**	**2.19**	0.21
s400	21	24	154.04	154.44	152.76	**0.83**	**1.08**	0.28
s420	16	43	100.73	100.46	98.12	**2.59**	**2.33**	0.48
s444	21	24	155.46	156.30	154.19	**0.81**	**1.35**	0.32
s510	6	54	114.03	113.75	112.53	**1.31**	**1.06**	0.24
s526	21	49	182.74	182.98	182.17	**0.31**	**0.44**	0.68
s641	19	21	172.88	176.55	161.08	**6.82**	**8.75**	0.47
s713	19	21	195.45	192.38	181.10	**7.34**	**5.86**	0.49
s820	5	93	138.03	137.65	135.55	**1.79**	**1.51**	0.51
s832	5	94	138.83	138.37	136.33	**1.79**	**1.47**	0.50
s838	32	75	187.95	187.56	185.14	**1.49**	**1.29**	6.35
s953	29	76	169.64	169.02	166.64	**1.76**	**1.40**	2.66
s1196	18	113	105.67	105.42	100.43	**4.95**	**4.73**	3.39
s1238	18	121	103.92	103.83	98.91	**4.82**	**4.74**	3.40
s1423	74	20	506.10	506.89	501.14	**0.98**	**1.13**	8.73
s1488	6	101	365.47	365.66	361.40	**1.11**	**1.16**	1.45
s1494	6	100	369.59	370.63	365.89	**1.00**	**1.28**	1.40
s5378	179	97	1808.88	1809.32	1791.68	**0.95**	**0.97**	826.89
s9234	211	105	3045.30	3045.51	3014.90	**0.99**	**1.01**	2637.05

Table 3: Experimental results for compact test set generated by MINTEST [20] when applying the proposed *BPIC* algorithm without scan latch and test vector ordering

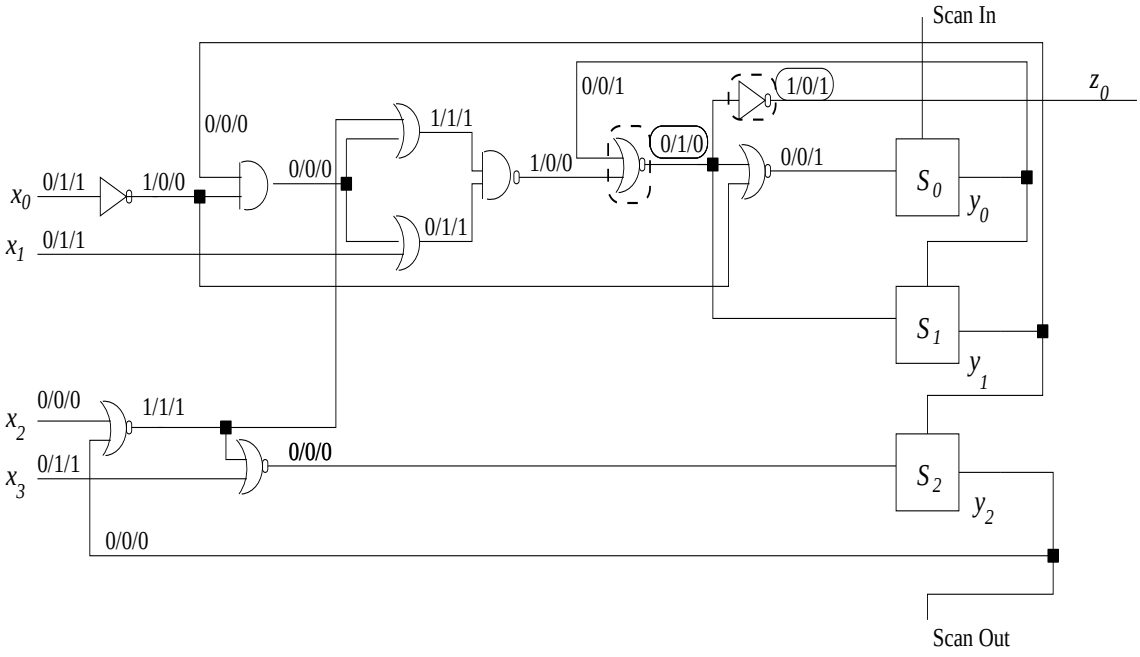
circuit	Test application strategy targeted during optimisation						CPU time (s)
	ASAP NTC	%reduction	ALAP NTC	%reduction	**BPIC** NTC	**%reduction**	
s208	48.39	12.64	49.19	11.19	**45.35**	**18.13**	24390
s298	97.97	15.09	92.49	19.84	**92.09**	**20.19**	33960
s344	115.55	12.08	119.68	8.93	**114.85**	**12.61**	34270
s349	118.62	10.45	121.01	8.64	**117.87**	**11.01**	35040
s382	125.93	13.22	125.98	13.18	**124.47**	**14.23**	40430
s386	70.50	18.60	71.86	17.03	**69.74**	**19.48**	41550
s400	128.97	11.85	132.12	9.70	**125.30**	**14.36**	34550
s420	93.94	12.35	94.51	11.82	**92.41**	**13.78**	43410
s444	130.27	12.61	134.33	9.89	**129.27**	**13.28**	42940
s510	98.91	14.35	101.60	12.02	**97.98**	**15.16**	36920
s526	162.13	12.75	160.96	13.37	**160.52**	**13.61**	37340
s641	142.19	23.85	141.44	24.25	**132.42**	**29.08**	42470
s713	146.91	26.13	144.98	27.09	**130.34**	**34.46**	44630
s820	111.71	19.75	112.10	19.47	**110.83**	**20.39**	43710
s832	115.19	16.80	114.07	17.61	**113.19**	**18.24**	36520
s838	193.50	3.16	193.80	3.01	**190.29**	**4.76**	45970
s953	128.24	24.53	128.61	24.31	**127.26**	**25.10**	46470

Table 4: Experimental results for non compact test set generated by ATOM [17] when applying the proposed *BPIC* algorithm integrated with test vector ordering and scan latch ordering

circuit	Test application strategy targeted during optimisation						CPU time (s)
	ASAP NTC	%reduction	ALAP NTC	%reduction	**BPIC** NTC	**%reduction**	
s208	47.85	12.68	47.90	12.59	**44.02**	**19.67**	8399
s298	91.48	15.49	96.22	11.11	**91.13**	**15.81**	12980
s344	94.92	23.66	100.27	19.37	**94.02**	**24.39**	15550
s349	104.62	18.48	110.23	14.11	**104.14**	**18.85**	13560
s382	120.37	18.61	124.09	16.10	**118.49**	**19.88**	29020
s386	70.33	18.00	69.72	18.71	**68.54**	**20.09**	24500
s400	120.51	21.76	123.36	19.92	**119.51**	**22.41**	29380
s420	90.97	9.69	87.61	13.02	**83.13**	**17.47**	28940
s444	129.44	16.73	132.04	15.06	**120.07**	**22.76**	29040
s510	95.79	15.99	97.68	14.33	**94.80**	**16.86**	22940
s526	151.31	17.19	158.35	13.34	**150.87**	**17.44**	29310
s641	143.36	17.07	130.56	24.48	**120.16**	**30.49**	29210
s713	152.77	21.83	144.71	25.96	**133.49**	**31.69**	24920
s820	110.61	19.86	111.23	19.41	**109.71**	**20.51**	28870
s832	112.39	19.04	112.30	19.10	**111.40**	**19.75**	28950
s838	170.01	9.54	170.75	9.15	**168.36**	**10.42**	30220
s953	128.15	24.45	128.70	24.13	**127.06**	**25.09**	30040

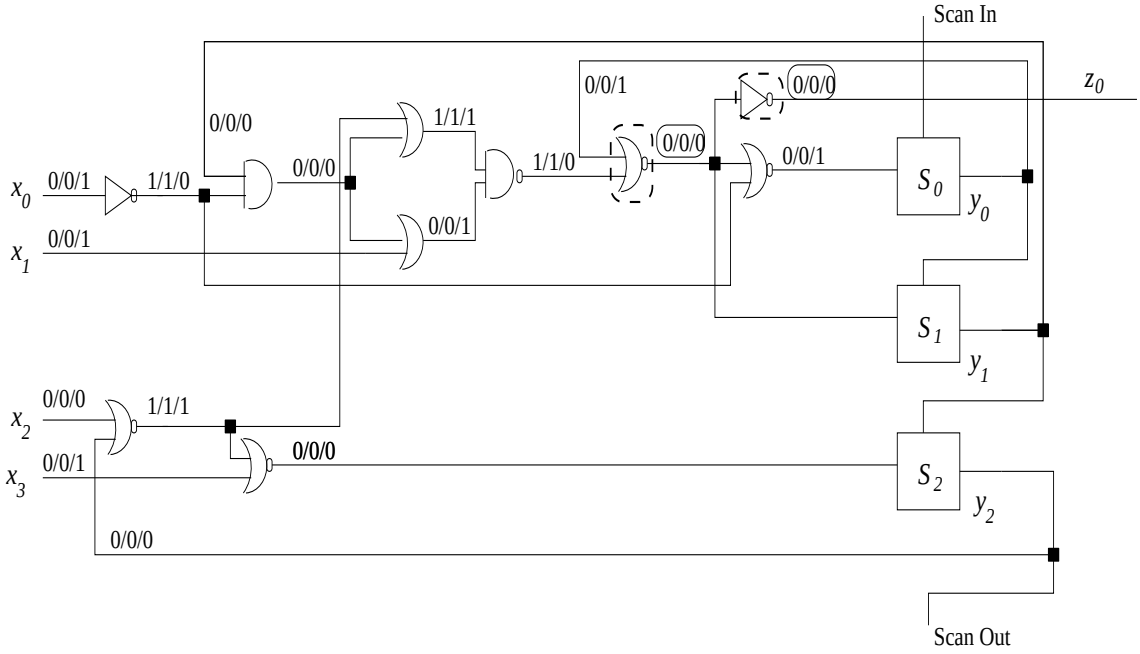
Table 5: Experimental results for compact test set generated by MINTEST [20] when applying the proposed *BPIC* algorithm integrated with test vector ordering and scan latch ordering

Figures



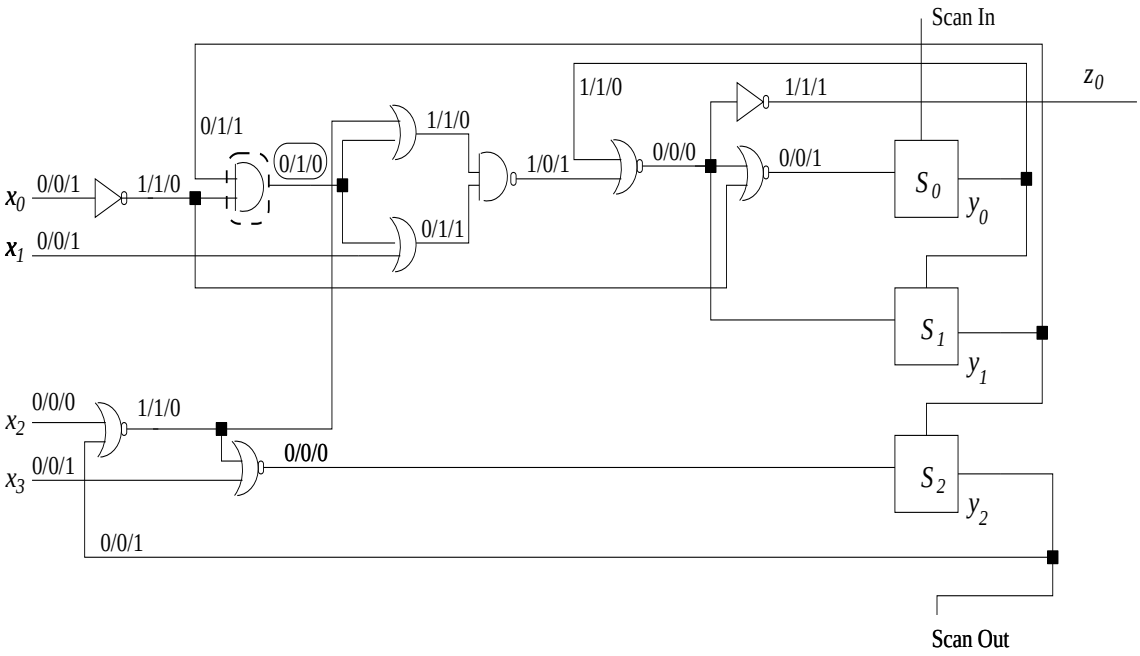
(a) Primary inputs change as soon as possible (ASAP) at t_0

Figure 1: Example circuit (*s27* from [13]) illustrating factors which lead to spurious transitions during test application



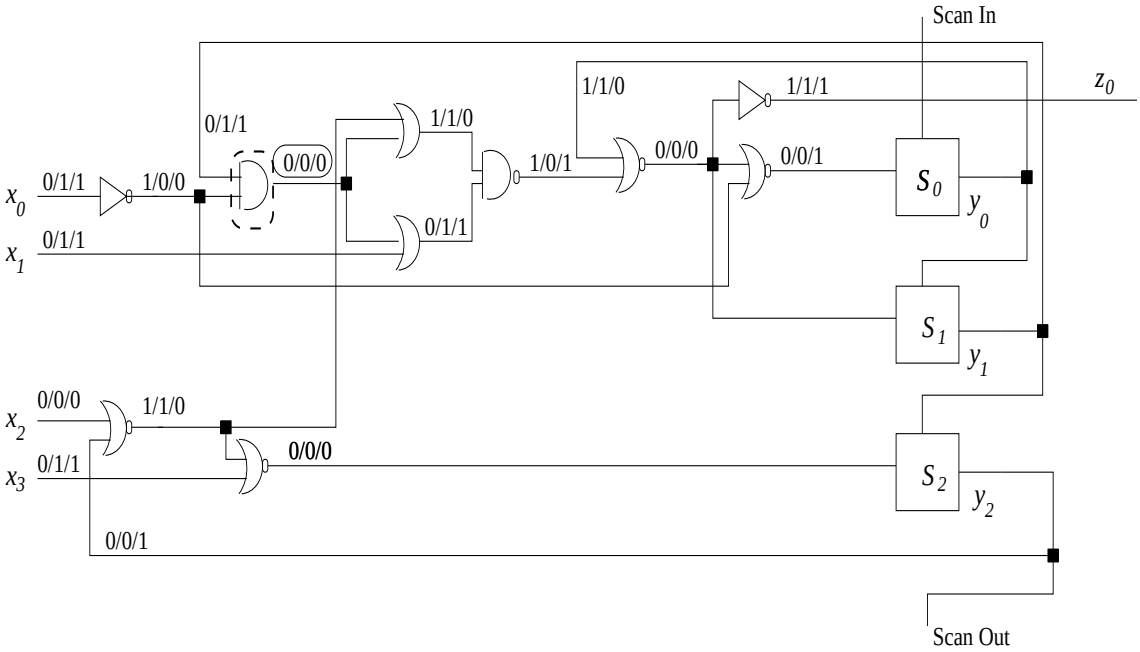
(b) Primary inputs change at t_1

Figure 1: Example circuit (*s27* from [13]) illustrating factors which lead to spurious transitions during test application



(c) Primary inputs change as late as possible (ALAP) at t_3

Figure 1: Example circuit (*s27* from [13]) illustrating factors which lead to spurious transitions during test application



(d) Primary inputs change at t_2

Figure 1: Example circuit (*s27* from [13]) illustrating factors which lead to spurious transitions during test application

```
function BPIC(Test Set S, Circuit C)
{
        for every V_i from S with i = 0,...,n-1
            for every t_{V_i} = t_j with j = 0,...,m
                compute NTC_{i,j} by simulating C
            get t_{j_i} such that NTC_{i,j_i} is minimum
        return {t_{j_0}, t_{j_1}, ..., t_{j_{n-1}}}
}
```

Figure 2: Proposed algorithm for determining the Best Primary Input Change time for each test vector

```
function OPTIMISE(Test Set S, Circuit C)
{
    S_INIT is set to S
    C_INIT is set to C
    repeat
        repeat
            Generate a new solution {S_NEW, C_NEW} as described in section 4.2
            Compute the number of transitions using BPIC(S_NEW, C_NEW)
                as described in section 4.1
            Accept or reject the new solution according
                to the SA acceptance criterion [16]
            if the best solution so far is reached
                S_BEST is set to S_NEW
                C_BEST is set to C_NEW
        until the number of solutions equals the solution sequence length
        decrease the control parameter value
    until the system is frozen
    return {S_BEST, C_BEST}
}
```

Figure 3: Proposed simulated annealing-based design space exploration for simultaneous test vector ordering, scan latch ordering and primary input freezing