

Behavior and effects of fluorine in annealed n^+ polycrystalline silicon layers on silicon wafers

C. D. Marsh^{a)}

Department of Materials, University of Oxford, Parks Road, Oxford OX1 3PH, United Kingdom

N. E. Moiseiwitsch

Department of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, United Kingdom

G. R. Booker

Department of Materials, University of Oxford, Parks Road, Oxford OX1 3PH, United Kingdom

P. Ashburn

Department of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, United Kingdom

(Received 12 October 1999; accepted for publication 4 February 2000)

A comprehensive study is made of the behavior and effects of fluorine in n^+ -polysilicon layers. The polysilicon is deposited in a conventional low pressure chemical vapor deposition furnace on (100) silicon wafers, implanted with $1 \times 10^{16} \text{ cm}^{-2} \text{ F}^+$ and $1 \times 10^{16} \text{ cm}^{-2} \text{ As}^+$ and annealed at 850, 950, 1015, and 1065 °C. Sheet resistance, transmission electron microscopy (TEM), and secondary ion mass spectroscopy are used to obtain quantitative data for the breakup of the interfacial oxide, the epitaxial regrowth of the polysilicon layer, and the fluorine and arsenic distributions. The fluorine significantly increases both the initial oxide breakup ($\sim 8\times$) and the initial polysilicon regrowth. It also produces inclusions in the layer which can affect the subsequent polysilicon regrowth and the arsenic distributions. Three regrowth stages and two regrowth mechanisms are distinguished and interpreted, and a value of $\sim 6 \times 10^{-11} \text{ cm}^2 \text{ s}^{-1}$ is deduced for the effective diffusivity of fluorine in polysilicon at 950 °C. The amounts of regrowth determined by TEM are compared with the corresponding changes in sheet resistance. The thermal budgets required to produce polysilicon layer regrowths of 1% and 50%, important for the performance of polysilicon emitter bipolar transistors, are given. All the thermal budgets are lower when fluorine is present. © 2000 American Institute of Physics. [S0021-8979(00)01410-9]

I. INTRODUCTION

Polysilicon emitters are now used for most high performance bipolar silicon transistors. For these emitters, a large amount of dopant is implanted into a polysilicon layer and this acts as a diffusion source to produce a shallow emitter-base junction in the underlying single-crystal silicon wafer. When the polysilicon layers are deposited on the silicon wafers in a conventional low pressure chemical vapor deposition (LPCVD) furnace, the commercial production process used for such transistors, there is invariably an interfacial oxide layer, typically 0.6–1.4 nm thick, between the deposited polysilicon layer and the silicon wafer, and during the subsequent dopant drive-in this significantly affects the interface and polysilicon structures,^{1,2} the dopant distributions,^{3,4} and the bipolar device characteristics.^{5,6} A drive-in that does not break up the interfacial oxide layer (case A) has the advantage of giving a device with a high current gain,^{1,5} but the disadvantage of a high emitter resistance.^{7,8} A drive-in that partly breaks up the oxide and begins to epitaxially regrow the polysilicon layer (case B) has the advantage of a lower emitter resistance but the disadvantages of a lower

current gain and the device characteristics are sensitive to small differences in the interfacial oxide structure.⁹ A drive-in that completely breaks up the oxide and significantly epitaxially regrows the polysilicon (case C) is similar to case B but has the further advantage that the device characteristics are much less sensitive to the interfacial oxide structure and hence gives more reproducible device characteristics.¹⁰ On going from case A to case B to case C, progressively higher thermal budgets are required for the emitter drive-in. However, higher thermal budget emitter drive-ins have the disadvantage of increased junction depth in the single-crystal silicon, which produces an undesirable increase in emitter/base capacitance.

The implantation of fluorine into a polysilicon emitter has been shown to enhance interfacial oxide breakup^{11–13} and hence to give a low emitter resistance at a reduced thermal budget.^{9,14} Fluorine has also been shown to give higher gains¹⁵ and improved base current idealities¹⁵ due to the passivation of dangling bonds at the oxide/silicon interface. Hence the incorporation of fluorine into the polysilicon can have major beneficial effects on both the materials and the devices, so it is important to understand the role played by the fluorine.

^{a)} Author to whom correspondence should be addressed; electronic mail: chris.marsh@materials.ox.ac.uk

Williams and Ashburn¹⁶ showed that, for polysilicon layers implanted with B^+ and annealed at 1150 °C for 10 s, 10% epitaxial regrowth occurred, whereas for these layers implanted with BF_2^+ only or B^+ plus F^+ and similarly annealed, 80% regrowth occurred. It was deduced that the faster regrowth with fluorine present occurred because of a faster breakup of the interfacial oxide and the suggested reason for this was the formation of Si–O–F complexes which could result in a weakening of the bonding structure of the interfacial oxide.¹⁵ It has also been suggested that fluorine increases boron diffusion down the grain boundaries of the polysilicon.¹⁷

Chen *et al.*¹⁸ showed that, for polysilicon layers implanted with BF_2^+ and annealed at 850–1100 °C, a broad band of small defects was present in the upper part of the layer and a narrow band of small defects at the interface. It was suggested that fluorine was gettered by residual damage defects in the layer and by the interfacial oxide to give in both cases fluorine bubbles and that boron was gettered by the fluorine bubbles.

Tsaur and Hung¹⁹ showed that, for undoped polysilicon layers, complete regrowth occurred for an anneal at 1150 °C for 120 min. For polysilicon layers implanted with As^+ , complete regrowth occurred for an anneal at 1150 °C for 10 s.¹⁰ For polysilicon layers implanted with F^+ plus As^+ complete regrowth occurred for an anneal at 1000 °C for 2 min.²⁰ For polysilicon layers implanted with F^+ plus As^+ , the thermal budget required for the As^+ drive-in to give complete regrowth could be still further decreased by performing a pre-anneal to start the breakup of the oxide after the F^+ implant but before the As^+ implant.¹⁶ It was considered for specimens implanted with As^+ or F^+ plus As^+ that the broken up interface structures corresponded to oxide particles.^{1,11}

Tseng *et al.*²¹ showed that, for polysilicon layers implanted with F^+ only and annealed at 950 °C, significant fluorine was lost from the layer and had diffused to the surface oxide capping layer, the 50 nm thick interfacial oxide layer, and the underlying silicon wafer. No values have yet been reported for the diffusion of fluorine in either single-crystal silicon or polysilicon and the diffusion mechanisms are uncertain. Nash *et al.*²² showed that the diffusivities of fluorine in amorphous silicon in the range of 600–700 °C were in the range $4.5\text{--}47 \times 10^{-14} \text{ cm}^2 \text{ s}^{-1}$ respectively.

In the present work, sheet resistance, transmission electron microscopy (TEM), and secondary ion mass spectroscopy (SIMS) are used to make a comprehensive investigation of the behavior and effects of fluorine on LPCVD polysilicon layers containing arsenic when they are subsequently annealed. The sequence of interfacial oxide breakup and polysilicon layer epitaxial regrowth is studied and new quantitative data are obtained. The structural results are correlated with the fluorine and arsenic distributions and mechanisms are suggested to explain the behavior that occurs. Values for the effective diffusivities of fluorine and arsenic in polysilicon are deduced. The processing conditions and thermal budgets to give the various structures are described and their relevance to polysilicon emitter bipolar transistors is

shown. All of the thermal budgets are lower when fluorine is present.

II. EXPERIMENT

Unpatterned (100) *p*-type Czochralski silicon wafers with resistivities of 3–35 $\Omega \text{ cm}$ were given a HF dip or RCA surface treatment, and produced surface oxide layers typically 0.6 and 1.4 nm thick, respectively. Polycrystalline silicon was deposited on the wafers at 610 °C using a conventional LPCVD furnace to give layers of 320 nm thickness. The specimens were implanted with $1 \times 10^{16} \text{ cm}^{-2} F^+$ at 50 keV followed by $1 \times 10^{16} \text{ cm}^{-2} As^+$ at 70 keV (called F specimens) or with the As^+ only for comparison purposes (called NF specimens). A LPCVD SiO_2 capping layer of 600 nm thickness was deposited at 400 °C. Furnace annealing in nitrogen was used for the 850 °C specimens annealed from 30 to 480 min and for the 950 °C specimens annealed from 15 to 30 min. Rapid thermal annealing in nitrogen, using a single wafer machine with lamp arrays, was used for the 950 °C specimens annealed from 2 to 300 s, the 1015 °C specimens annealed from 4 to 120 s, and the 1065 °C specimens annealed from 2 to 75 s. At 850 and 950 °C, specimens given a HF dip and specimens given an RCA surface treatment were both annealed. However, more HF specimens were available than RCA specimens so unless otherwise stated the 850 and 950 °C results given in this article are for HF specimens. At 1015 and 1065 °C, RCA specimens only were annealed.

The layer sheet resistances were measured using a four point probe at 22 °C. The sheet resistance of an n^+ -polysilicon layer on single-crystal silicon gives an indication of the occurrence of epitaxial regrowth because a decrease in resistance takes place when the polycrystalline material regrows as single-crystal material.¹⁶ The sheet resistance method provides rapid information and helps with the selection of specimens for subsequent TEM and SIMS studies. The TEM images were obtained using $\langle 110 \rangle$ cross-sectional specimens and a Philips CM20 operated at 200 keV. SIMS analysis was performed for fluorine and arsenic using O_2^+ primary ion beam bombardment. The oxide capping layer was removed before making the SIMS analyses.

The TEM cross-sectional images of the polysilicon layer/single-crystal silicon wafer specimens were obtained after initially tilting the thinned specimen in the microscope to the $\langle 110 \rangle$ on-axis diffraction condition of the wafer. Because the polysilicon grains were crystallographically randomly oriented, the individual grains were not then set to any specific diffraction conditions. Consequently, any small defects within the grains requiring specific diffraction conditions, e.g., small dislocation loops, were generally not imaged. However, defects within the grains that were less sensitive to the diffraction conditions, e.g., precipitate particles and microtwins, were imaged.

Due to the low contrast between a thin amorphous oxide layer and polysilicon grains not set to specific diffraction conditions, the TEM cross-sectional images in the present work did not directly show the initial breakup of the thin interfacial oxide layer when holes were beginning to occur in

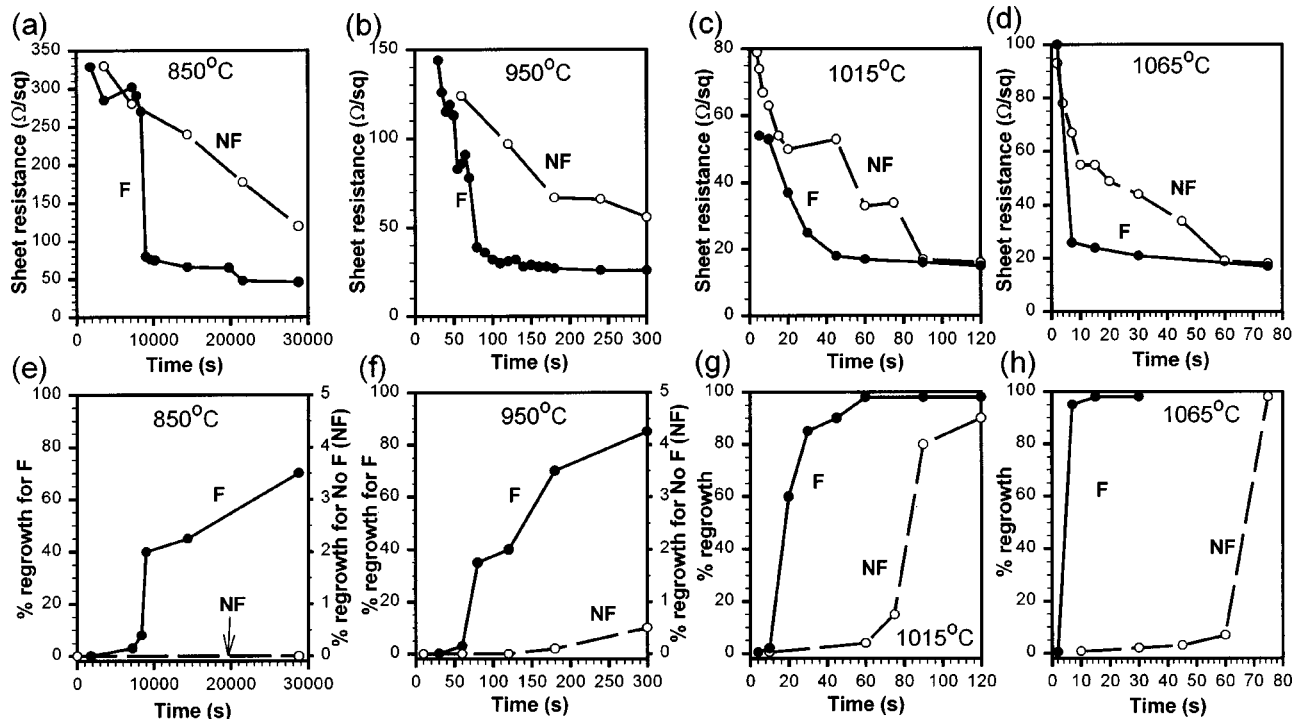


FIG. 1. Polysilicon layers implanted with either $1 \times 10^{16} \text{ cm}^{-2} \text{ F}^+$ and $1 \times 10^{16} \text{ cm}^{-2} \text{ As}^+$ (F specimens) or $1 \times 10^{16} \text{ cm}^{-2} \text{ As}^+$ only (NF specimens) and annealed at 850, 950, 1015, and 1065 °C. Sheet resistance [(a)–(d)] and the amount (average fractional volume expressed as a percentage) of polysilicon epitaxially regrown to single-crystal silicon [(e)–(h)] as a function of the anneal time. For each temperature the sheet resistance graph is above the regrowth graph and the resistance and regrowth graphs have the same time scales to facilitate comparisons.

the layer. However, this stage could be identified by the initial roughening of the interface that was observed when the single-crystal silicon of the wafer initially grew epitaxially through the holes in the interfacial oxide and into the polysilicon layer. The TEM images directly showed the subsequent stages of the oxide breakup and epitaxial regrowth.

III. RESULTS

A. Structures

TEM showed that the deposited polysilicon layers generally consisted of columnar grains 10–20 nm across. The surfaces of the layers ranged from relatively smooth to slightly rough and there were sometimes surface pits. When the layers were implanted with F^+ plus As^+ (F specimens) or As^+ only (NF specimens), the upper part of the layer was amorphized from the surface to depths of 175 and 105 nm, respectively. On annealing, the amorphous material rapidly crystallized, giving irregular grains. In general, as annealing proceeded, for the 850 and 950 °C F specimens, the grains in the upper part of the layer were equiaxed and increased to ~ 150 nm while the columnar grains in the lower part increased to 25–40 nm across. For the 1015 and 1065 °C specimens, all of the grains were equiaxed and increased to ~ 150 nm.

Figure 1(a)–1(d) show sheet resistance as a function of anneal time for 850, 950, 1015, and 1065 °C anneals, respectively [Figs. 1(e)–1(h) are discussed later and are included in Fig. 1 for direct comparison with Figs. 1(a)–1(d)]. It is generally considered that the slow decrease in resistance that sometimes occurs initially, e.g., for the whole of the 850 °C

NF curve, is mainly due to a slow increase in the electrical activation of the arsenic in the polysilicon grains together with a decrease in the number of grain boundaries arising from grain growth, these boundaries acting as potential barriers. The fast decrease in resistance that sometimes occurs subsequently, e.g., for the middle part of the 850 °C F curve, is due to epitaxial regrowth of the polysilicon. The redistribution of silicon and arsenic atoms at the growth front increases the activation of the arsenic that was present in the grains and the elimination of the grain boundaries removes the potential barriers and makes additional arsenic available for activation.

For the 850 °C NF specimens, the slow decrease in resistance up to 28 800 s indicates no regrowth. For the 850 °C F specimens, the slow decrease in resistance up to 8400 s indicates no regrowth, the fast decrease from 8400 to 9000 s indicates significant regrowth, and the slow decrease from 9000 to 28 800 s indicates little further regrowth. Using a similar procedure for the higher temperature anneals, the following behaviors can be deduced. For 950 °C, the NF specimens are not regrown up to 300 s whereas the F specimens are regrown after 80 s. For 1015 °C, the NF specimens are regrown after 90 s and the F specimens after 45 s. For 1065 °C, the NF specimens are regrown after 60 s and the F specimens after 7 s.

TEM examinations showed that, for the 950 °C F specimens annealed for 10 s [Fig. 2(a)], no interfacial oxide breakup or polysilicon layer regrowth was observed. For an anneal of 30 s, the oxide was beginning to break up and small areas of regrowth extending into the polysilicon were

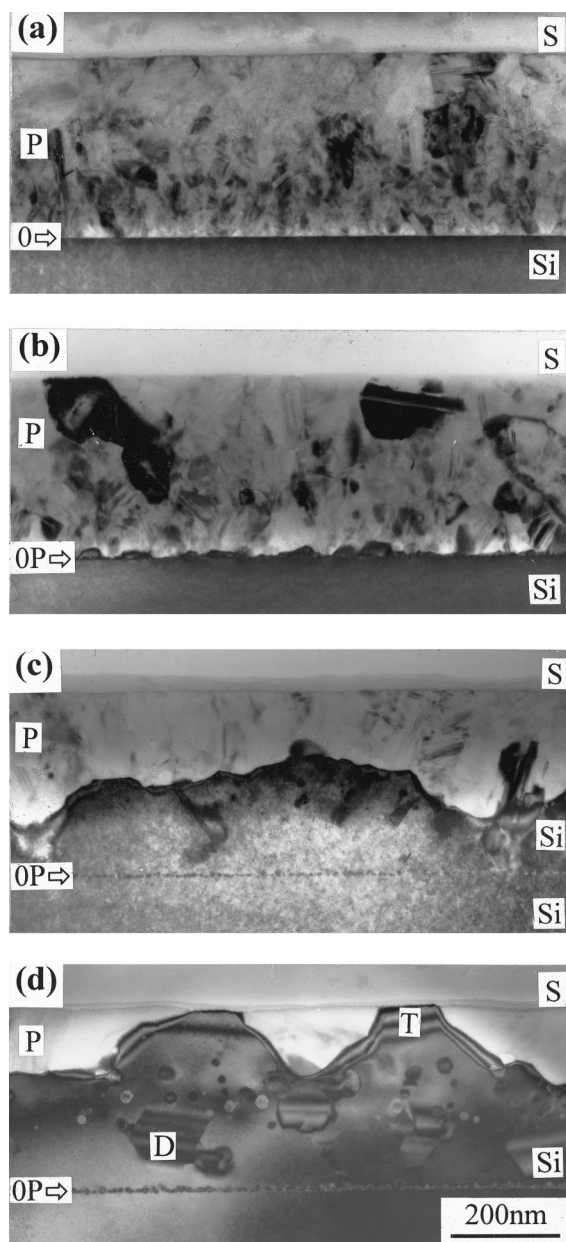


FIG. 2. Cross-sectional TEM micrographs of F specimens annealed at 950 °C for (a) 10, (b) 60, (c) 120, and (d) 300 s showing progressive stages of interfacial oxide breakup and polysilicon epitaxial regrowth (P=polysilicon, O=oxide, OP=oxide particles, D=stacking faults and twins, T=thickness fringes from inclined silicon/polysilicon boundary, S=surface).

just visible. For a 60 s anneal [Fig. 2(b)], the oxide was broken up and the small local areas of regrowth extended up to 45 nm into the polysilicon. This regrowth was pinned to the interfacial oxide and corresponded to a layer regrowth of 3% (the average fractional volume of the polysilicon layer regrown to single-crystal silicon deduced from the TEM images). For a 120 s anneal [Fig. 2(c)], the regrown polysilicon was no longer pinned to the interfacial oxide, there was a single wavy polysilicon/silicon growth front, and the regrowth was 40%. This behavior where the growth front has completely broken away from the oxide while no local region of the growth front is further than approximately half-way to the surface is termed here “parallel” regrowth. A

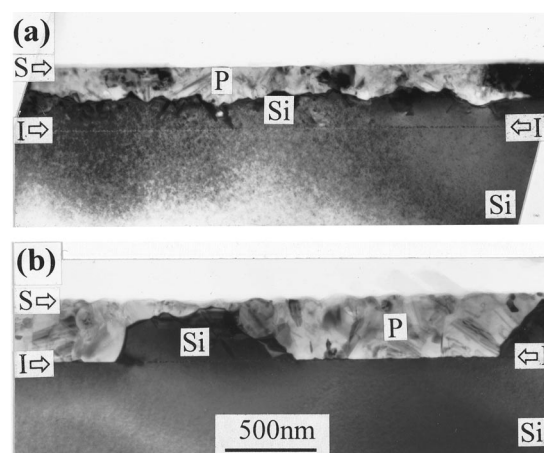


FIG. 3. Cross-sectional TEM micrographs showing (a) parallel polysilicon epitaxial regrowth, F specimen annealed at 950 °C for 120 s and (b) perpendicular polysilicon epitaxial regrowth, NF specimen annealed at 1015 °C for 75 s (I=position of original polysilicon layer/silicon wafer interface, P=polysilicon, S=surface).

lower magnification micrograph of this specimen which better illustrates parallel regrowth is shown in Fig. 3(a). For a 300 s anneal [Fig. 2(d)], some areas of regrowth extended to the polysilicon layer surface and the regrowth was 85%. For a 1800 s anneal the regrowth was 97%. The last small areas of the polysilicon adjacent to the layer surface were slow to regrow. During the regrowth, inclined stacking faults and twins formed in the single-crystal material and had number densities of typically 10^9 – 10^{10} cm⁻² (calculated for plan view). For the 950 °C NF specimens annealed for 60 s, no oxide breakup or polysilicon regrowth was observed. For anneals of 180, 900, and 1800 s, the oxide was broken up and the regrowths were 0.2%, 0.5%, and 1.0%, respectively.

For the 850 °C F specimens, the regrowth sequences were similar to those of the 950 °C F specimens, but with longer time scales. For the 1015 °C F and NF specimens and the 1065 °C F specimens, there were large variations in the amounts of regrowth along the interface. In some regions where regrowth started in a local area, it rapidly continued and often reached the polysilicon layer surface before any significant regrowth had occurred in the adjacent local areas. Here this behavior is called “perpendicular” regrowth. Figure 3(b) shows this regrowth for a 1015 °C NF specimen annealed for 75 s. For the 1065 °C F specimens, the regrowth occurred so rapidly that with the specimens available it was not possible to observe the intermediate stages of the regrowth sequence.

TEM showed for all of the specimens, except the 850 and 950 °C NF specimens, that the interfacial oxide layer progressively broke up during the annealing to give an array of small defects along the interface. These defects in a 950 °C F specimen annealed for 180 s (70% regrowth) are shown in Fig. 4(a) and a defect in a 950 °C F specimen annealed for 900 s (90% regrowth) is shown in the inset (defects present in regrown single-crystal silicon). The defect contrast, i.e., bright or dark, depends on the depth of the defect in the TEM thin foil specimen. For the 950 °C F speci-

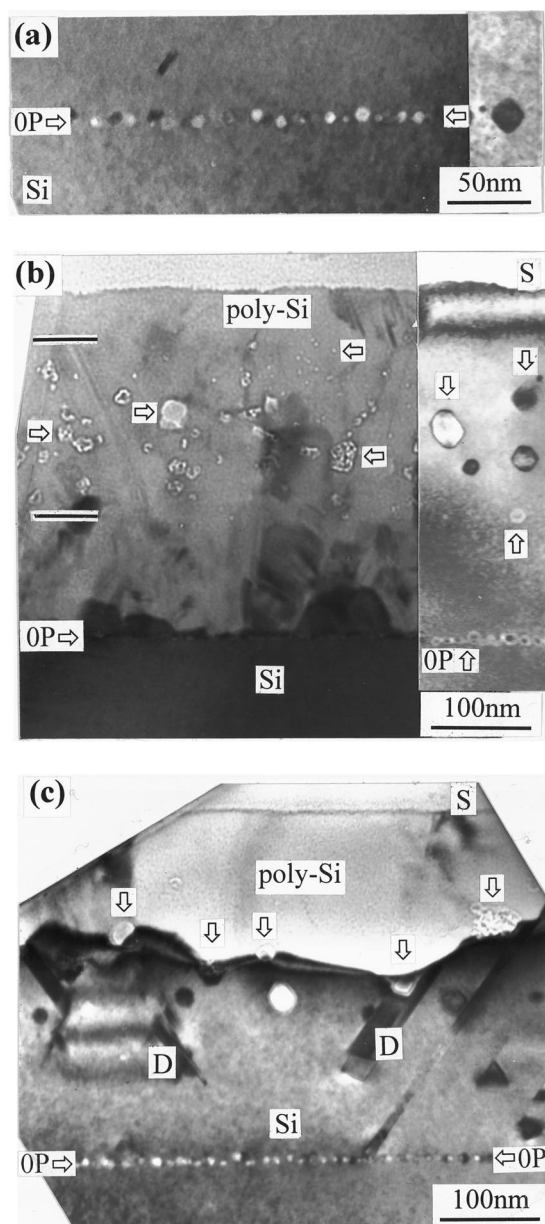


FIG. 4. Cross-sectional TEM micrographs of F specimens annealed at 950 °C for (a) faceted interfacial oxide particles after annealing for 180 s (shown by arrows) (the inset is after 900 s), (b) inclusions (shown by arrows) present in a band (between dark lines) in the polysilicon after annealing for 60 s [the inset shows faceted inclusions (indicated by arrows) in regrown single crystal silicon after annealing for 300 s], and (c) inclusions at the polysilicon/silicon growth front (shown by arrows) and also in the polysilicon and regrown silicon, after annealing for 180 s (OP=interfacial oxide particles, D=stacking faults and twins, S=surface).

mens annealed for 120, 300, 900, and 1800 s, the average defect sizes were 8, 10, 16, and 16 nm, respectively, and the larger defects were faceted. These interfacial defects occurred in both the F and NF specimens and are considered to be some form of oxide particle.

In order to assess the separate effects of fluorine and arsenic on the initial breakup of the interfacial oxide and the initial regrowth of the polysilicon layer during annealing, a comparison was made of undoped polysilicon layers that were either not implanted, implanted with As^+ only, implanted with F^+ only, or implanted with F^+ plus As^+ . TEM

showed that, compared with the unimplanted layers, the initial breakup and regrowth were increased by the As^+ only, the increases were greater for the F^+ only, and they were much greater for the F^+ plus As^+ .

For the F specimens, a band of small defects arose in the layer during annealing. The defects formed in the polysilicon, increased in size, and the increase continued in the regrown single-crystal silicon. For the 950 °C F specimens, for a 60 s anneal (3% regrowth), the defects were irregular in shape with sizes ranging from typically 5 to 30 nm and the larger defects occurred in the middle of the band, i.e., at a depth of ~ 130 nm [Fig. 4(b) shows defects present in polycrystalline silicon]. For a 300 s anneal (85% regrowth), the defect sizes ranged from typically 15 to 30 nm [the inset in Fig. 4(b) shows defects present in regrown single-crystal silicon]. For a 180 s anneal (70% regrowth), these defects occurred in the polysilicon, at the polysilicon/single-crystal silicon growth front, and in the regrown single-crystal silicon [Fig. 4(c)]. These defects in the regrown single-crystal silicon were faceted. For these defects at the growth front, the surfaces of the individual defects protruding into the regrown single-crystal silicon were faceted. For anneals of 10, 60, 120, and 300 s, the average defect sizes were 4, 17, 20, and 22 nm, respectively, and the number densities were 80, 5, 4, and $2 \times 10^{10} \text{ cm}^{-2}$, respectively (referred to as plan view). In addition, the depths of the upper boundary of the defect band were 30, 40, 60, and 85 nm, respectively, while the depths of the lower boundary were closely constant at 235 nm, i.e., the width of the defect band progressively decreased. Similar bands of defects occurred in the F specimens annealed at 850, 1015, and 1065 °C. However, these defects did not occur in the NF specimens and hence they are considered to be associated with the presence of the fluorine. These defects could be solid particles, liquid droplets, or gaseous bubbles and we shall initially refer to them as fluorine inclusions.

The amounts of regrowth determined from TEM for the F and NF specimens annealed at 850, 950, 1015, and 1065 °C are plotted as a function of anneal time in Figs. 1(e)–1(h). In general, each curve shows three successive stages of regrowth corresponding to slow, fast, and slow regrowth. Exceptions are that for the 850 °C NF specimens, there is no regrowth, while for the 950 °C NF specimens, only part of stage 1 occurs. The TEM structural results show that stage 1 corresponds to the initial interfacial oxide breakup and the initial polysilicon layer regrowth which is pinned to the interfacial oxide. For the 850 and 950 °C F specimens, stage 2 corresponds to rapid parallel regrowth. For the 850 °C F specimens, stage 3 corresponds to the regrowth front being significantly slowed down by the band of inclusions in the polysilicon layer. For the 950 °C F specimens, stage 3 corresponds to the front being slowed down initially by the inclusions and then by a “surface” mechanism [the latter based on specimens annealed for times up to 1800 s, not shown in Fig. 1(f)]. For the 1015 °C F and NF specimens and the 1065 °C NF specimens, stage 2 corresponds to rapid perpendicular regrowth, with the amount of the growth front pinned to the interfacial oxide progressively decreasing as the anneal time increases. For these latter three sets of specimens and the 1065 °C F specimens, stage 3 cor-

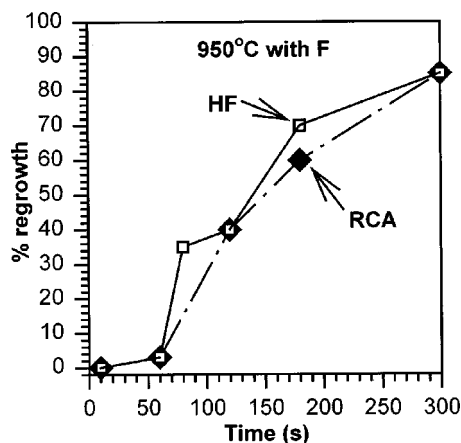


FIG. 5. F specimens annealed at 950 °C. The amount of regrowth of the polysilicon layer to single-crystal silicon for the initial silicon wafers given either HF or RCA surface treatments.

responds mainly to the surface mechanism. The latter mechanism may be associated with the pinning of the growth front by either surface pits or impurities swept to the surface region by the growth front.

The main effect of the fluorine is to decrease the time for stage 1. For example, TEM shows that the initial breakup of the interfacial oxide, which corresponds to a regrowth of $\sim 0.1\%$, takes ~ 20 s for the 950 °C F specimens compared with ~ 150 s for the 950 °C NF specimens, a decrease of $\sim 8\times$. The initial regrowth of the polysilicon for the 1015 °C F specimens is also significantly faster than for the 1015 °C NF specimens, and similarly for the 1065 °C F and NF specimens. For the F specimens annealed at 850, 950, 1015, and 1065 °C, the TEM times for complete regrowth ($>90\%$) are $>28\,800$, 900, 45, and 8 s, respectively. The corresponding times deduced from resistivity measurements were similar to the TEM times for the 1015 and 1065 °C anneals, but were less than the TEM times for the 850 and 950 °C anneals. The reasons for this discrepancy will be discussed in Sec. IV.

A comparison was made of the regrowths occurring for the 950 °C F specimens when the initial silicon wafers had been given either HF or RCA surface treatments. TEM showed that the amounts of regrowth upon going from 10 to 300 s were insignificantly different for the two treatments (Fig. 5). A similar result was obtained for the 850 °C F specimens upon going from 1800 to 28 800 s. This result indicates that, when fluorine is present, the original thickness of the interfacial oxide, e.g., 0.6 nm for HF and 1.4 nm for RCA surface treatments,¹ has little effect on the time required to break up the interfacial oxide. This is not the case when fluorine is not present, with the breakup taking a longer time for the RCA treatment.¹ Hence in Figs. 1(e)–1(h), for the F specimens the regrowth curves at the different temperatures can be directly compared, even though the 850 and 950 °C anneals were for HF specimens and the 1015 and 1065 °C anneals were for RCA specimens. For the NF specimens this is not the case since the amount of regrowth depends both on the temperature and the surface treatment. Analogous considerations apply to Figs. 1(a)–1(d).

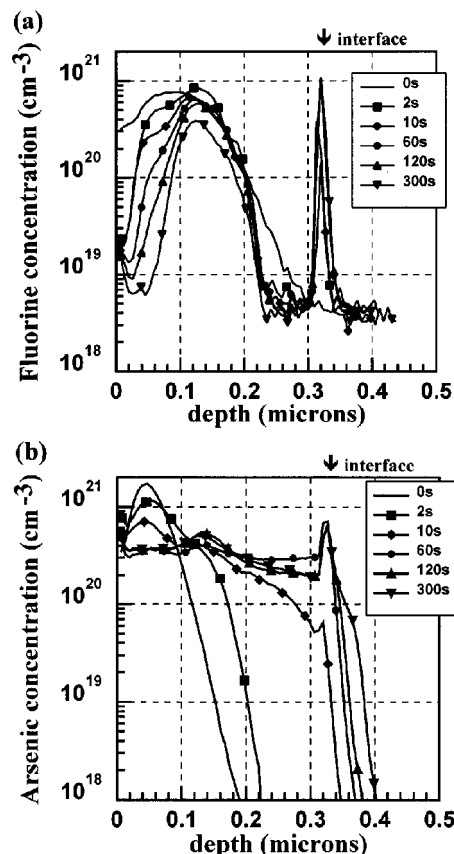


FIG. 6. F specimens as implanted and annealed at 950 °C. SIMS concentration profiles as implanted (0 s) and for anneals of 2, 10, 60, 120, and 300 s for (a) fluorine and (b) arsenic.

B. Fluorine and arsenic distributions

Figure 6(a) shows SIMS fluorine concentration profiles for the F specimens as implanted and annealed at 950 °C for different times. For the as-implanted specimen, there is a broad peak in the layer at a concentration of $7.5 \times 10^{20} \text{ cm}^{-3}$ and a depth of 95 nm. For a 2 s anneal, this layer peak has shifted deeper to 130 nm and some fluorine has reached the interface, where a narrow peak occurs at a depth of 320 nm. From 10 to 300 s, the layer peak concentration progressively decreases to $4 \times 10^{20} \text{ cm}^{-3}$ with its maximum remaining at 130 nm, whereas the interface peak concentration increases to $1.0 \times 10^{21} \text{ cm}^{-3}$ for a 60 s anneal and then remains constant. For the 2 and 10 s anneals, pronounced shoulders occur at a depth of 45 nm on the layer peak. For the annealed specimens, the position of the broad layer peak corresponds closely to the observed depth of the band of inclusions. The side of the layer peak nearer the surface progressively moves deeper into the layer, i.e., there is a progressive loss of fluorine from this region of the layer, while the side nearer the interface remains at the same depth. For all anneal times, the layer and interface peaks remain separate. These fluorine profiles cannot be explained by standard diffusion behavior.

Figure 6(b) shows SIMS arsenic concentration profiles for the F specimens as implanted and annealed at 950 °C in Fig. 6(a). For the as-implanted specimen, there is a layer peak at a concentration of $1.8 \times 10^{21} \text{ cm}^{-3}$ and a depth of

TABLE I. Fluorine specimens annealed at 950 °C. Amount (%) of the polysilicon layer regrown to single-crystal silicon and the integrated fluorine (F) and arsenic (As) doses in the layer and at the interface. The F and As integrated doses are also expressed as a percentage of the implanted doses (implanted doses $F=1 \times 10^{16} \text{ cm}^{-2}$ and $As=1 \times 10^{16} \text{ cm}^{-2}$).

Anneal time (s)	Regrowth of layer (%)	F in layer		F at interface		F total		As in layer		As at interface		As total	
		(cm^{-2})	(%)	(cm^{-2})	(%)	(cm^{-2})	(%)	(cm^{-2})	(%)	(cm^{-2})	(%)	(cm^{-2})	(%)
0	0	1×10^{16}	100	0	0	1×10^{16}	100	1×10^{16}	100	0	0	1×10^{16}	100
2	0	8.9×10^{15}	89	1.5×10^{14}	1.5	9×10^{15}	90	1×10^{16}	100	0	0	1×10^{16}	100
4	0	8.3×10^{15}	83	2.0×10^{14}	2.0	8.5×10^{15}	85	1×10^{16}	100	0	0	1×10^{16}	100
10	<0.1	7.9×10^{15}	79	3.9×10^{14}	3.9	8.3×10^{15}	83	9.9×10^{15}	99	1.4×10^{14}	1.4	1×10^{16}	100
60	3	6.5×10^{15}	65	1.0×10^{15}	10	7.5×10^{15}	75	8.6×10^{15}	86	1.4×10^{15}	14	1×10^{16}	100
120	40	5.5×10^{15}	55	1.2×10^{15}	12	6.7×10^{15}	67	8.2×10^{15}	82	1.8×10^{15}	18	1×10^{16}	100
300	85	3.4×10^{15}	34	1.4×10^{15}	14	4.8×10^{15}	48	7.7×10^{15}	77	2.2×10^{15}	22	9.9×10^{15}	99

45 nm. For a 2 s anneal, the peak concentration has decreased and the arsenic has penetrated further into the polysilicon layer. For a 10 s anneal, the peak concentration has further decreased and some arsenic has reached the interface, where a small narrow peak occurs at a depth of 320 nm. From 60 to 300 s the layer peak at 45 nm is replaced by a layer peak at 130 nm which increases to a concentration of $5 \times 10^{20} \text{ cm}^{-3}$. The interface peak increases to a concentration of $7 \times 10^{20} \text{ cm}^{-3}$ at 60 s and then remains constant. For an anneal of 300 s, there is arsenic penetration into the underlying silicon wafer. These arsenic profiles can be explained by standard arsenic diffusion behavior in polysilicon^{23–25} modified by arsenic segregation at the layer fluorine inclusions and the interfacial oxide.

Fluorine and arsenic integrated doses for the interface and the polysilicon layer of the F specimens annealed at 950 °C are shown in Table I. The interface arsenic doses for the longer anneal times include the arsenic tails that extend into the underlying silicon wafer. From 0 to 300 s, the interface fluorine dose progressively increases from 0 to $1.4 \times 10^{15} \text{ cm}^{-2}$, the layer fluorine dose progressively decreases from 1×10^{16} to $3.4 \times 10^{15} \text{ cm}^{-2}$ and the sum of these two doses progressively decreases from 1×10^{16} to $4.8 \times 10^{15} \text{ cm}^{-2}$. This progressive loss of fluorine from the specimen, taken as the implanted fluorine dose of $1 \times 10^{16} \text{ cm}^{-2}$ minus the sum of the interface and layer fluorine doses, is considered to be due to fluorine gettering by the oxide capping layer and possibly fluorine diffusion through the interface oxide and into the silicon wafer. From 0 to 4 s the interface arsenic dose is zero, from 10 to 60 s it increases rapidly from 1.4×10^{14} to $1.4 \times 10^{15} \text{ cm}^{-2}$, and from 120 to 300 s it increases slowly from 1.8 to $2.2 \times 10^{15} \text{ cm}^{-2}$. From 0 to 300 s, the layer arsenic dose progressively decreases from 1×10^{16} to $7.7 \times 10^{15} \text{ cm}^{-2}$. There is no significant loss of arsenic from the specimen. Figure 7 shows the fluorine and arsenic doses at the interface from 0 to 60 s.

IV. DISCUSSION

We first consider the F specimens and the roles played by the fluorine and arsenic in the initial breakup of the interfacial oxide, which corresponds to $\sim 0.1\%$ polysilicon layer regrowth (first part of stage 1). Upon annealing at 950 °C, TEM shows that this initial breakup corresponds to ~ 20 s.

SIMS shows that fluorine arrives at the interface before 2 s and arsenic arrives between 4 and 10 s (Fig. 7 and Table I). The interface fluorine and arsenic doses subsequently increase with the arsenic dose becoming larger than the fluorine dose after 30 s. These results indicate that the increase in the oxide breakup of the F specimens is due to the fluorine acting initially on its own and subsequently in combination with the arsenic. Although fluorine and arsenic concentrations were only determined for 950 °C, it is likely that analogous behavior occurs at 850, 1015, and 1065 °C.

The oxide breakup sequence consists of a progressive structural change from a thin oxide sheet to an array of discrete oxide particles. This is generally considered to be driven by the progressive decrease in the total area of the oxide/silicon interface, and hence in the total oxide/silicon interfacial energy (here silicon means single-crystal silicon and polysilicon). These structural changes in the oxide occur by bulk diffusion in both the oxide and the adjacent silicon together with surface diffusion at the oxide/silicon interface.

We now suggest a number of mechanisms to explain why the fluorine increases the breakup of the interfacial oxide. These are based partly on mechanisms suggested previously by other workers to explain the thermal oxidation of silicon^{26–30} and partly on some of our previous interfacial oxide annealing results.³¹

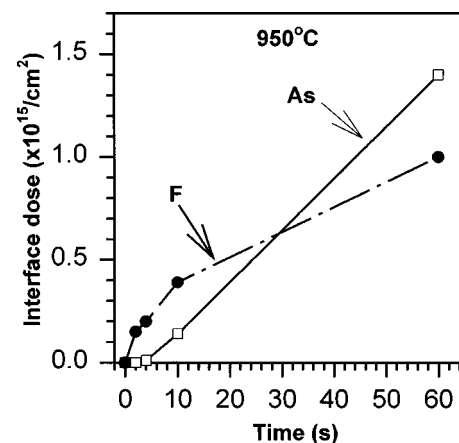


FIG. 7. F specimens annealed at 950 °C. Integrated fluorine (F) and arsenic (As) doses at the polysilicon/silicon interface as a function of anneal time.

First, fluorine is more electronegative than both oxygen and silicon³² and so fluorine readily breaks strained Si–O bonds. Hence, when fluorine is present in the interfacial oxide, the long chains of Si–O–Si are broken by the fluorine into shorter chains incorporating Si–F (Refs. 26, 29, and 33) and possibly O–F (Refs. 34 and 35) bonds. The creation of these shorter chains would decrease the viscosity of the oxide at these temperatures and hence increase the rate at which the structural changes occur in the oxide. Second, the oxygen atoms in the oxide freed by the formation of the Si–F bonds can diffuse to the oxide/silicon interface and oxidize the silicon there. This would increase the rate of oxide restructuring. Third, fluorine present at the oxide/silicon interface readily breaks Si–Si bonds at the interface to form Si–F bonds plus Si dangling bonds.^{30,36,37} The latter bonds can capture oxygen atoms³⁰ and this would increase the rate of oxide restructuring. Fourth, fluorine present at the interfacial oxide can under some conditions cause the discrete oxide particles to form a band at the interface (as viewed in cross section)³¹ rather than a planar array. It was suggested that this behavior could be explained by fluorine increasing the diffusion of the oxygen in the silicon during the annealing.³¹ If such an increased oxygen diffusion occurred in the F specimens of the present work, then this could also contribute to the oxide restructuring.

The initial polysilicon to single-crystal silicon regrowth (second part of stage 1) also occurs faster for the F specimens. When regrowth starts, the silicon/polysilicon growth front is pinned to the breaking up oxide at various places along the interface. As regrowth proceeds, the oxide structure coarsens, the number of pinning points decreases, and the growth front becomes progressively unpinned. It is considered that this initial polysilicon regrowth is faster for the F specimens mainly because the interfacial oxide breaks up faster. Once the growth front has become significantly unpinned from the interfacial oxide, rapid epitaxial growth occurs (stage 2) and this continues until the growth front becomes pinned by the inclusions, surface pits, or impurities swept to the surface (stage 3).

The slowing down of the growth front when close to the layer surface, i.e., after approx 80%–90% regrowth, occurs for 950, 1015, and 1065 °C anneals. For 1015 °C, the slowing down is similar for both the F and NF specimens [Fig. 1(g)] so pinning by fluorine does not seem to be responsible. For the 950 °C F specimens, TEM showed that the slowing down occurs upon going from 300 to 1800 s [not shown in Fig. 1(f)]. No SIMS arsenic profiles were available for these anneal times at 950 °C or for any time at the other anneal temperatures. Hence it is not possible to tell whether the arsenic had been swept into the surface region during regrowth; if it had, pinning by arsenic could be responsible. Other impurities, e.g., oxygen which was shown by SIMS to be present in other polysilicon layers deposited using the same equipment, could also be responsible.

Two types of regrowth occur, parallel for the 850 and 950 °C specimens and perpendicular for the 1015 and 1065 °C specimens. A possible reason for this is that, although both the rate of polysilicon regrowth and the rate of interfacial oxide breakup increase with temperature, the in-

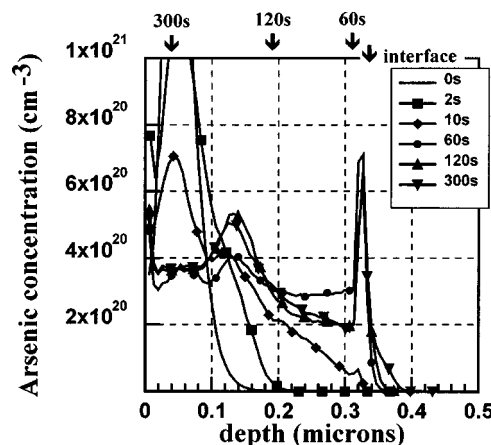


FIG. 8. F specimens annealed at 950 °C. The SIMS arsenic concentration profiles of Fig. 6(b) are replotted with a linear concentration scale. The interface and the average position of the polysilicon/silicon regrowth front are indicated by arrows for 60, 120, and 300 s anneals.

crease is greater for the polysilicon regrowth. Hence at the higher temperatures, once the interface oxide has broken up in one region, considerable regrowth will occur in that region before any regrowth starts in the adjacent regions. A further possible contribution is that, at the higher temperatures, larger grains form in the polysilicon adjacent to the interface, i.e., more widely spaced grain boundaries occur, and this causes the elastic strains and the arsenic concentrations along the interface to be less uniformly distributed. Consequently, the holes that arise in the interfacial oxide and the associated regrowth regions that form occur at a smaller number of places along the interface. Hence at the higher temperatures, perpendicular rather than parallel regrowth occurs.

With regard to the diffusion of fluorine and arsenic in the polysilicon at 950 °C, some fluorine travels from the implanted fluorine peak to the interface a distance L of ~ 150 nm in a time t of 2 s [Fig. 6(a)]. Use of the equation $L^2 = 2Dt$ then gives a value for the effective diffusivity D of fluorine in polysilicon at 950 °C of $\sim 6 \times 10^{-11} \text{ cm}^2 \text{ s}^{-1}$. This is to our knowledge the first time a diffusivity value has been reported for fluorine in polysilicon. Some arsenic travels ~ 200 nm in 10 s, giving an effective diffusivity at 950 °C of $\sim 2 \times 10^{-11} \text{ cm}^2 \text{ s}^{-1}$. This can be compared with values at 950 °C in the literature of 3×10^{-14} – $1 \times 10^{-11} \text{ cm}^2 \text{ s}^{-1}$.²³ In single-crystal silicon the arsenic diffusivity increases when the free carrier concentration exceeds the intrinsic carrier concentration $n(i)$ at the diffusion temperature.²³ This occurs for all four of our temperatures, e.g., $n(i)$ is $\sim 5 \times 10^{18} \text{ cm}^{-2}$ at 950 °C and the peak arsenic concentration is $> 1 \times 10^{21} \text{ cm}^{-3}$ after implantation and $> 3 \times 10^{20} \text{ cm}^{-3}$ after 10 s at 950 °C in our layers (Fig. 6). Hence our 950 °C value at the high end of the range in the literature may be due to the high peak arsenic concentration in our layers.

In order to reveal the arsenic diffusion behavior for the 950 °C F specimens more clearly, the SIMS arsenic profiles in Fig. 6(b) are replotted using a linear concentration scale in Fig. 8. From 10 to 60 s, the layer arsenic peak at a depth of 45 nm becomes smaller whereas the layer arsenic peak at 130 nm becomes more pronounced, the arsenic concentra-

tions in the lower part of the layer increase and the interface arsenic dose increases, i.e., arsenic is transferred from the upper to the middle and lower parts of the layer. From 60 to 120 s, the arsenic concentration in the lower part of the layer decreases whereas the layer arsenic peak at 130 nm becomes larger, i.e., arsenic is transferred back from the lower to the middle part of the layer. From 120 to 300 s, the arsenic distribution changes but only by a small amount.

The suggested reasons for the above are as follows. From 10 to 60 s, arsenic diffuses down the polysilicon grain boundaries to the interface. For a 60 s anneal, the polysilicon layer regrowth (average) is 3% (see arrow in Fig. 8) and many of the grain boundaries still extend to the interface. For a 120 s anneal, the regrowth is 40% and grain boundaries no longer extended to the interface. Consequently, upon going from 60 to 120 s, the arsenic fast diffusion path down the grain boundaries to the interface is progressively cutoff. Arsenic continues to arrive at the interface but at a slower rate (Table I). The moving growth front sweeps some of the arsenic ahead of it from the lower part of the layer towards the middle part. This arsenic is readily swept up in the lower part of the layer because there are no fluorine inclusions there to retain it. When this arsenic reaches the middle part of the layer, some of it segregates at the fluorine inclusions and this gives the increased peak at 130 nm. For a 300 s anneal, the regrowth is 85%. However, the arsenic is not readily swept from the middle to the upper part of the layer because most of it is retained by the fluorine inclusions, and so there is little further change in the arsenic distribution. The SIMS fluorine profiles of the F specimens [Fig. 6(a)] show no evidence of the sweeping of fluorine towards the surface as the polysilicon/silicon regrowth front moves.

With regard to the formation of the fluorine inclusions during annealing of the F specimens, it is considered that, due to the high concentrations of fluorine and arsenic and the large number of point defects present in the grains, small clusters and complexes form in a band centered at a depth of ~ 130 nm. Fluorine rapidly diffuses and is trapped by these defects and this initiates the fluorine inclusion band. Fluorine is rapidly released and trapped by the fluorine inclusions. The inclusions grow by Ostwald ripening but progressively lose fluorine to the interfacial oxide, the surface oxide capping layer, and possibly also the silicon wafer. The SIMS profiles in Fig. 6(a) do not show fluorine at the oxide capping layer because it was removed prior to the SIMS measurements.

The TEM results showed that the position of the fluorine inclusion band depended on the anneal time (Table II) and the temperature. For 950 °C, the fluorine concentrations at the position of the upper boundary of the band, taken from the individual SIMS profiles in Fig. 6(a), were all in the range of $4\text{--}5.5 \times 10^{19} \text{ cm}^{-3}$, and at the lower boundary were all in the range of $2\text{--}6 \times 10^{19} \text{ cm}^{-3}$ (Table II). Similar concentrations at the edges of the bands for all the times are characteristic of a precipitation process.

For these 950 °C F specimens, the upper boundary of the band of fluorine inclusions moves deeper into the layer due to progressive loss of fluorine from this region. For anneals of 2 and 10 s, a pronounced shoulder occurs on the fluorine

TABLE II. F specimens annealed at 950 °C. Shown are the depths of the edges of the inclusions bands, the fluorine concentration at these depths, and the widths of the inclusion bands.

Anneal time (s)	Upper edge of inclusion band		Lower edge of inclusion band		Width of inclusion band (nm)
	Depth (nm)	Fluorine concentration (cm^{-3})	Depth (nm)	Fluorine concentration (cm^{-3})	
10	30	5.5×10^{19}	235	$2\text{--}6 \times 10^{19}$	205
60	40	5×10^{19}	235	$2\text{--}6 \times 10^{19}$	195
120	60	4×10^{19}	230	$2\text{--}6 \times 10^{19}$	170
300	85	5×10^{19}	240	$2\text{--}6 \times 10^{19}$	155

profiles at a depth of 45 nm [Fig. 6(a)], which corresponds to the depth of the main peak of the arsenic profiles [Fig. 6(b)]. For anneals of 60 s and longer, these fluorine shoulders and arsenic peaks do not occur or are small. This suggests that there is an association between the fluorine and arsenic for high arsenic concentrations and so more fluorine is retained. The mechanism for this may be that arsenic clusters form at a depth of 45 nm and trap fluorine. This additional fluorine is responsible for the shoulders and these arsenic/fluorine defects are more stable when the local arsenic concentration [Fig. 6(b)] is above or close to the 950 °C arsenic solubility limit in silicon of $\sim 1 \times 10^{21} \text{ cm}^{-3}$. Conversely, upon annealing, the lower boundary of the inclusion band does not move significantly. The suggested reason is that the initiating defects for the inclusions in this region are the ion implantation end-of-range defects that are considered to be present immediately beneath the amorphous/polysilicon interface which occurred at a depth of 175 nm. These defects may be more stable than the other initiating defects and so most of the fluorine in this region is retained.

For these specimens, from the sizes and number densities of the inclusions determined by TEM (Sec. III A), the total volume of the inclusions in each band was calculated and converted to the total number of silicon vacancies, assuming that the inclusions were voids. This was then compared with the total number of fluorine atoms in the band obtained from the SIMS fluorine doses of Table I. For anneals of 10, 60, 120, and 300 s, the silicon vacancy/fluorine atom ratios were ~ 0.1 , 1.1, 1.4, and 2, respectively. If most of the fluorine is in the inclusions, as seems likely, then these ratios would indicate that the inclusions contain closely packed fluorine atoms. This suggests that the inclusions are not fluorine bubbles but could be fluorine precipitate particles.

Other workers have used TEM and transmission electron diffraction (TED) to investigate metals and semiconductors implanted with high doses of rare gases and then annealed, e.g., copper, nickel, and gold implanted with Kr^+ (Ref. 38) and aluminum and silicon implanted with Xe^+ .³⁹ The experimental results directly showed that what had previously been considered to be gas bubbles were crystalline particles or liquid droplets of the implanted element, with the physical state depending on the temperature and internal pressure. Thermodynamical calculations were in agreement with the experimental results.³⁹ For the fluorine inclusions of the

present work, TEM and TED examinations performed at room temperature did not reveal evidence of their crystallinity. However, the inclusions could be amorphous particles or liquid droplets. Further work is required to clarify this.

With regard to the sheet resistance method, the times for the polysilicon layers to be mostly regrown for the 850, 950, 1015, and 1065 °C F specimens were deduced from the change in slope of the resistance curves [Figs. 1(a)–1(d)] to be 9000, 80, 45, and 7 s, respectively. TEM showed that the regrowths for these temperatures and times for the 850, 950, 1015, and 1065 °C F specimens were 40%, 35%, 90%, and 95%, respectively. Hence for the two lower temperatures there is a discrepancy between the sheet resistance and TEM methods in determining the time at which the polysilicon layer is mostly regrown. The reason for this discrepancy is now considered.

For sheet resistivity measurements, the current flow is mainly parallel to the specimen surface. For the 850 °C F specimens, as the regrowth proceeds, a channel of single-crystal material parallel to the interface forms (parallel regrowth); this has a lower resistivity than the polysilicon layer above and the silicon wafer below, so the sheet resistance decreases rapidly. However, when the regrowth is 40%, the polysilicon/silicon regrowth front reaches the inclusion band and the inclusions significantly slow down the advancing growth front, so the sheet resistance subsequently slowly decreases. Consequently, the resistance method predicts that the polysilicon is mostly regrown when the regrowth is only 40%. For the 950 °C F specimens, similar behavior occurs although the slowing of the growth front by the inclusions is less pronounced.

For the 1015 °C F specimens, the inclusions have little effect on slowing the growth front, so a rapid decrease in sheet resistivity corresponding to most of the regrowth range might be expected. However, in many regions perpendicular regrowth occurs, so the current flow parallel to the specimen surface has to cross alternating regions of regrown and unregrown material. As annealing proceeds, the width of the regrown regions progressively increases, so the sheet resistance progressively decreases. A regrown channel parallel to the interface and free from grain boundaries does not form until the polysilicon is mostly regrown. Consequently, the resistance method correctly predicts when the polysilicon is mostly regrown although the slope of the resistance curve changes gradually rather than abruptly. A more detailed analysis of these parallel and perpendicular regrowth behaviors will be reported at a later date.⁴⁰

TABLE III. Anneal times required to give 1% and 50% regrowth of the polysilicon layer for NF and F specimens for anneal temperatures of 850, 950, 1015, and 1065 °C.

Specimen	Anneal temperature (°C)	Anneal time (s)	
		1% regrowth	50% regrowth
NF	850	>28 800	>28 800
NF	950	1800	>1800
NF	1015	30	80
NF	1065	15	65
F	850	3600	17 000
F	950	45	150
F	1015	6	20
F	1065	3	5

For the 1065 °C F specimens, the inclusions have virtually no effect on slowing the growth front. Furthermore, the regrowth is so rapid that, upon going from 2 to 7 s (no intermediate specimens were available), the polysilicon completely regrows. Consequently, the resistance decreases rapidly from 2 to 7 s and slowly thereafter, so the resistance method correctly predicts when the polysilicon is mostly regrown.

With regard to the effects of the initial wafer clean on the subsequent polysilicon regrowth behaviors, some possible mechanisms are as follows. For F specimens, the interfacial oxide is broken up rapidly for both the HF clean (thin oxide) and the RCA clean (thick oxide), so these surface treatments do not significantly affect the polysilicon layer regrowth times (Fig. 5). Conversely, for NF specimens, the oxide is broken up slowly and it takes longer for the thicker RCA oxide than the thinner HF oxide, so for the RCA oxide the initial polysilicon regrowth starts later. In addition, the larger volume of the RCA oxide present at the interface increases the time for the polysilicon/silicon growth front to break away from the oxide, so the initial regrowth also takes longer. From these results it follows for F specimens that any variations that may be present in the initial interfacial oxide thickness across individual wafers will not significantly affect the subsequent polysilicon regrowth or the polysilicon emitter bipolar transistor characteristics.

From the bipolar point of view, the annealing (emitter drive-in) conditions are often selected so as to use the lowest thermal budget that will give a low emitter resistance. This occurs when the interfacial oxide is partly broken up and the amount of epitaxial regrowth is ~1% (Ref. 9) (case B, Sec.

TABLE IV. Anneal temperatures, deduced from the results of Table III, required to give 1% and 50% polysilicon regrowth for NF and F specimens for anneal times of 30, 300, and 3000 s.

Specimen	Anneal temperatures (°C) required for 1% regrowth and different anneal times			Anneal temperatures (°C) required for 50% regrowth and different anneal times		
	30 s	300 s	3000 s	30 s	300 s	3000 s
NF	1015	975	940	>1065	990	955
F	960	905	855	1000	935	880

I). Alternatively, a higher thermal budget is used to give a slightly lower emitter resistance and more reproducible device characteristics, but a deeper junction. This occurs when the interfacial oxide is completely broken up and the amount of epitaxial regrowth is $\sim 50\%$ (case C, Sec. I).

Various combinations of annealing temperature and time to give 1% and 50% regrowth for the NF and F specimens, taken from the TEM results of Figs. 1(e)–1(h) [and also from TEM results for 950 °C anneals from 300 to 1800 s not included in Fig. 1(f)], are given in Table III. From these data the temperatures required for three different annealing times to give 1% and 50% regrowth for the NF and F specimens were deduced (Table IV). Errors for the temperatures in Table IV are estimated to be in the range of ± 10 – ± 20 °C. These results show that for 1% regrowth and a 30 s anneal, the temperature decreases from 1015 °C for a NF specimen to 960 °C for a F specimen. For 50% regrowth and a 30 s anneal, the corresponding temperatures are >1065 and 1000 °C.

V. SUMMARY AND CONCLUSIONS

LPCVD polysilicon layers were deposited on (100) silicon wafers, implanted with $1 \times 10^{16} \text{ cm}^{-2} \text{ F}^+$ plus $1 \times 10^{16} \text{ As}^+$ and annealed at 850, 950, 1015, or 1065 °C (F specimens) or similarly processed without the F^+ implant (NF specimens). For the F and NF specimens, three stages of polysilicon layer regrowth were distinguished. Stage 1 corresponded to the initial interfacial oxide breakup plus the initial polysilicon regrowth with the polysilicon/silicon growth front still pinned to the interface (slow regrowth). Stage 2 was the regrowth after the growth front had broken away from the interface (fast regrowth). Stage 3 was the subsequent regrowth which was affected by either a band of fluorine inclusions that formed in the middle of the layer (F specimens only) or a mechanism associated with the polysilicon layer surface (slow regrowth). Investigation of the inclusions suggested that they were fluorine particles or droplets rather than fluorine bubbles. The main effect of the fluorine was to decrease the times for the initial breakup of the interfacial oxide (by $\sim 8\times$) and the initial epitaxial regrowth of the polysilicon layer, and hence to decrease the time for stage 2 to start. Two regrowth mechanisms were distinguished. For the specimens annealed at 850 and 950 °C, a single channel of regrown material parallel to the interface formed, whereas for the specimens annealed at 1015 °C, many channels of regrown material perpendicular to the interface formed. The parallel and perpendicular regrowths affected the layer sheet resistance in different ways.

For the F specimens, upon annealing the band of fluorine inclusions grew by Ostwald ripening and fluorine diffused from the inclusions to the interfacial oxide, the oxide capping layer, and possibly the silicon wafer. Arsenic diffused in the polysilicon to the interfacial oxide and the silicon wafer, with segregation occurring at the fluorine inclusions. The fluorine increased the initial breakup of the interfacial oxide because it arrived at the interface before the arsenic and because the oxide breakup rate (determined by separate experiments) was increased more by fluorine than by arsenic. Ef-

fective diffusivities for fluorine and arsenic in polysilicon at 950 °C were deduced to be ~ 6 and $\sim 2 \times 10^{-11} \text{ cm}^2 \text{ s}^{-1}$, respectively. The former is to our knowledge the first diffusivity value reported for fluorine in polysilicon.

For the F specimens annealed at 850 and 950 °C, the amount of polysilicon regrowth did not depend significantly on the thickness of the interfacial oxide, in contrast to our previous results¹ for similar specimens without fluorine. Hence, the introduction of fluorine into the polysilicon enables the same regrowth to be achieved independent of which initial wafer surface clean is used. It should also give better control of the amount of regrowth occurring and hence more reproducible polysilicon bipolar transistor characteristics because they will be independent of any local variations in the oxide thickness on individual wafers and from wafer to wafer. In all cases, for the F specimens compared with the NF specimens, either a greater amount of polysilicon regrowth occurred at the same temperature or the same amount of regrowth occurred at a lower temperature. The decreases in anneal temperature for particular anneal times when fluorine was present were determined for 1% and 50% regrowth, two cases that are important for polysilicon emitter bipolar transistors. The significant decreases that resulted are important for these kinds of transistors where lower thermal budgets are generally advantageous.

ACKNOWLEDGMENTS

The authors wish to thank EPSRC, UK, for financial support and the staff of the University of Southampton Clean Room for processing specimens.

- ¹G. R. Wolstenholme, N. Jorgensen, P. Ashburn, and G. R. Booker, *J. Appl. Phys.* **61**, 225 (1987).
- ²J. S. Hamel, D. J. Roulston, C. R. Selvakumar, and G. R. Booker, *IEEE Trans. Electron Devices* **ED-39**, 2139 (1992).
- ³J. M. C. Stork, M. Arienzo, and C. Y. Wong, *IEEE Trans. Electron Devices* **ED-32**, 1766 (1985).
- ⁴K. Sagara, T. Nakamura, Y. Tamaki, and T. Shiba, *IEEE Trans. Electron Devices* **ED-34**, 2286 (1987).
- ⁵G. L. Patton, J. C. Bravman, and J. D. Plummer, *IEEE Trans. Electron Devices* **ED-33**, 1754 (1986).
- ⁶I. R. C. Post, P. Ashburn, and G. Wolstenholme, *IEEE Trans. Electron Devices* **ED-39**, 1717 (1992).
- ⁷E. F. Chor, P. Ashburn, and A. Brunnschweiler, *IEEE Electron Device Lett.* **EDL-6**, 516 (1985).
- ⁸P. A. Potyraj and D. W. Greve, 1987 Bipolar Circuits and Technology Meeting Technical Digest, 1987, p. 82.
- ⁹J. Schiz, N. E. Moiseiwitsch, C. D. Marsh, P. Ashburn, and G. R. Booker, *Proceedings of the 26th ESSDERC Meeting, Bologna, Italy, 1996*, p. 461.
- ¹⁰J. L. Hoyt, E. F. Crabbe, J. F. Gibbons, and R. F. W. Pease, *Appl. Phys. Lett.* **50**, 751 (1987).
- ¹¹C. D. Marsh, N. E. Moiseiwitsch, G. R. Booker, and P. Ashburn, *Inst. Phys. Conf. Ser.* **146**, 457 (1995).
- ¹²N. F. Moiseiwitsch, C. D. Marsh, P. Ashburn, and G. R. Booker, *Appl. Phys. Lett.* **66**, 1918 (1995).
- ¹³C. D. Marsh, N. E. Moiseiwitsch, G. R. Booker, and P. Ashburn, *Inst. Phys. Conf. Ser.* **157**, 411 (1997).
- ¹⁴C. D. Marsh, N. E. Moiseiwitsch, J. Schiz, G. R. Booker, and P. Ashburn, *Mater. Res. Soc. Symp. Proc.* **523**, 195 (1998).
- ¹⁵N. E. Moiseiwitsch and P. Ashburn, *IEEE Trans. Electron Devices* **ED-41**, 1249 (1994).
- ¹⁶J. D. Williams and P. Ashburn, *J. Appl. Phys.* **72**, 3169 (1992).
- ¹⁷S. L. Wu, C. L. Lee, T. F. Lei, C. F. Chen, L. J. Chen, H. Z. Ho, and Y. C. Ling, *IEEE Electron Device Lett.* **EDL-15**, 120 (1994).
- ¹⁸T. P. Chen, T. F. Lei, C. Y. Chang, W. Y. Hsieh, and L. J. Chen, *J. Electrochem. Soc.* **142**, 2000 (1995).

- ¹⁹B. Y. Tsaur and L. S. Hung, Appl. Phys. Lett. **37**, 648 (1980).
- ²⁰C. D. Marsh, N. E. Moiseiwitsch, G. R. Booker, and P. Ashburn (unpublished results).
- ²¹H. H. Tseng, M. Orlowski, P. Tobin, and R. Hance, IEEE Electron Device Lett. **EDL-13**, 14 (1992).
- ²²G. R. Nash, J. W. F. Schiz, C. D. Marsh, P. Ashburn, and G. R. Booker, Appl. Phys. Lett. **75**, 3671 (1999).
- ²³S. Jones and C. Hill, *Properties of Silicon*, EMIS Data Review Ser. No. 4 (INSPEC, London, 1988), p. 947.
- ²⁴W. K. Schubert, J. Mater. Res. **1**, 311 (1986).
- ²⁵C. Hill and S. K. Jones, Mater. Res. Soc. Symp. Proc. **182**, 129 (1990).
- ²⁶M. Morita, T. Kubo, T. Ishihara, and M. Hirose, Appl. Phys. Lett. **45**, 1312 (1984).
- ²⁷P. J. Wright and K. C. Saraswat, IEEE Trans. Electron Devices **ED-36**, 879 (1989).
- ²⁸U. S. Kim, C. H. Wolowodiuk, and R. J. Jaccodine, J. Electrochem. Soc. **137**, 2291 (1990).
- ²⁹D. Kouvatso, J. G. Huang, and R. J. Jaccodine, J. Electrochem. Soc. **138**, 1752 (1991).
- ³⁰A. Kazor, C. Jeynes, and I. W. Boyd, Appl. Phys. Lett. **65**, 1572 (1994).
- ³¹C. D. Marsh, N. E. Moiseiwitsch, G. R. Nash, G. R. Booker, and P. Ashburn, Inst. Phys. Conf. Ser. **164**, 477 (1999).
- ³²W. L. Jolly, *Modern Inorganic Chemistry*, 2nd ed. (McGraw-Hill, New York, 1985).
- ³³D. Kouvatso, F. P. McCluskey, R. J. Jaccodine, and F. A. Stevie, Appl. Phys. Lett. **61**, 780 (1992).
- ³⁴S. R. Kasi, M. Liehr, and S. Cohen, Appl. Phys. Lett. **58**, 2975 (1991).
- ³⁵L. A. Zazzera and J. J. F. Moulder, J. Electrochem. Soc. **136**, 484 (1989).
- ³⁶D. J. Ostra, A. Harding, and A. E. de Vries, J. Vac. Sci. Technol. B **4**, 1278 (1986).
- ³⁷C. G. Van de Walle, F. R. McFeely, and S. T. Pantelides, Phys. Rev. Lett. **61**, 1867 (1988).
- ³⁸J. H. Evans and D. J. Mazey, J. Phys. F: Met. Phys. **15**, L1 (1985).
- ³⁹J. C. Dosoyer, C. Templier, J. Delafond, and H. Gare, Nucl. Instrum. Methods Phys. Res. B **19/20**, 450 (1987).
- ⁴⁰G. R. Booker, P. Ashburn, C. D. Marsh, and N. E. Moiseiwitsch (unpublished).