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ANALOGUE FILTER SYNTHESIS FROM VHDL-AMS

(Invited Paper)

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ABSTRACT

An analogue synthesis technique for VHDL_AMS behavioural descriptions of very high-frequency filters is described. The technique is based on automatic netlist extraction from VHDL-AMS parse trees. The primary application of this work is automated synthesis of high-frequency filter blocks in analogue or mixed-signal ASIC designs. The technique is demonstrated with a practical example of a second-order, 1GHZ bandpass silicon LC filter.

1. INTRODUCTION

Due to the growing importance of mixed-signal ASICs, development of integrated analogue and mixed-signal synthesis techniques has become a burning issue. Many modern mixed-signal ASIC designs incorporate analogue high-frequency filters design with applications in the highly integrated wireless communications sector. A type of filter most suitable for such applications is the active LC filter [1,2,3,4]. LC filters can now be implemented on silicon, mainly because of the recent development in on-chip spiral inductor technologies [5,6]. Silicon inductors with value of several to several dozen nH, with Q more than 6 in the 1-5 GHz frequency range have now become available [1]. We propose to use high-level VHDL-AMS descriptions for synthesis of such filters because filters of this type can exist in a larger, mixed-signal environment and can be described in both time and frequency domain. For example, VHDL-AMS may be used to design and synthesis a single-chip receiver front-end of a communication system employing a bandpass filter. It is envisaged that future developments in VHDL-AMS synthesis will provide methods for automated synthesis of entire communication circuits, not only the filter itself. We have developed a technique of automated filter synthesis based on recognisable patterns in VHDL-AMS parse trees. These description patterns can represent time-domain differential equations of a filter or frequency-domain transfer functions.

2. ARCHITECTURAL FILTER SYNTHESIS FROM VHDL-AMS

Fig. 1 shows the filter synthesis process flow from the high-level VHDL-AMS description level to the netlist level. The procedure starts with a syntax check of the input description, and generation of a parse tree. The synthesizer then performs a synthesis rule check, then a mapping to generic filter cells, and finally it produces a circuit-level HSPICE netlist for the filter. As VHDL-AMS is not originally written for synthesis, users need to put certain restrictions or have rules on the way to describe models for synthesis [7]. Filters can be described both as time-domain models and with their frequency-domain s-transfer functions. Conventionally, the latter is the most common way to represent a filter to a synthesis system. In VHDL-AMS, this can be done using the LTF attribute.

3. Syntax restrictions and checking

Both the time and frequency domain models are to follow certain syntax restrictions. Firstly, entity can only contain port with quantity declarations as the interface. The quantities for input and output must both be of type real, for example:

```
entity filter is
      port (quantity Vin: real;
            quantity Vout: out real);
end entity filter;
```

Secondly, frequency domain models are described using the LTF attribute. The numerator and the denominator coefficients of the transfer function must be arranged in an ascending manner, for example, the transfer function of $(2.7) / (1 + 3s + 2s^2)$ is written as shown in the following example:

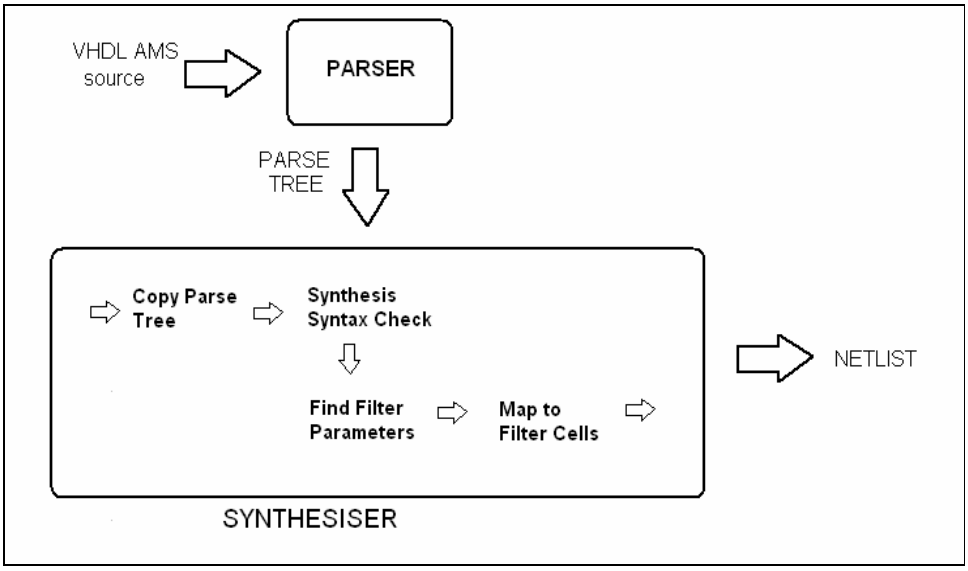

Figure 1. Block diagram for the filter synthesis system.

```
architecture transfer of filter is
    constant num: real_vector:= (2.7);
    constant den: real_vector:= (1.0,
                    3.0, 2.0);
begin
      Vout == Vin'LTF(num,den);
end architecture;
```

Also, all the coefficients of the numerator and denominator must be non-zero. Filters of any order can be described using this model, keeping in mind only those with the denominator order larger or equal to the numerator order are realisable.

Thirdly, time domain filter models are described using Differential Algebraic Equations in simple simultaneous statements using the DOT attribute, as shown in the example below. The highest-order filter segment that can be described by a simple simultaneous statement is 2. The coefficients associated with the output and its first and second derivatives must be static expressions, for example:

```
vin == coeff1*vout'dot'dot +
   coeff2*vout'dot  + coeff3*vout;
```

Checking the syntax compliance during the initial synthesis stage is done by traversing the parse tree of the architecture body and search for a simultaneous statement. For an s-domain (frequency-domain) filter model, the program further searches for occurrences of the LTF attribute, and real vectors for the numerator and denominator.

For a time domain model, the program proceeds to search for the pattern shown in Figure 2.

4. EXAMPLE

As an example, we present the synthesis of a high-frequency Q-enhanced active-RLC bandpass filter, based from [2] with modifications in the amplifier circuit. It's VHDL-AMS time-domain description is shown below.

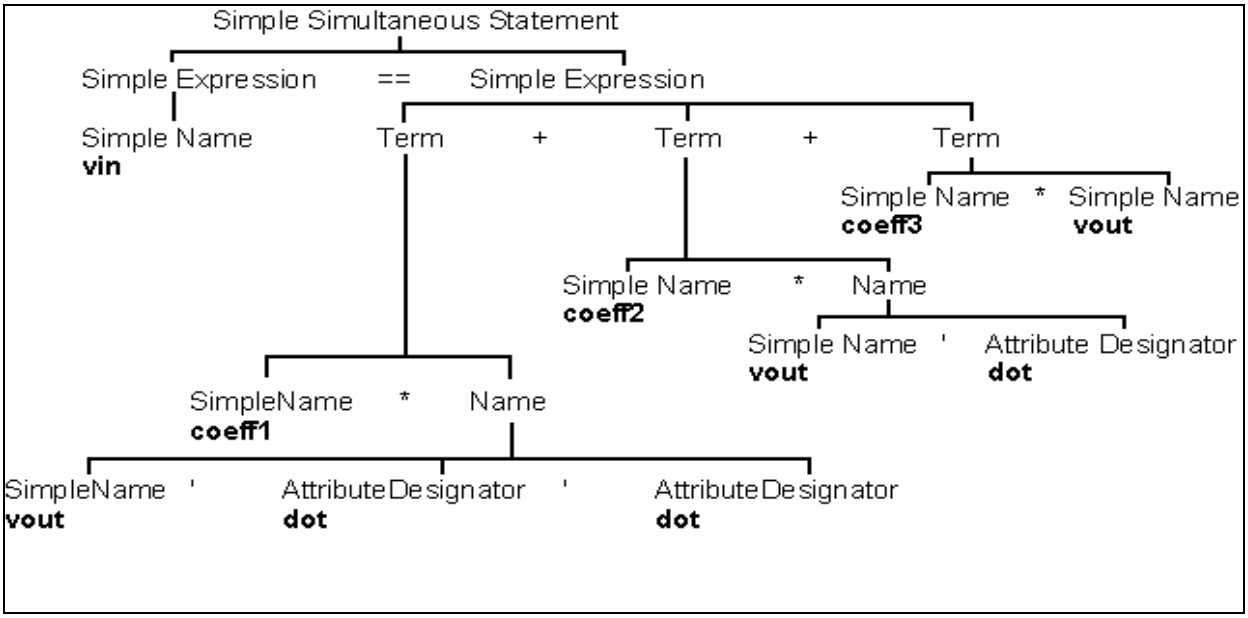

Figure 2. Parse tree for a second-order filter described by:
`vin == coeff1*vout'dot'dot + coeff2*vout'dot + coeff3*vout.`

```
entity filter is
      port (quantity vin: real;
            quantity vout: out real);
end entity filter;

architecture behavioral of filter is
   constant coeff1: real:= 9.3792e-21;
   constant coeff2: real:= 1.3097e-11;
   constant coeff3: real:= 0.3703;

begin
  vin'dot == coeff1*vout'dot'dot +
       coeff2*vout'dot  + coeff3*vout;
end architecture;
```

This filter can be implemented in silicon. The netlist uses 0.35 micrometer CMOS transistor models and is simulated using HSPICE [8] with the simulation results shown in Figure 4. This description gives a bandpass filter with the centre frequency f_c of 1 GHz and circuit Q factor of 4.5. The schematic of the synthesised circuit is shown in Figure 5.

The model of the spiral inductor, which includes the parasitic capacitance (CP1=CP2=100pF) from the spiral to ground [9] is shown in Figure 3. The inductance value L is 11nH and loss resistance R = 9Ω.

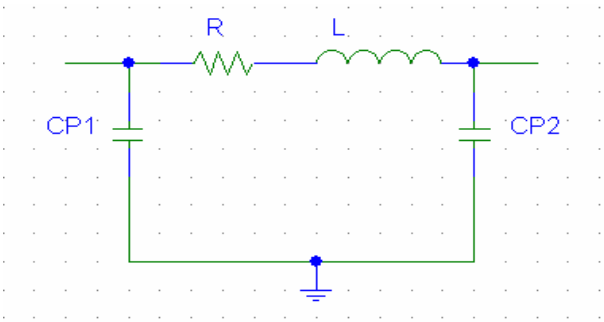

Figure 3. : Model of spiral inductor.

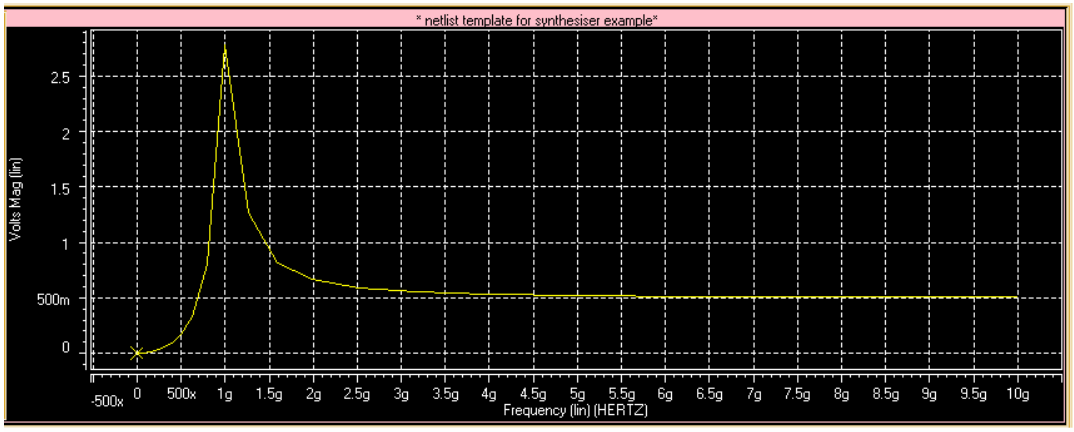

Figure 4.: HSPICE simulation result of the synthesised bandpass filter.

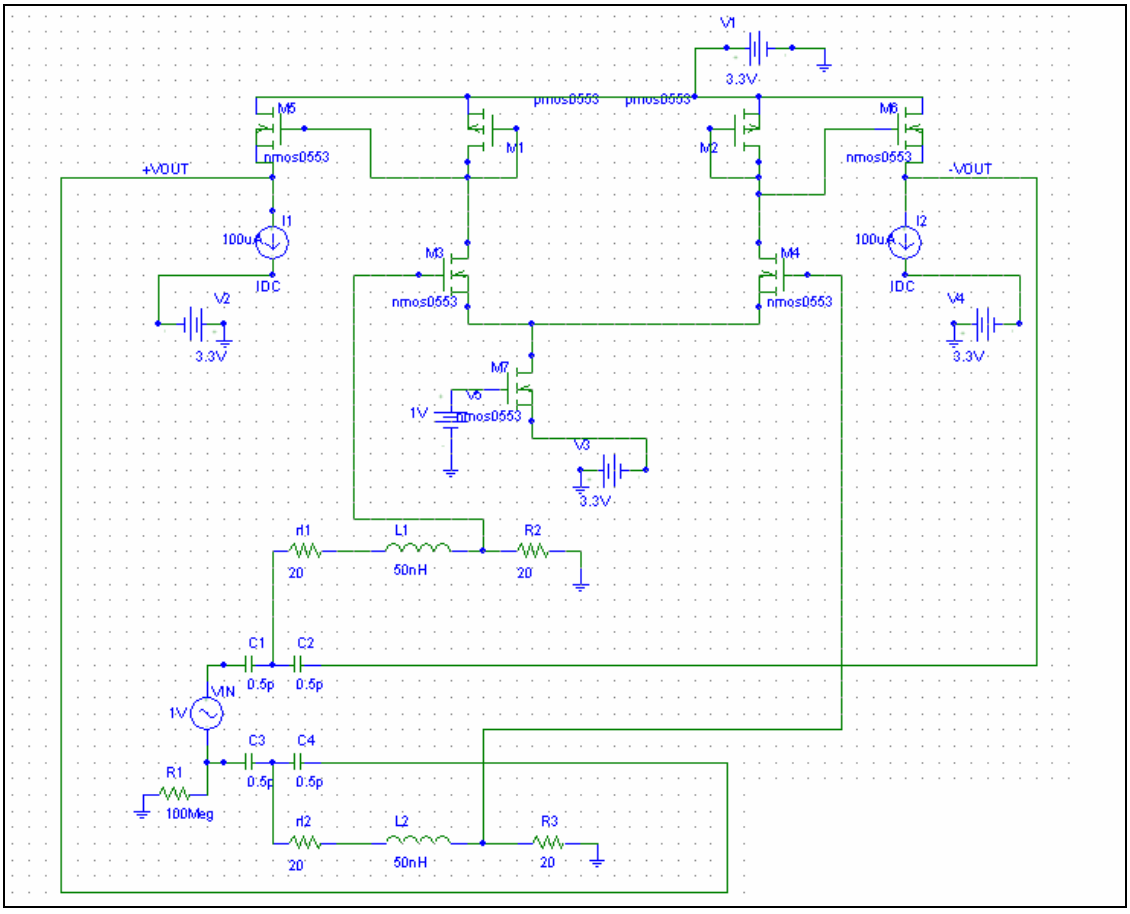

Figure 5.: Schematic of the Q-enhanced bandpass filter circuit.

5. CONCLUSION

We have demonstrated the capability of VHDL-AMS to describe synthesisible analogue models of very high-frequency filters. A synthesis procedure for analogue filters are presented, which starts from the architectural synthesis of the VHDL-AMS filter model down to the production of HSPICE netlist. The filter may be implemented in silicon using 0.35 micrometer CMOS technology. Architecture synthesis from parse tree makes the synthesis procedure simple and efficient.

6. REFERENCES

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