

Embedded Systems Modelling and Validation based on Extended Petri Nets

Mauricio Varea and Bashir Al-Hashimi
m.varea@ecs.soton.ac.uk bmah@ecs.soton.ac.uk

Department of Electronics and Computer Science
University of Southampton
Southampton, SO17 1BJ, UK

Summary

Embedded Systems are inherently heterogeneous. Thus, a model with a variety of perspectives for the representation of the embedded system functionality is of major interest in the design methodology. The underlying heterogeneity of an embedded system specification comes from (a) the existence of a mixed hardware/software structure for efficiently meeting the designer constraints and (b) the need for improving the performance of a design composed of at least two disjoint domains, *i.e.* control and data flow.

Previous research has shown that supporting heterogeneity in the internal design representation (IDR) of an embedded system plays an important role in the optimisation of the design. However, identifying a suitable IDR is not a trivial matter. There is a trade-off as to how much of one perspective should be considered in comparison to the others. For example, a purely state-oriented model might be well suited for performing improvements in the control flow of the embedded system specification, but provides little information about the data flow. On the other hand, activity- or structure-oriented models would fit better in the design of the data flow of such a system, despite its poor applicability to model the control flow part of the design.

Over the last two years, research at the University of Southampton has focus on the development of a Petri net based IDR, called *Dual Flow Nets* (DFN), for efficient mapping of specification tasks into hardware and software of the final implementation. In order to deal with this aim, DFN is capable of handling both control and data flow using a unified approach which exploits Petri net's effectiveness for concurrency manipulation. Some preliminary results in the development of this model has been recently presented [1].

A major issue in the design of embedded systems is its ever growing complexity due to the continuing availability of powerful devices. Formal verification is increasingly becoming a viable validation technique in this area, as opposed to traditional methods which involves *simulation* and *testing*. Based on this, we have extended the work applying model checking to reason about properties of the DFN model, therefore validating the design far ahead the synthesis process.

The aim of this work is to:

- Review DFN models, its syntax and semantics.
- Introduce, through motivational examples, why DFN based unified approach is beneficial.
- Outline a formal verification methodology for the validation of DFN.
- Future development of DFN and possible areas of applications.

References

- [1] Mauricio Varea and Bashir Al-Hashimi. Dual Transitions Petri Net based Modelling Technique for Embedded Systems Specification. In *Design, Automation and Test in Europe (DATE)*, pages 566–71, Munich, Germany, March 2001. IEEE/ACM.