Leakage Current Mechanisms in SiGe HBTs Fabricated Using Selective and Nonselective Epitaxy

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***Abstract*—SiGe heterojunction bipolar transistors (HBTs) have been fabricated using selective epitaxy for the Si collector, followed in the same growth step by nonselective epitaxy for the p^+ SiGe base and n-Si emitter cap. DC electrical characteristics are compared with cross-section TEM images to identify the mechanisms and origins of leakage currents associated with the epitaxy in two different types of transistor. In the first type, the polysilicon emitter is smaller than the collector active area, so that the extrinsic base implant penetrates into the single-crystal Si and SiGe around the perimeter of the emitter and the polycrystalline Si and SiGe extrinsic base. In these transistors, the Gummel plots are near-ideal and there is no evidence of emitter/collector leakage. In the second type, the collector active area is smaller than the polysilicon emitter, so the extrinsic base implant only penetrates into the polysilicon extrinsic base. In these transistors, the leakage currents observed depend on the base doping level. In transistors with a low doped base, emitter/collector and emitter/base leakage is observed, whereas in transistors with a high doped base only emitter/base leakage is observed. The emitter/collector leakage is explained by punch through of the base caused by thinning of the SiGe base at the emitter perimeter. The emitter/base leakage is shown to be due to a Poole–Frenkel mechanism and is explained by penetration of the emitter/base depletion region into the p+ polysilicon extrinsic base at the emitter periphery. Variable collector/base reverse leakage currents are observed and a variety of mechanisms are observed, including Shockley–Read–Hall recombination, trap assisted tunneling, Poole–Frenkel and band to band tunneling. These results are explained by the presence of polysilicon grains on the sidewalls of the field oxide at the collector perimeter.**

***Index Terms*—Epitaxial growth, heterojunction bipolar transistor (HBT), selective epitaxial growth, SiGe.**

I. Introduction

RAPID progress has been made in SiGe heterojunction bipolar transistor (HBT) technology since initial results were published in 1989 [1], [2]. Very high frequency device performance has been achieved, for example values of f_T and $f_{\max}$ of 130 [3] and 160 GHz [4] respectively. Circuit applications include high frequency digital circuits with gate delays around 10 ps [5], [6] and high frequency analog circuits for wireless communication systems [7]. However, in spite of this impressive progress, no single process architecture has yet emerged as the dominant approach for manufacturing SiGe HBT integrated circuits.

Selective SiGe epitaxy [3], [5], [6] is being investigated for integrating SiGe HBTs into double polysilicon bipolar processes. In this approach, a SiGe base is selectively grown in an emitter window after fabrication of p^+ polysilicon base contacts. The collector is previously grown in a separate Si epitaxy step and the emitter is subsequently formed by diffusion from a polysilicon contact. The polysilicon contact is heavily doped, so the doping in the SiGe base is kept below 5×10^{18} cm^{-3} to avoid emitter/base tunneling leakage [8]. This approach has the advantage of being compatible with conventional double polysilicon bipolar technology, which minimizes parasitic collector/base capacitance and gives very fast digital circuit performance. ECL gate delays of 11 ps [5] and 9.3 ps [6] have been reported for this approach.

An alternative approach for analog BiCMOS applications is differential epitaxy on oxide patterned active device areas [7]. In this approach, deep and shallow trench isolation is used to create isolation regions in an epitaxial collector layer. The SiGe base is then formed using differential epitaxy, which gives single-crystal growth in active device regions and polysilicon growth on the field oxide regions. The polysilicon on the field oxide is later used to form p^+ polysilicon base contacts. The germanium concentration is graded across the base to generate a built-in electric field [9] and reduce the base transit time. A heavily doped polysilicon emitter contact is again used, so the base doping is limited to about 5×10^{18} cm^{-3} to avoid emitter/base tunneling leakage. Typical performance with this approach is an f_T of 45 GHz and an $f_{\max}$ of 65 GHz [10].

Differential epitaxy technology has been further developed by combining a heavily doped p^+ SiGe base with an n-Si low doped emitter [11], [12]. A high base doping concentration is desirable because it reduces the base resistance and allows the basewidth to be dramatically reduced. The p^+ SiGe base is typically doped at a concentration of around 1×10^{20} cm^{-3} and the n-Si low doped emitter at a concentration of 2×10^{18} cm^{-3} [4] to avoid emitter/base tunneling leakage. Very high frequency performance and low values of base resistance can be achieved using this approach. For example, an $f_{\max}$ of 160 GHz has been reported on discrete mesa transistors incorporating a low doped emitter [4].

The aforementioned integrated circuit SiGe HBT technologies [5]–[7], [12] use two separate epitaxial growths, one for the

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collector and one for the SiGe base. It would be advantageous if these two epitaxy steps could be combined, as it would simplify the process and reduce the costs associated with the epitaxy. In this paper, we therefore investigate a process in which the Si collector is grown using selective epitaxy (SEG) and the SiGe base and the Si low doped emitter using nonselective epitaxy (NSEG) in the same growth step. Cross section TEM and DC transistor measurements are used to characterize the SEG/NSEG growth and to identify sources of leakage currents.

II. Fabrication

Fig. 1 shows a schematic cross-sectional view of the SiGe HBT concept. The Si collector was selectively grown (SEG) at a pressure of 72 mtorr and a temperature of 800 °C in a silicon dioxide window using a Thermo VG Semicon CV 200 System. The growth gases were SiH_4 and PH_3 and the pressure was determined by the pumping speed of the system. The $Si_{0.92}Ge_{0.08}$ base and Si emitter cap were then grown nonselectively (NSEG) during the same growth step by switching H_2 to the growth chamber and controlling the pressure at 500 mtorr via a throttle valve. The selective epitaxy was achieved using silane only [13], which avoids many of the problems associated with the use of chlorine chemistry [14]. Bases were grown with two different boron concentrations, as summarized in Table I. During the nonselective growth, polycrystalline SiGe and Si are deposited on the field oxide, which is later used to produce the extrinsic base contact of the transistor. This was done using a 5×10^{15} cm^{-2}, 80 keV boron implant, which was self-aligned to the ion implanted n^+ polysilicon emitter contact. The implanted dopant was activated using an emitter anneal of 60 s at 975 °C.

For transistor operation at high frequencies, it is important to minimize the collector/base capacitance, which is partly determined by the spacing α in Fig. 1. In the transistor shown in Fig. 1, the n^+ polysilicon contact is smaller than the collector active area (positive α), so the extrinsic base implant penetrates into both the polycrystalline and single-crystal Si and SiGe around the perimeter of the emitter. Transistors were also produced in which the collector active area was smaller than the n^+ polysilicon contact (negative α). In this case, the extrinsic base implant only penetrates into the polycrystalline Si and SiGe around the emitter perimeter. Transistors with negative values of α have the advantage of lower collector/base capacitance, but they rely on the lateral diffusion of boron during the emitter anneal for the formation of the extrinsic base. Transistors were produced with values of α of -0.5, -0.3, -0.05, $+0.5$ μm and larger.

This process has a number of simplifications compared with many of the processes described in the literature [5]–[7], [12]. First, the collector, base and emitter are all grown in a single epitaxy step, thereby eliminating the requirement for a separate collector epitaxy step. Second, oxide isolation is an intrinsic part of the device structure and hence no separate trench or LOCOS isolation is required. Third, the original growth interface is buried deep in the collector, far away from the collector/base depletion region. Hence any impurities, such as carbon and oxygen, at the growth interface will have little effect on the transistor characteristics.

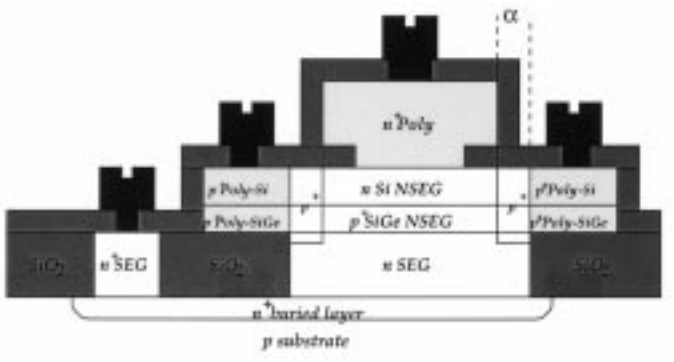

Fig. 1. Schematic cross-sectional view of the transistor structure illustrating the critical dimension α.

TABLE I
Summary of the Base Sheet Resistance and Peak Boron Base Concentrations in the Transistors With High and Low Doped Bases

Transistor	Base sheet resistance Ω/sq	Peak boron SIMS doping cm^{-3}
low doped	642	8.8×10^{18}
high doped	440	2.3×10^{19}

Transistor electrical measurements were made on a 4145 Semiconductor Parameter Analyzer. TEM images of the SEG/NSEG layers were taken on test structures on the same wafer as the transistors.

III. Results

Fig. 2(a) shows Gummel plots for five SiGe HBTs with a low doped base and a positive value of α. The transistors were measured on different parts of the same wafer. The five transistors measured have very similar Gummel plots, indicating good control of the nonselective growth across the wafer. The collector characteristics are ideal, with an ideality factor of 1.01 and the base characteristics are near-ideal, with an ideality factor at $V_{BE} = 0.55$ V of between 1.16 and 1.20. For comparison, Fig. 2(b) shows Gummel plots for five equivalent transistors with a negative value of α. The collector characteristics are very varied and there is significant emitter/collector leakage on all five transistors. At a base/emitter voltage of 0.55 V, the emitter/collector leakage varies from 1.1×10^{-6} on the best transistor to 8.0×10^{-5} on the worst transistor. The base characteristics are more varied than those in Fig. 2(a) (positive α) and also show increased emitter/base leakage. At a base/emitter voltage of 0.55 V, the base current ideality factor is 1.56 on the best transistor and 1.71 on the worst transistor.

Fig. 3(a) shows Gummel plots for five SiGe HBTs with a high doped base and a positive value of α. The collector characteristics are ideal, with an ideality factor of 1.00 and the base characteristics are near-ideal, with an ideality factor at $V_{BE} = 0.55$ V of between 1.08 and 1.09. The base current ideality factors on the transistors with a high doped base are therefore slightly better (1.08–1.09 compared with 1.16–1.20) than those in Fig. 2(a) for transistors with a low doped base. For comparison, Fig. 3(b) shows Gummel plots for five transistors with a high doped base, but a negative value of α. The collector characteristics are very different than those in Fig. 2(b) for the tran-

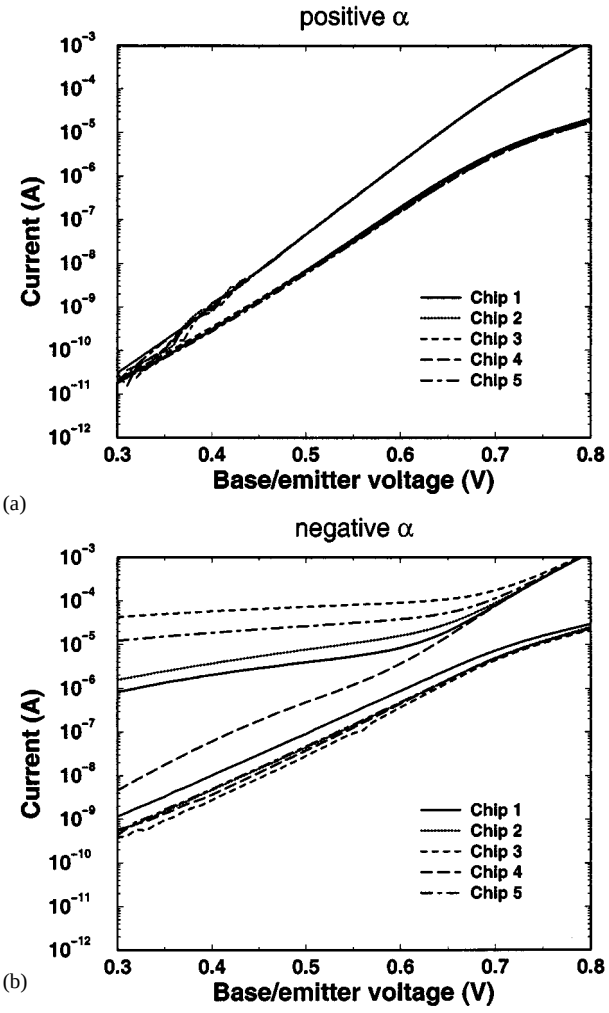

Fig. 2. Gummel plots on five different chip sites for transistors with a low doped base: (a) positive α; (b) negative α.

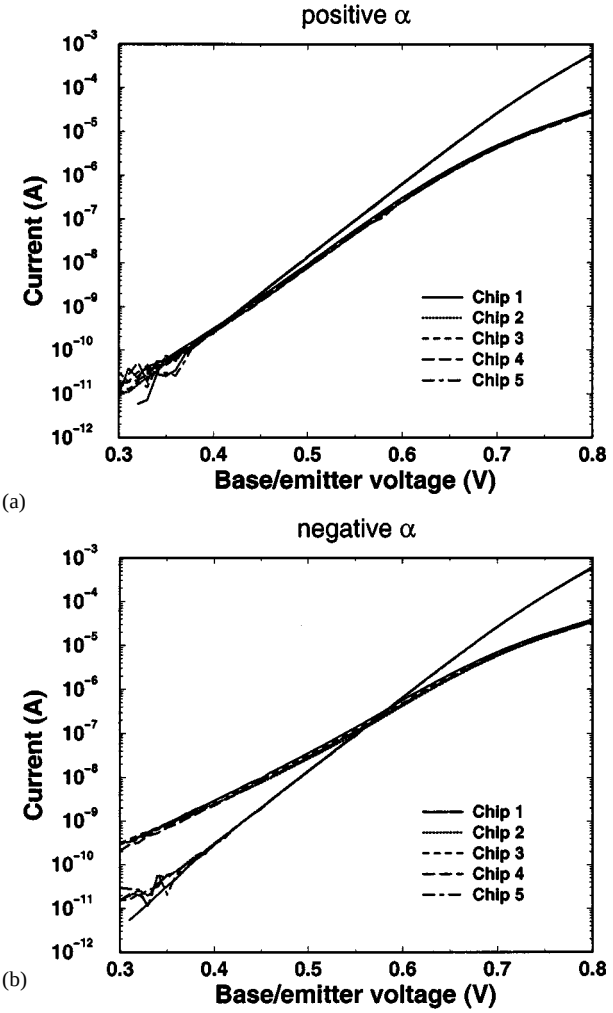

Fig. 3. Gummel plots on five different chip sites for transistors with a high doped base: (a) positive α; (b) negative α.

sistors with a low doped base. In this case, the collector characteristics are ideal, with an ideality factor of 1.00, and show no evidence of emitter/collector leakage. The base characteristics show increased emitter/base leakage with an ideality factor of 1.38 on the best transistor and 1.39 on the worst transistor at a base/emitter voltage of 0.55 V. These values of base current ideality factor are better than those in Fig. 2(b) for the transistors with a low doped base and are also less variable.

Fig. 4 shows typical reverse emitter/base diode characteristics for transistors with high and low doped bases and positive and negative values of α. The devices with a positive value of α have a leakage current of around 1–2 pA at a reverse bias of 2 V, compared with 1–2 nA for the devices with a negative value of α. The shapes of the characteristics for positive and negative α are also different, which suggests that different mechanisms control the reverse diode current in the two cases. For positive α, the slopes of the characteristics increase on going from a reverse bias of 1 V to 4 V, while for negative α, the slopes decrease over the same bias range. Theoretical curves are also shown which will be discussed later in the paper.

Fig. 5 shows the temperature dependence of the emitter/base diode reverse current for positive and negative values of α. Results are shown for devices with a low doped base, but similar results were obtained for devices with a high doped base. For positive α, the slopes of the characteristics vary very weakly with reverse bias; activation energies of 0.38, 0.38 and 0.35 eV are obtained for emitter/base reverse biases of 1, 2 ,and 3 V respec-

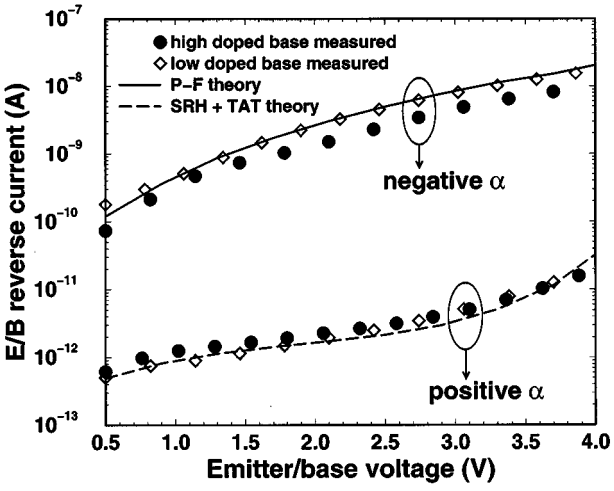

Fig. 4. Measured and theoretical emitter/base reverse diode characteristics for transistors with high and low doped bases and positive and negative α.

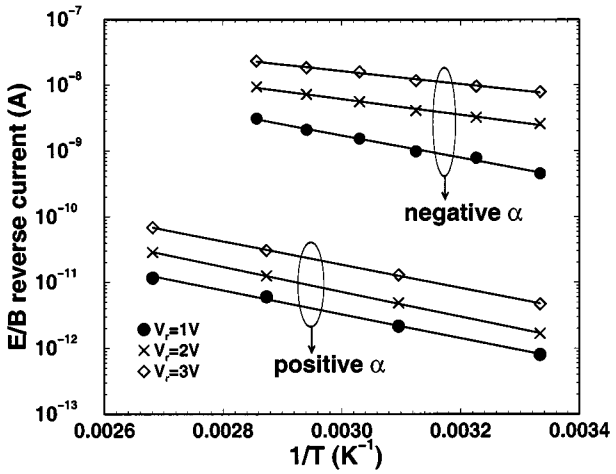

Fig. 5. Temperature dependence of the emitter/base diode reverse leakage current for transistors with a low doped base. Plots are shown for emitter/base reverse biases of 1, 2, and 3 V.

tively. For negative α, the slopes of the characteristics vary significantly with emitter/base reverse bias, indicating a field dependent leakage current. Activation energies of 0.34, 0.24, and 0.20 eV are obtained for emitter/base reverse biases of 1, 2, and 3 V respectively. These results indicate that a strongly field-dependent mechanism controls the emitter/base reverse currents of devices with negative α and a weakly field-dependent mechanism for transistors with positive α.

Fig. 6(a) shows reverse collector/base diode characteristics for transistors with high and low doped bases and positive and negative values of α. The collector/base reverse diode characteristics of the two transistors with negative α are similar in shape to the emitter/base reverse diode characteristics in Fig. 4 for the negative α transistors. In particular, the slopes of the characteristics decrease on going from a reverse bias of 1 V to 3 V. For the transistors with positive α, the collector/base reverse currents are lower, but there is some variability in the magnitudes of the currents and the shapes of the characteristics, as shown in Fig. 6(b) for five different positive α devices with a high doped base. The cause of this variability will be discussed later in the paper.

Fig. 7 shows the temperature dependence of the collector/base diode reverse diode current for positive and negative α transistors with a low doped base. For negative α, the slopes of the characteristics vary significantly with collector/base reverse bias, indicating a leakage current mechanism with a strong field dependence. Activation energies of 0.36, 0.24, and 0.19 eV are obtained for emitter/base reverse biases of 1, 2, and 3 V respectively. These values of activation energy are very similar to those obtained for the equivalent emitter/base diodes with negative α. For positive α, the characteristics show a small field dependence; activation energies of 0.45, 0.42 and 0.38 eV are obtained for collector/base reverse biases of 1, 2 and 3 V respectively. For transistors with a high doped base and negative α the results are very similar indicating the same process as for the low doped base devices. For positive α, a field dependence is seen, with activation energies of 0.53, 0,48, and 0.41 eV for collector/base reverse biases of 1, 2, and 3 V respectively.

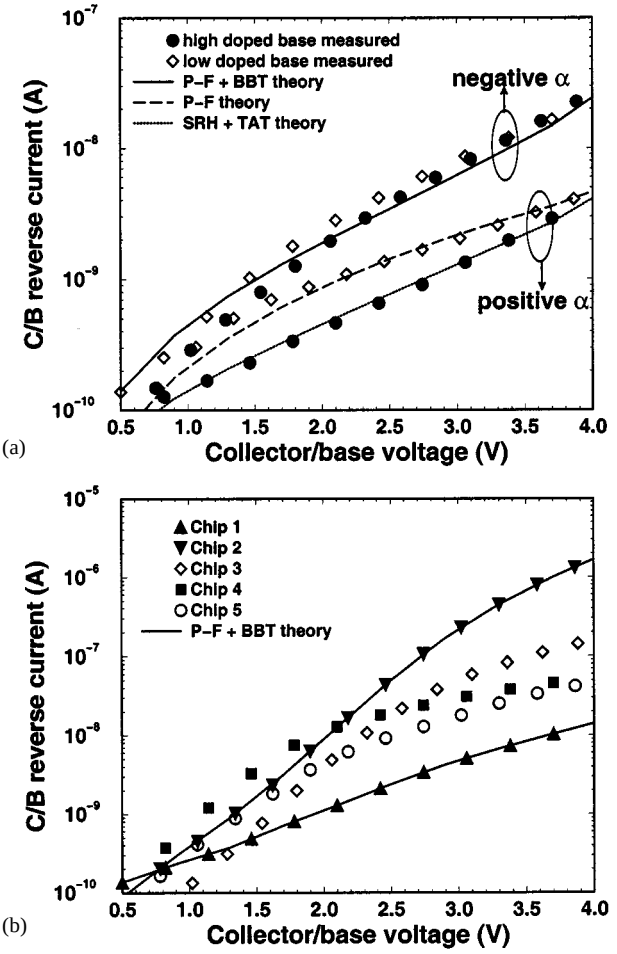

Fig. 6. Comparison of measured and theoretical collector/base reverse diode characteristics. (a) Results for transistors with high and low doped bases and positive and negative α. (b) Characteristics on five different chip sites for transistors with positive α and a high doped base.

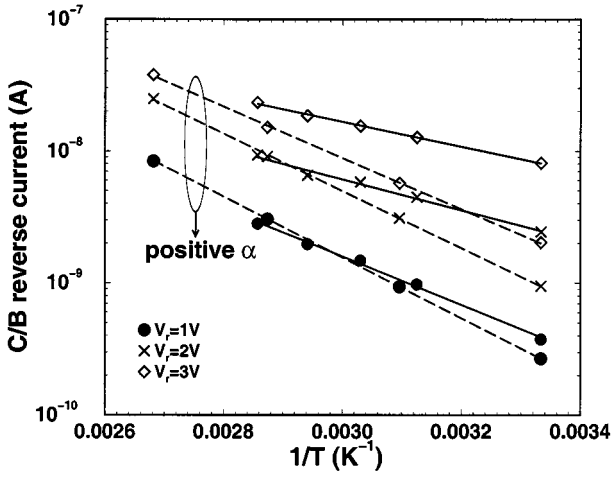

Fig. 7. Temperature dependence of the collector/base diode reverse leakage current for transistors with a low doped base. Plots are shown for emitter/base reverse biases of 1, 2, and 3 V.

Fig. 8(a) shows a typical cross-section TEM image of a complete SiGe HBT with a high doped base. The figure shows that the Si and SiGe layers have grown as single-crystal material in the middle of the device, but as polycrystalline material over the

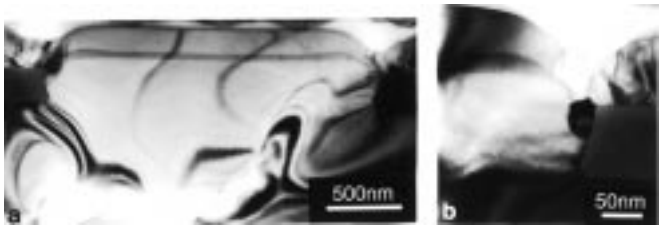

Fig. 8. Cross-sectional TEM images of the transistor structure.

field oxide. Away from the field oxide layer, the SiGe layer is uniform in thickness, with a value of 46 nm. However, as the SiGe layer approaches the field oxide, the thickness initially increases and then decreases. Similarly, the thickness of the whole SEG/NSEG stack decreases as it passes over the edge of the field oxide. The transition from polycrystalline to single-crystal material occurs in the vicinity of the edge of the oxide layer, with the polycrystalline material extending slightly inside the oxide window and partly over the sidewall of the field oxide. These effects are shown more clearly in Fig. 8(b), which shows a magnified image of the perimeter of a transistor with a low doped base. It is observed that the top of the sidewall of the field oxide is in contact with polycrystalline material, whereas the bottom is in contact with single-crystal material.

IV. Discussion

Transistors with positive α show near-ideal Gummel plots, with no evidence of emitter/collector leakage, and only residual emitter/base leakage. In these devices, the p^+ extrinsic base implant penetrates into the single-crystal Si and SiGe around the emitter perimeter. Hence the transition region from polycrystalline to single-crystal silicon at the emitter perimeter is over-doped p-type during the extrinsic base implant. This p-type doping is effective in suppressing the emitter/collector and emitter/base leakage currents that are seen in the transistors with negative α.

The mechanisms responsible for the leakage current have been investigated by comparing with theoretical curves using the approach of Hurkx *et al.* [15]. Good fits have been obtained with appropriate mixtures of the mechanisms Shockley–Read–Hall recombination (SRH), trap assisted tunneling (TAT), Poole–Frenkel (P–F) and band to band tunneling (BBT). The strategy applied in this work was to use the generation lifetime τ_g as the only fitting parameter. Reasonably, SRH recombination, TAT and BBT are expected to be area dependent, hence the active area of the device (196 μm^2) was used in fitting these components. The P–F component is expected to be related to the polysilicon regions so an effective annular area at the perimeter was defined, of width 1 μm estimated from the nominal spacing of α. The value of this effective area was 56 μm^2. Full details of the equations used to calculate the theoretical curves are given in the Appendix.

The mechanisms responsible for the emitter/base leakage are investigated in Fig. 4, where the measured reverse leakage is compared with theoretical curves. For positive α devices, the voltage dependence can be well described by SRH recombination at low voltages and trap-assisted tunneling at high voltages, using lifetimes of 2.45 ns and 1.43 ms, respectively. The large value for the TAT lifetime could suggest that generation is actually occurring at discrete sites within the active area, implying a smaller effective area for the leakage. The tunneling step of the TAT mechanism is most likely to occur close to the higher doped base side of the junction where the field is highest. We would suggest therefore that this leakage current arises from tunneling of valence band electrons from the base, into mid gap traps, with subsequent emission to the conduction band. The TAT mechanism is frequently observed in epitaxial base SiGe HBTs [15] and can be taken as an indication that the emitter/base junction is of reasonable quality.

Transistors with negative α show significantly higher emitter/base leakage currents than transistors with positive α, as shown in Fig. 4. The field dependent activation energy obtained for these devices in Fig. 5 suggests a P–F mechanism. The theoretical curves in Fig. 4 show that for negative α, the voltage dependence of the reverse emitter/base diode leakage can be well described by a P–F mechanism alone, using a lifetime $\tau_g = 2.8$ ns. Poole–Frenkel is often seen in thin film transistors, where p–n junctions are formed in polycrystalline silicon [16]. This suggests that the emitter/base leakage current in the negative α transistors is caused by the polycrystalline material at the emitter periphery as shown in Fig. 9. When the n^+ polysilicon contact is bigger than the collector active area, the formation of the extrinsic base relies on the lateral diffusion of boron during the emitter anneal. In the negative α transistors, the diffusion of the boron into the single-crystal silicon at the emitter perimeter may be insufficient, so that the emitter/base depletion region penetrates into the p^+ polysilicon. Measurements on devices with different values of α indicate that emitter/base leakage is initially seen when the n^+ polysilicon contact overlaps the field oxide by about 0.3 μm for an emitter anneal of 60 s at 975 °C or about 0.1 μm for an emitter anneal of 60 s at 900 °C.

The mechanisms controlling the collector/base leakage current are considered in Fig. 6(a), where again, the measured characteristics are compared with theoretical models [15]. The transistors with negative α can be reasonably well described by a P–F mechanism (lifetime 1.0 ns), with a band to band tunneling (BBT) component becoming dominant at higher bias. The P–F mechanism was also observed in the emitter/base leakage of the transistors with negative α, and was explained by the penetration of the emitter/base depletion region into the p^+ polysilicon extrinsic base. The proposed explanation for the collector/base leakage in the transistors with negative α is the intersection of the collector/base depletion region with the polysilicon material on the sidewall of the field oxide.

For positive α, transistors with low and high doped bases show different behavior, as shown in Fig. 6(a). The characteristic of the transistor with a high doped base can be very well described by SRH recombination at low bias and trap assisted tunneling at high bias, with $\tau_g = 0.1$ and 0.02 ns for SRH and TAT respectively. However, there is considerable variation in the collector/base characteristics of these transistors, as was shown in Fig. 6(b). A combination of the P–F and BBT mechanisms allows good fits to be obtained for both the best and worst cases. Fits were obtained by the use of the direct BBT mechanism for the worst case and indirect (phononassisted) BBT for the best

case. The difference in formulation for these two cases is to be found in the pre-exponential factor [17]. The characteristic of the transistor with a low doped base in Fig. 6(a) can be reasonably well described by a Poole–Frenkel mechanism, with a lifetime $\tau_g = 1.9$ ns. Results on five different transistors with a low doped base showed that the Poole–Frenkel mechanism was consistently seen over the five chips measured although with slight variations in lifetime.

The evidence of the Poole–Frenkel mechanism in the collector/base characteristics of many of the positive α transistors suggests that the collector/base depletion region is intersecting the polysilicon grains on the sidewall of the field oxide. This in turn implies that the extrinsic base implant is not penetrating beyond the polysilicon grains on the sidewall of the field oxide. The variability in the collector/base characteristics could then be explained by variations in the size, location and doping of the sidewall grains. For example, the difference in the tunneling mode in Fig. 6(b) could be due to variations in the base doping concentrations associated with boron out diffusion from the sidewall grains. Similarly the SRH + TAT mechanisms in the positive α device in Fig. 6(a) could be explained if the sidewall grain in this device was small so that the extrinsic base implant penetrated beyond the sidewall grain.

There are a number of growth factors that could have contributed to the presence of the polysilicon material on the sidewall of the field oxide. First, the thickness of the SEG/NSEG stack has been found to decrease as it passes over the edge of the field oxide. This might be due to a decrease in the growth rate at the window edge during the selective epitaxy. As a consequence at the perimeter, the oxide window might not have been completely filled with silicon at the beginning of the nonselective growth step. Second, selectivity of the growth could have been lost before the oxide window was completely filled with silicon. This would lead to the nucleation of polysilicon on the sidewall of the field oxide as was seen in the TEM images. The thickness of selective Si epitaxy achievable with the silane-only process is determined primarily by the growth temperature. Experiments at a higher growth temperature have shown that selective Si layers of thickness 1.2 μm can be successfully grown at 950 °C.

Figs. 2(b) and 3(b) showed that transistors with negative α and a low base doping concentration exhibited emitter/collector leakage, whereas transistors with negative α and a high base doping concentration did not. The proposed explanation for this behavior is punch-through at the emitter perimeter due to the thinning of the SiGe base, as illustrated in Fig. 9. This only occurs for negative values of α, because for positive values of α, the perimeter of the emitter is overdoped p-type by the extrinsic base implant. The emitter/collector leakage is not observed in transistors with a high base doping concentration because the doping is sufficiently high to suppress punch-through of the base. The thinning of the SiGe base adjacent to the field oxide is accompanied by a thickening of the SiGe base on moving further away from the field oxide, as shown in Fig. 8(b). Similar behavior was observed by Kamins *et al.* [18], and was attributed to the faster growth rate of selective SiGe near feature edges due to an increased local partial pressure of the Ge-containing species due to lateral transport of depositing materials. If lateral Ge transport was responsible for the vatiations in SiGe thickness, a more uniform base could be obtained by growing the SiGe at a lower temperature to reduce the mobility of the Ge.

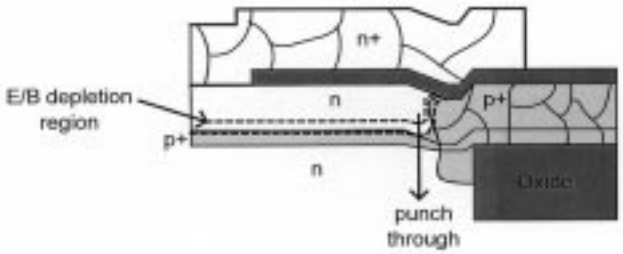

Fig. 9. Schematic diagram illustrating the origin of the the emitter/base leakage current in transistors with negative α and the origin of the emitter/collector leakage current on transistors with negative α and a low doped base.

V. Conclusions

SiGe HBTs have been fabricated using selective epitaxy for the Si collector, followed in the same growth step by nonselective epitaxy for the p^+ SiGe base and n-Si emitter cap. This approach has the advantage of eliminating the requirement for separate Si collector and SiGe base epitaxy steps and for separate trench and LOCOS isolation. Transistors with near-ideal Gummel plots are obtained provided the extrinsic base implant penetrates into the single-crystal Si and SiGe around the perimeter of the emitter. In this situation, the extrinsic base implant over-dopes the transition region from polycrystalline to single-crystal silicon at the emitter perimeter and eliminates potential sources of leakage currents. In transistors where the extrinsic base implant only penetrates into the polysilicon extrinsic base, leakage currents are observed which depend on the base doping level. In transistors with low doped bases, emitter/collector and emitter/base leakage is observed, whereas in transistors with high doped bases only emitter/collector leakage is observed. The emitter/collector leakage has been explained by punch-through at the perimeter of the base due to thinning of the SiGe layer. The emitter/base leakage can be fitted by a Poole–Frenkel mechanism, which has been explained by the penetration of the emitter/base depletion region into the p^+ extrinsic base polysilicon at the perimeter of the emitter. Variable collector/base leakage currents have been observed due to the presence of polysilicon grains on the sidewall of the field oxide at the collector perimeter.

Appendix

The equations used in the fitting to experimental data are detailed in this Appendix.

i) Shockley–Read–Hall (SRH) generation:

$$J_{gen} = \frac{1}{2}\, q \frac{n_i}{\tau_g}\, W \tag{A1}$$

where

q electronic charge;
n_i intrinsic carrier concentration (value for Si was assumed);
τ_g minority carrier generation lifetime;

W depletion width with voltage dependence $V^{1/2}$, assuming constant doping.

ii) Trap-assisted tunneling [5]:

$$J_{TAT} = \sqrt{3\pi}\,\frac{qn_i}{2\tau_g}\,W\frac{\gamma}{\xi}\left[\exp\left(\left(\frac{\xi}{\gamma}\right)^2\right) - \exp\left(\left(\frac{\xi W_0}{\gamma W}\right)^2\right)\right] \tag{A2}$$

$$\gamma = \frac{\sqrt{24m^*(kT)^3}}{q\hbar}$$

where

W_0 zero bias depletion width;

ξ electric field;

m^* effective mass (taken as 0.18 times the free electron mass);

k is Boltzmann's constant;

T is absolute temperature;

h is Plank's constant.

iii) Poole–Frenkel generation mechanism [19]:

Coulombic mid-gap traps, well spaced within the depletion region were assumed:

$$J_{PF} = \frac{2qn_i}{\alpha\tau_g}\left[\frac{V_r^{1/4}}{\beta}\exp\left(\beta V_r^{1/4}\right) - \frac{1}{\beta^2}\left(\exp\left(\beta V_r^{1/4}\right) - 1\right)\right] \tag{A3}$$

$$\alpha = \left[\frac{2qN_B}{\varepsilon_0\varepsilon_s}\right]^{1/2}$$

$$\beta = \frac{q}{kT}\left[\frac{2q^3N_B}{\pi^2\varepsilon_0^3\varepsilon_s^3}\right]^{1/4}$$

N_B doping concentration of the low doped side of the junction.

iv) Band-to-band tunneling [15], [17]:

$$J_{bbt} = C_{bbt}\cdot V_{bi}\cdot FM^{\sigma}\cdot\exp\left(\frac{-\xi_o}{\xi_M}\right)$$

$$C_{bbt} = c\cdot q$$

where

ξ_o $= 1.93\times 10^9$ V/m;

c $= 5\times 10^{15}$ cm$^{-1/2}$V$^{-5/2}$s^{-1} (best case): 4×10^{17} cm$^{-1/2}$V$^{-5/2}$s^{-1} (worst case);

σ $= 3/2$ for direct or 1 for or indirect tunneling;

ξ_M maximum field;

V_{bi} built in voltage of the junction.

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