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SiGe HBTs on bonded wafer substrates

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Abstract

Silicon germanium (SiGe) heterojunction transistors have been fabricated on bonded wafer, silicon-on-insulator (SOI) substrates. The devices have application in low power, radio-frequency electronics. The bonded wafer substrates incorporate poly-Si filled, deep trenches for isolation. A novel selective and non-selective low pressure chemical vapour deposition (LPCVD) growth process was used for the epitaxial layers. Experimental transistors exhibit good uniformity across the wafers and collector currents are seen to be ideal, showing the expected enhancement for the SiGe devices compared to Si. Anomalies in device characteristics at high current levels are investigated. © 2001 Elsevier Science B.V. All rights reserved.

Keywords: Bonded wafer; SOI; SiGe; HBT

1. Introduction

Silicon germanium (SiGe) heterojunction transistors allow Si technology to penetrate lucrative radio-frequency application markets of mobile communications and local area networks. For the bipolar transistor, the silicon-on-insulator (SOI) technology brings advantages of reduced collector capacitance and reduced cross-talk for mixed signal circuits. In the context of BiCMOS, the CMOS circuitry gains much advantage from SOI; namely simplified process flow and latch-up immunity together with enhanced MOSFET device performance. In particular, the lower threshold voltage and low junction capacitance associated with SOI-CMOS is particularly suited to low-voltage, low power applications. The SiGe HBT also offers enhanced performance at lower current levels due to the collector current enhancement thus there are overall benefits for lower power, high performance SOI-BiCMOS circuits. BESOI (bond and etch back SOI) is preferred for HBT application due to the

better Si and SiO$_2$ quality. A HBT on bonded wafer SOI has been reported recently by NEC [1]. We report here, early results for SiGe HBT on bonded wafer technology. Fabrication details are presented, followed by electrical results with proposed explanations for anomalies in the device characteristics.

2. Fabrication details

A schematic diagram of the SiGe HBT is shown in Fig. 1. The bonded SOI wafers used feature a 1-μm buried oxide layer with the surface Si layer thinned to a nominal thickness of 1.5 μm. Deep, poly-Si filled trenches provide isolation through to the buried oxide layer. The patterned SOI layer is used to provide the heavily doped buried collector as well as the crystalline seed layer for subsequent epitaxial layer growth of the silicon collector and SiGe base layers. Before the silicon epitaxial growth the SOI layer is implanted with a 5×10^{15} cm^{-2} dose of arsenic ions at an energy of 160 keV to form the buried collector contact layer. The transistor layers are grown using selective epitaxial growth (SEG) for the Si collector, followed in the same growth step by non-selective epitaxial growth (NSEG) for the p + SiGe base (nominally 12% Ge) and the n-Si emitter cap [2]. The selective Si collector was grown at 900°C and the non-selective SiGe base and Si emitter cap at 750°C. The advantages of this approach are that the basic transistor structure is grown in a single epitaxy step and the growth interface is kept away from the transistor active regions. Fig. 2 shows a TEM image of the SEG/NSEG layers after growth using silane-only epitaxy. Polycrystalline material can be seen over the field oxide and single-crystal material in the transistor active area. Good coverage is obtained over the edge of the field oxide. Transistor characteristics show good uniformity across the wafer implying good control of the Ge and B concentrations across the wafer during the non-selective SiGe growth.

3. Results and discussion

Fig. 3 shows a comparison of transistor Gummel plots from four representative wafers with bulk (#10) and SOI (#6, 8, 9) substrates. Wafers #6, 8, 10 contain HBT devices and #9 is an all-Si control device. We consider first the ideal region of current at medium bias levels with $V_{BE} = 0.6$ V. The bulk transistor (wafer 10) has a slightly higher (10%) collector current than the SOI transistors,
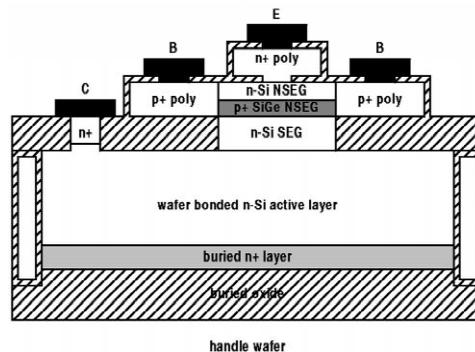

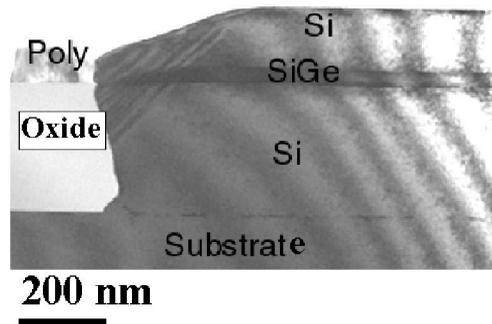Fig. 1. Schematic diagram of the bonded wafer SOI device architecture.

Fig. 2. Cross-sectional TEM micrograph showing SEG and NSG growth in an oxide window.

which could be due to a difference in base doping, since the base sheet resistance of the bulk transistor was measured as 5.1 kΩ/sq, compared with 4.9 kΩ/sq for the SOI transistor. The collector currents of SiGe transistor are enhanced by a factor of ~30 over that of the Si transistor. This compares with a calculated factor of 34 obtained from the measured SIMS profiles using the bandgap data of People [3], the density of states data of Poortmans et al. [4] and the minority carrier mobility data of Richey et al. [5]. Fig. 4 shows Arrhenius plots for the ideal regime of operation. The zero Kelvin band-gap reduction of 90 meV, due to heavy doping and SiGe, is consistent with the above analysis. The base currents of SOI transistors are about 40% lower than that of the bulk transistor in the ideal region of the characteristics. From Fig. 4, $I_B(T)$ in this regime shows activation energies of 0.97 and 0.92 eV for Si and SiGe devices, respectively. Ideal, reverse injection base current would exhibit 1.17 eV: the band-gap of the Si emitter. The ideality factor of base currents are all >1 however, indicative of non-ideal components, consistent with the activation energies. We can conclude at this point, that HBTs on SOI with theoretical I_C enhancement have been successfully demonstrated.

We consider now the non-ideal regions of the plots of Fig. 3. To gain further insight, Fig. 5 summarises experiments which serve to demonstrate whether the currents I_C and I_B, have area or
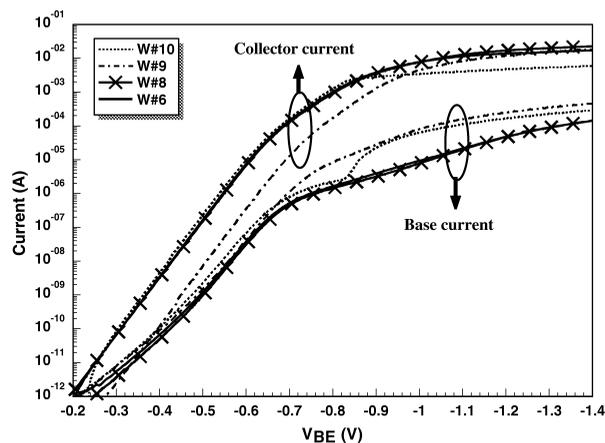

Fig. 3. Gummel plots from four wafers: bulk substrate (#10), SOI (#6, 8, 9); wafers #6, 8, 10 are HBT devices, #9 is a Si control.
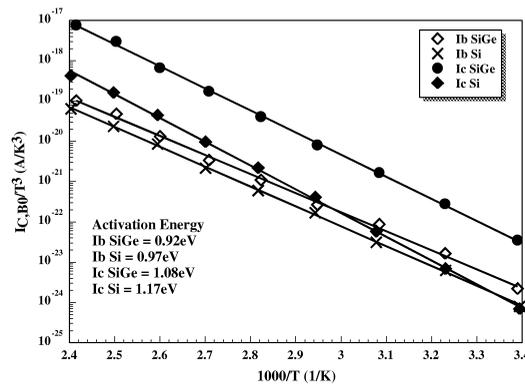
Fig. 4. Arrhenius plots, I_C and I_B for HBT and Si control at medium bias levels.

perimeter dependence. By way of example, I_C of the Si transistor shows areal dependence up to a bias level of about 0.75 V after which a transition to perimeter dependence is apparent. Comparing Figs. 3 and 5, the non-ideal regions (ideality factor, $n \sim 2$) apparent at very low bias for SOI transistors show perimeter-like dependence and are likely to be associated with recombination within the emitter-base depletion region at the edge of the device, defined by the SiO_2/Si interface. At high bias levels, the ideality factor of all collector currents goes to $n \sim 2$ and the base currents for SiGe HBTs show an anomalous 'turn-over' effect. Investigation of the temperature dependence in this regime is shown in Fig. 6. The Si device shows an activation energy for I_C of 0.57 eV ($\sim E_g/2$) and this combined with the ideality factor of two and the current crowding (perimeter dependence) apparent from Fig. 5 all point to the high injection mechanism. Further evidence is provided from the bias dependence of current gain (not shown) where the gain in the '$n=2$' region is seen to reduce with increasing temperature. However, from Fig. 3, the $n=2$ region commences at a bias level of $V_{BE} \sim 0.75$ V whereas a simple calculation shows that the injected minority carrier concentration becomes comparable to that of the base doping at a bias level of $V_{BE} \sim 1$ V. The high injection-like behaviour is anomalous therefore. From Fig. 5, I_B for the Si device (#9) switches from perimeter to area to
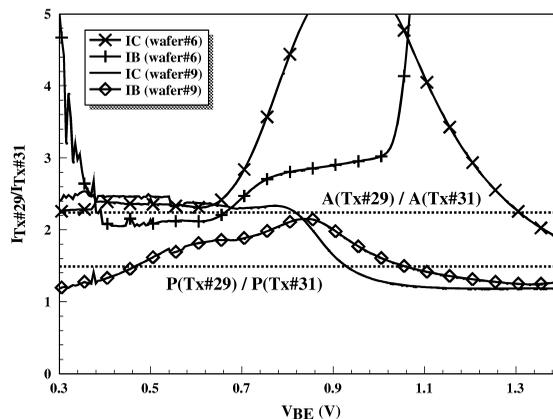

Fig. 5. Area: perimeter dependencies of I_C and I_B for HBT and Si control devices.
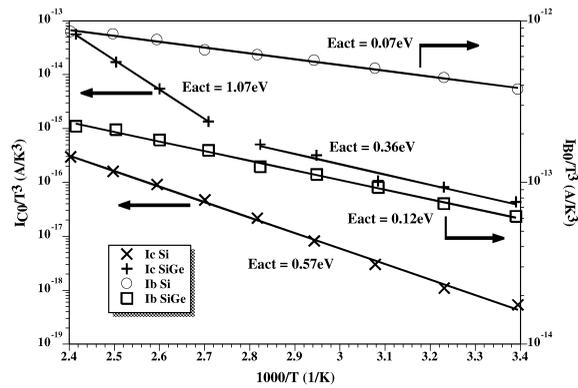
Fig. 6. Arrhenius plots, I_C and I_B for HBT and Si control in the high current regime.

perimeter dependency consistent with the explanations given above for low and medium bias. For the HBT, Fig. 5 shows a loss of area dependence after $V_{BE} \sim 0.7$ V with I_C eventually approaching perimeter dependence whereas the I_B behaviour is anomalous. We have observed such dependency for HBTs in the past and attributed it to non-homogeneous conduction at discrete sites. Thermal imaging experiments are underway to test the validity of this hypothesis. Fig. 6 shows two activation energies for I_C (HBT, #6) with the value of 0.37 eV at lower temperatures indicative of high injection although the value is somewhat less than $E_g(SiGe)/2$ and the onset is again at an anomalously low bias level.

Turning now to the anomalous turn-over effect of I_B seen in Fig. 3, we note that the effect is seen only in SiGe devices, both bulk and SOI but not in the all-Si on SOI device. (The large 'kink' in I_B and associated quasi-saturation of I_C for #10 has been shown to arise from high collector resistance.) The anomaly is thus likely to be related to the presence of SiGe rather than a result of fabrication with SOI substrates. Fig. 6 shows an activation energy of 120 meV in the I_B high current regime for SiGe devices from wafer #8. Si devices show an activation energy of 70 meV at $V_{BE} = 0.8$ V with no evidence for an activated conduction mechanism thereafter. It is worth noting that I_B for a SiGe device in the turn-over regime, shows a reasonably good fit to a power law, $I_B \sim V_{BE}^5$. This voltage dependence, combined with the activated nature of the process suggests a bulk limited regime for the hole transport associated with I_B possibly related to conduction in a non-crystalline 'bottle neck' at the periphery of the device.

4. Conclusions

We have successfully demonstrated a process for realising SiGe HBTs on SOI, bonded wafer substrates. Collector current enhancement in agreement with theoretical prediction has been obtained in the medium bias regime. Strong evidence for high injection is presented for I_C but at relatively low bias levels. This regime remains anomalous but could be a result of boron segregation into the surrounding SiO_2. HBT base current shows some non-ideality in the medium bias regime with an anomalous turn-over effect apparent at higher biases. The mechanism is activated, follows a power law dependency and it is proposed that it is related to hole transport in non-crystalline regions possibly at the periphery of the device.

Acknowledgements

References

[1] F. Sato et al., IEEE Trans. Electron Dev. 46 (1999) 1332.
[2] J.F.W. Schiz, A.C. Lamb, F. Cristiano, J.M. Bonar, P. Ashburn, S. Hall, P.L.F. Hemment, IEEE Trans. Electron Dev., (2001) in press.
[3] R. People, IEEE J. Quantum Electron. 22 (9) (1986) 1696.
[4] J. Poortmans et al., ESSDERC (1993) 317.
[5] D.M. Richey et al., IEEE Trans. Electron Dev. 44 (3) (1997) 431.