A 50nm channel vertical MOSFET concept incorporating a retrograde channel and a dielectric pocket

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Abstract

A novel architecture for a vertical MOSFET is proposed and initial investigations conducted by numerical simulation. A 'dielectric pocket' incorporated on top of the vertical transistor turret is used to control encroachment of the drain doping into the channel and reduce short channel effects. Growth of an epitaxial layer after turret formation allows the realisation of a retrograde channel in the device with all the known benefits of lower threshold voltage and higher channel mobility.

1. Introduction

The use of vertical channel MOSFETs provides a route to very short channel devices within a more relaxed lithographic process. The channel length can be defined in a very well-controlled manner by either epitaxy or ion-implantation. For the devices to be competitive for mainstream logic application, very short channels must be demonstrated. One problem is the difficulty of achieving doping variation laterally across the turret, for threshold and short channel effect (SCE) control. This means that the high body doping required to obviate SCE effects produce unacceptably high threshold voltages for the 50nm technology node. We address this issue by proposing growth of a thin, low doped epitaxial layer over the etched turret to produce a retrograde channel. Further problems are the control of source/drain doping diffusion, particularly in the case of the p-MOST, and parasitic bipolar transistor action. The latter is of more concern in the case of the n-MOST due to the higher ionisation coefficient for electrons. We propose to limit these effects by the use of a so-called dielectric pocket. This concept has also been shown to bring other benefits for threshold voltage roll-off [1]. The work presented constitutes an initial study to demonstrate feasibility.

2. Device architecture

Figures 1a,b) show the structures used in the simulations. Figure 1a) represents a simple, 'baseline' technology similar to that demonstrated in [2]. A 1μm wide turret was used with a somewhat conservative 3nm gate oxide. The body doping

concentration was set at $5 \times 10^{18} cm^{-3}$ (As). This high concentration was used so that a comparison could be made with the retrograde/pocket device which is seen to require this high level of doping to attain acceptable threshold voltage and off-currents, as will be shown. Figure 1b) shows the design including the retrograde and dielectric pocket concepts. This device also uses a 1µm wide turret with a 3nm gate oxide. The retrograde channel thickness was set at 10nm and the doping concentration was $1 \times 10^{16} cm^{-3}$ As. A relatively thin pocket is required to avoid problems associated with nucleation when growing subsequently the epitaxial retrograde layer; the thickness of the SiO_2 dielectric pocket was set at 10nm for these simulations.

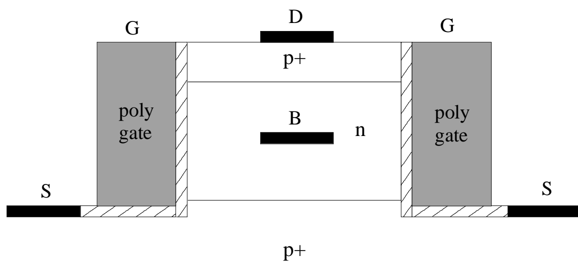

Figure 1a). Simple baseline technology structure

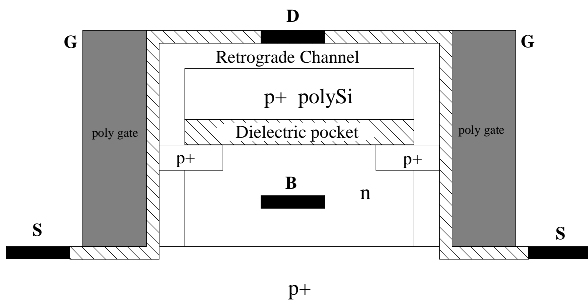

Figure 1b). Advanced retrograde/pocket device structure

For both technologies the drain contact was assumed to be at the top of the turret and the source contact at the bottom, although in practice, the device may be operated in both modes.

3. Results

The transfer characteristics for a 50nm channel, retrograde/pocket device shown in figure 2), illustrate the effect of increasing the body doping concentration from $2 \times 10^{18} cm^{-3}$ to $1 \times 10^{19} cm^{-3}$. The threshold voltage for a body doping of 2×10^{18} cm^{-3} was found to be 0.03V using the extraction method given in [3] and the off-current was 2.3µA. These are clearly unacceptable values for circuit operation. A threshold voltage of –0.23V with an off-current of 6.2nA was obtained with a body doping of $5 \times 10^{18} cm^{-3}$ and this is acceptable for sub-1.5V supply circuits to maintain drive capability and avoid excessive off-state power consumption. Devices have been demonstrated with such high levels of body doping [4].

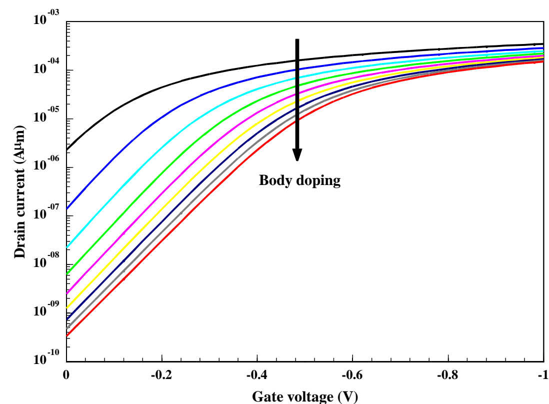

Figure 2). Transfer characteristics for retrograde/pocket device as a function of body doping (ranging from $2 \times 10^{18} cm^{-3}$ to $1 \times 10^{19} cm^{-3}$ in steps of $1 \times 10^{18} cm^{-3}$)

The effects on the threshold voltage of channel reduction are shown in figure 3). The simulations were performed for both technologies at Vds = 0.1V and Vds = 1V. Threshold voltage roll-off occurs for devices with channel lengths smaller than approximately 150nm for both baseline and retrograde/pocket variations demonstrating the slight leverage that the concepts bring to Vt roll-off [1]. The very significant reduction in threshold voltage demonstrates the advantage of introducing the retrograde channel layer.

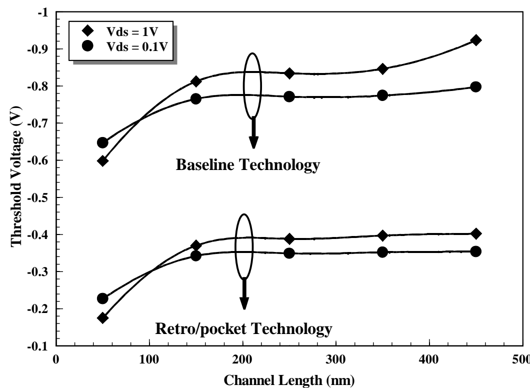

Figure 3). Threshold voltage roll-off comparison of baseline and retrograde/pocket technologies

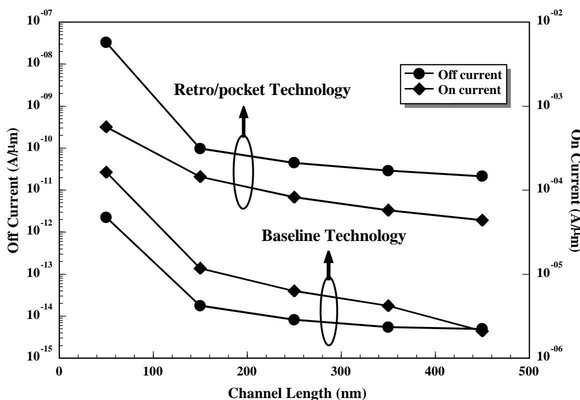

Figure 4). Comparison of baseline and retrograde/pocket technologies off and on currents

The off-state leakage currents are shown in figure 4) along with the on-currents (at Vds = 1V) for the devices. The off-currents of the retrograde/pocket device show a constant increase of approximately 4 decades of current for all channel lengths over the baseline technology. Values of 33nA/μm and 2.2pA/μm were obtained for the 50nm variants of the retrograde/pocket and baseline technologies respectively. The on currents do not show the same constant increase between the two technologies, with the difference reducing with the channel length.

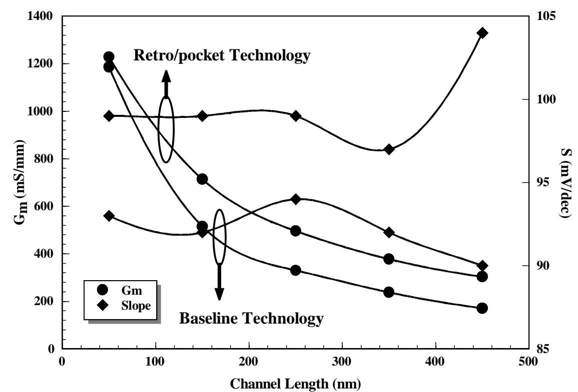

Figure 5). Comparison of transconductance and subthreshold slope for baseline and retrograde/pocket technologies

The maximum transconductance for both technologies is given in figure 5). Values of 1230mS/mm and 1190mS/mm were obtained for the retrograde/pocket and baseline technologies respectively. The difference between the two variants is again not constant and reduces with the reducing channel length. The subthreshold slope for the retrograde/pocket device is about 5mV/decade worse than that of the baseline technology. Further optimisation of retrograde channel width and doping density is required to reduce this slope.

The output characteristics for both technologies are shown in figure 6). The gate voltage is stepped by 0.5V from 0.5V to 1.5V. These characteristics serve to demonstrate the enhanced performance that can be obtained using these concepts. Note that impact ionisation was 'turned-off' for these initial simulations, to allow faster convergence and to obtain a first cut design.

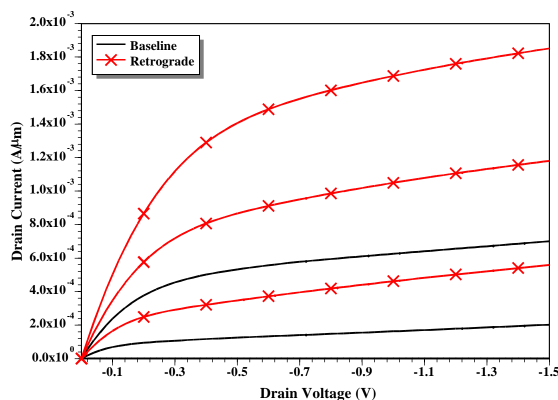

Figure 6). Output characteristics for both the baseline and retrograde technologies

The output characteristics for the retrograde/pocket device with impact ionisation switched on are shown in Figure 7) which demonstrates that the device can operate safely at 1V supply voltage.

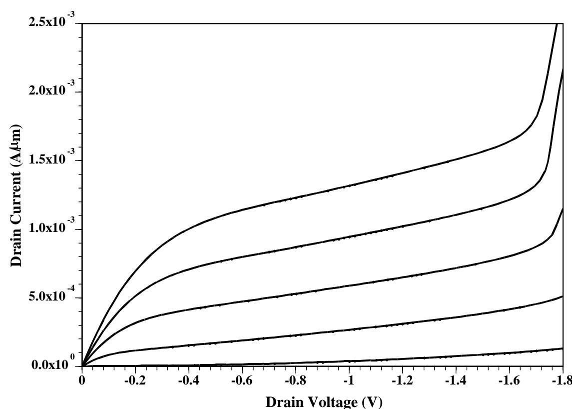

Figure 7). Output characteristics for retrograde/pocket device with impact ionisation.

4. Conclusions

The results of this initial investigation serve to demonstrate the feasibility for a vertical MOS device concept that can achieve 50nm channel length. The structure includes a dielectric pocket at the top of the turret which can prevent out diffusion from the drain into the channel. A retrograde channel is used to reduce the threshold voltage of the device. Simulations of the device predict good sub-threshold and output characteristics coupled with relatively low off-state leakage currents.

5. Acknowledgements

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6. References

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