System-on-Chip Methodologies & Design Languages
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Chapter 5. Analog circuit synthesis from VHDL-AMS

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Abstract

While digital circuit designs are now fully automated and can be delivered extremely quickly, the analogue part of a typical ASIC still needs to be designed manually. This paper discusses a way forward to overcome one of the obvious difficulties in analogue synthesis namely the lag in the development of appropriate synthesis methodologies to support mixed-signal ASICs. The recent emergence of VHDL-AMS has enabled high-level analogue descriptions to be synthesized into hardware automatically. An example of synthesis and optimization of a 1GHz VLSI LC bandpass filter is presented based on identification of synthesizable constructs from a VHDL-AMS parse tree.

1 Introduction

The advances in integrated circuit technology have led to the growing popularity and a decrease in cost of mixed-signal ASICs (Application Specific Integrated Circuits), which comprise both analogue and digital circuit blocks. Significant application areas of mixed-signal ASICs include for example signal processing, mobile telephony and computer networking. However, the development of CAD tools in recent years has concentrated mainly on automatic design of digital circuits while the automation of analogue designs remains largely a heuristic and a labor-intensive task. There are two main reasons for the significant popularity high-level digital synthesis has gained during the last decade. Firstly, high-level digital design specifications are now very well supported by suitable hardware description languages, which allow design constraints and functional descriptions to be clearly stated. Secondly, methods and algorithms for digital synthesis and design optimization have been well established and are supported by a large number software tools used on an industrial scale throughout the integrated circuit design community.

Recently the IEEE DASC (Design Automation Standards Committee) formally adopted the 1076.1 standard for VHDL informally called VHDL-AMS (VHDL hardware description language with analogue and mixed-signal extensions) [1,2]. VHDL-AMS extends the modeling power of VHDL to the domain of continuous and discrete-continuous systems. The new hardware description standard has enabled description of behavioral modeling of mixed-signal systems with complex analogue parts. Analogue SPICE-like simulators, which have so far been used for most VLSI analogue simulations, do not support behavioral modeling and do not lend themselves easily to system-level modelling.

Many mixed-signal ASICs use very high-frequency filters, eg. in receiver front-end circuits. Such filters are usually active LC filters [3], which can currently be implemented on silicon using on-chip spiral inductors [4,5], in the manner that employs a Q-enhancement technique [3,6-8]. The currently available VHDL-AMS synthesis systems, such as VASE (VHDL-AMS Synthesis Environment) [10,11], and NEUSYS [12], are not directly suitable to high-level architectural synthesis of filters. However, we have developed an extension of the technique previously implemented in NEUSYS to enable filter synthesis. The synthesis stage is followed by an optimization stage, which chooses a set of parameter values to produce a filter circuit with the best Q factor. The input to the synthesizer is a VHDL-AMS description of the filter, from which a successful synthesis will produce a HSPICE netlist

As the filter is intended for implementation on a silicon chip, the netlist will contain a spiral inductor. Such inductors have significant losses and, in a bandpass filter, this will result in a very low Q factor. A Q-enhancement method is used to cancel the effect of these losses by introducing a negative resistance. In our implementation we propose a very effective, Colpitts-type LC oscillator to achieve an enhancement of the Q factor.

The classical approach to analogue synthesis starts from the selection of a circuit and subsequent optimization of the circuit parameters such as the techniques used, for example by OPASYN [13] and OAC [14]. The parametric optimization stage finds a set of component values, which optimize an objective function. One of the optimization constraints is the silicon inductor value, which in order to minimize the losses and parasitic capacitances, should be kept to a minimum [15].

2 Architectural synthesis from VHDL-AMS parse trees applied to analog filters

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Figure 1 shows the general outline of our synthesis procedure. The process starts with syntactic and semantic checks of the input description and the generation of its parse tree. Several syntax limitations are placed on the VHDL-AMS simultaneous statements to make the synthesis feasible. The tool accepts a subset of VHDL-AMS, which supports quantity and constant declarations, component invocations, simple, conditional and procedural simultaneous statements, break statements, subprograms and some sequential statements. The parse tree (figure 3) is then used to create an intermediate netlist, which is subsequently optimised into a final HSPICE netlist.

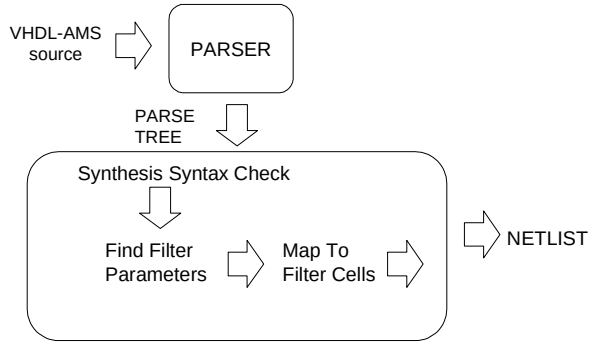

Fig. 1: Block diagram for the synthesis system.

The procedure starts with the parser performing a VHDL-AMS syntax check, and then generating the parse tree for the synthesizer, which performs a synthesis rule check. If the input description is found to be synthesizable, then a mapping to generic cells is done to produce the circuit-level netlist. Filters can be described using VHDL-AMS in two ways: as time-domain models or alternatively as frequency-domain s-transfer functions.

Conventionally, the latter is the most common way to represent a filter to a synthesis system where in VHDL-AMS this is done using the LTF attribute. However, with the intention of having an analogue filter integrated with other digital components in a communication system, for example, where the digital part can also be modeled using VHDL-AMS, it may be more practical to describe the filter in its time domain.

An example of a time-domain VHDL-AMS description of a bandpass filter model is shown in Fig. 2. The minimum value of the Q factor is specified to be 50, and the filter mid-band frequency is 1 GHz. Here, the VHDL-AMS code contains both the constraints to be optimized together with the desired behavior of the circuit. A fragment of the parse tree generated by the parser for the this part of the VHDL-AMS code is shown in Fig. 3.

```
entity filter is
    port  (quantity vin: real;
           quantity vout: out real;
           variable Q: real:= 50.0;
           variable F: real:= 1e9);
end entity filter;

architecture behavioural of filter is
    constant W: real:= 2*3.142*F;
    constant coeff1: real:= Q/W;
    constant coeff2: real:= 1.0;
    constant coeff3: real:= Q*W;
begin
    vin'dot == coeff1*vout'dot'dot +
    coeff2*vout'dot  + coeff3*vout;
end architecture behavioural;
```

Fig. 2: VHDL-AMS code for a second-order bandpass filter.

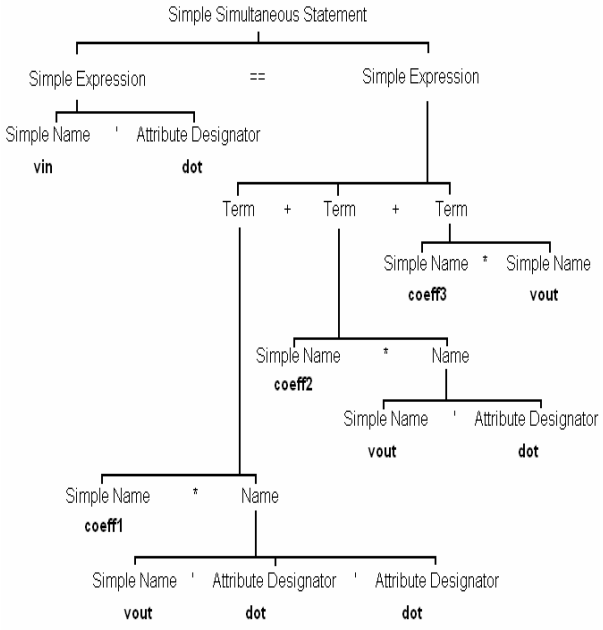

Fig. 3: Parse tree for a second-order bandpass filter described by vin'dot == coeff1* vout'dot'dot + coeff2*vout'dot + coeff3*vout.

This second order bandpass filter construct is mapped to a filter cell. Further parsing is done to establish the parameter values, in this case, Q and F (filter Q factor and frequency respectively), which are used to calculate the component values and device parameters in the circuit netlist. The components that directly affect the Q factor and filter frequency are the inductor and capacitors. The netlist produced by the synthesizer for this bandpass filter is shown in Fig. 4.

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```
L1     N7 N2 8n
RL1    N7 N1 5
C1     N2 N3 4p
C2     N3 N4 16p
M1     N2 N5 N3 N4 nmos L=0.35u W=0.65u
R      N2 N1 10k
I1     N3 N4 DC 1.5mA
V1     N6 0 1.5V
VDD    N1 0 3.3V
VSS    0 N4 3.3V
VIN    N5 N6 AC 1V
```

Fig. 4: HSPICE Netlist for the bandpass filter.

Inductor L1 is a spiral inductor whose losses are modeled by a series resistor RL1. More accurate models have also been described in literature [15,16]. Although it is possible to construct a higher-value spiral inductor, it is more practical to choose a value of less than 10nH [15]. In the above example the inductor is chosen to be 8nH, and the corresponding loss resistance RL1 is 5 ohms.

3 Parametric Optimisation

The LC bandpass filter is constructed around a Colpitts oscillator to bootstrap Q as shown in Fig. 5. The positive feedback reduces the effect of losses generated by the spiral inductor L1, resulting in an improved Q factor [1]. The amount of feedback is controlled by the ratio of capacitors C1 and C2, where the value of both capacitors in series together with inductor L1 determine the frequency of the bandpass filter.

The Q factor is determined by the feedback provided by the capacitors C1 and C2, the current flowing into the transistor from current source I1, and the width of the transistor M1. Thus, the parameters being optimized by the optimizer are the capacitors C1 and C2, current I1 and the width of M1. One possible optimization aim is to obtain a circuit with the highest Q factor, while at the same time, ensuring the total series capacitance of C1 and C2 together with the inductor value of 8nH are matched and kept within realizable ranges to ensure a mid-band frequency of 1 GHz.. The current optimization strategy minimizes a single objective function within the prescribed parameter space but will in the future be expanded to use more sophisticated methods such as the simulated annealing technique, to allow efficient optimization of more than one object function [17].

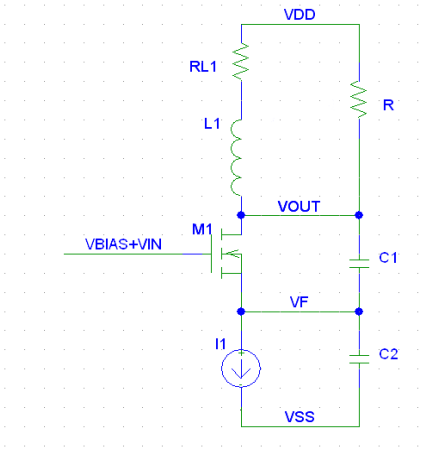

Fig. 5: Colpitts circuit producing a Q-enhanced bandpass behavior at output VOUT.

4. Experimental Results

The Q factor of the lossy LC circuit without Q-enhancement at 1GHz is 10.3, as shown in figure 6. This is confirmed by a by-hand calculation; in which the Q factor of the lossy LC filter without the amplifier circuit at 1 GHz is about 10. The best Q factor found by the optimizer is approximately 217, which the optimizer took just 74 seconds to find performing 118 HSPICE simulations (figure 7).

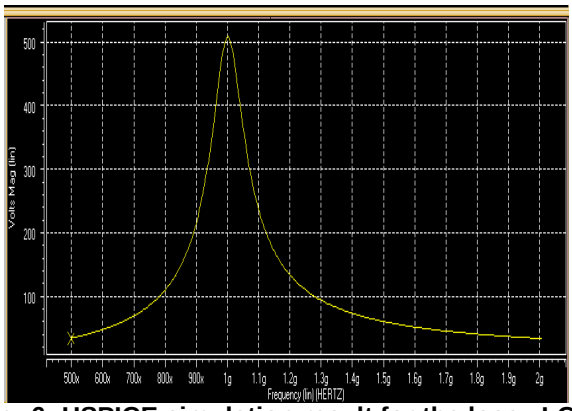

Fig. 6: HSPICE simulation result for the lossy LC circuit without Q-enhancement.

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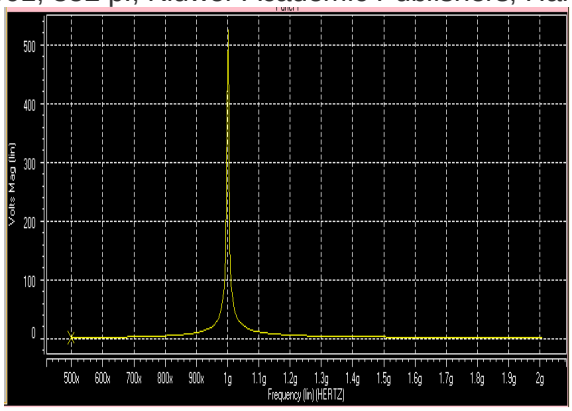

Fig. 7: HSPICE simulation result of the optimized filter.

5 Conclusion

This contribution presents an extension of the technique based on netlist extraction from VHDL-AMS parse trees for architectural synthesis and optimization of high-frequency analog filters. VHDL-AMS provides a simple yet accurate and natural way to represent high-performance analog circuits that can potentially be embedded in larger, mixed-signal VHDL-AMS systems.

The successful operation of the synthesizer and optimizer has been demonstrated using a 1GHz Q-enhanced silicon LC filter in which final circuit exhibits a Q factor greater than 200. The CPU time for both the automated synthesis and optimization is negligible.

6 References

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