Implementing On-Line Testable Designs in Behavioural Synthesis

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Abstract

When modern digital systems operate in a hostile environment, or when faults while the system is operating cannot be tolerated at all, some fault tolerance strategy has to be applied. The first step towards fault tolerance is error detection, provided by on-line testing. Behavioural (or high-level) synthesis, on the other hand, provides fast and efficient design space exploration and enables the designer to consider several realisations of his conceptual specification, in order to choose the one that best accommodates his needs. In this work, we are dealing with the automatic insertion of on-line testing resources in behaviourally synthesized designs.

A well-discussed issue in technical literature is the utilisation of system components' idle cycles for testing purposes. A component is considered to be idle during a clock cycle (in a synchronous system) if it is neither processing any useful data nor producing any useful results during that particular cycle. A common concept is to utilise those idle cycles in order to (algorithmically) duplicate and compare normal results, thus verifying their validity or detecting any possible errors. We provide an additional degree of freedom to this approach, by introducing our inversion testing technique. In this technique, normal results are no longer duplicated; rather, they are inverted to reproduce the original inputs, which are consequently compared with the functional input signals, to produce the error or error-free indication. Provided it is fault-secure (as is the case for arithmetic components, e.g. adders, subtractors), applying the inversion technique has been shown (through our experiments) to potentially produce smaller designs in a number of cases. Working in behavioural synthesis allows us to identify those cases early in the design process and choose the technique (duplication or inversion) that leads to better results in the first place.

In order to implement our ideas, we have been using the MOODS (Multiple Objective Optimisation in Data and control path Synthesis) High-Level Synthesis Suite, developed in the University of Southampton during the last decade. It is fed by behavioural VHDL descriptions of the conceptual designs, together with user requirements (in terms of area, delay, power dissipation etc.) and produces RT-level designs composed of control and data paths. Its unique characteristic is that it starts off with an initial, naïve and totally inefficient design realisation and moves towards fulfilling designer requirements by applying several high-level (scheduling, allocation etc.) transformations, in an iterative fashion. The whole iterative optimisation process is driven by a cost function that encapsulates designer specifications and is controlled by some optimisation algorithm. Several transformations, several user requirements and a selection of different optimisation algorithms provide practically infinite possibilities for design space exploration. Implementing our on-line testing resource insertion within the above-mentioned system is done by defining a few additional transformations. Further, in order to bias the system towards applying those transformations, we need to include some metric of on-line testability within the cost function. The percentage of system operations made on-line testable, the existence of idle time and error latency (number of clock cycles between appearance and detection of error) are all candidates to be included (together with appropriate weights) in an analytical expression quantifying on-line testability.

It is to be noted that after implementing all this, our system will be capable of producing on-line testable designs simply at the designer's request, without any modification of initial VHDL descriptions. It is the first time (to our knowledge) that a high-level synthesis system will provide such a capability and we consider it a contribution of some importance, because it clearly allows on-line testable designs of realistic size to be made easily realisable.