Quantifying on-line test

★ $T_{on\text{-}line}=f(P_1,P_2,L)$

where

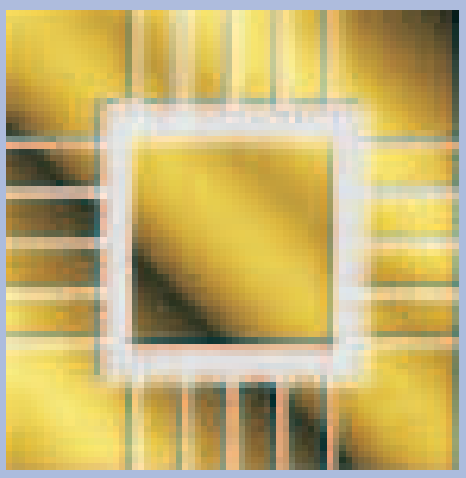
P_1=percentage of operations that have had on-line testing schemes attached to them

P_2=average idle time availability

L=average error latency

★ Now $Cost=f(area,delay,T_{on\text{-}line})$

★ Design space becomes 3-dimensional!!!



Department of Electronics a

11/06/2002