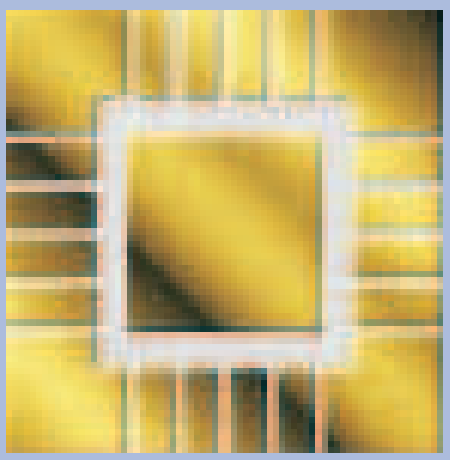
p							
Inverted_1	*306*	*948*	*15*	*4 MHz*	*31.3*	*15.4*	
Inverted_2	*316*	*996*	*18*	*25 MHz*	*35.6*	*38.5*	*0*

Table 3 : Diffeq benchmark synthesis results (Target technology Xilinx Virtex XCV800 FPG

Version	*Target Technology*	*Resource Usage*		*Cycles*	*Testing Penalty*	
		Slices	*Tristate Buffers*		*Hardware Overhead (slices %)*	*Performa Degrada (cycles*
Original	*Xilinx Virtex XCV800*	*465*	*2910*	*33*	*-*	*-*
Original	*Xilinx XC95288XV*	*548*	*2910*	*33*	*-*	*-*
Dupl_1	*Xilinx Virtex XCV800*	*589*	*4874*	*77*	*26.7*	*133.3*
Inv_1	*Xilinx Virtex XCV800*	*600*	*5000*	*77*	*29.0*	*133.3*
Dupl_1	*Xilinx XC95288XV*	*702*	*4874*	*77*	*28.1*	*133.3*
Inv_1	*Xilinx XC95288XV*	*671*	*5000*	*77*	*22.4*	*133.3*
Dupl_2	*Xilinx Virtex XCV800*	*654*	*5208*	*42*	*40.6*	*27.3*
Inv_2	*Xilinx Virtex XCV800*	*630*	*5441*	*43*	*35.5*	*30.3*

Table 4 : Qrs benchmark synthesis results



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