ANALOGUE FILTER IP CORES FOR DESIGN REUSE

Reuben Wilcock and Bashir Al-Hashimi
Electronic Systems Design Group, University of Southampton, UK
{rw01r, bmah}@ecs.soton.ac.uk

ABSTRACT

This paper addresses important considerations concerning the design of analogue filters, to ensure their suitability for use in a system on chip environment as intellectual property filter cores. We argue that switched-current is the most suitable circuit design technique and furthermore that the wave filter design methodology is favourable over an integrator approach. To speed up the design process some level of automation is clearly necessary and a system implemented in the SKILL language and within the Cadence Design Framework is particularly attractive given the access to powerful circuit analysis tools. A design flow is presented encompassing all of these attributes.

1 INTRODUCTION

In the last few years, shrinking circuit features and advances in integrated circuit design methods have allowed complete systems to be integrated onto a single chip. Referred to as a systems on chip (SoC), they offer a number of advantages over traditional multi-chip approaches, including lower power consumption, higher performance and smaller size [1]. SoCs are becoming increasingly diverse and complex, containing a true mix of circuitry including digital, RF and mixed signal sections. In order to achieve a short time to market in such demanding circumstances, design reuse of functional building blocks is commonly employed. What started as block re-use within individual companies has now opened up a rapidly expanding industry in the design of third party intellectual property (IP) cores, with analysts predicting an exponential growth in this area [2, 3].

Digital IP cores are readily traded in terms of process independent high-level descriptions, which can later be synthesized into transistor level designs using standard libraries. It is far more difficult to produce analogue circuit designs in such a tradable format, for whilst digital circuits can gain performance from a shift to a smaller process, analogue circuits often loose performance or possibly stop working altogether [2]. To ensure reliability and hence customer confidence, it is therefore necessary for analogue cores to be redesigned and verified for the particular specifications and process they are intended for, an exercise which can be very tedious. However, with careful consideration of circuit design technique, methodology, and suitable levels of automation one can ensure that a derived transistor level design is suitable for different processes and its redesign is swift and efficient.

This paper aims to address these considerations in terms of analogue *filter* cores, by first suggesting the most appropriate circuit design technique, then based on this, a suitable filter design methodology and a recommended level of automation. Furthermore we describe a semi-automated design flow capable of efficiently designing versatile analogue filter cores to given specifications, capable of optimisation at different stages.

2 CIRCUIT DESIGN TECHNIQUE

In order to be versatile, an analogue IP core should employ a design technique compatible with present and future processes. SoCs comprise mostly of digital circuitry and as a result most modern processes are optimised for low interconnect capacitance and resistance to achieve high performance in these digital functions. This is converse to the needs of conventional analogue integrated designs, which often require high quality integrated resistors and capacitors. Furthermore, the decreased voltage headroom resulting from lower supply voltages can severely affect performance and limit feasibility of complex analogue circuit topologies [2]. Only the simplest low-level blocks should be used in order to make design and analysis easier, hence leading to better understanding of design tradeoffs such as performance and power. It should also be noted that low-level structures which are regular lend themselves to automated generation.

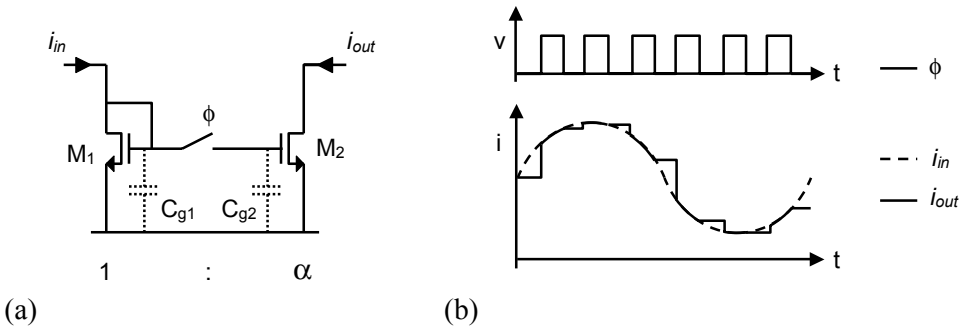

Figure 2.1 Switched-current memory cell principle (a) and example waveforms (b).

With processes optimised for digital performance, passive integrated filter implementations demand excessive area, and poor tolerance on integrated passive devices limit their performance. The switched capacitor (SC) technique requires only integrated capacitors and op-amps and allows tuning of filter parameters. However, high quality capacitors require two poly layers and can be large, so are expensive to fabricate and voltage mode op-amps are likely to suffer worse signal to noise ratio as process supply voltage reduces [4]. Various continuous-time current-mode approaches, such as operational transconductance amplifier and capacitor (OTA-C) techniques have been proposed and demonstrated with good success but again these still require capacitors and the OTA design can be complex especially if a tuning mechanism is required with these structures [5].

Careful consideration has led us to believe that the switched-current (SI) technique satisfies best the requirements for designing successful analogue IP cores for present and future use in SoCs. The principle of a switched-current memory cell, shown in Figure 2.1, was first proposed in 1987 and relies on the parasitic capacitance at the gate of a MOS transistor to maintain its drain current [6, 7]. Construction of simple full period delay cells by the cascade of two memory cells allows filter functions to be realised with transistors alone [8]. The following advantages indicate why SI offers itself as an excellent candidate for use in SoC analogue cores:

- SI does not require linear passive components and could therefore be designed for any CMOS process having only the most basic digital layers.
- A current-mode approach and the simplicity of SI designs ensure their ability to function at low voltages, making the technique suitable for future processes [4].
- Consisting mainly of simple current mirrors, SI circuits are easy to design and the regular structures lend themselves towards automated generation.
- Time constants in SI relate to transistor dimensions allowing high frequency design [9].

Non-ideal effects, such as mismatch, settling, conductance ratio and most notably clock-feedthrough errors, limited the performance of the first SI cells, which was certainly less than SC equivalents. However, modern iterations of the basic cell are showing good promise in terms of high accuracy and low power [10]. A direct comparison of SI with SC in [4], with past and future processes, showed how the general 'figure of merit' of SI is likely to stay constant over future process advances with that for SC dropping below this within the next decade. The high accuracy S^2I cell, shown in Figure 2.2(a), seems to be the most successful at reducing charge injection errors. Furthermore, by deriving a virtual earth at its inputs, conductance ratio problems are minimised removing the need for cascodes and with only two transistors required between vdd and ground the topology is therefore particularly suitable for low voltage design [11]. It is speculated, however, that the more recent low-power class AB cell, shown in Figure 2.2(b), will be the first to truly challenge SC performance, despite a lower accuracy, simply because of its low power consumption as compared to class A cells [4]. It is clear that there is a choice of memory cells to use, and in reality this choice would depend on the end filter application, where if this requires a high accuracy the S^2I cell might be employed whereas if power was a more important constraint the AB cell could be chosen. In this work we initially used only the S^2I cell, mainly because of the greater amount of detailed literature available on its design [12, 13].

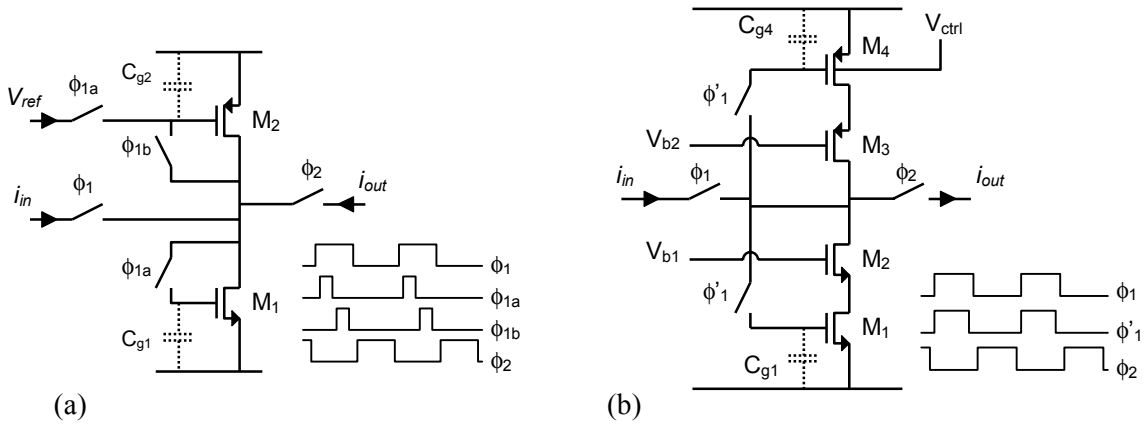

Figure 2.2 High performance memory cells, the S^2I cell from [11] (a) and the AB cell from [14] (b).

3 FILTER DESIGN METHODOLOGY

What requirements should a filter design methodology satisfy in order to be most suitable for IP core and SoC applications? Methodologies resulting in regular structures would allow for easier automation and block simplicity, hence speeding up the design phase. Having decided on SI, which is a sampled data technique, we have a choice of transformation into the digital domain. It is widely accepted that the bilinear transform is most useful as it allows the nyquist limit to be approached, allowing for higher frequency filters [15]. Methodologies based on passive LC ladder circuits would enjoy low sensitivity to component variations and therefore reduced accuracy requirements.

The most well known SI filter realisations use the bilinear integrator to simulate the signal flow graph of LC networks, but despite using the bilinear transform and being based on LC ladder circuits, this design methodology has a number of drawbacks. High quality integrators are not only difficult to design but by their very nature noise and charge injection errors are integrated as well as the signal, giving a significant limitation on the achievable dynamic range [15]. Furthermore, the filter transfer function directly affects the integrator coefficients which are set by current mirror ratios so the filter area, power and accuracy is dependent on the filter being realised. Finally, integrators with multiple outputs results in an increased capacitive load, lowering the achievable bandwidth [15].

We believe that wave filter design offers the best filter design methodology solution in the context of analogue cores. Covered in a now classical paper by Fettweis [16], wave digital filters emulate the behaviour of passive lossless filters by transforming passive L and C elements into one-port digital elements defined by an incident signal, a reflected signal and a port resistance. Adaptors are used to connect these one-port elements, with a simple third order lowpass example being shown in Figure 3.1 (refer to [16] for more information). Wave filters were originally found impractical for implementation in analogue continuous-time or SC as the resulting filter structures were too complex. However, the operations required to realise wave filters are summation and multiplication by a constant, these being easily achieved in current-mode. Wave filters also exhibit the following advantages:

- Wave filters are inherently based on the bilinear transform, allowing high frequency filters.
- Wave structures are formed by interconnection of easily designed building blocks
- The sum of coefficient values in any adaptor must equal two, which means that the end transistor dimensions do not have to have a one-to-one correspondence with transfer function coefficients unlike integrator based designs [17].
- The freedom in choice of adaptor coefficient values can be exploited to optimise the transistor level design for low sensitivity to element tolerances and nonideallities [15].
- Wave filters inherit the excellent passband sensitivities enjoyed by the passive filters from which they are derived.
- Some variations on the wave filter methodology have been shown to be efficient for designing high order filters [18].

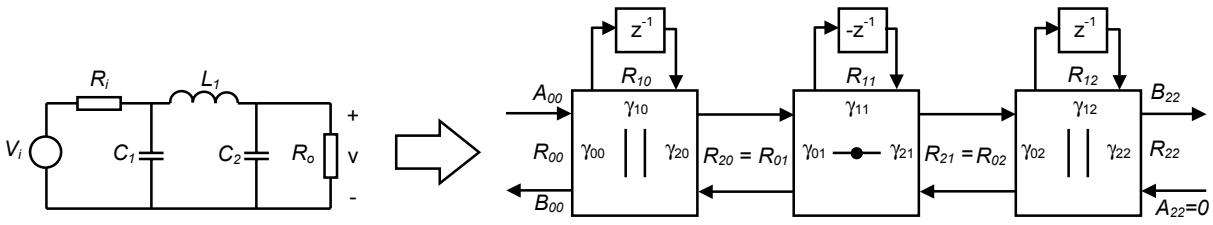

Figure 3.1 Example of a third order wave filter design a technique see [16] for more information.

4 AUTOMATION

The primary goal of design reuse and IP retargeting is to design a core to meet customer specified performances in the shortest possible time. The ideal solution to this would be computer aided design (CAD) software capable of creating a reliable analogue core from specifications in the shortest possible time. Realistically, any level of automation at any stage of the design flow resulting in an increase in productivity is beneficial.

It is important to draw attention to the differences between analogue synthesis and the semi-automated design reuse approach, which is widely agreed to be more suitable for development of high performance analogue cores [19-21]. Analogue synthesis implies complete transistor-by-transistor generation from high-level descriptions whereas a design reuse approach captures expert knowledge in the form of pre-designed and verified building blocks, and the automation is simply to tune these quickly and efficiently to new specifications or technologies. The most successful examples in the literature have included [19], a complete methodology for retargeting of analogue blocks to different specifications and technologies, [21] a similar technique from industry and indeed [22] for SI filters, although using integrators, not wave filter design. We believe that the success of these approaches has been due to their simple focus on increasing productivity, based at a very practical level. The choice of SI and a wave filter design methodology in Sections 2 and 3 were partly to give the modular approach which makes the implementation of a system similar to those detailed above particularly straightforward.

Any process to obtain a first cut transistor level design is necessarily approximate and it is important to subsequently tune the resulting transistor dimensions based accurate simulations. It is therefore important that any automation attempt should be integrated into design software capable of invoking simulators and circuit analysis tools. We have come to the conclusion that a tool implemented in the SKILL language and within the Cadence Design Framework best satisfies this need, given the ease with which the powerful proprietary tools can be invoked and the extensive use of Cadence Design Framework in industry. In fact the total solution should include a combination of high-level design including automatic optimisation if necessary, followed by a first cut transistor level process, and interactive simulation allowing manual intervention and design tuning.

5 PROPOSED DESIGN FLOW

Shown in Figure 5.1 is the proposed design flow for analogue SI wave filter cores based on the considerations made in this paper. All wave structures are based on passive reference filters, and these must first be derived, step 1 is therefore to design the reference LC filter from filter tables and to a given specification, verifying the filter shape by simulation. Step 2 derives the wave structure, in terms of ideal adaptors and delay cells for the passive filter, optimising adaptor coefficients for minimised sensitivity in a manner described in [15]. All of the transistor level design comes from that of the delay cell, made of two memory cells, as this also sets the unity transistor dimensions for the wave adaptors. Given a specified signal to noise ratio and power and along with certain process parameters, step 3 involves the design of this cell, with equations giving a first cut design as described in [12, 13] and simulation in the flow allowing manual optimisation of the cell. Step 4 is to construct the entire SI wave filter from the designed delay cells and adaptors, verifying performance at transistor level using a suitable switched network simulator such as Spectre RF. Although not considered in this project, layout would form step 5 and would be based on parameterised cells, these being well documented [21].

Progress so far has included the memory cell design section, which was considered the most important step. As was mentioned previously the system currently uses the S^2I cell as more literature was available on its design, however, the choice of memory cell is likely to be included as part of the flow at a later stage, providing an even more flexible system.

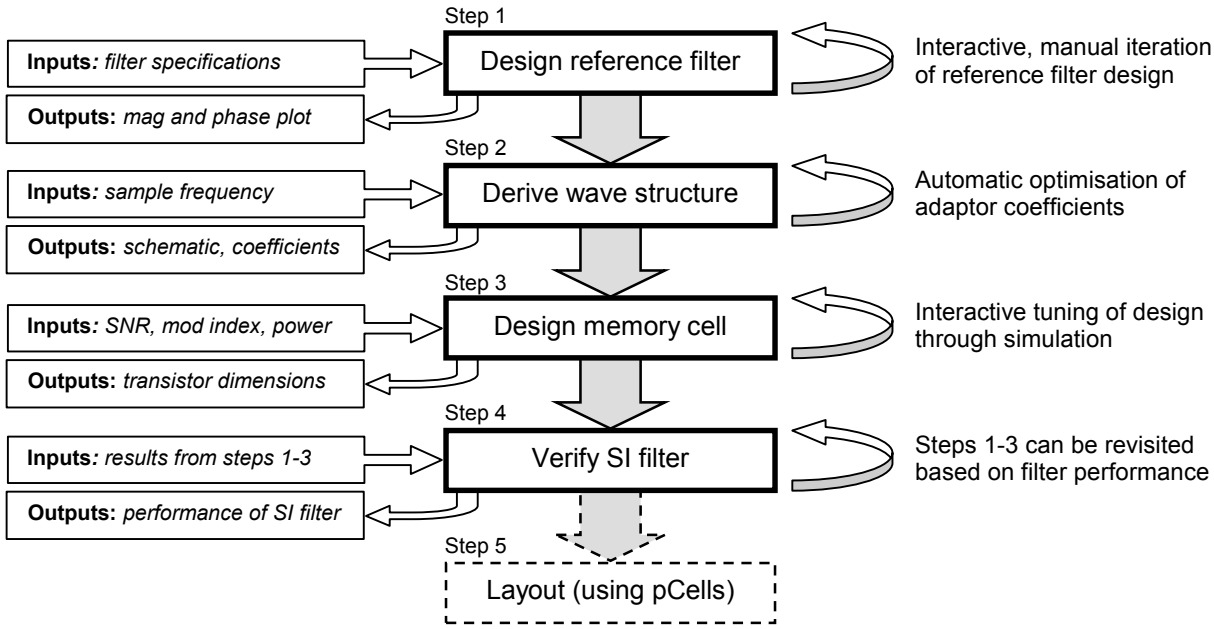

Figure 5.1 A design flow suitable for designing high performance SI wave filter IP cores.

6 CONCLUSIONS

This paper has addressed how careful consideration of design technique and methodology can result in analogue IP filter cores most suitable for present and future SoC applications. It has been shown that the SI design technique is particularly suitable for core design and SoC as it requires only a standard digital process, has simple easily designed building blocks and the potential to operate at low voltages. Furthermore, a wave filter design methodology is easily implemented using SI and has a number of advantages over an integrator approach including simpler design, less dependence of transistor dimensions on filter transfer function, and the ability to optimise the low spread of adaptor coefficients. To speed up the design process, some level of automation is necessary, but rather than complete synthesis, this should be of a knowledge based approach, reusing proven building blocks to increase productivity, with interactive simulation and both manual and automatic parameter optimisation. We have presented a design flow to address the considerations made in this paper and facilitate the rapid development of SI wave analogue filter cores. Current work involves completing the implementation of this automated system within a CAD tool extensively used in industry.

7 REFERENCES

[1] E. J. Marinissen, R. Kapur, M. Lousberg, T. McLaurin, M. Ricchetti, and Y. Zorian, *"On IEEE P1500's Standard for Embedded Core Test"*, Submission manuscript for Journal of Electronic Testing: Theory and Applications, vol. 18, August 2002.

[2] S. Ohr, *"PANEL: Analog Intellectual Porperty: Now? Or Never?"* presented at the IEEE Design Automation Conference, New Orleans, pp. 181-182, June 2002.

[3] P. L. Levin and R. Ludwig, *"Crossroads For Mixed-Signal Chips"*, in IEEE Spectrum, 2002, pp. 38-43.

[4] J. B. Hughes, A. Worapishet, and C. Toumazou, *"Switched-Capacitors Versus Switched-Currents: A Theoretical Comparison"*, presented at the IEEE International Symposium on Circuits and Systems, Geneva, Switzerland, pp. 409-412, May 2000.

[5] Y. Tao and J. K. Fidler, *"Electronically Tunable Dual-OTA Second-Order Sinusoidal Oscillators/Filters with Non-Interlacing Controls: A Systematic Synthesis Approach"*, IEEE Transactions on Circuits and Systems I, vol. 47, pp. 117-129, Feburary 2000.

[6] N. C. Bird *"Storing sampled analogue electrical currents"*, UK Patent 2209895, 16th Sept 1987

[7] N. C. Bird *"A method of and a circuit arrangement for processing sampled analogue electrical signals"*, UK Patent 2213011, 16th Sept 1987

[8] J. B. Hughes, I. C. Macbeth, and D. M. Pattulllo, *"Switched Current Filters"*, IEE Proceedings - Pt G, vol. 137, pp. 156-162, April 1990.

[9] A. Yufera and A. Rueda, *"Studying the Effects of Mismatching and Clock-Feedthrough in Switched-Current Filters Using Behavioural Simulation"*, IEEE Transactions on Circuits and Systems II, vol. 44, pp. 1058-1067, December 1997.

[10] A. Worspishet, R. Sitdhikorn, and J. B. Hughes, *"Low-Power Complex Channel Filtering Using Cascoded Class AB Switched-Currents"*, presented at the IEEE International Symposium on Circuits and Systems, Scottsdale, Arizona, pp. 453-456, May 2002.

[11] J. B. Hughes and K. W. Moulding, *"S2I: A Switched-Current Technique for High Performance"*, Electronics Letters, vol. 29, pp. 1400-1401, 5th August 1993.

[12] I. O. Conner and A. Kaiser, *"Automated Synthesis of Current-Memory Cells"*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 19, pp. 413-424, April 2000.

[13] J. B. Hughes, *"Top-down Design of a Switched-Current Video Filter"*, IEE Proceedings - Circuit Devices and Systems, vol. 147, pp. 73, Feburary 2000.

[14] N. C. Battersby and C. Toumazou, *"Class AB Switched-Current Memory for Analogue Sampled Data Systems"*, Electronics Letters, vol. 27, pp. 873-875, May 1991.

[15] A. Yufera, A. Rueda, and J. L. Huertas, *"Programmable Switched Current Wave Analog Filters"*, IEEE Journal of Solid-State Circuits, vol. 29, pp. 927-935, August 1994.

[16] A. Fettweis, *"Wave Digital Filters: Theory and Practice"*, Proceedings of the IEEE, vol. 74, pp. 270-327, Feburary 1986.

[17] C. Toumazou, J. B. Hughes, and N. C. Battersby, *"Switched-currents: an analogue technique for digital technology"*: Peter Peregrinus Ltd., 1993.

[18] J. D. Lancaster, B. M. Al-Hashimi, and M. Moniri, *"Efficient SI Wave Elliptic Filters Based on Direct and Inverse Bruton Transformations"*, IEE Proceedings of Circuits Devices and Systems, vol. 146, pp. 235-241, October 1999.

[19] R. Castro-Lopez, F. V. Fernandez, M. Delgado-Restituto, F. Medeiro, and A. Rodriguez-Vazquez, *"Generation of Technology-Portable Flexible Analog Blocks"*, presented at the IEEE International Symposium on Circuits and Systems, Scottsdale, Arizona, pp. 61-64, May 2002.

[20] R. Castro-Lopez, F. V. Fernandez, M. Delgado-Restituto, and A. Rodriguez-Vazquez, *"Retargeting of Mixed-Signal Blocks for SoCs"*, presented at the Design Automation and Test in Europe, Munich, Germany, pp. 772-773, March 2001.

[21] J. N. Xu, J. Vital, and N. Horta, *"Reusability Methodology of IC Layout - Part II"*, presented at the Design Automation and Test in Europe, Workshop, Munich, Germany, March 2001.

[22] J. B. Hughes, K. W. Moulding, J. Richardson, J. Bennett, W. Redman-White, M. Bracey, and R. S. Soin, *"Automated Design of Switched-Current Filters"*, IEEE Journal of Solid-State Circuits, vol. 31, pp. 898-907, July 1996.