Circuit fabrication: The wafer used for circuit fabrication consisted of the following layers grown by MOVPE on a semi-insulating InP substrate: 300 nm *i*-InP buffer, 10 nm *i*-InGaAs spacer, 8 nm *n*-InGaAs 2×10^{18} cm^{-3} channel, 5 nm *i*-InGaAs spacer, 50 nm *i*-InAlAs gate insulator and 5 nm *i*-InGaAs cap. HFET fabrication has been discussed previously [3, 4]. The devices were mesa-isolated prior to first level metal deposition, at which stage the bottom plate of MIM capacitors was deposited. Next, the devices were fully passivated with 100 nm of silicon nitride. A polyimide process was then used to interconnect the devices, with the majority of CPW metallisation deposited on nitride at second level metal stage in 1·1 μm thick TiAu.

Electrical results: At DC 100 μm wide devices had a peak transconductance of 280 mS/mm at $V_{ds} = 3$ V, and a pinchoff voltage of $-1{\cdot}75$ V. On-wafer measurements were made using an HP8510B network analyser up to a frequency of 50 GHz. Discrete 0·25 μm gate length HFETs had a peak f_t of 80 GHz and an f_{max} of 140 GHz. Fig. 2 shows the measured gain (S_{21}) against frequency for the single stage, doped-channel HFET amplifier when optimally biased with $V_{ds} = 3{\cdot}0$ V, $V_{gs} = -0{\cdot}75$ V with a source–drain current of 23 mA. Peak gain of 14·4 dB was obtained at 39 GHz, within the designed frequency band. S_{12} was below -10 dB at the peak gain point. Fig. 3 shows the return characteristics of the amplifier: the input and output return losses were better than -10 and -3 dB in the peak gain region, respectively.

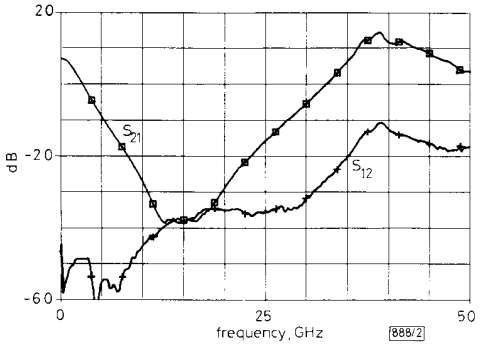

Fig. 2 *Measured gain against frequency for 38·6–40 GHz single stage, MMIC CPW doped channel HFET amplifier on InP*

Peak gain (S_{21}) of 14·45 dB was measured at 39 GHz; S_{12} is below -10 dB at 39 GHz

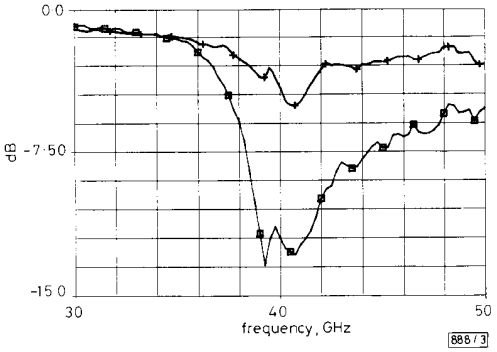

Fig. 3 *Magnitude of S_{11} and S_{22} of single stage amplifier against frequency between 30 and 50 GHz*

□ S_{11}
+ S_{22}

Conclusions: We have designed and fabricated, to our knowledge, the first MMIC using doped-channel HFETs and CPW interconnect on InP. The circuit was designed to have peak gain in the 38·6–40 GHz band, and a gain of 14·4 dB was measured at 39 GHz. This result illustrates the potential of doped channel HFETs for use in MMICs and MMOEICs.

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28th April 1993

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PACKET RESERVATION MULTIPLE ACCESS FOR WIRELESS MULTIMEDIA COMMUNICATIONS

M. Eastwood, L. Hanzo and J. C. S. Cheung

Indexing terms: Digital communication systems, Multi-access systems

Packet reservation multiple access (PRMA) is portrayed as a multimedia packet multiplexer conveying speech, data and video signals, which ensures that the slot occupancy of conventional time division multiple access (TDMA) links is approximately doubled. In addition to 20 speech users the 20 slot 720 kbit/s scheme presented supported 20 data users and up to seven video users, while maintaining a slot occupancy in excess of 80%.

Introduction: Packet reservation multiple access (PRMA) was conceived in order to multiplex speech users onto time division multiple access (TDMA) links [1]. The objective speech performance of a PRMA assisted cordless telecommunications (CT) scheme was reported in Reference 2, while Wong and Goodman studied the performance of a mixed speech and data PRMA scheme in Reference 3.

In contrast to previous studies, we portray PRMA as a multimedia packet multiplexer for conveying a mixture of speech, data and video information from mobile multimedia portable stations (PSs) to a central base station (BS) on a demand basis and evaluate its performance for a variety of transmission scenarios.

System description: In speech transmissions the voice activity detector (VAD) [4] of the PS queues speech packets of the speech encoder to contend for an up-link TDMA time slot and if the PS obtains permission to transmit, it reserves its time slot for future transmissions. When the VAD detects a silent gap, it surrenders the time slot for other speech, data or video users, who are becoming active. If a speech user cannot obtain a reservation within 30 ms, its packet must be dropped but the dropping probability must be kept below $P_{drop} = 1\%$ [1].

Data users on the other hand cannot afford to drop packets at all, but tolerate longer delays and can be allocated to slots, which are not reserved by speech users in the present frame. Wong and Goodman [3] proposed an integrated PRMA (IPRMA) protocol in which data users contend for a number

of subsequent vacant slots determined from the total number of vacant slots in the frame and the number of packets to be transmitted in the data queuing buffer. Accordingly, stacking the consecutive TDMA frames vertically above each other, a speech user requires reservation of vertically matching slots, while data users can be granted horizontal reservation of some or all idle time slots within each frame, but contending afresh for reserving slots of the consecutive frames [3]. Similarly to speech users, data users are assumed a negative exponential packet generation model and are assigned a permission probability that either allows or refuses permission to contend during any particular slot for a reservation within the current TDMA frame. An interesting feature of the IPRMA scheme is that it is advantageous to allow data users to contend only if they have a certain minimum number of packets in their buffers in order to prevent too frequent contentions and collisions for the sake of delivering a single packet. Whereas speech stability is maintained until $P_{drop} < 1\%$, data transmission stability is defined in terms of maximum data delay or buffer length.

In our multimedia PRMA multiplexer, apart from speech and low-rate data users, we also accommodated mobile video phone users having transmission rates between 32 and 48 kbit/s [5]. These sources were not allowed to drop packets and had a negative exponential source packet arrival rate, but contended for reservation immediately without imposing a minimum buffer content condition, when a video packet reached the contention buffer. This allowed us to minimise the video delay and retain adequate 'lip synchronisation' for voice and video.

Results and discussion: In our experiments the PRMA channel rate was 720 kbit/s, and we used 20 time slots of 1 ms duration and a speech rate of 32 kbit/s. Initially no video users were served and the optimum speech permission probability was $P_{sp} = 0.3$, and the data permission probability $P_d = 0.03$. System stability was defined as $P_{drop} < 1\%$, and a maximum data buffer length of 200 packets, each delivering 640 bits. The total maximum storage required was then $200 \times 640/8 = 16$ kbyte. At the stability limit the maximum supported data rate was found to be 13·6 kbit/s, when assuming 20 speech plus 20 data users. Explicitly, owing to PRMA we provided an extra 13·6 kbit/s data channel for each user in addition to unimpaired speech communications, which was equivalent to a total channel capacity gain of $20 \times 13.6 = 272$ kbit/s or a relative gain of $272/640 = 42.5\%$, normalised to the primary information rate of $20 \times 32 = 640$ kbit/s. When defining slot occupancy as the proportion of actively exploited time slots, the slot occupancy at a speech activity of 42% became $(20 \times 0.42 \times 32 + 20 \times 13.6)/640 = 84.5\%$, which was achieved because only the 20 speech users had a strict delay limit of 30 ms, whereas the remaining data users were found to experience a 700 ms average delay.

In our next experiment we replaced the data users with video users characterised by a negative exponential packet arrival model, whose stability was defined as an average packet delay below 100 ms. The PRMA channel parameters were unchanged. The number of 32 and 48 kbit/s video users supported with a delay below 100 ms alongside 20 speech users with $P_{drop} < 1\%$ is seen in Fig. 1 to be seven and five, respectively. The channel capacity gain was slightly more modest than for data users, namely $7 \times 32 = 224$ and $5 \times 48 = 240$ kbit/s, respectively. As demonstrated by Fig. 1, this was achieved at a slot occupancy of ~77%, and the optimum video permission probability was $P_v = 0.15$. Higher throughput was achieved only at the expense of increased video packet delay and speech dropping rate.

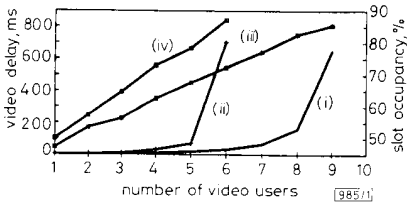

Fig. 1 *Video delay and channel efficiency against number of video users*
(i) —— video delay (32 kbit/s)
(ii) —+— video delay (48 kbit/s)
(iii) —*— slot occupancy (32 kbit/s)
(iv) —□— slot occupancy (48 kbit/s)

These initial findings culminated in the addition of 20 2·4 kbit/s, data users into the mixed speech and video model, which required an extra $20 \times 2.4 = 48$ kbit/s channel capacity. Therefore we had to reduce the number of 32 kbit/s video users from seven to six. A rate of 2400bit/s is low in comparison to the speech and video user rates and is suitable for facsimile or other low rate applications. Delays of up to a few seconds are acceptable for such users.

Fig. 2 portrays the joint effect of the data permission probability P_d on the speech packet dropping probability P_{drop}

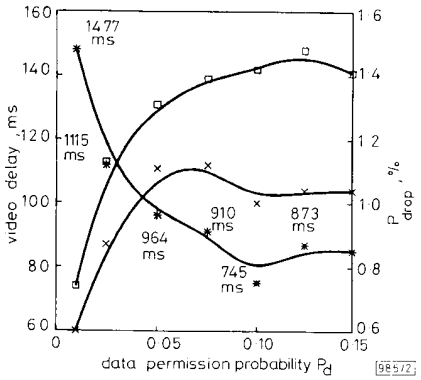

Fig. 2 *Video delay and packet dropping probability against P_d*
—*— data delay
—□— P_{drop}
—×— video delay

scaled on the right hand side axis, the video delay scaled on the left axis as well as data delay, for which scaling is displayed as individual delay values in milliseconds. Observe from the Figure that the speech packet dropping stability constraint was slightly more stringent than the video delay stability limit and, to maintain overall stability, $P_d < 0.02$ had to be ensured. The minimum number of data packets to allow contention was six in this experiment in order to avoid excessive collisions. Further experiments showed no significant system performance dependence on this parameter in the range 2–6. Observe furthermore that for $P_d > 0.02$, the speech dropping probability exceeded 1% and the video delay also exceeded the stability limit of 100 ms at a concomitant reduction in data delay. This was explained by a higher chance of data packets competing for available slots and thus reducing their delay. At the same time the priority of the video users was less marked and hence the delay for video packets rose before levelling off. The benefit of using PRMA is the additional capacity to serve another 20 2·4 kbit/s data users and six 32 kbit/s video users with a resulting channel efficiency of $(20 \times 0.42 \times 32 + 20 \times 2.4 + 6 \times 32)/640 = 79.5\%$.

The overall system performance is characterised with the aid of Fig. 3, where the maximum data rate and the slot

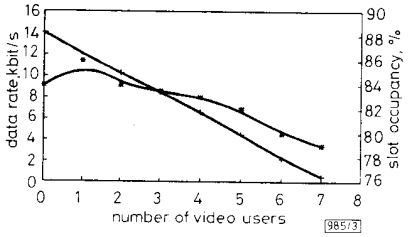

Fig. 3 *Data rate and channel efficiency against number of video users*
—+— data rate
—*— slot occupancy

occupancy are plotted against the number of 32 kbit/s video users. As expected, the supported data rate was inversely proportional to the number of video users, the highest slot occupancy was attained with only a low number of video users, and the highest slot occupancy was attained with only a low number of video users. This was explained by the added priority needed for the video users to maintain a packet delay below 100 ms, which required a higher proportion of vacant slots. Furthermore, the data messages tolerated higher delays and hence were conveyed using a lower proportion of vacant slots.

7th May 1993

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DIRECT EXTRACTION OF MOSFET DYNAMIC THERMAL CHARACTERISTICS FROM STANDARD TRANSISTOR STRUCTURES USING SMALL SIGNAL MEASUREMENTS

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Indexing terms: Field-effect transistors, Transistors

A method is presented for directly obtaining the temperature rise in MOSFETs due to channel current self-heating. The technique is based on small signal measurements, and also provides thermal time-constant data. No special layout structures are needed, making it suitable for bulk and SOI technologies. Experimental results are compared with data obtained using thermal noise measurements with a special SOI MOSFET, and the two figures show good agreement.

Introduction: Dynamic thermal feedback in MOS transistors is the mechanism by which heat generated in the channel modifies the instantaneous device characteristics on a *per-instance* basis, resulting in a reduction in output current [1]. The effect is particularly serious in SOI devices where the transistor is fabricated on an oxide layer, which has a much lower thermal conductivity than bulk silicon. This can give rise to overshoot transients when gate voltage is stepped [2], or drain characteristics which have a negative slope [3]. Because the device has a finite volume, this thermal feedback also has a time constant [4], and when viewed in small-signal terms, gives rise to frequency dependent drain conductance [5, 6]. Fig. 1 shows the effect on the drain current characteristic of an ideal device.

Difficulties with direct measurement: Whereas the physics of this effect are fairly straightforward, and it is clear that it must be taken into account in design, the characterisation of the effect in any particular device (i.e. with particular width, length etc.) is less simple. Clearly, the behaviour will vary with the

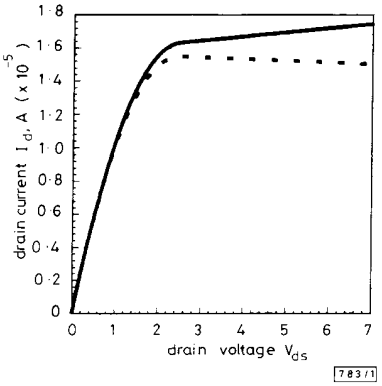

Fig. 1 *Effect of self-heating in MOSFET devices, as shown by ideal simulation*
——— behaviour at constant temperature
– – – – effect of self-heating showing negative output conductance in saturation

bias (i.e. power input), the width and length (thermal capacity and heat loss path to substrate) and interconnecting wiring (heat loss path to pads etc.). Several time constants can be identified [7] but small-signal measurement shows only one to be dominant [5, 6].

To obtain the thermal capacity, we can measure the dominant time constant directly, but the total thermal resistance still needs to be determined [5]. Direct measurement of the channel temperatures in operation is difficult, but some data have been obtained with special structures [5]. A recent method based on the thermal noise level in the body of a partially depleted SOI device [8] appears most promising; however, this requires the use of special body contacted structures.

Small signal drain conductance measurement: Measurements of the drain conductance of SOI MOSFETs as a function of frequency reveal unusual characteristics [5, 6]. If there is an electrically floating body, a pole-zero doublet is evident, due to body transconductance feedback. This can be easily identified as such due to its movement in frequency as a function of bias. In fully depleted or body tied devices, this is not normally present, but there remains another pole-zero doublet due to the lowpass filtering of the thermal feedback.

Fig. 2 shows the saturation drain conductance as a function of frequency taken from samples of body-tied partially depleted SOI devices. The thermally related doublet is quite clear, and on either side of it can be seen two distinct conductance levels. Some insight into the physical origins of these

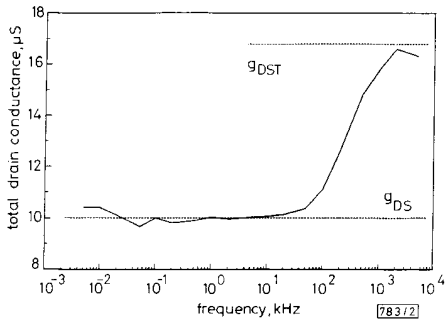

Fig. 2 *Measured drain conductance against frequency for 20 μm wide, 3 μm partially depleted SIMOX MOSFET with source connected body-tie* [8]
$V_{DS} = 2$ V, $I_{DS} = 745\,\mu$A