Analysis of mirror mismatch and clock-feedthrough in Bruton transformation switched current wave filters

B.M. Al-Hashimi, Y. Xie and M. Zwolinski

Abstract: The paper describes the modelling and analysis of the non-ideal performance of recently introduced Bruton transformation switched current (SI) wave filters. Two sources of errors are considered: mismatching in current mirrors and clock-feedthrough in delay cells. Using transistor-level realisations, analytical non-ideal models for the main components of Bruton transformation wave filters are developed, including capacitive source and load, and frequency dependent negative resistors. These models are integrated with MATLAB to study the influence of these errors on the filter frequency response. The non-ideal performance of 3rd-order low-pass and 5th-order high-pass elliptic filters using second-generation and S^2I delay cells are analysed and included.

1 Introduction

Switched current (SI) is a relatively new analogue sampled-data technique that has received considerable attention due to its numerous advantages over the switched capacitor technique. This includes implementation simplicity, low-voltage and low-power operation, and more importantly, compatibility with standard digital CMOS processes [1]. Recently we proposed a new efficient design method for SI wave filters [2, 3]. It has been shown how the application of direct [4] and inverse Bruton transformations to a suitably selected LC prototype prior to conversion to a wave filter yield significant reduction in SI circuit transistor count when compared with traditional wave filters (i.e. without transformations [5]). For example, it was shown that a 14th-order high-pass filter based on Bruton transformations utilises 15% fewer transistors than an equivalent wave filter designed without transformations. Fig. 1*a* shows a 3rd-order elliptic low-pass LC filter, and Fig. 1*b* gives the direct Bruton transformed wave filter. The direct Bruton transformation wave filter consists of capacitive source and load, serial and parallel adaptors, and FDNR components. More details on the design of Bruton transformation wave filters are given in [3]. SI circuits suffer from fundamental sources of error that produce deviations in terms of DC offset, gain and harmonic distortion [1]. The errors include finite conductance ratios, charge injection, transistor mismatch and clock-feedthrough. Numerous enhanced SI cells have been proposed to improve performance. Examples include regulated cascade current mirrors [1] for high output resistance, *N*-step scheme [6] for charge injection cancellation, and S^2I [7] and S^3I [8] techniques for reducing clock-feedthrough. Although the proposed techniques improve SI cell performance, they do not eliminate the errors completely, particularly transistor mismatch and clock-feedthrough errors. The effects of these two sources of error on SI filter performance must therefore be considered in order to assess how SI filters perform in practice. The aim of this paper is to present a detailed analysis of the non-ideal performance of Bruton transformation wave SI filters due to mismatching error in current mirrors and clock-feedthrough error in delay cells.

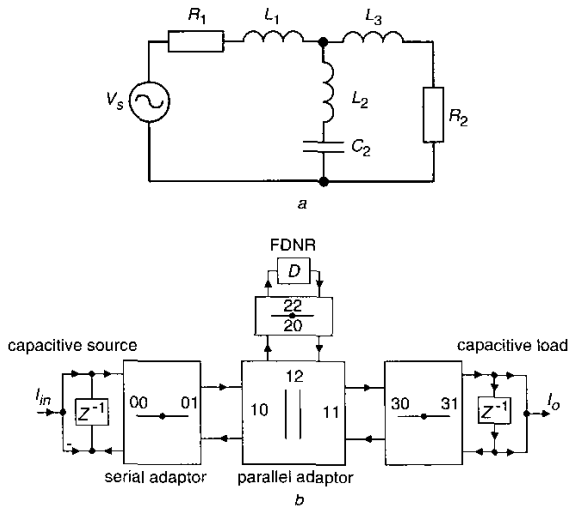

Fig. 1 *Third-order filters*
a Elliptic low-pass LC filter
b Direct Bruton transformation wave SI elliptic filter

2 Non-ideal behaviour of current mirrors and SI delay cells

This Section discusses briefly non-ideal current mirrors and SI delay cells and shows how their non-ideal performance is represented using simple models. The discussion is a short summary of the work reported in [9], and is included here since it is used in the development of the analytical non-ideal models of Bruton transformation filter components

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The authors are with the Electronic Systems Design Group, Department of Electronics and Computer Science, University of Southampton, Southampton, SO17 1BJ, UK

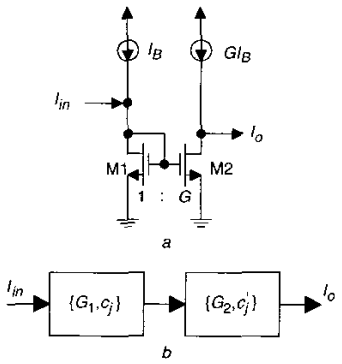

Fig. 2 *Simple current mirror with gain G, and block diagrams of cascaded current mirror*
a Simple current mirror
b Cascaded current mirror

outlined in Section 3. Fig. 2*a* shows a simple current mirror with gain G. The current mirror suffers from mismatch errors due to the small difference in the DC characteristics of each transistor, M1 and M2. The effect of this mismatch is to produce a DC offset, gain and nonlinear coefficient, leading to the non-ideal equation [9]

$$I_o \simeq c_o + c_1 I_{in} + c_2 I_{in}^2 \tag{1}$$

The error mismatching coefficients c_o, c_1 and c_2 are given in Table 1 for the nominal and non-ideal cases, where

$$E_o = -GI_B\left(\frac{\Delta\beta_2}{\beta_2^0} - \frac{\Delta\beta_1}{\beta_1^0}\right) + GI_B\frac{2(\Delta V_{t2} - \Delta V_{t1})}{(V_{GS1} - V_{t1}^0)_Q}$$

$$E_1 = G\left[\left(\frac{\Delta\beta_2}{\beta_2^0} - \frac{\Delta\beta_1}{\beta_1^0}\right) + \frac{(\Delta V_{t2} - \Delta V_{t1})}{(V_{GS1} - V_{t1}^0)_Q}\right]$$

$$E_2 = \frac{-G(\Delta V_{t2} - \Delta V_{t1})}{4I_B(V_{GS1} - V_{t1}^0)_Q}$$

The parameters β_1^o, β_2^o, $V_{t1}^o$and $V_{t2}^o$are the nominal values of the current factors and threshold voltages of transistors M1 and M2, respectively. Transistor mismatch errors are random in nature [10], and so these four mentioned parameters are affected by $\Delta\beta_1$, $\Delta\beta_2$, $\Delta V_{t1}$and ΔV_{t2}, which have normal distribution variations as discussed in Section 4. SI filters contain cascaded current mirrors, Fig. 2*b* shows a block diagram representation of a cascaded current mirror of two simple current mirrors with gains G_1 and G_2. The parameters c_j and $c_j'$are the error transistor mismatch coefficients of the simple current mirror given in Table 1. Since transistor mismatch errors are random in nature, the three coefficients are different from one current mirror to another.

Using (1), it can be readily shown that the non-ideal input–output relationship of the cascaded current mirror

Table 1: Error coefficients due to transistor mismatch in simple current mirror [9]

Coefficient	Nominal	Error term
c_0	0	E_0
c_1	$-G$	E_1
c_2	0	E_2

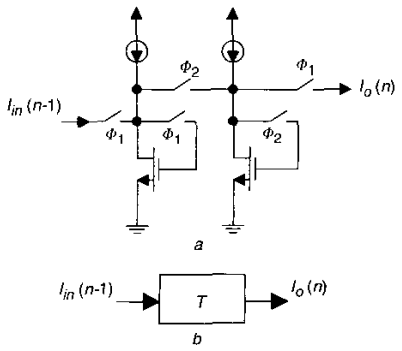

Fig. 3 *Second-generation SI delay cell (a), and block diagram representation of a delay cell (b)*

due to transistor mismatch is [9]

$$I_o = C_0 + C_1 I_{in} + C_2 I_{in}^2 \tag{2}$$

where

$$C_0 = c_0' + c_1' c_0 + c_2' c_0^2$$
$$C_1 = c_1' c_1 + 2c_1 c_0 c_2'$$
$$C_2 = c_1' c_2 + c_2' c_1^2 + 2c_2 c_2' c_0$$

Transistor mismatch in single and cascaded current mirrors have been considered. Now, clock-feedthrough error in SI delay cells is examined. A delay cell using second-generation SI is shown in Fig. 3*a*, and its block diagram representation is given in Fig. 3*b*. The delay cell suffers from clock-feedthrough error due to the switches Φ_1 and Φ_2. The effect of this clock-feedthrough is to produce a DC offset, gain and nonlinear errors as shown in (3):

$$I_o(n) = M_0 + (1 + M_1)I_{in}(n-1) + M_2 I_{in}^2(n-1) \tag{3}$$

where

$$M_0 = -m_0 m_1$$
$$M_1 = 2m_1 + m_1^2 - 2m_0 m_2$$
$$M_2 = m_2 m_1$$

and

$$m_0 = -2\Delta v_f\sqrt{I_B\beta_n} - \Delta v_f^2\beta_n$$

$$m_1 = \Delta v_f\sqrt{\frac{\beta_n}{I_B}}$$

$$m_2 = \frac{\Delta v_f\sqrt{\beta_n I_B}}{4I_B^2}$$

The parameter Δv_f is the incremental increase in the transistor gate voltage due to clock-feedthrough error, I_B is the cell bias current, and β_n is the tranconductance parameter of an NMOS transistor. Typical values for these parameters are given in Section 4.

3 Models of non-ideal components of Bruton transformation SI wave filters

The effects of transistor mismatch and clock-feedthrough on the frequency response of SI traditional wave filters (i. e. without transformations) were studied in [9]. The Bruton transformation SI filters [2, 3] are based on new wave components, which are not used by the traditional wave design method. This section develops analytical models for these new wave components using the results outlined in

Section 2. Each non-ideal component model is developed in the form of a difference equation representing the input–output relationship of the wave component including transistor mismatch and clock-feedthrough errors. The modelling process involves the following three main steps:

(i) identification of the current signal path of each term in the wave component ideal difference equation physical SI realisation

(ii) obtaining the input–output relationship of each current signal path of the wave component using the mismatch and/or clock-feedthrough error expressions given in (1)–(3)

(iii) summing the contributions of all the component current signal paths to yield the non-ideal model of the wave component in the form of a difference equation.

To illustrate the modelling process, models for the main components of Bruton transformation filters, including capacitive source and load, and FDNR are developed. Also, a model for a non-ideal series adaptor is developed. Note that the presented modelling process is general and can be applied to develop models of wave components implemented using different SI implementation techniques including first-generation, second-generation and S^2I. In this paper, component models based on second-generation SI delay cells are developed as examples, and the effect of second-generation and S^2I implementation techniques on the filter frequency response is analysed and compared in Section 4.

3.1 Capacitive source wave component

The capacitive source wave component is shown in Fig. 4. The difference equation of the ideal capacitive source is

$$B(n) = I_{in}(n) - I_{in}(n-1) + A(n-1) \tag{4}$$

where $I_{in}(n)$, $I_{in}(n-1)$ and $A(n-1)$ are the input, delayed input and filter feedback signals, respectively, and $B(n)$ is the output signal of the capacitive source.

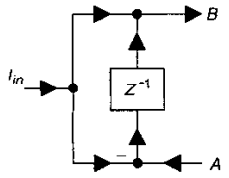

Fig. 4 *Capacitive source wave component*

The capacitive source circuit using second-generation SI realisation is shown in Fig. 5. It consists of one delay cell, T, and three current mirrors (M1–M2), (M1–M3) and (M4–M5). The current sources are marked: CM1, CM2 and CM3. Following step 1 of the modeling process, the current signal paths of the ideal difference equation of the capacitive source (4) are identified and presented in Fig. 6.

The first term of the capacitive source difference equation, the signal current $I_{in}(n)$ flows through the current mirrors CM1 and CM3. Hence it is affected by the mismatch of these two current mirrors as shown in Fig. 6. The input–output relationship of a non-ideal current mirror due to transistor mismatch (1) has three coefficients: DC offset (c_o), gain (c_1) and nonlinear coefficient (c_2). Assume that the transistor mismatch coefficients of currents mirrors CM1 and CM3 are $\{c_{10}, c_{11}, c_{12}\}$ and $\{c_{30}, c_{31}, c_{32}\}$, respectively, and, using the input–output relationship of a non-ideal cascaded current mirror, the input–output

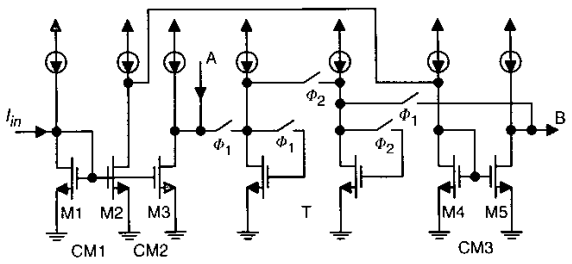

Fig. 5 *Capacitive source circuit using second-generation SI delay cells*

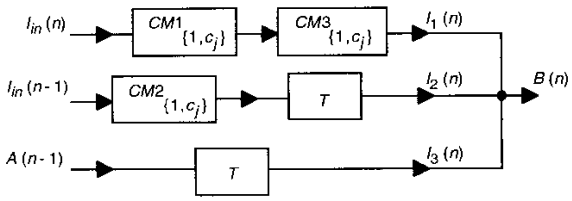

Fig. 6 *Block diagram model of non-ideal capacitive source wave component*

relationship of the first term of the ideal capacitive source difference equation is

$$I_1(n) = C_0 + C_1 I_{in}(n) + C_2 I_{in}^2(n) \tag{5}$$

where

$$C_0 = c_{30} + c_{31}c_{10} + c_{32}c_{10}^2$$
$$C_1 = c_{31}c_{11} + 2c_{11}c_{32}$$
$$C_2 = c_{31}c_{12} + c_{32}c_{11}^2 + 2c_{10}c_{12}c_{32}$$

Note that the first digit in the transistor mismatch coefficient index indicates the current mirror number and the second digit represents the error mismatch coefficient of the input–output relationship. For example, c_{30} denotes current mirror three (CM3), coefficient c_0 of Table 1.

Consider the second term of the difference equation of ideal capacitive source, $I_{in}(n-1)$. Fig. 5 shows that this current flows through current mirror CM2 and the delay cell. Hence it is affected by both transistor mismatch error due to the current mirror and clock-feedthrough error due to the delay element. Assume that the transistor mismatch coefficients in current mirror CM2 are $\{c_{20}, c_{21}, c_{22}\}$, and the input–output relationship of a non-ideal delay cell due to clock-feedthrough is (3), and the input–output relationship of the second term of the ideal capacitive source difference equation is

$$I_2(n) = M_0 + c_{20} + c_{20}M_1 + (c_{21} + c_{21}M_1)I_{in}(n-1) + (c_{22} + c_{22}M_1 + c_{21}^2M_2)I_{in}^2(n-1) \tag{6}$$

Finally, the third term of the capacitive source difference equation is considered – the feedback signal, $A(n-1)$. Fig. 5 shows that this signal flows only through the delay cell, and hence it is affected by clock-feedthrough error. Using (3), the input–output relationship of this term is

$$I_3(n) = M_0 + (1 + M_1)A(n-1) + M_2A^2(n-1) \tag{7}$$

Having obtained the input-output relationship of the various terms of (4), the model for the non-ideal capacitive source wave component is obtained by summing the

expressions of (5)–(7) to yield

$$B(n) = I_1(n) + I_2(n) + I_3(n) \tag{8}$$

3.2 FDNR component wave component

The FDNR wave component is shown in Fig. 7. The difference equation of the ideal FDNR component is

$$B(n) = 2A(n-1) - B(n-2) \tag{9}$$

where $A(n-1)$ is the delayed input signal and $B(n-2)$ is the delayed output signal.

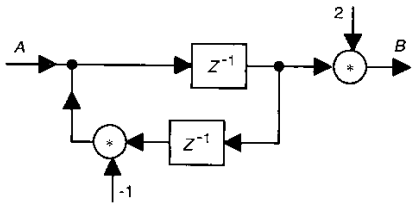

Fig. 7 *FDNR wave component*

Fig. 8 shows the FDNR component circuit using second-generation SI delay. The circuit consists of two delay cells, T1 and T2, used to generate the necessary delays of (9), and three current mirrors: (M1–M2), (M1–M3) and (M4–M5). The current mirrors are marked CM1, CM2, and CM3, respectively. Note that CM1 is used to provide a gain of 2 for the first term of (9).

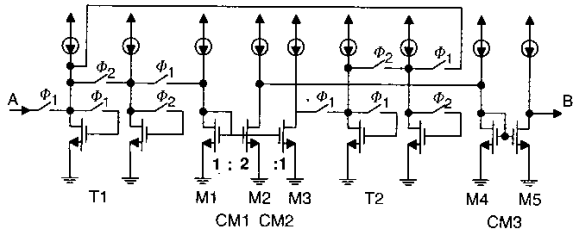

Fig. 8 *FDNR circuit using second-generation SI delay cells*

Examining the circuit in Fig. 8, the signal paths of the FDNR difference equation are identified and presented in Fig. 9*a*. The input signal, A, flows through delay cell, T1, and current mirrors CM1 and CM3. Therefore, signal A is affected by the clock-feedthrough of T1 and the transistor mismatch of CM1 and CM3. The term $B(n-2)$ of (9) is the output of the FDNR component two clock cycles earlier which flows through the entire FDNR component as shown in Fig. 9*a* as the feedback and feed-forward loops.

To derive the analytical model of the non-ideal FDNR component, the input–output relationship of each signal path of Fig. 9*a* needs to be obtained. To facilitate this, Fig. 9*a* is redrawn as Fig. 9*b* showing more clearly the signal paths of the FDNR component. The signal $B_1(n)$ is the output of the forward path of the FDNR component, and $B_2(n)$, is the combined feedback and feed-forward paths signal. Assuming that $\{c_{10}, c_{11}, c_{12}\}$, $\{c_{20}, c_{21}, c_{22}\}$ and $\{c_{30}, c_{31}, c_{32}\}$ are the transistor mismatch coefficients in CM1, CM2 and CM3 respectively, and the coefficients of the clock-feedthrough in T1 and T2 are (M_{10}, M_{11}, M_{12}) and (M_{20}, M_{21}, M_{22}), respectively, the input–output relationship of $B_1(n)$ is

$$B_1(n) = a_0 + a_1 A(n-1) + a_2 A^2(n-1) \tag{10}$$

where

$$\begin{aligned} a_0 &= C_0 + C_1 M_{10} + C_2 M_{10}^2 \\ a_1 &= C_1 + C_1 M_{11} + 2C_2 M_{10} \\ a_2 &= C_1 M_{12} + C_2 \end{aligned}$$

Similarly, the input–output relationship of the $B_2(n)$ signal is

$$B_2(n) = b_0 + b_1 B(n-2) + b_2 B^2(n-2) \tag{11}$$

where

$$\begin{aligned} b_0 &= C_0 + M_{10} + (c_{20} + M_{20})(1 + M_{11}) \\ b_1 &= (1 + M_{11})(1 + M_{21})c_{21} \\ &\quad + 2(M_{20} + c_{20})(1 + M_{21})c_{21} M_{12} \\ b_2 &= M_{12} c_{21}^2 (1 + M_{21})^2 + (1 + M_{11})(c_{22}(1 + M_{21}) \\ &\quad + c_{21}^2 M_{22}) + C_2((1 + M_{11})(1 + M_{21})c_{21})^2 / C_1 \end{aligned}$$

The difference equation of the non-ideal FDNR component is given by summing the contributions of the two signals: $B_1(n)$ and $B_2(n)$.

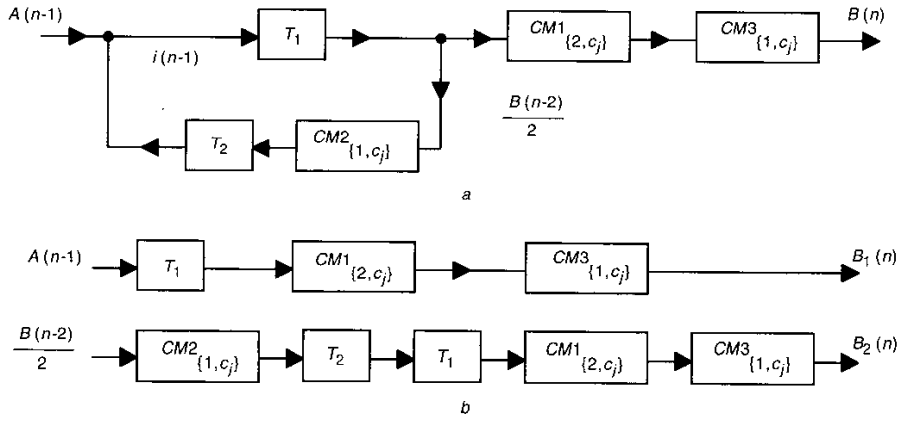

Fig. 9 *Block diagram model of non-ideal FDNR wave component of Fig. 8*
a Signal paths
b Alternative diagram

3.3 Capacitive load wave component

The capacitive load component is shown in Fig. 10. The difference equation of the ideal capacitive load is:

$$B(n) = A(n-1)$$

$$I_o(n) = A(n) + B(n) \tag{12}$$

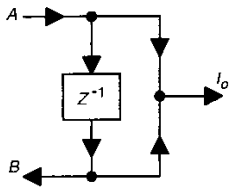

Fig. 10 *Capacitive load wave component*

Fig. 11 shows the capacitive load circuit using second-generation SI delay cells. The circuit consists of one delay cell, T, and five current mirrors: CM1, CM2, CM3, CM4 and CM5.

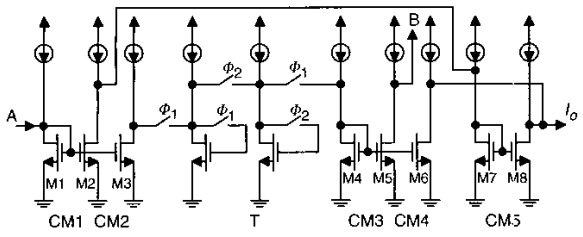

Fig. 11 *Capacitive load circuit using second-generation SI delay cells*

Using a similar analysis to that used in identifying the current signal paths of the previous wave components, Fig. 12 shows the block diagram model of the non-ideal capacitive load.

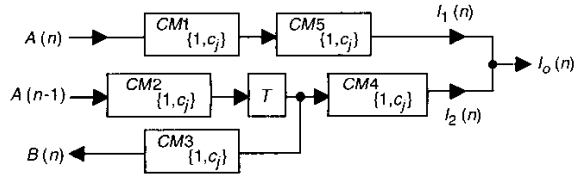

Fig. 12 *Block diagram model of non-ideal capacitive load component*

Assume the $\{C_0, C_1, C_2\}$ are the transistor mismatch coefficients of the cascade current mirror, CM1 and CM5, the signal $I_1(n)$ is

$$I_1(n) = C_0 + C_1A(n) + C_2A^2(n) \tag{13}$$

Similarly, assume $\{c_{20}, c_{21}, c_{22}\}$ $\{c_{20}, c_{21}, c_{22}\}$and $\{c_{40}, c_{41}, c_{42}\}$are the transistors mismatch coefficients of the simple current mirrors CM2 and CM4 and, making use of (3), the signal $I_2(n)$ is

$$I_2(n) = a_0 + a_1A(n-1) + a_2A^2(n-1) \tag{14}$$

where

$$a_0 = c_{40} + c_{41}M_0 + c_{41}c_{20}$$

$$a_1 = c_{41}c_{21} + 2c_{20}c_{21}c_{42} + 2c_{42}c_{21}M_0$$

$$a_2 = c_{41}c_{22} + c_{21}^2c_{42} + 2c_{42}c_{21}^2M_1$$

Clearly, the output current, $I_o(n)$, of the capacitive load component is given by the summation of (13) and (14). Now, the input–output relationship of the capacitive load feedback signal $B(n)$ is obtained. As can be seen from Fig. 12, this signal path consists of CM2, delay cell T and CM3. Assume that $\{c_{30}, c_{31}, c_{32}\}$is the transistor mismatch coefficient of the simple current mirror CM3. The $B(n)$ signal is

$$B(n) = b_0 + b_1A(n-1) + b_2A^2(n-1) \tag{15}$$

where

$$b_0 = c_{30} + c_{31}M_0 + c_{31}c_{20}$$

$$b_1 = c_{31}c_{21} + 2c_{21}c_{20}c_{32} + 2c_{32}c_{21}M_0$$

$$b_2 = c_{31}c_{22} + c_{21}^2c_{32} + 2c_{32}c_{21}^2M_1$$

The model of the non-ideal capacitive load is given by (13)–(15).

3.4 Wave adaptors

Up to this point, analytical models for non-ideal (mismatch and clock-feedthrough errors) wave components introduced by the Bruton transformations have been developed. To complete the modelling of Bruton transformations wave filter non-ideal performance, adaptors need to be considered [11]. There are two types of adaptors–series and parallel–used to connect the various elements of the filter structure, for example as shown in Fig. 1*b*. Adaptors affect the performance of wave filters as reported in [9], where a model for a non-ideal three-port parallel adaptor was proposed. In this paper, the non-ideal performance of a two-port series adaptor is developed. Both adaptor models are used in Section 4 when analysing the non-ideal frequency response of Bruton transformation SI wave filters. Fig. 13 shows the symbol of a two-port series adaptor, where A denotes the incident variables and B denotes the reflected variables.

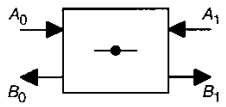

Fig. 13 *Two-port series adaptor symbol*

The input–output relationship of a two-port serial adaptor in matrix form is

$$\begin{bmatrix} B_1(n) \\ B_0(n) \end{bmatrix} = \begin{bmatrix} 1-y_1 & -y_1 \\ -y_0 & 1-y_0 \end{bmatrix} \begin{bmatrix} A_1(n) \\ A_0(n) \end{bmatrix} \tag{16}$$

where y_0 and y_1 are the adaptor coefficients, which are set using current mirrors. The circuit of a two-port series adaptor is shown in Fig. 14. The SI circuit as current mirrors and no delay cells; therefore, the adaptor operation is only affected by transistor mismatch errors. To obtain the input–output relationship of the non-ideal adaptor, consider the first entry of the above matrix,

$$B_1(n) = A_1(n) - y_1A_1(n) - y_1A_0(n) \tag{17}$$

With reference to Fig. 14, it can be seen that the current path of the first term in (17) has two current mirrors, (M4–M5) and (M12–M13), and the second term current path has three current mirrors, (M4–M6), (M7–M9) and (M12–M13). The current path of the third term has three current mirrors: (M1–M3) (M7–M9) and (M12–M13). Similarly, the current paths of $B_0(n)$ are the same as those of $B_1(n)$. The general block-diagram model of a non-ideal two-port series adaptor due to transistor mismatch is shown in

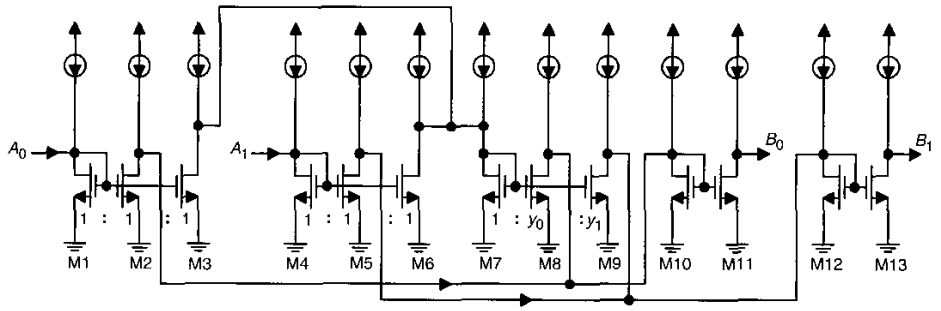

Fig. 14 *Two-port series adaptor circuit [12]*

Fig. 15, where Fig. 15*a* shows the current signal paths of the main diagonal elements of (16), and Fig. 15*b* shows the signal paths of the non-diagonal elements of (16).

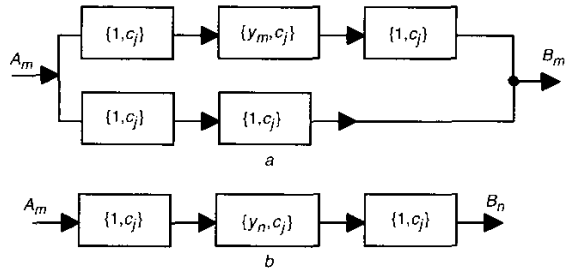

Fig. 15 *Signal paths of main diagonal and non-diagonal elements in input-output relationship of 2-port series adaptor*
a Diagonal
b Non-diagonal

Assume that $\{C_{t0}, C_{t1}, C_{t2}, t = 0, 1, 2, 3, 4, 5\}$are the transistor mismatch coefficients of the cascaded current mirrors: (M1–M2,M10–M11), (M1–M3,M7–M8), (M4–M6,M7–M8),(M4–M5, M12–M13), (M4–M6, M7–M9) and (M1–M3, M7–M9), respectively. Also, assume that $\{c_{00}, c_{01}, c_{02}\}$,$\{c_{10}, c_{11}, c_{12}\}$are the transistor mismatch coefficients of the simple current mirrors (M10–M11) and (M7–M9), respectively. Using Fig. 15, it can be shown that the input–output relationship of a non-ideal two-port serial adaptor is:

$$B_0 = (C_{00} + C_{01}A_0 + C_{02}A_0^2) + c_{00} + c_{01}((C_{10} + C_{11}A_0 + C_{12}A_0^2) + (C_{20} + C_{21}A_1 + C_{22}A_1^2)) + c_{02}((C_{10} + C_{11}A_0 + C_{12}A_0^2) + (C_{20} + C_{21}A_1 + C_{22}A_1^2))^2 \quad (18)$$

$$B_1 = (C_{30} + C_{31}A_1 + C_{32}A_1^2) + c_{10} + c_{11}((C_{40} + C_{41}A_1 + C_{42}A_1^2) + (C_{51} + C_{51}A_0 + C_{52}A_0^2)) + c_{12}((C_{40} + C_{41}A_1 + C_{42}A_1^2) + (C_{51} + C_{51}A_0 + C_{52}A_0^2))^2 \quad (19)$$

4 Simulation results

In this section, the effects of transistor mismatch in current mirrors and clock-feedthrough errors in delay cells on the frequency response of Bruton transformation SI filters are investigated. To facilitate this investigation a computer program was developed and interfaced with MATLAB [13]. The program flow chart is shown in Fig. 16.

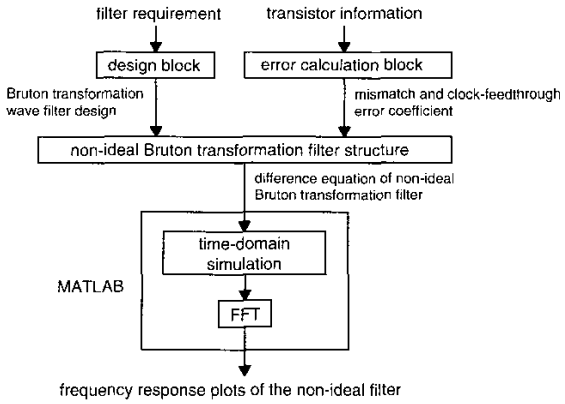

Fig. 16 *Program flow chart for analysing non-ideal performance of Bruton transformations SI wave filters*

The inputs to the design and error calculation blocks are filter requirements and transistor information, respectively. The filter requirements are: filter type (LP, HP, BP, BS); frequency specification (cutoff frequency, passband ripple, stopband edge and stopband attenuation). The filters are designed according to the Bruton transformations wave design method outlined in [3]. The output of the design block is a Bruton transformation wave based filter structure with adaptor coefficients that meets the required specification. The inputs to the error calculation block are: K_β, K_{vt} (technology-dependent parameters), W/L (transistor sizes), G (nominal gain), $(V_{GS}-V_t)$, I_B (bias current), β_n (trancon-ductance of NMOS transistor) and Δv_f (incremental increase in gate voltage). The outputs of the error calculation block are values of the mismatch and clock-feedthrough coefficients (m_0, m_1, m_2) given in Table 1 and (3), respectively, based on the transistor information supplied. The simulation results presented in this section were obtained using the following transistor information [9]: $K_\beta = 0.02\,\mu$m, $K_{vt} = 20\,\mu$m, $W/L = 60/10$, $G = 1$ (current mirror gain), $(V_{GS}-V_t) = 0.6$ V, $I_B = 10\,\mu$A, $\beta_n = 221\,\mu$A/V^2, and different values of Δv_f as shown later when presenting the simulation results. Considering the random origin of matching errors, N times Monte Carlo simulation are used to simulate filter performance, which includes the mismatch effect. The outputs of the design and error calculation blocks are used with the analytical models developed in Section 3 to derive the difference equation of the non-ideal Bruton transformations wave filter in the

presence of mismatch and clock-feedthrough errors. Using MATLAB, time domain simulation is carried out on the non-ideal filter difference equation, from which frequency response plots of the filter are obtained following an FFT analysis.

To examine the effects of transistor mismatch and clock-feedthrough errors on SI wave Bruton transformation filters, two examples are considered. The first example is a 3rd-order elliptic low-pass filter, Fig. 1*b*. The low-pass filter specification is: passband ripple $\varepsilon = 0.177$ dB; passband edge $fp = 0.0969$; stopband edge $fs = 0.229$; stopband attenuation > 36 dB. The filter adaptor coefficients are: $y_{00} = 0.3282$, $y_{01} = 0.5$, $y_{10} = 0.1718$, $y_{11} = 0.5$, $y_{12} = 1.3282$, $y_{20} = 0.5$, $y_{22} = 0.7527$, $y_{30} = 0.2055$ and $y_{31} = 0.3927$. Fig. 17*a* shows the filter ideal magnitude response, and when the filter suffers from clock-feedthrough error, assuming different values of $\Delta v_f = 10$ mV, 4 mV, 2 mV, −2 mV and −4 mV. This shows that the filter passband ripple and stopband (notch position) response are affected by this error. For example, the notch depth has decreased from ~70 dB in the ideal case, to ~40 dB when $\Delta v_f = 10$ mV. To examine the effect of clock-feedthrough error on the filter passband in detail, consider Fig. 17*b*. This shows that the filter passband ripple is increased from 0.177 dB in the ideal case to ~2.5 dB when $\Delta v_f = 10$ mV, for example. A number of techniques have been proposed to reduce the effect of clock-feedthrough on SI circuits, for example the S^2I technique [6]. Fig. 18*a* shows the frequency response of the same filter with clock-feedthrough error when its filter is designed using S^2I delay cells. Clearly this shows that the filter performs better when S^2I delay cells are employed. Fig. 18*b* shows the filter passband response in more detail.

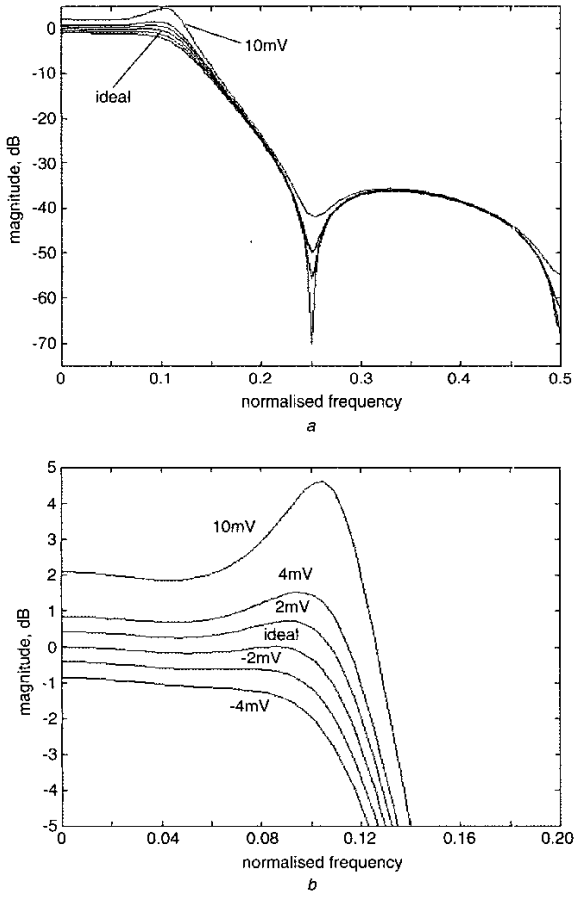

Fig. 17 *Frequency response of 3rd-order Bruton transformation wave low-pass elliptic filter in the presence of clock-feedthrough error using second-generation delay cells, and passband ripple response*
a Frequency response
b Detailed passband response

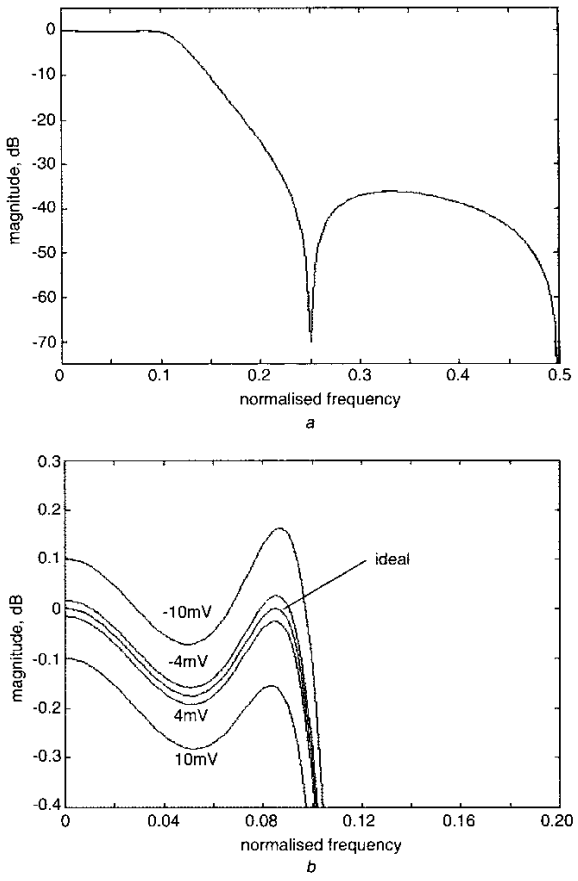

Fig. 18 *Frequency response of 3rd-order Bruton transformation wave low-pass elliptic filter in the presence of clock-feedthrough error using S^2I delay cells*
a Frequency response
b Detailed passband response

Up to this point, only the clock-feedthrough error effect on the filter performance has been considered. Now, the effects of mismatch error combined with clock-feedthrough are considered. Table 2 gives a summary of the filter performance parameters (passband ripple (ε), passband frequency (*fp*), notch frequency (*f*1), and DC gain *H*(0)) in the presence of only mismatch errors (i.e. when $\Delta v_f = 0$ mV), and when the filter has both mismatch and clock-feedthrough errors (i.e. when $\Delta v_f = 2$ mV and 4 mV) for second-generation (SI) and S^2I delay cells. As can been seen from columns 2 and 3, the filter performance parameters are little affected by the mismatch error. For example the passband ripple is 0.1773 dB in the case of SI implementation compared to the ideal passband ripple of 0.177 dB. However, the error in filter performance parameters increases when mismatch and clock-feedthrough are combined, and gets worse as Δv_f increases. For example, the passband ripple is 0.8484 dB when $\Delta v_f = 4$ mV. Table 2 shows, as expected, that S^2I delay cell based filters are less affected than second generation SI based filters by mismatch and clock-feedthrough errors.

Table 2: Summary of the 3rd-order low-pass filter parameters performance in the presense of mismatch, and when mismatch and clock feedthrough errors are combined

Δv_f, mV	0		2		4	
Cell	SI	S^2I	SI	S^2I	SI	S^2I
ε, dB	0.1773	0.1774	0.4564	0.1793	0.8484	0.1858
ε std%	0.39	0.43	0.71	0.45	0.88	0.44
ε error%	0.19	0.25	157.85	1.32	379.3	4.95
Fp	0.0965	0.0965	0.1043	0.0966	0.1094	0.09675
fp std%	0.045	0.0552	0.053	0.05	0.061	0.0472
fp error%	0.4128	0.4128	7.637	0.31	12.9	0.155
*f*1	0.25	0.251	0.251	0.251	0.252	0.251
*f*1 std%	0.065	0.07	0.0478	0.052	0.12	0.078
*f*1 error%	0.24	0.159	0.159	0.159	0.555	0.159
H(0), dB	0.0042	0.0036	0.431	−0.0069	0.8514	0.0158

The second example is a 5th-order high pass elliptic filter (Fig. 19). The normalised high pass filter specifications are: passband ripple $\varepsilon = 0.177$ dB, passband edge $fp = 0.18$; stopband edge $fs = 0.1$; stopband attenuation > 60 dB. The filter adaptor coefficients are: $y_{00} = 0.842$, $y_{01} = 0.5$, $y_{10} = 1.03$, $y_{11} = 0.5$, $y_{12} = 0.47$, $y_{20} = 1.928$, $y_{50} = 1.834$, $y_{30} = 0.752$, $y_{31} = 0.5$, $y_{40} = 0.980$, $y_{41} = 0.5$, $y_{42} = 0.519$, $y_{60} = 0.965$ and $y_{61} = 0.606$. It has been shown that the filter frequency response is affected by mismatch and clock-feedthrough errors as shown in Figs. 20*a*, *b*. The filter frequency response improves when S^2I delay cells are used as shown in Figs. 21*a*, *b*. Table 3 gives a summary of the filter performance parameters (passband ripple (ε), passband frequency (*fp*), notch frequency (*f*1, *f*2), 3 dB frequency ($f(-3\,\text{dB})$), magnitude in passband $|H(j\omega)|_p$ and magnitude in stopband $|H(j\omega)|_s$), in the presence of only mismatch errors and when the filter has both mismatch and clock-feedthrough errors for second-generation (SI) and S^2I delay cells. Again the filter frequency response is less affected by the two sources of errors when S^2I delay cells are used.

The two examples show the effectiveness of the analytical models developed in studying the influence of different switched current implementation techniques on the filter frequency response. This should prove very useful during the design of practical Bruton transformation wave SI filters. To comment on how the non-ideal performance of Bruton transformation wave SI filters compare with that of traditional wave filters, the two filter examples considered in this section were also designed using the traditional wave method [5] and simulated. It has been shown that wave Bruton transformation based filters and traditional wave filters have similar non-ideal frequency responses in the presence of transistor mismatch and clock-feedthrough in delay cells. To be able to compare the results with previous work in [9], the non-ideal frequency response of a 3rd-order low-pass Chebyshev was given. Fig. 22 shows a comparison between the non-ideal frequency response of the filter in [9] with that of an equivalent Bruton transformation wave filter when there is a clock-feedthrough error of $\Delta v_f = 5$ mV. As can be seen, the two filters exhibit similar performance. Previous research has shown that adaptors impose the main speed limitation of SI wave filter realisation based on standard current mirror topologies ([1], chap. 11). For the case of the low-pass filter, following the analysis in [1], it can be shown that the time constant of the most restrictive path in the 3-port parallel adaptor is $(3C_{dx} + 4C_{gs})/g_m$. Similarly, for the high-pass

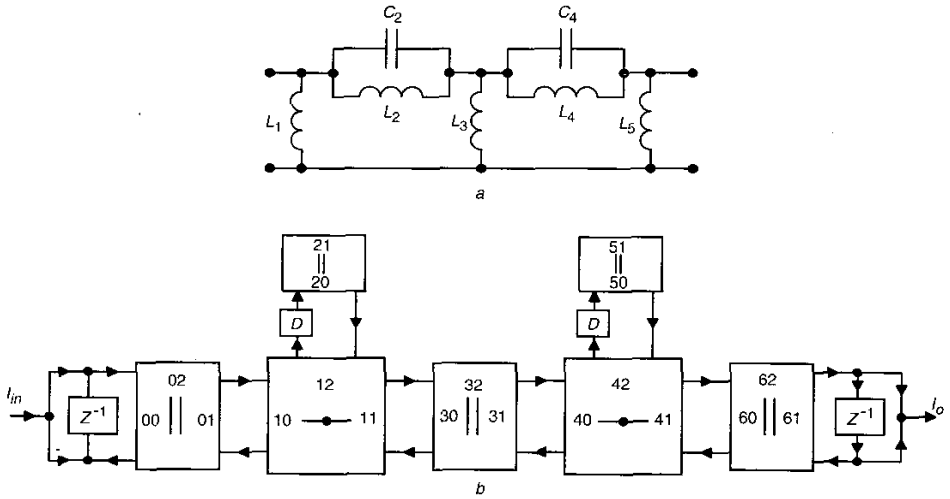

Fig. 19 *5th-order elliptic high-pass LC filter (a) and 5th-order direct Bruton transformation wave SI elliptic filter (b)*

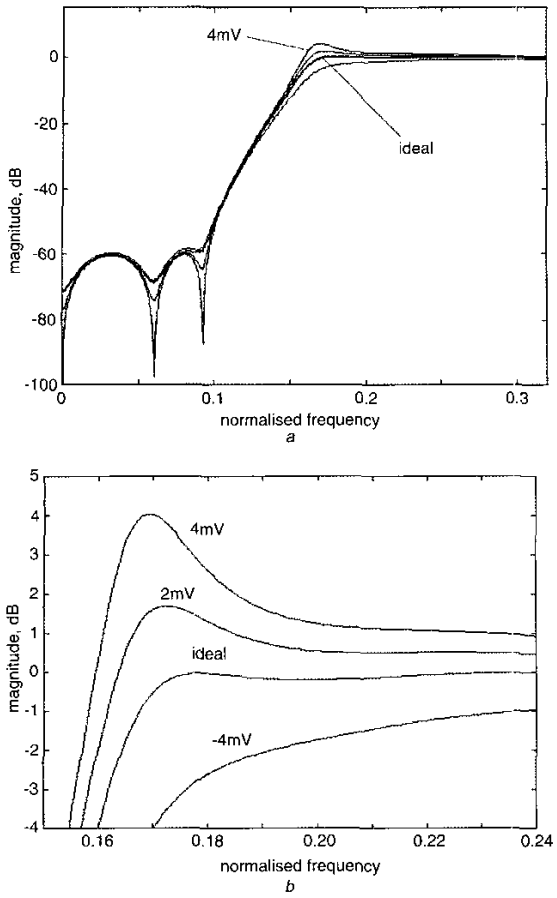

Fig. 20 *Frequency response of 5th-order Bruton transformation wave high-pass elliptic filter in the presence of clock-feedthrough error in second-generation delay cells, and passband ripple response*
a Frequency response
b Detailed passband response

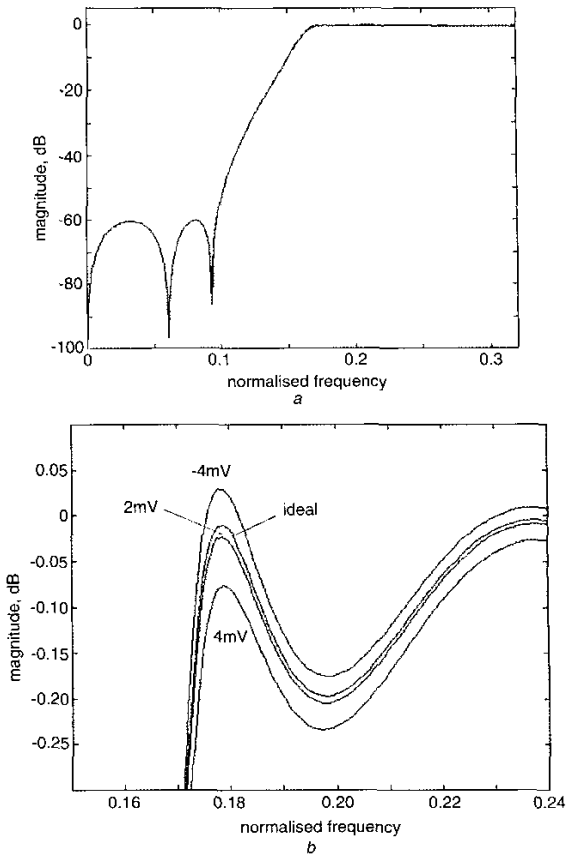

Fig. 21 *Simulated frequency response of 5th-order Bruton transformation wave high-pass elliptic filter in the presence of clock-feedthrough error in S^2I delay cells, and passband ripple response*
a Frequency response
b Detailed passband response

Table 3: Summary of the 5th-order high-pass filter parameters performance in the presense of mismatch, and when mismatch and clock-feedthrough errors are combined

Δv_t, mV	0		2		4	
Cell	SI	S^2I	SI	S^2I	SI	S^2I
ε, dB	0.1803	0.1779	1.1923	0.1856	4.0779	0.207
ε, std%	1.35	1.39	2.71	1.11	5.56	1.61
ε, error%	1.86	0.48	573.63	4.87	2204.3	16.95
Fp	0.1784	0.1786	0.1723	0.1786	0.1689	0.1781
Fp std%	0.0714	0.0612	0.0617	0.0574	0.0478	0.0731
fp error%	0.0896	0.0224	3.51	0.0224	5.41	0.257
f(−3 dB)	0.1619	0.1619	0.1583	0.1619	0.1557	0.1616
f(−3 dB) std%	0.047	0.04877	0.0569	0.0581	0.0481	0.0488
*f*1	0.0607	0.0608	0.0614	0.0607	0.0604	0.0602
*f*1 std%	0.17	0.17	0.14	0.16	0.16	0.19
*f*1 error%	0.33	0.496	1.49	0.33	0.165	0.5
*f*2	0.0932	0.0932	0.0924	0.0929	0.0901	0.0927
*f*2 std%	0.092	0.0962	0.0952	0.11	0.11	0.12
*f*2 error%	0.43	0.43	0.43	0.11	2.9	0.11
$\lvert H(j\omega)\rvert$, dB	−0.0312	−0.0261	0.3937	−0.0377	0.8195	−0.014
$\lvert H(j\omega)\rvert$, dB	−60.79	−61.53	−58.04	−62.887	−54.52	−61.177

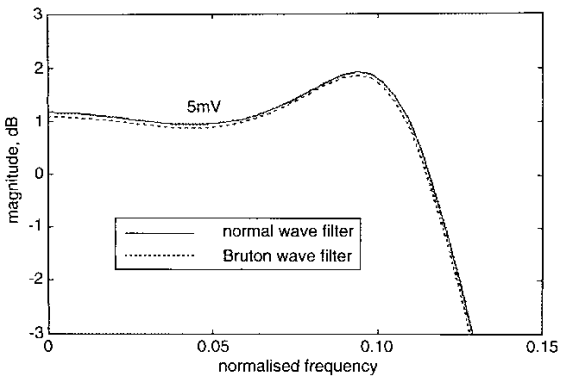

Fig. 22 *Non-ideal frequency response of 3rd-order Chebyshev low-pass filter designed using traditional wave method [5] and Bruton transformation wave method [3]*

filter, the time constant of the most restrictive path in the 3-port series adaptor is $(4C_{ds}+3C_{gs})/g_m$. If $g_m=264\,\mu A/V$, $C_{ds}=0.24\,pF$, and $C_{gs}=0.6\,pF$ (1 μm CMOS process), the maximum sampling frequencies of the low-pass and high-pass filters are 13.47 MHz and 15.2 MHz respectively.

5 Concluding remarks

This paper has analysed and modelled the non-ideal performance of Bruton transformation wave SI filters in the presence of current mirror mismatch and delay cell clock-feedthrough errors. Models of the filter main components incorporating these sources of errors have been derived from analysing the physical realisation of the components' input–output relationships. The developed models have been integrated with MATLAB and used to examine the effect of such errors on the filter's frequency response. It has been shown that transistor mismatch in current mirrors and clock-feedthrough in SI delay cells degrades the frequency response of the filters, and the level of degradation depends on the type of SI design technique. It has been found that filters designed using S^2I delay cells are little affected by these errors and appear to provide a good choice when considering the practical implementation of Bruton transformation wave SI filters, which is the subject of current research by the authors.

6 Acknowledgments

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