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High current gain silicon-based spin transistor

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Abstract
A silicon-based spin transistor of novel operating principle has been demonstrated in which the current gain at room temperature is 1.4 (n-type) and 0.97 (p-type). This high current gain was obtained from a hybrid metal/semiconductor analogue to the bipolar junction transistor which functions by tunnel-injecting carriers from a ferromagnetic emitter into a diffusion driven silicon base and then tunnel-collecting them via a ferromagnetic collector. The switching of the magnetic state of the collector ferromagnet controls the collector efficiency and the current gain. Furthermore, the magnetocurrent, which is determined to be 98% (140%) for p-type (n-type) in −110 Oe, is attributable to the spin-polarized base diffusion current.

1. Introduction

Since the discovery of giant magnetoresistance (GMR) [1] in 1988, interest has been steadily growing in magnetically sensitive devices. This has resulted in several attempts to fabricate spin transistors that exploit the spin dependent scattering of charge carriers to yield a device with high current gain and high magnetic sensitivity. The first such attempt was Johnson's all-metal three-terminal device [2], which added a third terminal to the middle paramagnetic layer of a GMR multilayer. The electrical characteristics of this purely Ohmic device are magnetically tunable, but, due to its all-metal construction, its operation yields only small voltage output changes and no power gain.

Subsequent versions of the spin transistor attempted to integrate semiconductors with spin electronics in order to generate novel functionality. There are two major variants. In the first, the metallic components retain their spin selectivity while the semiconductor is used only to control the distribution of applied potentials across the device. Most versions [3–5] fall into this category, including the Monsma hot electron spin valve transistor [3]. This device sandwiched a GMR multilayer between two pieces of silicon, forming an emitter Schottky barrier, which injected electrons into the metallic base, and a collector Schottky barrier, whose height determined which carriers were collected. The magnetic configuration of the metallic GMR multilayer controlled the energy of the electrons reaching the collector Schottky barrier. Although the electrical characteristics of this transistor were magnetically sensitive, all the manipulation of the electrons' spin occurred in the GMR multilayer. Furthermore, the thickness of the metal-base layer, which must accommodate at least two (preferably more) ferromagnetic layers plus spacer layers, defined not only the degree of magnetic sensitivity, but also the magnitude of the current gain; the more layers present, the greater the magnetic sensitivity, but the lower the current gain. The best value [4] for the ratio of collector current to emitter current in the hot electron spin valve transistor is 1×10^{-3}.

The second variant, the experimental realization of a spin-FET based on the proposal by Datta and Das [6], was being developed concurrently. This transistor is a modification of a field effect transistor (FET) in which an applied electric field changes the width of the depletion region and hence the output current magnitude. In a spin-FET, spin-polarized electrons are injected from a magnetic source into a semiconductor channel. During passage through the channel, these electrons undergo Rashba precession, the frequency of which depends

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upon the gate voltage. Finally, the electrons are analysed by spin-selective scattering in the magnetic drain. Therefore, the electrical characteristics[6] are dependent upon not only the magnetic orientation of the source and drain, but also on the gate voltage. Gardelis and co-workers [7] have made progress towards realizing this device, but the gate functionality remains to be convincingly demonstrated.

The spin transistor [8, 9] described in this paper is markedly different from all of these in that it exploits spin transport in the silicon as well as using minority carriers in order to achieve high current gain and magnetic sensitivity. It functions by using a ferromagnetic emitter to inject spin-polarized electrons via a tunnel barrier into a silicon base. These spin-polarized minority carriers traverse the base diffusively and are harvested by the ferromagnetic collector via another tunnel barrier. The spin selectivity derives from the back-biased collector presenting a different density of final spin states to the spin-polarized minority carriers in the base. Furthermore, as in the bipolar junction transistor, the carrier scattering and recombination rates in the base may be very low, so that the current gain (given by the differential ratio of the collector current to the base current: $\beta = \Delta I_C/\Delta I_B$) is potentially very large compared to the Johnson and Monsma metal-base devices discussed above. Unlike all other three-terminal spin devices, this spin transistor design exhibits a maximum current gain greater than unity (1.4) and an average current gain (over all applied base currents) slightly less than unity (0.9), in addition to being magnetically sensitive (magnetocurrent changes by up to 140% in -110 Oe). The expected performance is analysed in the next section.

2. Theoretical analysis

Recent work [10] has analysed the spin injection efficiencies of different spin electronic devices. For ease in analysing the spin transistor fabricated and measured in this paper, we make several assumptions. The modelled transistor (see figure 1(*a*)) has a direct-injected base (of width b, height h, and length c, where c is also the length of the collector) with a half-metallic ferromagnetic collector separated from the base by a tunnel barrier. We assume that the base width b is less than both the recombination length and the minority carrier spin diffusion length. In addition, the emitter injector has spin channels with a common diffusion constant D, but different densities of states $\rho_\uparrow$ and $\rho_\downarrow$. The emitter spin diffusion length l_F is large compared with the emitter-base depletion layer thickness so that variations in the electrochemical potentials $\mu_\uparrow$ and $\mu_\downarrow$ across the depletion layer can be ignored. Since the spin up current is smaller than the spin down current by a factor of b/c, it may be neglected. Therefore, the figure of merit for this device, which is the collected current[7] ratio for oppositely

[6] It may be noted that the characteristics of the spin-FET differ from those of the device we describe in that its g_m may be a periodic function of gate voltage and may change sign on application of a magnetic field.

[7] Maximum current gain is achieved with a base significantly smaller than the carrier diffusion length, by minimizing recombination in the base, and with a large enough voltage drop across the collector tunnel barrier that the carriers can tunnel into the collector easily. However, the silicon base width must be less than the spin diffusion length in silicon in order to have any magnetic sensitivity.

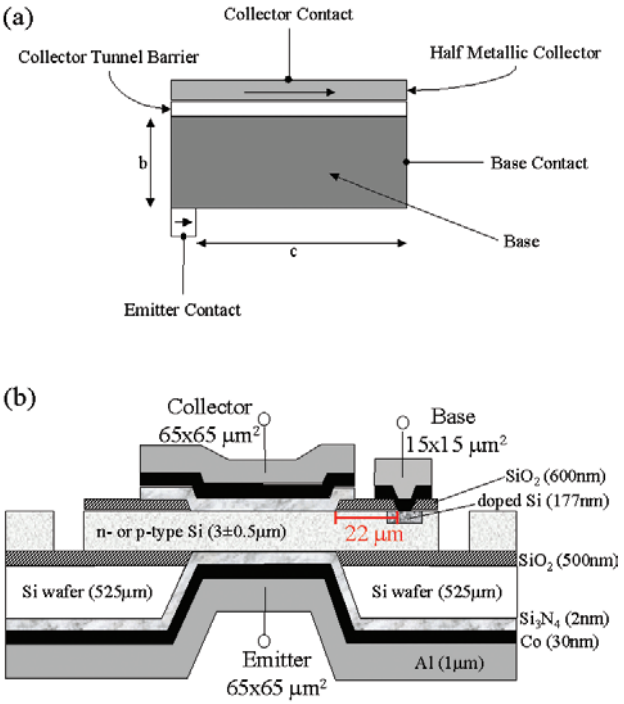

Figure 1. (*a*) Schematic of the modelled device where the emitter-base injector is a forward biased n–p junction. (*b*) Schematic of the fabricated spin transistor with silicon base.

magnetized collector configurations, may be readily shown to be [10]:

$$\frac{J_{T\downarrow}}{J_{T\uparrow}} = \frac{2b(\rho_\uparrow + \rho_\downarrow)kT + (D_S/D_F)l_F n_0 e^{qV/kT}(\rho_\downarrow/\rho_\uparrow)}{2b(\rho_\uparrow + \rho_\downarrow)kT + (D_S/D_F)l_F n_0 e^{qV/kT}(\rho_\uparrow/\rho_\downarrow)} \qquad (1)$$

where D_S and D_F are the base and emitter diffusion coefficients, respectively; n_0 is the equilibrium minority carrier density in the base; and V is the emitter-base voltage. Under high voltage conditions ($qV \gg kT$), this reduces to $(\rho_\downarrow/\rho_\uparrow)^2$ for a direct-injected device. For a tunnel-injected device, the corresponding ratio is $(\rho_\downarrow/\rho_\uparrow)$.

3. Design and fabrication

The devices were fabricated using standard photolithography on n- and p-type silicon-on-insulator (SOI) wafers with an active silicon layer resistivity of 17–33 Ω cm. All of the devices (shown in figure 1(*b*)) were fabricated according to the following process:

(a) An insulating layer of 600 nm of SiO_2 was grown on the front (active silicon) side of the SOI wafer.
(b) The SiO_2 was removed in selected areas to create the base contacts.
(c) The silicon in the base contacts was ion implanted with As^+ or BF_2^+ for active silicon doped n- or p-type, respectively. This yielded a surface concentration of $\sim 1 \times 10^{20}$ atoms cm^{-3}, forming a good ohmic contact.
(d) The SiO_2 was removed in selected areas to create the collector contacts.
(e) On the back (handle silicon) of the wafers, a layer of Si_3N_4 was deposited with low-pressure chemical vapour deposition.

(f) The Si_3N_4 was removed in selected areas and a pit was wet-etched down to the buried oxide layer.
(g) The remaining back-surface Si_3N_4 layer and the buried oxide layer (in the selected region) were removed. This exposed the active silicon layer where the emitter will be formed.
(h) Tunnelling barriers[8] [11] of Si_3N_4 were formed on both the front and back of the wafers by low-pressure epitaxy using a self-limiting nitride process. However, on the front of the wafers, the Si_3N_4 was removed by reactive ion etching (RIE) in order to make the base contacts ohmic. The emitter and collector contacts are metal-insulator-semiconductor junctions and the base contact is a metal-semiconductor (ohmic) junction.
(i) Thirty nanometres of Co and 1 μm of Al (for the electrical contacts) were deposited on both sides of the wafers.
(j) The front side was then etched (to remove the Al) and ion milled (to remove the Co) in order to isolate the base and collector contacts. The emitter remains as a common contact for all the transistors.
(k) An isolation trench was milled by RIE to isolate each transistor from its neighbours.

The transistors were fabricated on two 4-inch SOI wafers—one with the active silicon layer doped p-type and the other with the active silicon layer doped n-type. From a single chip of each wafer containing 18 devices, six were chosen (based upon the quality of their two-terminal I–V characteristics), mounted into a chip package with silver epoxy, and wire bonded for further electrical and magnetic characterization.

4. Results and discussion

4.1. Electrical characteristics in zero applied magnetic field

4.1.1. Two-terminal I–V characteristics. I–V characteristics of the emitter/collector and the emitter/base configurations were measured at room temperature in the circuit configurations shown in figures 2(*a*) and (*b*). As seen in figure 3, the results differ slightly between the two configurations, although the overall form is the same in both, indicating that tunnelling dominates over the ohmic base conduction. For these Si_3N_4 barriers, the functional form of the I–V curves close to zero voltage ($<\sim$0.5 V) is given by

$$I = Ae^{BV^{1/4}} + CV + D \qquad (2)$$

which implies that the dominant conduction mechanism is Mott's variable range hopping [12, 13]. This is in general agreement with previous work [14–17] that Si_3N_4 tunnel barriers conduct primarily by electron hopping near the Fermi level due to defects or dangling bonds. For voltages greater than $\sim$0.5 V, the functional form of the curves changes to:

$$I = AV^2e^{(B/V)} + CV + D \qquad (3)$$

(The experimental transition points between regimes were determined by numerically differentiating the I–V curves

[8] Alternative tunnel barriers of SiO_2 instead of Si_3N_4 were also used. However, the two-terminal I–V characteristics of these barriers were not stable, and exhibited equilibration times in excess of several hours [14]. The Si_3N_4 measurements stabilized in less than a second.

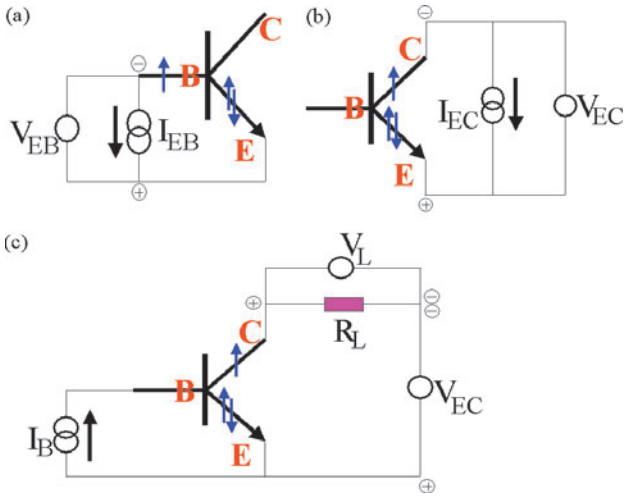

Figure 2. DC measurement circuits: (*a*) the emitter-base configuration; (*b*) the emitter-collector configuration; and (*c*) common-emitter configuration where $R_L = 10\,k\Omega$.

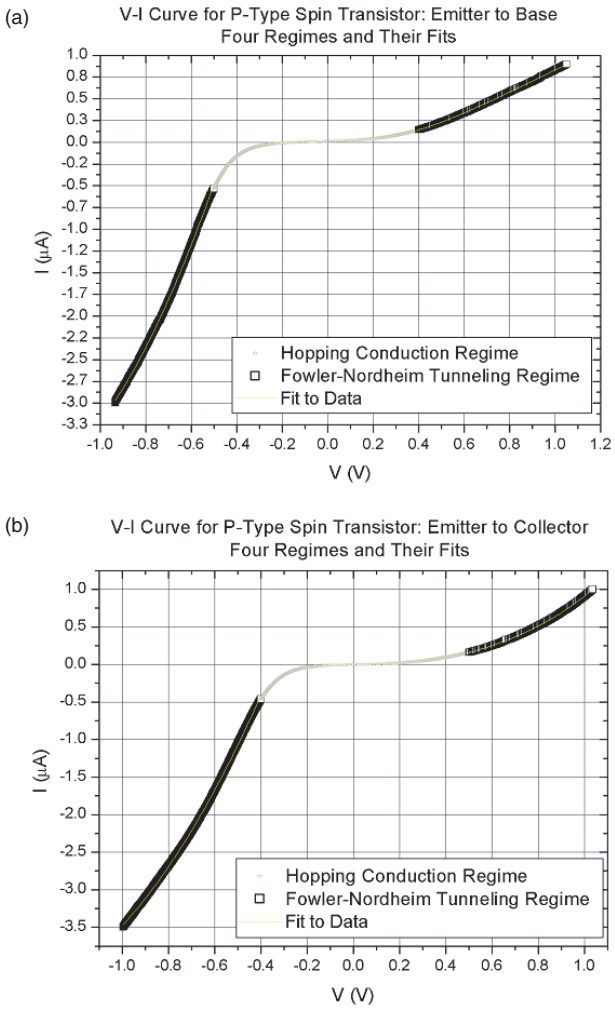

Figure 3. The two-terminal characteristics of the p-type transistor: (*a*) emitter to base and (*b*) emitter to collector. In both cases, the dots indicate measured data points and the solid blue lines are fits to equations (2) or (3), as indicated.

and are indicated in table 1.) This change in dominant conduction method was also observed [14] in double structures of Al/Ta_2O_5/Si_3N_4/n-Si. Moreover, the factor of four between the onsets ($\sim$0.5 V in our spin transistors compared to 2 V in the double structures [14]) correlates very satisfactorily with the thickness difference (2 nm in our barriers as opposed to 8 nm in the double structures). In addition, it is well known that hopping conduction destroys the spin-polarization of carriers [18]. Therefore, no magnetic sensitivity should be observed in the hopping conduction regime. This is verified in section 4.2.1 and lends additional support to our interpretation of the conduction mechanisms.

4.1.2. Three-terminal I–V characteristics. When connected in common emitter configuration (shown in figure 2(*c*)), the transistor exhibits similar characteristics (see figure 4) to that of a conventional bipolar transistor. However, unlike an ideal conventional bipolar junction transistor, the base is not field-free so the position dependence of the base minority carrier density is dependent upon the local voltage. This is indicated in the spreading resistance data, which indicates a non-uniform doping profile as well as a weak p–n junction in the silicon base. The collector current as a function of base current and collector–emitter voltage may be as high as 5.7 μA ($-3.2\,\mu$A) for p-type (n-type). This occurs at $V_{CE} = 1$ V (-1 V) and $I_B = 1.0\,\mu$A, which is not only a higher output current than in the previously discussed devices, but also occurs at a lower voltage. Furthermore, at these collector currents, the current gain (β) is 0.97 (1.4) for p-type (n-type). The observed differences in the transistor responses between n- and p-type are most likely due to the doping of the silicon base.

Table 1. Voltage ranges for hopping conduction as determined by numerical differentiation.

	Emitter to base (V)	Emitter to collector (V)
p-type transistor	(-0.5, 0.4)	(-0.4, 0.5)
n-type transistor	(-0.6, N/A)	(0, 0.5)

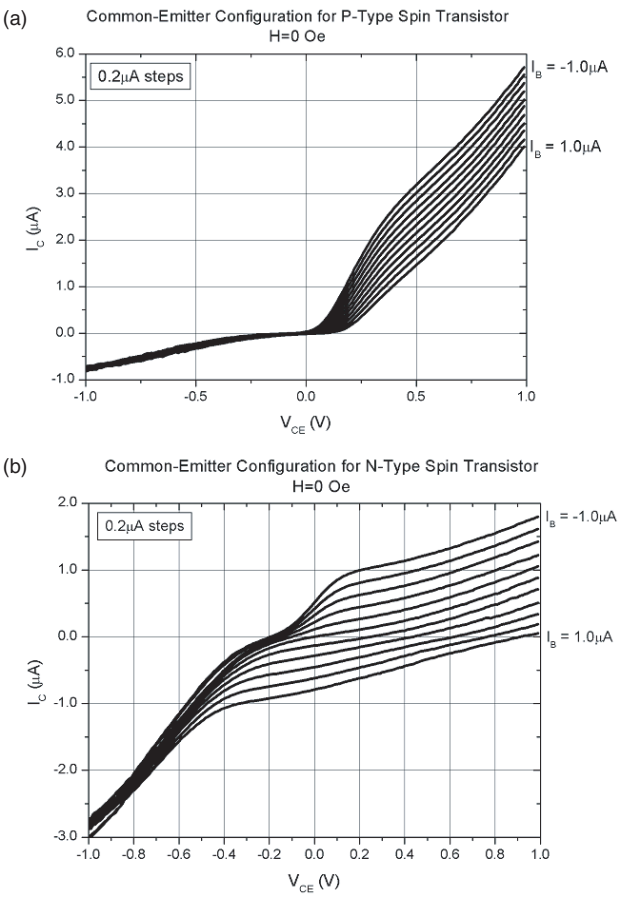

Figure 4. *I–V* characteristics of spin transistors in common-emitter configuration and zero applied field: (*a*) p-type and (*b*) n-type.

4.2. Electrical characteristics in an applied magnetic field

The magnetic response of the Co layers in the spin transistors was measured using a vibrating sample magnetometer (VSM). The silicon background was subtracted from the measurement in order to yield the inset to figure 7. These hysteresis loops indicate that differential switching is occurring in the devices. By removing the collector and base contacts on the top surface, further analysis indicates that the emitter (bottom) contact switches at the lower field of 40 Oe.

Application of a magnetic field is expected to affect the *I–V* characteristics in two ways. First, the magnetization of the emitter and collector Co contacts can be differentially manipulated, thereby introducing a spin-selective tunnelling magnetoresistance (TMR) effect that modulates the collector current. Second, the applied magnetic field decreases the mean free path in the silicon base via Lorentz magnetoresistance (LMR), also affecting the collector current.

4.2.1. Two-terminal magnetic I–V characteristics. The two-terminal measurements of section 4.1.1 were repeated with a magnetic field applied in the plane of the transistor (perpendicular to the current). There are three important results (shown in figure 5) from these measurements. First, the *I–V* characteristics are a function of applied magnetic field. Second, no magnetic sensitivity is observed for voltages below the onset of Fowler–Nordheim tunnelling (as indicated by the red arrows). This further substantiates the claim that hopping conduction is occurring at low voltages. Third, most of the activity (shown in the inset of figure 5 as deviations from a straight line) in the electrical characteristics occur around the magnetic transition region, between -90 and -115 Oe. These deviations (of magnitude $\sim$0.01 V) are outside of the noise level of the measurement, which is $\pm$0.005 V. Furthermore, the fields at which the deviations occur stay consistent from measurement to measurement, although the exact collector-emitter voltage location and amplitude varies. This suggests that the deviations may be due to magnetic domain formation and/or motion in the Co layers changing the magnetic state seen in different regions of the tunnel barrier, since neither the deviations nor the magnetic domain pattern would be exactly reproducible.

4.2.2. Three-terminal magnetic I–V characteristics. The transistor was again operated in common-emitter mode with the magnetic field applied in the plane of the transistor

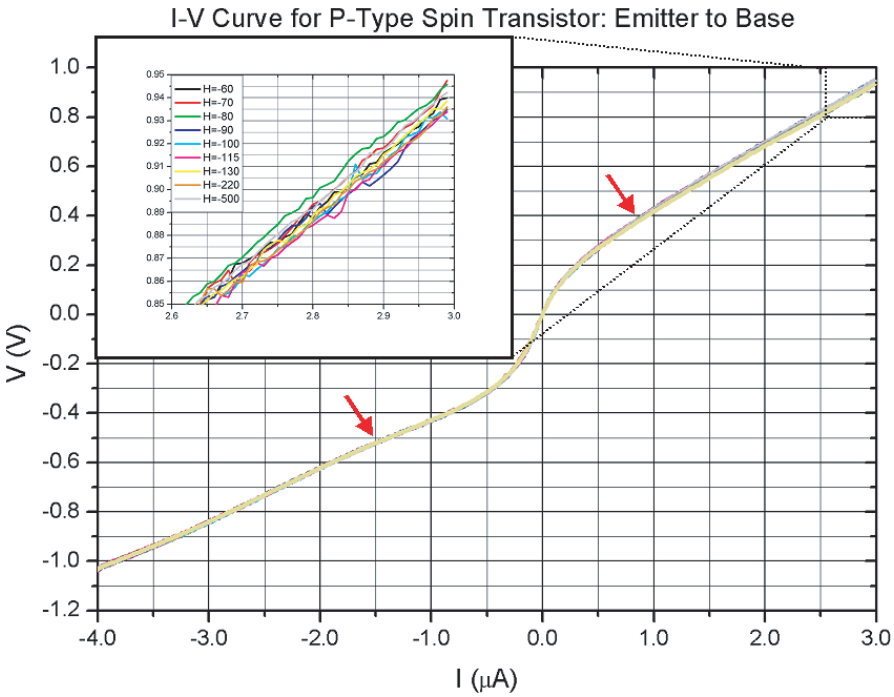

Figure 5. The two-terminal (emitter to base) characteristics of the p-type transistor as a function of applied magnetic field. The red arrows indicate the transition voltages.

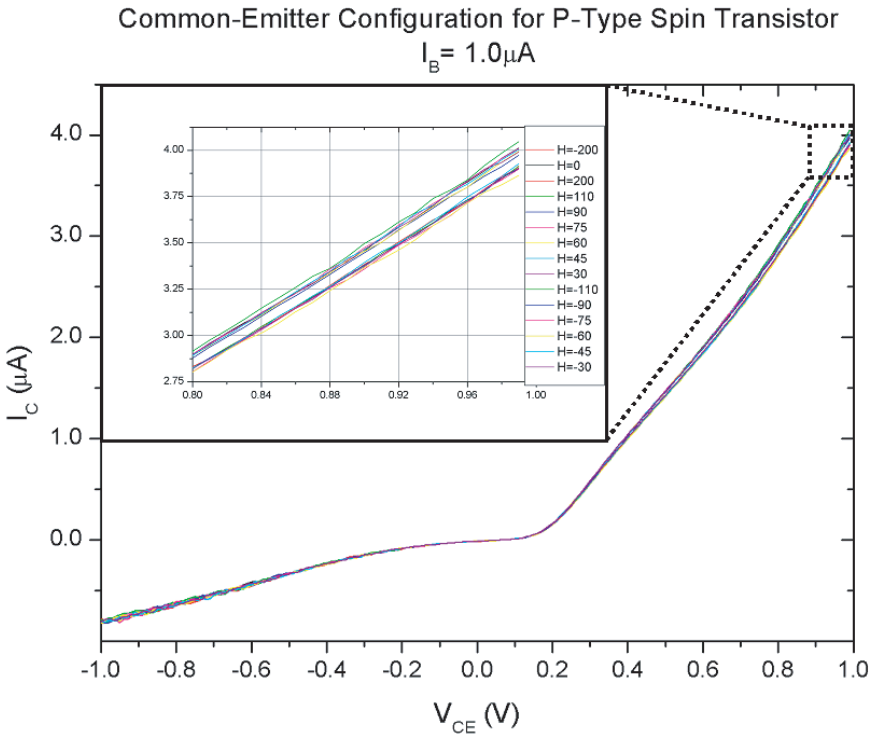

Figure 6. Three-terminal I–V characteristics as a function of applied magnetic field of the p-type spin transistor in common-emitter configuration with $I_B = 1\ \mu$A.

(perpendicular to the current). The results (figure 6) show a variation[9] in the collector current as a function of magnetic field indicating that the transistor behaves as a magnetically tunable device with a field dependent gain. The maximum variation of the average (taken over all applied base currents)

[9] It should be noted that while the large deviations from a straight line occur in figure 5, they do not appear in figure 6. This is a direct result of the measurement in figure 5 being two-terminal and in figure 6 being three-terminal. The addition of the base current in the three-terminal configuration has a greater influence on the collected current due to its impact on the collector tunnel barrier height than the domain wall motion/formation and furthermore, stabilizes the circuit by not letting the third terminal float.

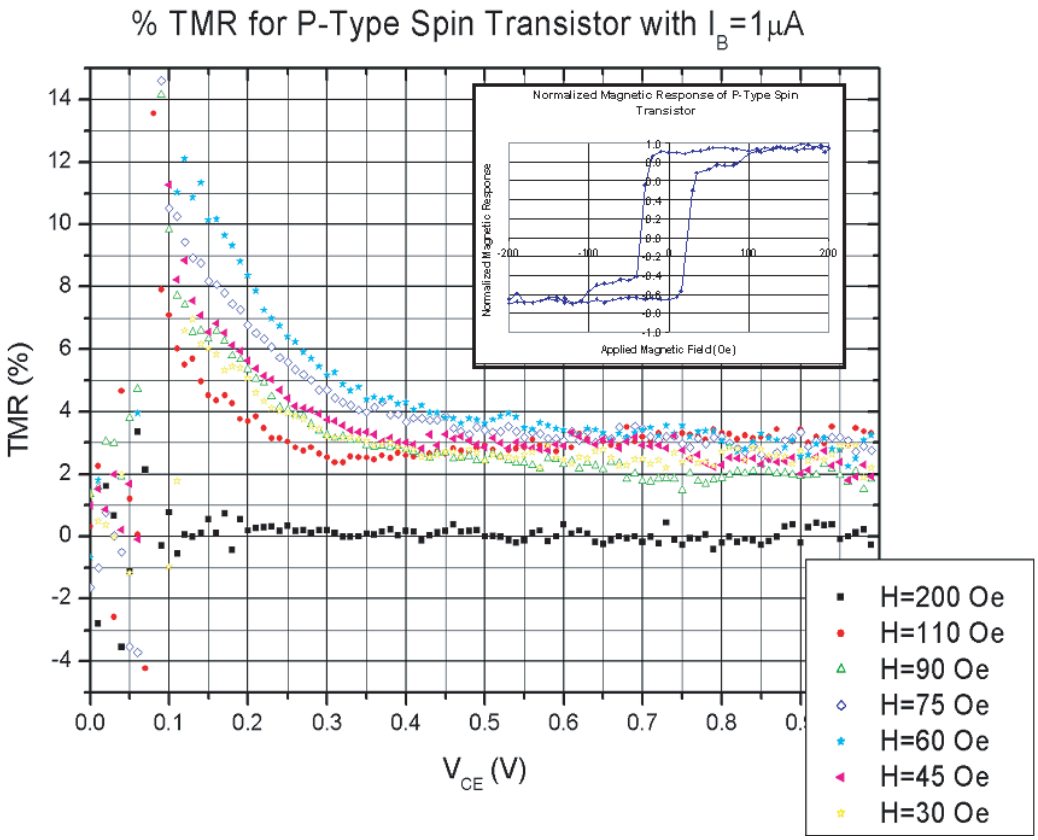

Figure 7. TMR effect on the collector current with the Lorentz contribution removed for the p-type spin transistor. Inset: normalized magnetization curve.

current gain was $2.2 \pm 0.3\%$ which occurred at -110 Oe. This percentage change was independent of device type.

Furthermore, LMR and TMR are both present in the device. The LMR is of the same order of magnitude as the TMR, so it is effectively disguised in a simple MR measurement. However, these two phenomena may be deconvoluted by magnetically saturating in one direction and then subtracting the positive and negative field swept data for the TMR

$$\mathrm{TMR} = \left(\frac{I_{\mathrm{H_{Neg}}} - I_{\mathrm{H_{Pos}}}}{I_{\mathrm{H=0}}} \right) \times 100$$

where $I_{\mathrm{H=0}}$ is the collector current at zero field. This yields (see figure 7) a percentage change of $3.3 \pm 1\%$ ($13 \pm 1\%$) in the collector current[10] at $I_{\mathrm{B}} = 1.0\,\mu$A between the parallel and anti-parallel configurations for the p-type (n-type) spin transistor. (The effect is zero for the ± 200 Oe data since the magnetic elements are all in parallel, as seen in the magnetization curve shown in the inset.) Furthermore, the difference between the positive and negative V_{CE} regimes is the result of the collector current being 'switched off', resulting in little to no TMR signal, and the noise around $V_{\mathrm{CE}} = 0$ V is the result of division by $I_{\mathrm{C}} \approx 0$ A.

In addition, the currents calculated by removing the LMR contribution represent the collected current in parallel or anti-parallel configuration, depending upon the applied field. Therefore, the magnetocurrent defined as

$$\mathrm{MC} = \left(\frac{I_{\mathrm{P}} - I_{\mathrm{AP}}}{I_{\mathrm{AP}}} \right) \times 100$$

can be calculated to be $98 \pm 7\%$ ($140 \pm 13\%$) for p-type (n-type).

Finally, the figure of merit is calculated using the theory developed in section 2. For Co, $\rho_{\uparrow} = 0.1740$ and $\rho_{\downarrow} = 0.7349$ states/eV, yielding an ideal figure of merit of 4.2 for tunnel injection and 17.8 for direct injection (calculated from equation (3) assuming high bias). The experimental figure of merit is 1.05 (1.1) for p-type (n-type). At this point, it should be noted that one of the assumptions in deriving equation (3) is that the collector is a half-metallic ferromagnet. This is clearly not the case in the actual device. A normal collector ferromagnet would be expected to permit some spins aligned antiparallel to its magnetization direction to tunnel into the collector. This would essentially dilute the purity of the tunnelling spins, thereby decreasing the figure of merit. However, this is not expected to be sufficient to explain the full factor of four differences between the theoretical and experimental figure of merit. Other possible reasons for this are presented in the next section.

5. Conclusions

Proof of concept has been established by a high current gain (greater than one), magnetically sensitive, silicon-base spin

[10] The TMR signal has artificially large values around 0.1–0.3 V due to the onset of the spread in the collected current (due to IB), not due to any magnetic dependence in the tunneling. Fowler–Nordheim tunneling does not dominate conduction until 0.45 V (although it occurs at lower voltages), so it settles into the final value at this point.

transistor. In zero magnetic field and at room temperature, the collector I–V characteristics are similar to those of conventional transistors and offer a current gain of 0.97 (1.4) for p-type (n-type). The current gain of the device can be magnetically tuned (up to a $2.2 \pm 0.3\%$ change in -110 Oe in the average current gain; $3.3 \pm 1\%$ ($13 \pm 1\%$) for p-type (n-type) for the TMR contribution alone; and $98 \pm 7\%$ ($140 \pm 13\%$) for p-type (n-type) for the calculated magnetocurrent). Moreover, the base current and collector–emitter voltage control this field-dependent gain. However, several improvements can be made to future generations for better device characteristics, including: (1) improved tunnel barriers (2) improved differential magnetic switching (3) optimized electrode geometry as determined from recent modelling [10] and (4) uniform doping profile.

Acknowledgments

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