Application of Polycrystalline SiGe for Gain Control in SiGe Heterojunction Bipolar Transistors

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Abstract

This paper reports a method of controlling the gain of a bipolar transistor by incorporating Ge in the polysilicon emitter. Measured results show that varying the Ge content in the polySiGe from 0 to 33% gives a change in base current of approximately four. The competing influences of the Ge and the interfacial layer at the polySiGe/Si interface are investigated theoretically using an effective surface recombination velocity for the polySiGe emitter. Good agreement between theory and measured results is obtained. When incorporated into a SiGe HBT, the polySiGe emitter will allow the best trade-off between gain and BV_{CEO} to be achieved for a given Ge and B profile in the base.

1. Introduction

To achieve high values of f_T and f_{max} in SiGe HBT's, it is necessary to minimise delay times in the base and collector of the transistor [1-3]. The base delay is minimised by using a narrow basewidth and large Ge gradient across the base to create a built-in electric field [1]. Such aggressive Ge profiles can give very high values of common emitter current gain ß [3]. The collector delay is minimised by increasing the collector doping to decrease the transit time and to suppress the Kirk effect. Unfortunately high collector doping concentrations have the disadvantage of degrading the common emitter breakdown voltage BV_{CEO} of the transistor [4].

The trade-off between BV_{CEO} and β can be understood from the following well known equation:

$$BV_{CEO} = \frac{BV_{CBO}}{\sqrt[n]{\beta}} \quad (1)$$

This equation shows that if the gain of the transistor is too high, the common emitter breakdown voltage is degraded. To address this problem, a method is needed of reducing the gain without modifing the base Ge and B profiles.

In SOI CMOS technology, single-crystal SiGe has been used in the sources of MOS tranistors to supress parasitic bipolar gain[5].

In this paper, Ge is incorporated in polycrystalline silicon to create a novel polySiGe emitter. This approach is compatible with existing BiCMOS technologies in which a polysilicon emitter is used to make contact to the very shallow emitter/base junction. When applied to a SiGe HBT, this method will allow the gain to be controlled independently of the Ge and B profiles in the base.

An issue that needs to be addresses in polySiGe emitters is the competing influence of the Ge, which gives increased base current, and the interfacial layer, which gives reduced base current. A theory is developed which quantifies these two competing machanisms and a comparison made with measured devices.

2. Transistor Fabrication

Silicon bipolar transistors were fabricated with polySiGe emitters with Ge contents in the range 0 to 33%. The in-situ phosphorus doped poly SiGe layer was deposited in a Thermo VG Semicon CV200 LPCVD system at a temperature of 540°C after an ex-situ HF etch. The polySiGe emitter was completed by annealing for 30s at either 900 or 800°C. SIMS measurements were made to characterise the germanium, phosphorus and oxygen profiles in the polySiGe emitter, and Gummel plots were measured to characterise the electrical properties of the resulting bipolar transistors.

3. Results

Figure 1 shows a typical SIMS profile for a polySiGe layer with 11% Ge after an anneal of 30s at 800°C. It can be seen that the Ge and phosphorus profiles are reasonably uniform across the polySiGe layer, and there

is very little penetration of the phosphorus into the single-crystal silicon. The oxygen profile shows a dose of $6.4\times10^{14}cm^{-2}$ oxygen at the polySiGe/Si interface. Assuming a uniform silicon dioxide layer, this is equivalent to an interfacial oxide thickness of 0.21nm.

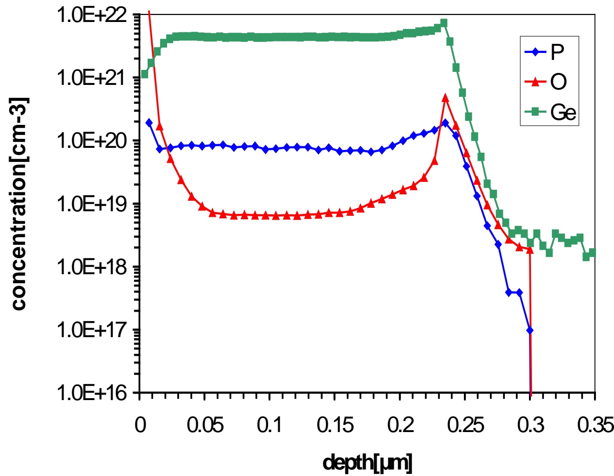

Figure 1: Typical SIMS profile for a polySi$_{0.89}$Ge$_{0.11}$ emitter given an anneal of 30s at 800°C.

Figure 2 compares Gummel plots for transistors with polySi and polySiGe emitters given an anneal of 30s at 900°C. The collector characteristics are ideal with ideality factors of 1.07 and the base characteristics near-ideal with minimum ideality factors of 1.20, 1.14 and 1.13 at V_{BE}=0.6V for 0, 10 and 19% Ge respectively. The base current increases with Ge content, rising by a factor of 2.9 on going from 0 to 10% and by a factor of 4.0 on going from 0 to 19%.

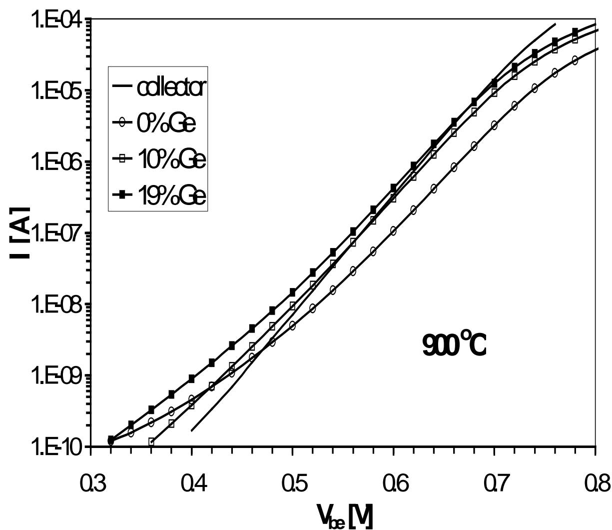

Figure 2: Gummel plots of transistors with polySi and polySiGe emitters annealed for 30s at 900°C.

Figure 3 shows similar Gummel plots for transistors with polySi and polySiGe emitters annealed for 30s at 800°C. The base characteristics of these transistors are less ideal than those in figure 2, with minimum ideality factors of 1.3, 1.3 and 1.2 at V_{BE}=0.55V for 0, 11 and 33% Ge respectively. This is due to the very light anneal used in the transistor fabrication and the consequent small degree of phosphorus penetration into the single-crystal silicon, as shown in figure 1. Nevertheless, these Gummel plots show a similar trend to those in figure 2, namely an increase in base current with increasing Ge content. This increase is a factor of 3.3 on going from 0 to 11% Ge and 4.0 on going from 0 to 33%.

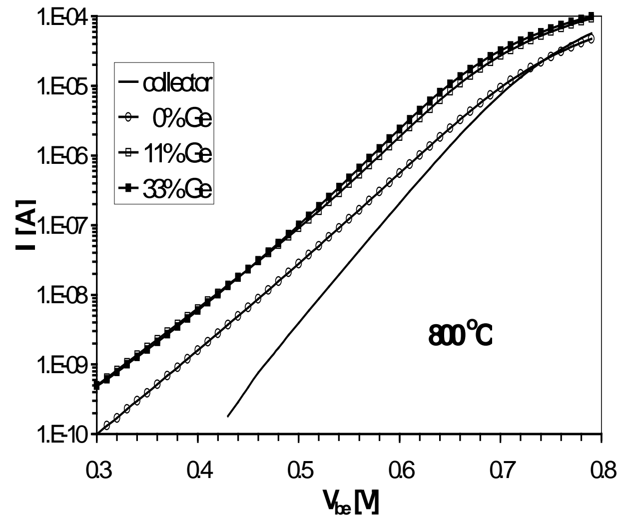

Figure 3: Gummel plots of transistors with polySi and polySiGe emitters annealed for 30s at 800°C.

4. Theory

In order to explain the above dependence of base current on Ge content in the polySiGe emitter, a theory has been developed for polySiGe emitters. The approach used defines an effective surface recombination velocity for the polySiGe emitter analogous to that used by Yu et al [6] for polySi emitters.

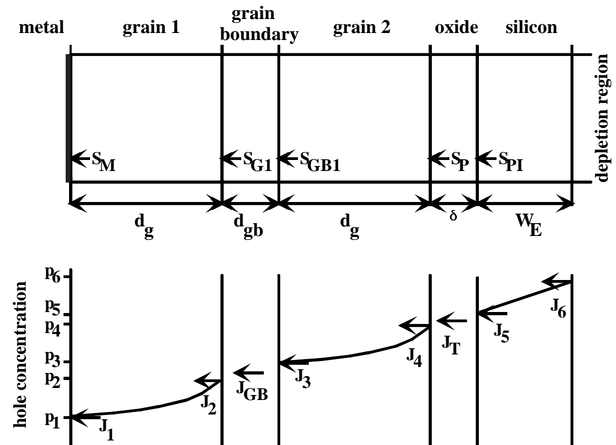

Figure 5: Schematic illustration showing the definition of effective surface recombination velocities.

An effective surface recombination velocity is defined at each interface in the polySiGe emitter, as illustrated in figure 5. The current at each interface is then written in terms of these recombination velocities. For example, the current density J_1 adjacent to the metal contact is given by:

$$J_1 = qS_M p_{1SiGe} \quad (2)$$

where S_M is the surface recombination velocity at the metal contact and p_{1SiGe} is the hole concentration in the SiGe layer adjacent to the metal contact.

Following the work of Yu et al [6], an equation for the current density J_4 at the left of the interfacial oxide layer can be defined:

$$J_4 = qS_P p_{4SiGe} \quad (3)$$

where S_P is an effective surface recombination velocity given by:

$$S_P = a_g - \frac{b_g^2}{a_g + S_{GB1}} \quad (4)$$

The parameters a_g and b_g depend on the physical properties of the polySiGe grains and are given by:

$$a_g = \frac{D_{pSiGe}}{L_{pSiGe}} \coth\left(\frac{d_g}{L_{pSiGe}}\right) \quad (5)$$

and

$$b_g = \frac{D_{pSiGe}}{L_{pSiGe}} \operatorname{csch}\left(\frac{d_g}{L_{pSiGe}}\right) \quad (6)$$

where d_g is the grain width, and L_{pSiGe} and D_{pSiGe} are the hole diffusion length and hole diffusivity in the polySiGe grain. The recombination velocity after the grain boundary shown in figure 5 is given by:

$$S_{GB1} = a_{gb} - \frac{b_{gb}^2}{a_{gb} + S_{G1}} \quad (7)$$

$$a_{gb} = \frac{D_{gbSiGe}}{d_{gb}} + S_{gbSiGe} \quad (8)$$

$$b_{gb} = \frac{D_{gbSiGe}}{d_{gb}} \quad (9)$$

where d_{gb} is the grain boundary width, and D_{gbSiGe} is the hole diffusivity in the polySiGe grain boundary and S_{gbSiGe} the recombination velocity at the grain boundary interface. S_{G1} is then given by:

$$S_{G1} = a_g - \frac{b_g^2}{a_g + S_M} \quad (10)$$

Transport across the interfacial oxide layer is assumed to be by tunnelling, and the band diagram is illustrated in figure 6.

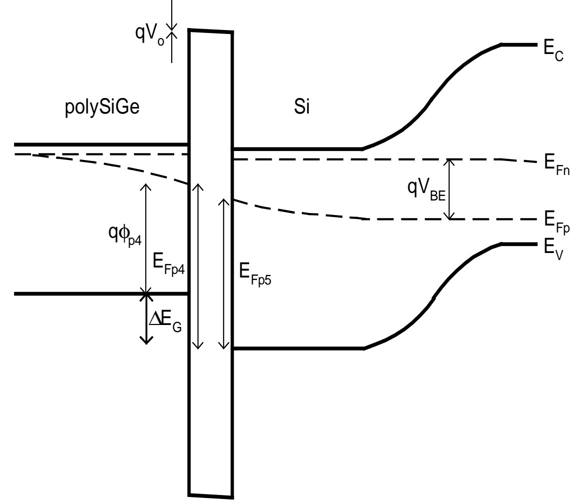

Figure 6: Band diagram of a polySiGe emitter

Using this band diagram, and noting that the energy E_{Fp4} contains the bandgap difference between Si and SiGe ΔE_G, the following equation for the effective surface recombination velocity S_{PI} of the polySiGe emitter can be derived:

$$S_{PI} = S_I + \left(\frac{T_I(S_P + S_I)}{\frac{T_I}{F} + S_P + S_I}\right) \quad (11)$$

where the parameter F represents the effects of the Ge:

$$F = \frac{N_{VSiGe}}{N_{VSi}} \exp\left(\frac{\Delta E_G}{kT}\right) \quad (12)$$

In these equations T_I models tunnelling through the interfacial layer and S_I recombination at the polySiGe/Si interface.

5. Discussion

In practical polySiGe emitters, there will be a conflict between increased base current from the presence of the Ge and decreased base current from the interfacial layer. To illustrate this interaction, figure 7 shows a graph of the modelled value of S_{PI} as a function of interfacial layer thickness. In calculating the value of S_{PI}, the parameter values in [6] were used. At high values of interfacial layer thickness, T_I is small and hence $S_{PI} \approx S_I$ in equation 11. Consequently, the Ge in the polySiGe layer

has no effect on the value of S_{PI}. At low values of interfacial layer thickness, T_I in equation 11 is large, so S_{PI} approaches a value of $F\ (S_P + S_I) \approx F\ S_P$. In this situation the polySiGe layer has a strong effect on the value of S_{PI}.

Using the measured value of interfacial oxide thickness obtained from the SIMS profile in figure 1 (0.21nm), figure 7 predicts an increase in S_{PI} by a factor of 3.4 on going from 0% to 10% Ge and 4.8 on going from 0% to 19% Ge. These factors are consistent with the measured increases in base current seen in figure 2, namely 2.9 and 4.0. In a shallow polySiGe emitter, where there is little recombination in the single-crystal emitter, it would be expected that the base current would be proportional to S_{PI}. In which case, the above comparison demonstrates good agreement between theory and measurement. Higher increases in the value of S_{PI} could be obtained by using a thinner interfacial layer. For example, an interfacial layer thickness of 0.1nm would give an increase in S_{PI} by a factor of 13.5 for 20% Ge.

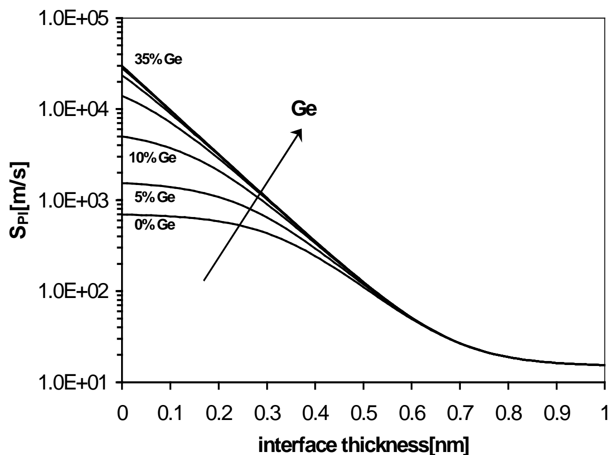

Figure 7: Modelled effective surface recombination velocity S_{PI} as a function of interfacial layer thickness for Ge contents of 0 to 35% in 5% steps.

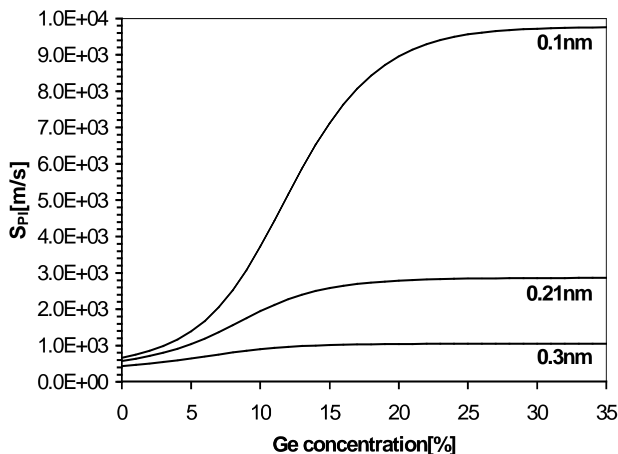

Figure 8: Modelled effective surface recombination velocity S_{PI} as a function of Ge contents for different interfacial layer thickness

The increase in the value of S_{PI} achieved by Ge incorporation in the polySi emitter is very rapid at low Ge concentrations, but saturates at high Ge concentrations. This is illustrated in figure 8 for thin interfacial oxide layers. For an interfacial oxide thickness of 0.1nm, S_{PI} saturates for Ge concentrations greater than approximately 20%. This situation occurs because the term $T_I\ /\ F$ in equation 11 becomes smaller than $(S_P + S_I)$ as the Ge content rises. With increasing interfacial layer thickness, the onset of saturation occurs at lower Ge concentrations. In practice there is therefore little benefit to be obtained by increasing the Ge concentration above 20%.

6. Conclusions

It has been shown that the incorporation of Ge into a polySi emitter allows the base current to be adjusted independently of the base profile. Measured results show that Ge content of 10% gives an increase in base current by a factor of 4. Theory predicts that higher factors could be achieved by reducing the interfacial layer thickness.

7. Acknowledgement

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8. References

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