Ultralow Silicon Substrate Noise Crosstalk Using Metal Faraday Cages in an SOI Technology

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***Abstract*—Ultralow substrate crosstalk is demonstrated using a novel metal Faraday cage isolation scheme in silicon-on-insulator technology. Over ten times reduction in crosstalk is demonstrated up to 10 GHz, compared to previously reported substrate crosstalk suppression technologies.**

***Index Terms*—Faraday cage, integrated circuit noise, microwave devices, substrate crosstalk, silicon-on-insulator (SOI), s-parameters.**

I. Introduction

INTEGRATION in mixed-signal high-frequency telecommunications circuits is often limited by the requirement to isolate sensitive analog circuits from noisey digital circuits at high frequencies. For a given frequency band, one finds that a larger proportion of the radio frerquency (RF) section of wireless transceivers is comprised of digital circuitry as the switching speed of digital circuits increases. This cointegration of digital and analog circuitry in the frontend RF section complicates the presence of digital noise via the common substrate corrupting analog circuit function. Modern RF system-on-a-chip (SoC) technology invariably incorporates significant digital sections for intermediate and base band signal processing in the form of a digital signal processor (DSP). Fully integrated SoC RF systems also incorporate large area passives such as integrated inductors and capacitive varactors that act as efficient antennas for picking up substrate noise from spurious signals emanating from other portions of the on-chip circuitry. Lower power in combination with higher frequency operation in portable wireless transceivers results in the existence are higher reactive and resistive impedance nodes in analog circuitry that are more sensitive to small voltage noise transients emanating from the substrate. Consideration must be made to reducing substrate noise transmission between disparate circuit elements as an integrated RF system is scaled to lower power and higher frequency operation using smaller lithography technologies that are becoming available in today's ultrasubmicron CMOS and BiCMOS processes.

Several studies [1]–[3] as well as new methodologies [4]–[7] have appeared in the literature that are aimed at understanding and/or improving isolation of high-frequency circuits from one another in a silicon-based technology. In [2], an excellent study is conducted that represents the degree of substrate noise suppresion that can be attained in main stream bulk silicon CMOS and BiCMOS technologies using p–n junction isolated wells and guard rings. In [3], the degree of substrate noise suppression that can be obtained in silicon-on-insulator (SOI) technologies is systematically studied using various combinations of diffused guards rings, oxide isolation, and high resistivity substrates. Various new schemes have been explored to suppress substrate noise coupling between circuit elements in an attempt to improve upon what can be obtained in standard bulk silicon or SOI technologies. In [5], a bulk micromachining process is used to create localized regions on a silicon wafer where the silicon substrate is locally thinned from the backside using anisotropic etching and coated with an Al metal backside ground plane. In this paper, substrate crosstalk suppression was measured between two inductors where a 60-μm-wide metal-filled trench, that extended through the locally thinned substrate to the backside metal ground plane, was placed between the inductors. A Faraday cage structure isolation scheme was fabricated [6] in a bulk thinned silicon substrate coated with a backside metal ground plane where the vertical walls of the cage comprised of high aspect ratio 10×10 μm^2 metal-filled vias separated from one another by 10 μm and connected through to the backside ground plane. In [7], porous silicon was used to provide isolation between two circuit elements, where the porous silicon was extended through the entire silicon substrate between the elements.

SOI is gaining importance as an alternative to bulk silicon for the implementation of high-frequency low-power mixed-signal telecommunication integrated circuits (ICs) [8]. The buried oxide layer in SOI offers superior dc/low-frequency isolation in conjunction with more compact integration of active devices. At high frequencies, however, signal isolation in SOI is known to vanish [3] as the buried oxide becomes capacitively transparent to RF/microwave signals.

In this paper, a new crosstalk suppression strategy is proposed. It uses a Faraday cage structure where the isolation region is surrounded completely by solid metal walls in an SOI process that encorporates a buried WSi_2 metal ground plane beneath the buried oxide layer. This work represents the highest

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degree of crosstalk suppression to be reported to date in a silicon IC technology. A factor of ten increase in crosstalk suppression up to 10 GHz is achieved compared to the best previously reported results in a silicon technology. The Faraday cage is comprised of a buried metal tungsten silicide ground plane beneath the buried oxide layer to form the bottom of the cage, and vertical metal-lined n^+ polysilicon-filled trenches in the active silicon layer to form the cage walls.

SOI offers the possibility of economical incorporation of a buried metal layer directly beneath the buried oxide, thus forming what is referred to as a ground plane silicon-on-insulator (GPSOI) technology. The buried metal silicide ground plane can act as both an electrical ground plane as well as a means to extract heat from overlying circuitry [9]. The ability of the ground plane alone to suppress substrate noise has been investigated [4], [10] without the presence of the active silicon layer (i.e., test structures built directly on the buried oxide over the ground plane). The presence of a ground plane in a full SOI structure (i.e., including the active silicon layer) affords the possibility of incorporating a complete Faraday cage structure consisting of solid metal around noisy circuitry to prevent such circuitry from interfering with sensitive analog circuitry on the same die.

The presence of such ground planes will not adversely affect circuits that are sensitive to capacitive loading (i.e., most active circuitry) as the larger ground plane capacitance appears in series with the smaller overlying device capacitances in the active silicon layer. Indeed, essentially the same approach is being used in standard CMOS and BiCMOS technologies [2] where a locally grounded low sheet resistance (10 to 20 Ω per square) buried n^+ layer is used as a buried ground plane below active circuitry to isolate the circuitry from crosstalk noise that propagates through the common substrate. Such buried diffusions take up significant chip area to realize a low sheet resistance and can load overlying devices, such as inductors, that depend upon magnetic phenomenon for their operation. Below inductors the buried n^+ layer in standard bulk silicon processes can be eliminated using in its place a patterned ground plane [11] formed in a lower metal or polysilicon interconnect layer. This ground plane is patterned in such a way as to break up magnetically induced eddy currents but terminate electric field lines thereby simultaneously providing lower ac substrate losses and higher substrate noise immunity at the expense of a slightly higher parasitic capacitance and hence slightly lower self-resonant frequency. The buried silicide ground plane in this work can also be patterened if placed beneath an inductor so as to short out any eddy currents induced in the ground plane by the magnetic field of the overlying inductor.

The buried metal ground described in this paper is most effective if locally grounded to the surface ground lines using vertical metal-filled trenches that can be quite narrow (2-μm-wide trenches are being used in this work) since the distance between the surface and the buried metal ground plane is only the thickness of the active silicon layer and the buried oxide layers combined. This contrasts with the much wider high aspect ratio trenches required in thinned bulk silicon processes [5], [6] that must reach through 10s or 100s of microns of the thinned silicon substrate to the backside metal ground plane.

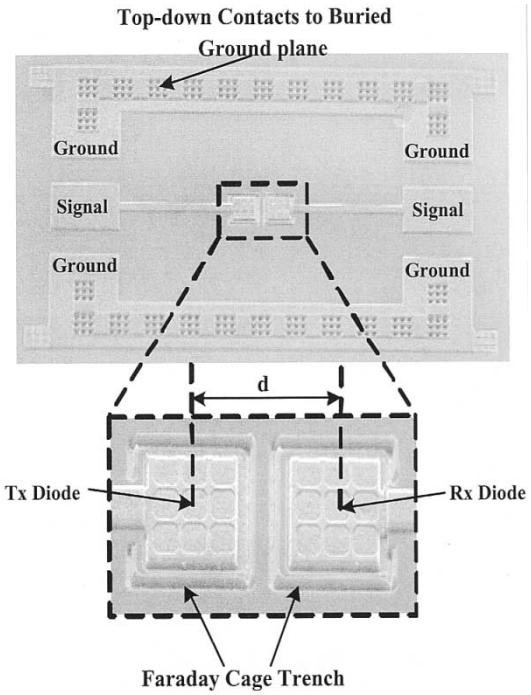

Fig. 1. Plan view of the crosstalk test structure for GPSOI with Faraday cages (config #3) surrounding the Tx and Rx diodes.

Section II describes the physical structure of the Faraday cage isolation formed in the GPSOI technology. In Section III experimental results are shown of substrate noise suppression in the GPSOI with Faraday cages. Experimental results of comparisons to controls in conventional SOI and also to the use of diffused guard rings in lieu of vertical metallized trenches for the Faraday vertical walls in the GPSOI are also reported. Experimental comparisons to other recently reported methods to reduce substrate crosstalk in silicon-based technologies are made followed by insight obtained from modeling in Section IV and onclusions in Section V.

II. Description of the Test Structures

Fig. 1 shows a top view photograph of the ground-signal-ground (GSG) coplanar s-parameter test structure used to measure the crosstalk between a transmitter (Tx) and receiver (Rx). Fig. 2 depicts an idealized cross-sectional view of the SOI structure with buried metal ground plane and a vertical metal-lined n^+-polysilicon filled trench.

Tx and Rx structures consisted of p^+n diodes fabricated in the silicon active layer with junction depths of 0.5 μm and contact pads 50×50 μm^2. The 0.6-μm-thick silicon active layer was doped n-type to 10^{16} cm^{-3}, and the buried oxide layer was 1.0-μm-thick. The Faraday cage structure consisted of 2.0-μm-wide trenches surrounding the Tx and Rx diodes and extending downward through the silicon active and buried oxide layers to contact an underlying buried metal silicide ground plane. The buried metal ground plane consisted of a 0.2-μm-thick 2.0-Ω per square metal silicide (WSi_2) on top of an n^+ doped silicon layer at the top of the low-doped n-type silicon substrate. The vertical trenches were lined with the same 0.2-μm 2.0-Ω per square metal silicide WSi_2 silicide material and then filled with

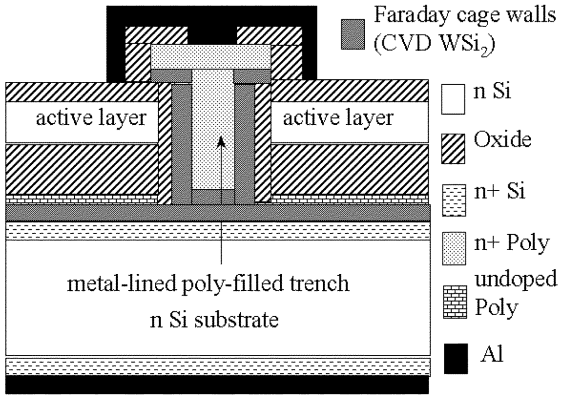

Fig. 2. Idealized schematic cross-sectional view of the metal-lined polysilicon filled trench used in the GPSOI with the Faraday cage structure (config #3) including active SOI layer and buried ground plane.

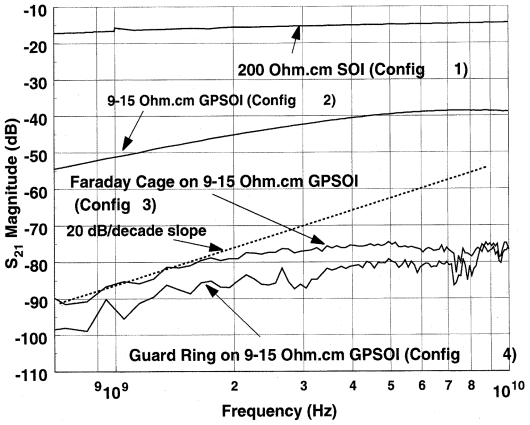

Fig. 3. Comparison of crosstalk in all configurations for 100 μm Tx to Rx pad spacing. (config $\#1$ = SOI only, config $\#2$ = GPSOI with buried metal ground planes only, config $\#3$ = GPSOI with Faraday cages (buried metal ground plane and metal-lined n^+-polysilicon-filled vertical trenches), and config $\#4$ = GPSOI with buried metal ground planes but where diffused guard rings are used in place of metal-lined n^+-polysilicon-filled trenches).

n^+-polysilicon. The entire Faraday cage structure consisting of the buried silicide layer and the vertical metal-lined polysilicon-filled trenches was grounded locally to the ground ring of the GSG coplanar s-parameter structure. An undoped polysilicon layer resided above the metal ground plane to assist in planarization before bonding the silicon active layer in the bonding and etch-back process to form the SOI. The backside of the SOI wafers consisted of an aluminum layer placed on top of an n^+-doped silicon region.

This SOI substrate is manufacturable by bonded silicon technology in a similar manner to that for silicon on metal-silicide on insulator (SMI or SSOI) substrates [9]. In this case, the difference in the process is that the WSi layer is at the interface between the handle wafer (substrate) and the buried oxide rather than between the active layer and the buried oxide. For SOI substrates manufactured by bonded silicon technology the buried ground plane requires three additional process steps: 1) chemical vapor deposition (CVD) of WSix, 2) contact via etch and, 3) refill. This is very similar to the addition of an extra layer of metallization and will incur a similar cost penalty.

Four types or configurations of the SOI structure were fabricated. In the first configuration (config #1) the Faraday cage was omitted (including the buried metal ground plane, metal-lined trenches, and n^+ layers beneath buried oxide layer) so as to act as a control to which the other structures could be compared. In other words, the only thing existing below the buried oxide for the control structure was a 200 Ω–cm silicon substrate. The only means of crosstalk suppression in this configuration consisted of a high-resistivity (200 Ω–cm) substrate which is sometimes used to increase crosstalk isolation in standard high frequency SOI technologies. The second configuration (config #2) employed a standard substrate resistivity (9 to 15 Ω–cm) as well as the buried metal silicide ground plane that was grounded locally to the GSG coplanar structure, but no metal-lined trenches. This configuration was useful in determining what fraction of the crosstalk was being suppressed by the buried metal ground plane compared to the metal-lined trenches in devices employing the full Faraday cage isolation scheme. The third configuration (config #3) was identical to config #2, but included the vertical metal-lined trench walls surrounding both the Tx and Rx diode structure, and hence the full Faraday cage isolation. The final configuration (config #4) was identical to config #3 but where the metal-lined vertical trenches of the Faraday cage were replaced with a solid diffused 0.5-μm-deep n^+ guard ring around each diode that was grounded via top metallization to the surface coplanar probe ground planes. Configs #2–#4 are referred to as GPSOI substrates to distinguish them from the SOI without ground plane (i.e., config #1).

III. Experimental Findings and Discussion

The S_{21} transmission crosstalk versus frequency was measured between the diodes as a means of determining the degree of isolation afforded by the various isolation schemes investigated. Fig. 3 shows measurements of the S_{21} transmission parameter for each of the four configurations for 100-μm separation between pad centers of Tx and Rx diodes over a frequency range of 1 to 10 GHz. Configs #3 and #4 show the highest degree of suppression relative to config#1 (SOI only) exhibiting on the order of at least 60 dB suppression relative to the SOI only (config #1) up to 10 GHz. This is at minimum 20-dB more suppression, or ten times more reduction in crosstalk than reported previously in other substrate crosstalk suppression schemes in a silicon-based technology, be it bulk or SOI-based. Comparison between S_{21} measurements for configurations #2 and #3 indicate that the buried ground plane alone contributes on the order of 30-dB crosstalk suppression with the vertical metal-lined n^+-polysilicon-filled trenches contributing an additional 30 dB of suppression. In other words, the buried metal ground plane is suppressing approximately 99% of the crosstalk on a linear signal amplitude scale. This is because most of the substrate crosstalk in a nonshielded technology emanates from underneath the crosstalk sources via complicated three dimensional patterns that find their way through the substrate to receiving nodes of the overlying circuitry or devices.

No significant difference in measurements was observed with a grounded or a floating backside contact to the wafers. Configs #2 to #4 were also fabricated with a higher substrate resistivity

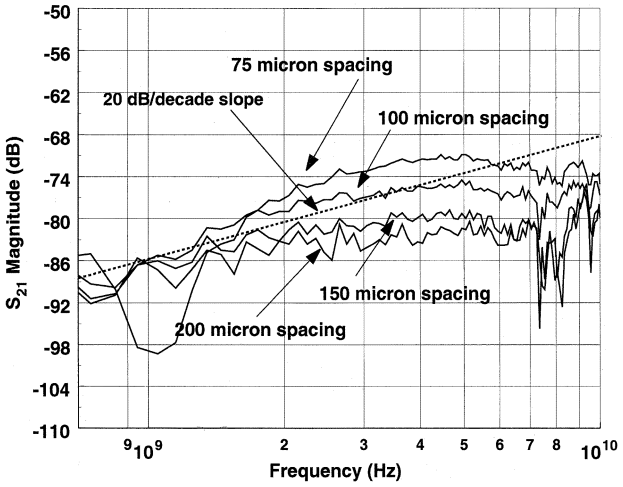

Fig. 4. Crosstalk suppression versus frequency with distance between centers of the Tx and Rx pads as a parameter for Faraday cage (config #3) where the vertical walls of the cage are comprised of metal-lined n^+-polysilicon-filled trenches grounded to the underlying metal silicide ground plane.

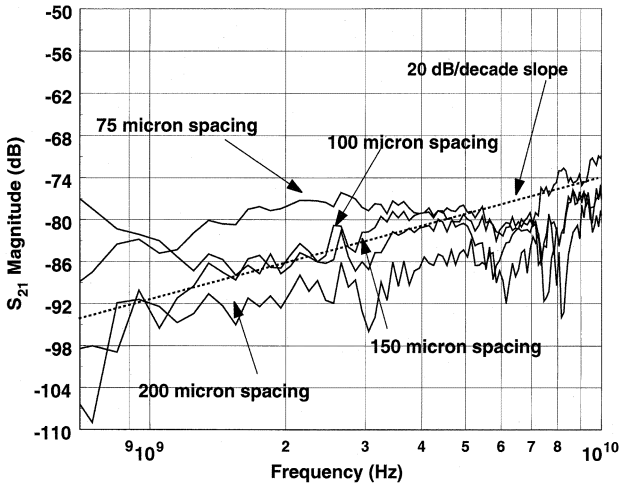

Fig. 5. Crosstalk suppression versus frequency with distance between centers of the Tx and Rx pads as a parameter for Faraday cage (config #4) where the vertical "walls" of the cage are comprised of diffused n^+ guard rings that are grounded to the underlying metal silicide ground plane.

(200-Ω – cm) with no differences observed in their S_{21} transmission measurements compared to the results shown in Fig. 3.

Effect of distance between Tx and Rx pad centers on crosstalk was investigated for 75-, 100-, 150-, and 200-μm separation. Figs. 4 and 5 show the dependency of crosstalk on Tx to Rx pad distance for both configs # 3 and #4, respectively. Distance is measured between the centers of the 50×50-μm^2 pads. Crosstalk was observed to decrease approximately 3 to 5 dB per 50-μm increase in spacing over a frequency range from 1 to 10 GHz for all configurations for both types of Faraday cage structures.

Table I compares this work with previously reported crosstalk suppression measurements in other technologies. Crosstalk suppression values for each technology are given relative to the controls in that same technology, where nothing was done to suppress substrate crosstalk in the controls. It is interesting to note that all of the technologies B to F as listed in the table do not out perform what can be achieved in standard bulk CMOS processes (A in the table) where junction isolation is used to suppress crosstalk between separate wells. Crosstalk suppression in this work (G in the table) with the use of solid metal Faraday cages is 20 to 30 dB greater (or over ten times greater) than previously reported in other silicon-based technologies at RF frequencies.

TABLE I

COMPARISON OF THIS WORK TO OTHER RECENT STATE-OF-THE-ART SUBSTRATE CROSSTALK SUPPRESSION TECHNOLOGIES IN SILICON. ALL DISTANCES BETWEEN TX AND RX STRUCTURES ARE 100 μm EXCEPT FOR [2]. DISTANCE BETWEEN TX AND RX PADS IS NOT GIVEN FOR TECHNOLOGY A IN [2]. FOR TECHNOLOGY E IN [5], TX AND RX CONSISTED OF SPIRAL INDUCTORS SEPARATED BY 540 μm WITH A 60-μm-WIDE METAL-FILLED TRENCH INBETWEEN AND BACKSIDE METAL GROUND PLANE BENEATH INDUCTORS. SUBSTRATE RESISTIVITY IS NOT GIVEN FOR TECHNOLOGIES A IN [2], E IN [6], AND F IN [5]. LABELS FOR TECHNOLOGIES ARE FROM REFERENCES: A: [2],B/C: [3],D:[7],E:[6], F:[5]

Label and Ref.	Technology	Suppression Compared To Control in Same Technology
A	Junction isolated p-well in standard bulk CMOS process with p^- Si substrate	40 dB at 1 GHz 35 dB at 10 GHz
B	Diffused guard rings in SOI with 20 Ohm-cm substrate	10 dB 1 GHz to 10 GHz
C	Diffused guard rings in SOI with 200 Ohm-cm substrate	30 dB at 1 GHz 15 dB at 5 GHz 10 dB at 10 GHz
D	Porous silicon in bulk Si substrate with silicon removed below porous silicon	35dB at 2 GHz 15 dB at 8 GHz
E	Metal-filled vias in thinned bulk silicon substrates with back-side metal ground plane	40 dB at 1 GHz 36 dB at 5 GHz
F	Bulk-micromachining with local backside metal ground planes and vertical dielectric trenches	30 dB 1GHz to 10 GHz
G *This Work*	Solid metal Faraday cage in SOI with buried metal ground planes in 9 to 15 Ohm-cm Si substrate	70 dB at 1 GHz 55 dB at 5 GHz 55 dB at 10 GHz

IV. MODELING

Fig. 6 depicts a lumped element model for the GPSOI structure where Faraday cages are being used for isolation in the active silicon layer. Fig. 7 shows measurements (for 100-μm spacing between Tx and Rx pad centers) versus 3-D electromagnetic numerical simulation (using Agilent's Momentum simulator) and the lumped element model of Fig. 6. Values for the various lumped element model parameters are listed in Table II.

With the assistance of the lumped element model the behavior of the crosstalk can be explained as follows. At lower frequencies, the ac impedance consisting of the diode junction capacitance C_J and R_1 branch does not dominate the behavior of s_{21} with most of the crosstalk passing through C_2 capacitance. C_2 models the trans-capacitance through the active silicon layer (which is mostly blocked by the vertical metal-lined trenches) and the buried oxide layer (where there is nothing to block capacitive signal energy). This leads to a

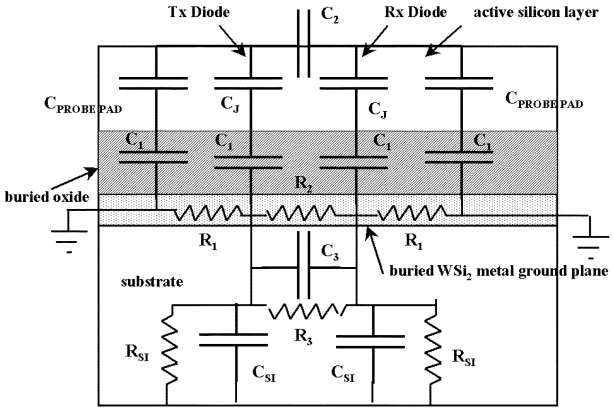

Fig. 6. Physically based lumped element model for GPSOI with Faraday cage isolation (configuration # 3).

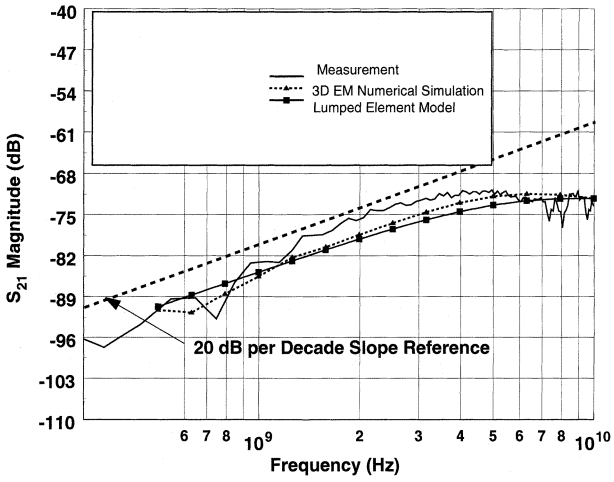

Fig. 7. Comparision between measurements of S_{21} magnitude for GPSOI structure (config #3), 3-D electromagnetic numerical simulation, and lumped element modeling. Tx/Rx pad separation distance is 100 μm for each structure.

TABLE II
PARAMETERS FOR LUMPED ELEMENT MODEL OF FIG. 6

Lumped Element Model Values for GPSOI			
C_J	1.2 pF	R_1	0.4 Ω
C_1	>> C_J	R_2	2.2 Ω
C_2	0.093 fF	R_3	3.83 kΩ
C_3	3.25 fF	R_{SI}	4.57k Ω
$C_{Probe\ Pad}$	0.3 pF	C_{SI}	3.43 fF

single zero Z_oC_2 or 20-dB-per-decade increase in crosstalk exhibited in Fig. 7 over the lower portion of the frequency range. Z_o is the characteristic impedance of 50 Ω used in the measurement system. As the frequency increases, the decreasing ac impedance associated with the vertical diode junction capacitance begins to compete with the C_2 path shunting energy through R_1 to the local ground. This introduces a pole that competes with the zero in the crosstalk transfer function resulting in the crosstalk s_{21} magnitude "flattening out" at higher frequencies. Hence, the diode capacitance, as well as the probe pad capacitance, loads the crosstalk transfer function from Tx to Rx. The low valued R_2 through the buried metal ground plane effectively shunts out any crosstalk via the much larger C_3 that represents crosstalk capacitance through the substrate itself. It is this shorting out of C_3 that is the principal reason for the significant crosstalk reduction observed in the GPSOI structure compared to the conventional SOI structure. R_2 appears in parallel with a low valued R_1 and hence does not contribute significantly to crosstalk. The ground plane therefore essentially shorts out the substrate crosstalk leaving only the buried oxide layer itself as the principal crosstalk path.

V. CONCLUSIONS

GPSOI technology enables the use of a metal Faraday cage structure as a means to suppress crosstalk between circuit components in an telecommunication IC. It has been demonstrated experimentally in this work that such a Faraday cage comprised of metal silicide walls can provide crosstalk suppression to a significantly greater extent that other reported silicon-based technologies to date. This work suggests that SOI with buried metal ground planes can offer superior crosstalk immunity than standard or nonstandard bulk silicon technologies.

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