Reduction of Parasitic Capacitance in Vertical MOSFETs by Spacer Local Oxidation

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***Abstract*—Application of double gate or surround-gate vertical metal oxide semiconductor field effect transistors (MOSFETs) is hindered by the parasitic overlap capacitance associated with their layout, which is considerably larger than for a lateral MOSFET on the same technology node. A simple self-aligned process has been developed to reduce the parasitic overlap capacitance in vertical MOSFETs using nitride spacers on the sidewalls of the trench or pillar and a local oxidation. This will result in an oxide layer on all exposed planar surfaces, but no oxide layer on the protected vertical channel area of the pillar. The encroachment of the oxide on the side of the pillar is studied by transmission electron microscopy (TEM) which is used to calibrate the nitride viscosity in the process simulations. Surround gate vertical transistors incorporating the spacer oxidation have been fabricated, and these transistors show the integrity of the process and excellent subthreshold slope and drive current. The reduction in intrinsic capacitance is calculated to be a factor of three. Pillar capacitors with a more advanced process have been fabricated and the total measured capacitance is reduced by a factor of five compared with structures without the spacer oxidation. Device simulations confirm the measured reduction in capacitance.**

***Index Terms*—LOCOS oxidation, parasitic capacitance, surround-gate, vertical MOSFETs.**

I. Introduction

THIN body double-gate devices are promising for scaling complementery metal oxide semiconductor (CMOS) devices into the nanoscale regime. Vertical transistors can easily incorporate double or surround gates, enabling increased packing density at a defined lithographical node as compared to standard CMOS transistors [1]–[10]. A disadvantage of the vertical MOSFET is the large overlap capacitance of the gate with drain, source and body regions and the reduction of this capacitance is a recurring theme in recent research. Gate oxide formation before selective epitaxial growth has been used in epitaxial vertical MOSFETs to reduce the parasitic capacitance [1]. A vertical replacement gate reduces the capacitance in a vertical MOSFET defined by solid-state diffusion [5]. Ion implanted vertical MOSFETs are the preferred manufacturing method since they are CMOS compatible, and surround gate ion-implanted vertical transistors were recently fabricated by Schulz *et al.* [6]. One option to reduce parasitic capacitance in these transistors is enhanced oxidation on the planar surfaces by amorphising a superficial layer by a high dose implant [11]. In this paper a simple method is proposed to reduce the parasitic capacitance, and especially the gate to bottom electrode capacitance in ion implanted vertical MOSFETs. The idea is tested by means of transmission electron microscopy (TEM), current-voltage (C–V) measurements, simulations, and fabrication of surround gate vertical MOSFETs.

Manuscript received November 19, 2002; revised March 28, 2003. This work was supported by the SIGMOS Project of the European Commission and EPSRC Grant GRM93178. The review of this paper was arranged by Editor R. Singh.

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Digital Object Identifier 10.1109/TED.2003.813334

II. Spacer Local Oxidation

A. Process

Fig. 1(a) shows a schematic of a surround gate ion-implanted vertical MOSFET. The parasitic capacitance is associated with the gate track in the active area (gate to bottom) and with the gate to top capacitances on the top and on the side of the pillar. spacer or fillet local oxidation (FILOX) is a self-aligned process to grow a thin second field oxide in the active area without oxidizing the sidewalls of the pillars (the use of a second field oxide in lateral MOSFETs has been described by Lau *et al.* [12]). Unlike a lithography defined oxide, the FILOX process does not need to take into account any alignment tolerance and can hence be grown much closer to the channel area. By using an oxide thickness much smaller than for a standard field isolation, bird's beak formation is suppressed while the parasitic capacitance is reduced significantly. Fig. 2 shows a schematic of the process steps of the FILOX process. After the pillar or trench etch of the vertical MOSFET, a thin stress relief oxide is grown over the structure. A nitride layer is deposited over the pillar by chemical vapor deposition (CVD) and anisotropically etched to expose the stress relief oxide on the horizontal surfaces, while leaving nitride spacers on the sidewalls of the trench or pillar. A subsequent local oxidation will result in the growth of an oxide layer on all exposed planar surfaces, but no or a limited oxide layer will grow on the protected vertical channel area. After the removal of the nitride spacers by wet etching, the grown oxide covers the active area, while the vertical sidewalls of the pillar contain the original stress relief oxide which doubles up as sacrificial oxide. After the nitride strip, the sacrificial oxide including any encroached oxide in the channel area is etched back. Afterwards, processing of the transistors can be continued as usual. The extra oxide in the trench and on top of the pillar will reduce

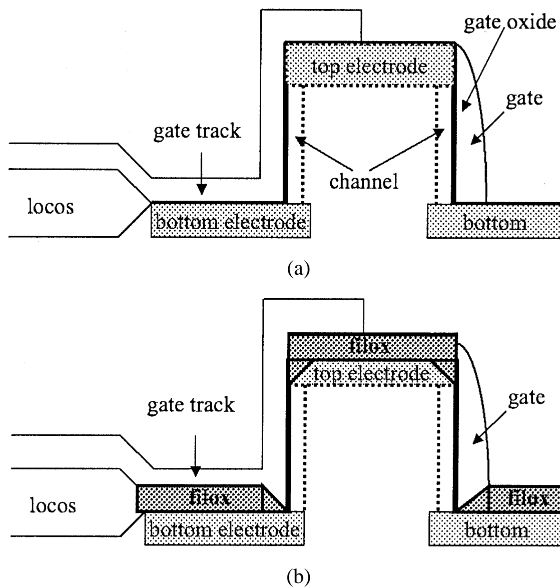

Fig. 1. (a) Schematic cross-section of a typical ion implanted vertical MOSFET with surround gate contacted at one side. Parasitic capacitances arise from the gate track on the bottom electrode and the gate overlapping the top electrode due to the alignment tolerance. (b) A similar vertical MOSFET with FILOX process.

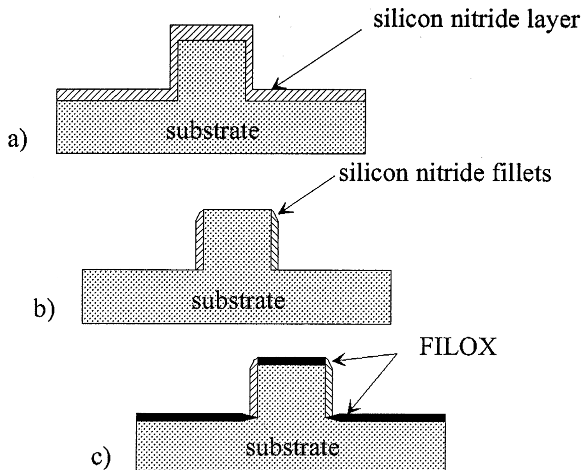

Fig. 2. Principle of the spacer local oxidation (FILOX) process. A nitride layer is deposited over the pillar (a) and subsequently anisotropically etched to leave the nitride spacers (b). A local oxidation process will oxidize the exposed surfaces (c). The process is completed by wet etching the nitride spacers.

the parasitic capacitance by a factor proportional to the ratio of the gate oxide and the FILOX oxide as is shown in Fig. 1(b). The method is hence a simple maskless process to strongly reduce the parasitic capacitance of a vertical MOSFET [13].

B. Oxide Encroachment

1) Transmission Electron Microscopy (TEM): Test structures for the spacer local oxidation were fabricated by reactive ion etching of Si pillars. A 5 nm stress relief oxide was grown by thermal oxidation, followed by a 70 nm Si_3N_4 layer deposited by CVD over the pillar and trenches. This nitride layer was etched anisotropically in CHF_3 to leave spacers on the sidewall. The spacer local oxidation (FILOX) was a 40 nm wet oxide grown at 1000 °C. Fig. 3 shows a TEM micrograph

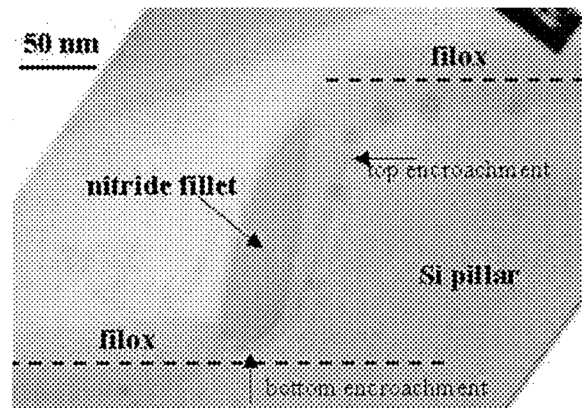

Fig. 3. TEM ⟨110⟩ cross-section of the FILOX process directly after the oxidation (see text for details).

of a pillar capacitor just after the spacer oxidation. The original pillar height before oxidation was derived from profilometer measurements and its height of 215 nm is shown as a dashed line in the figure. It can be seen that the nitride spacer is slightly over etched by 25 nm with regard to the original pillar height. The figure shows clearly the influence of the FILOX oxidation on the oxide thickness. The FILOX oxidation consumes silicon and it thickness away from the side wall is 40 nm in agreement with expectations. At the bottom of the pillar the nitride spacer protects the Si channel very well against oxide encroachment and no birds beak is visible. The oxide thickness below the nitride spacer is identical to the 5 nm of the stress relief oxide that has been grown before deposition of the nitride layer. However, at the top of the pillar significant oxide encroachment has caused an increase of the oxide thickness on the sidewall extending almost to the bottom of the pillar.

2) Process Simulations: To investigate the oxide encroachment, the spacer local oxidation process was simulated using Silvaco's package "ATHENA." The oxidation process took place at 1000 °C which is a high enough temperature to allow viscous flow of the oxide, and this flag was switched on in the simulations. The software also takes into account that the oxide is expected to grow faster in the vertical ⟨110⟩ plane than in the horizontal ⟨100⟩ plane of the wafer. Recent measurements in the context of vertical MOSFETs show an increase in oxidation rate of a factor of 1.4 [14]. However, using the default parameters or alternative parameters [15], [16] for the oxide and nitride viscosity, the experimental results in Fig. 3 could not be reproduced. Both sets of parameters result in a similar encroachment of the oxide at the top of the pillar as on the bottom. By reducing the nitride viscosity slightly, the experimental results could be reproduced, as displayed in Fig. 4. The effect of the nitride viscosity on the oxide thickness is displayed in Fig. 5. These results can be understood by realizing that the thickness of the nitride spacer perpendicular to the oxide-nitride interface is much larger at the bottom of the pillar than at the top of the pillar. When the nitride viscosity is reduced to allow oxidation at the interface, the oxidation will in the first instance only happen at the top of the pillar where it is easier for the oxide to bend the nitride spacer. Only when the nitride viscosity is reduced further, does a birds beak also appear at the bottom of the pillar. The experimental results

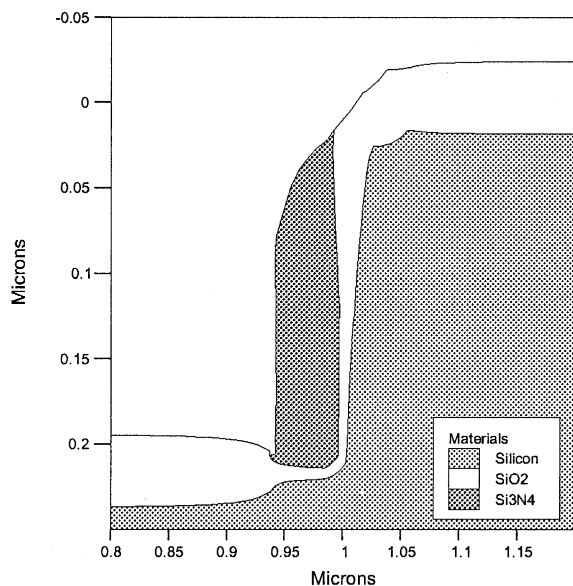

Fig. 4. Cross section of the FILOX process as simulated by Silvaco software package Athena using the viscous flow model and oxide and nitride viscosity of 2×10^{18} g/cm-s and 1.6×10^{16} g/cm-s at 1000 °C, respectively.

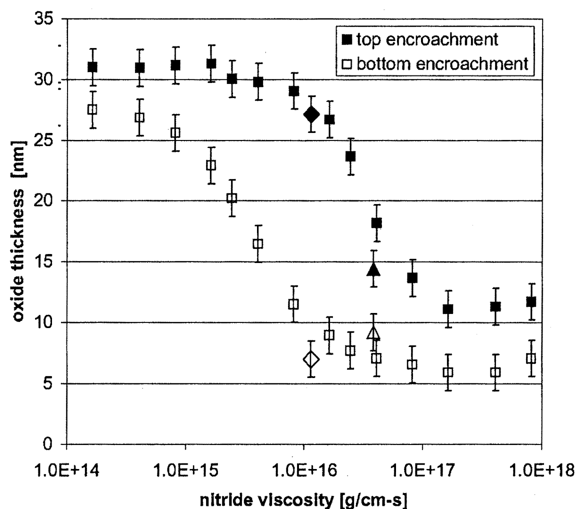

Fig. 5. Oxide encroachment on top and bottom of the pillar as a function of nitride viscosity, measured at $y = 0.06$ μm and $x = 0.0965$ μm, with oxide viscosity of 2×10^{18} g/cm-s. The experimental points are plotted as diamonds at nitride viscosity of 1.2×10^{16} g/cm-s. The default simulation values are plotted as triangles.

correspond almost exactly with the maximum achievable difference in encroachment between the top and bottom oxide.

The oxide encroachment at the top of the pillar is not as detrimental as one may expect because the top of the pillar will correspond to the implanted source in a vertical transistor. In the next section, it will be shown that the encroachment can even be used to our advantage to reduce the parasitic capacitance between gate and top electrode on the side of the pillar.

C. Stress

The other major concern of a LOCOS oxidation near the channel area is the stress induced in the Silicon during the oxidation. We used TEM to analyze test wafers with FILOX oxide thickness. Near the active area and channel area, the volume expansion of a two-dimensional (2-D) oxidation must be accommodated by the visco-elastic flow of the SiO_2, otherwise plastic deformation with accompanying dislocations will occur [17]. Because the size of the pillars and trenches is only 1.5 μm, this condition applies to both the top and the bottom of the wafer. This will degrade device performance significantly. The wafers with a thick 120 nm FILOX oxide showed a large number of line defects on top of the silicon pillars making an angle of 55° with the direction of the (110) cross section. This corresponds to dislocations along the $\langle 211 \rangle$ direction. Fig. 6 is a TEM micrograph of a corner of a pillar with a 120 nm thick FILOX oxide and shows a dislocation at the edge of the pillar. Unlike the thin and straight $\langle 211 \rangle$ dislocations on the top, this dislocation is not along a crystallographic direction (it even bends slightly).

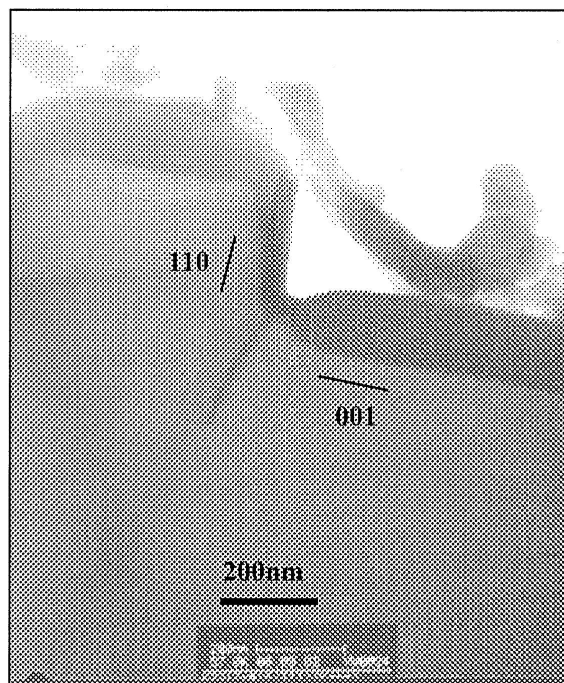

Fig. 6. TEM cross section of the FILOX process with 40 nm nitride spacer and 120 nm filox oxide. A clear dislocation is visible at the bottom of the corner where the stresses are highest. No such dislocations where found in similar structures with a 40 nm FILOX oxide.

The wafers with thin FILOX oxide (40 nm) show considerably less defects on top of the pillar and no dislocation were visible in the channel area or near the edge of the pillar. Since dislocations are nucleated at the interface of the oxide and silicon, the shear stress in the FILOX oxide is a good predictor of the dislocations in the silicon. A 2-D stress model in Athena [15] shows significant lower shear stress in the pillars with the thinner oxide thickness as is shown in Fig. 7. This is in qualitative agreement with the TEM graphs and simulations by Matsumoto *et al.* [18]. It can hence be concluded that to reduce the bird's beak and the stress it is beneficial to choose the FILOX oxide as thin as compatible with a large reduction in parasitic capacitance.

III. Device Characterization

A. Vertical MOSFETs

Double gate and surround gate vertical NMOS transistors incorporating the FILOX process were fabricated using stan-

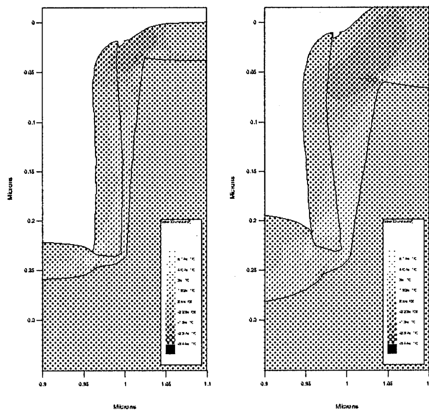

Fig. 7. Calculation of the stress profile in capacitors with the FILOX oxidation for a 40 nm nitride spacer and 40 nm (left) and 120 nm (right) FILOX oxide. The light and dark regions indicate large positive and negative tensile stress, respectively. The tensile stress at the Si-SiO_2 interface is considerably larger in the thicker oxide (2.5 versus 1.5 GPa).

dard processing steps. A $\langle 100 \rangle$ substrate was implanted with 5×10^{14} cm^{-2} Boron body doping, which results, according to v/d Pauw measurements, to a doping on the top and bottom of the pillar of 5×10^{18} cm^{-3} and 4×10^{18} cm^{-3}, respectively. This was followed by dry etching of the Si pillars in HBr to a height of 200 to 300 nm. To define the active area a local field oxidation (LOCOS) was grown after the pillar etch. This removes a significant parasitic gate to body capacitance at the edge of the LOCOS field oxide. A 20 nm stress relief oxide and a 130 nm nitride layer were deposited over the pillar and the active area was defined by lithography followed by a 600 nm LOCOS oxidation. The same nitride layer was subsequently anisotropically etched to define the spacers at the sides of the pillar. A 60 nm FILOX oxide was grown at 1000 °C. The nitride spacers were afterwards used to protect the channel during the As source and drain implant. The dose of the implant was 6×10^{15} cm^{-2} and the energy 120 keV and 50 keV for the wafers with and without FILOX oxide, respectively. The nitride spacers were subsequently removed. A 20 : 1 HF dip etch was applied to remove the stress relief/sacrificial oxide. The overetch has to be limited to ensure that the FILOX oxide is not consumed during the etch. A 3 nm gate oxide was grown at 800 °C followed by gate deposition and patterning. The gate was doped *in-situ* with 1×10^{20} cm^{-2} Phosphorus, but could also have been doped by implantation. By depositing the gate after source and drain implant an increase in channel width is achieved because the sidewall under the gate track is now part of the channel as well. The increase in the parasitic gate to bottom capacitance due to this step is prevented by the FILOX oxidation. A rapid thermal anneal (RTA) for 10 s at 1100 °C activated the dopants. Boron phosphorus silica glass (BPSG) was deposited on 100 nm undoped silicon dioxide (SILOX) and contact windows were etched before Al deposition. A photograph of the fabricated surround gate vertical transistor is shown in Fig. 8. The total channel width of the depicted transistor is 24 μm.

Fig. 9 shows a field emission scanning electron microscope (FESEM) graph of the vertical transistor with the FILOX

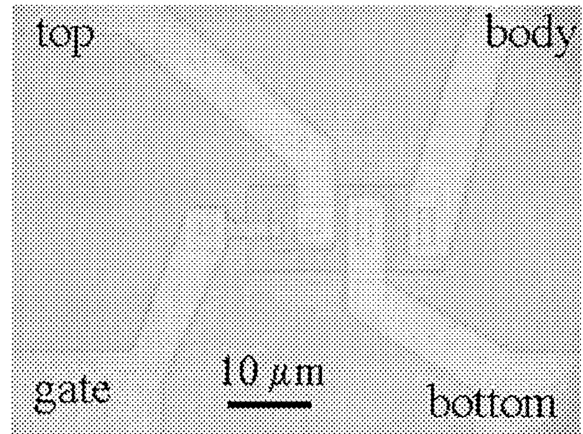

Fig. 8. Top view of a surround-gate ion-implanted vertical NMOS transistor showing the overlap of the gate track with the active area and pillar. The FILOX oxide and the gate spacers surrounding the pillar are not visible.

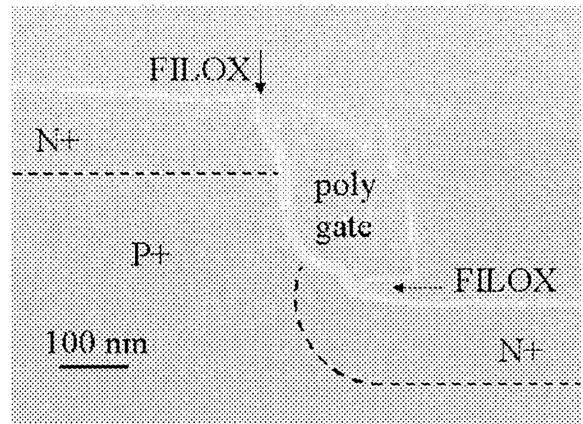

Fig. 9. Field emission SEM cross-section of a surround gate ion-implanted vertical NMOS transistor with the FILOX process. Both pillar top and bottom have a 60 nm thick FILOX oxide as visible under the gate electrode. The interface of the FILOX oxide and BPSG is not discernible. Encroachment of the oxide on top is reducing the gate to top electrode parasitic capacitance on the side of the pillar. The gate oxide thickness in the channel area is not affected.

process. The shape of the gate spacer shows a dip on the bottom and a peak on top of the spacer. This is very likely due to focusing of the etchant during the anisotropic Si pillar etch and polySilicon gate etch. An identical peak on top of the gate spacer has been found by Schulz *et al.* [6]. Both dip and peak were also present in transistors without FILOX. The FILOX oxidation has increased the oxide thickness at the top and the bottom of the pillar and the encroachment of the oxide from the top to the side is visible. At the top of the pillar the FILOX oxide as shown in Fig. 9 does not encroach into the channel, unlike that shown in Fig. 3. The explanation for this result is that the FILOX oxide similar to the one shown in Fig. 3 has been partly removed during the HF dip after the removal of the nitride spacer and prior to the gate oxidation and gate spacer deposition and etch. The encroachment of the oxide is now limited to the top of the pillar only and does not influence the gate oxide thickness at the channel. The increased oxide thickness on top has the advantage of reducing the parasitic overlap capacitance between the gate and the top electrode.

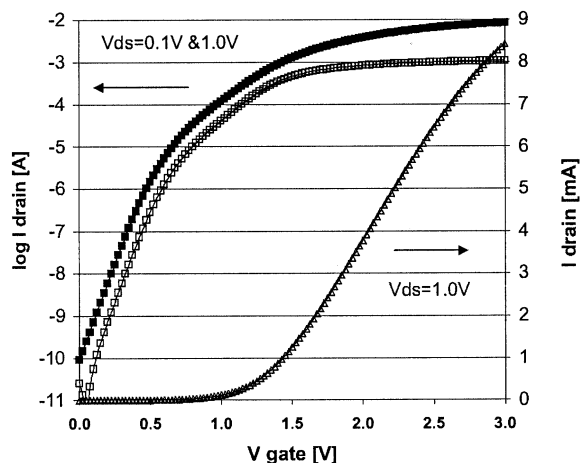

Fig. 10. Transfer characteristics of a drain on top surround gate ion-implanted vertical NMOS transistor with the FILOX process. Gate oxide thickness is 3 nm, channel width is 52 μm and channel length is estimated to be 100 nm.

The transistors were characterized using a HP4155A semiconductor analyzer and transfer characteristics of a transistor with FILOX process are shown in Fig. 10. Typical parameters with drain on top are $V_t = 1.0$ V, $S = 105$ mV/dec, $I_{on} = 170$ μA/ μm, and $I_{off} < 2$ pA/μm at V_{ds} of 1 V and V_{gs} of 3 V and 0 V, respectively. These values are comparable with transistors that were fabricated without the FILOX process. The FILOX process hence does not alter the transistor operation, indicating that the gate oxide is not degraded by the FILOX oxidation. The transistor characteristics are very similar to those published in [6] and are in excellent agreement with device simulations based on our process. Although direct probing of the intrinsic capacitance of the transistors is impossible due their small size, calculations based on the electron micrographs, and process and device simulations give an estimate of the expected capacitance reduction. Reduction in capacitance takes place both below the gate track and below the gate spacers and is strongly dependent on the ratio of the nitride spacer thickness to the gate spacer thickness and the lithography node. In the transistors discussed above, fabricated with a 200 nm gate spacer and 130 nm nitride spacer, the reduction of the intrinsic capacitance is roughly a factor of 3. By scaling the stress relief oxide, nitride spacer thickness and gate spacer thickness a similar reduction factor can be achieved as well at smaller dimensions with the FILOX oxide typically 5 to 10 times as thick as the gate oxide.

In the above process the nitride spacers have been used to align the source and drain implant. In the transistors fabricated by Schulz *et al.* [6], the gate has been patterned before the ion implantation of the source and drain. This self aligns the gate, but at the same time decreases the width of the channel since no drain is present below the gate track. It would be possible to combine both processes by implanting a low doped drain (LDD) aligned to the nitride spacer followed by a high doped drain (HDD) aligned to the gate spacer. It should be stressed that the FILOX process can be applied in the same way on a shallow trench isolated (STI) transistor.

A back of the envelop calculation shows that a vertical MOS with FILOX oxide could have similar or even lower parasitic capacitance than a lateral MOSFET at the same lithography node even at minimum geometry, but this does requires major effort in control and reproducibility of the FILOX oxidation and implant depth on top of the pillar. We do emphasize, however, that the major advantage of vertical MOSFETs is the smaller area and the increased current drive due to smaller channel length at the same lithography node. We recently assessed the parasitic capacitances and performance potential of a vertical MOSFET with FILOX oxide in a circuit environment, showing a significantly improved performance in speed [10].

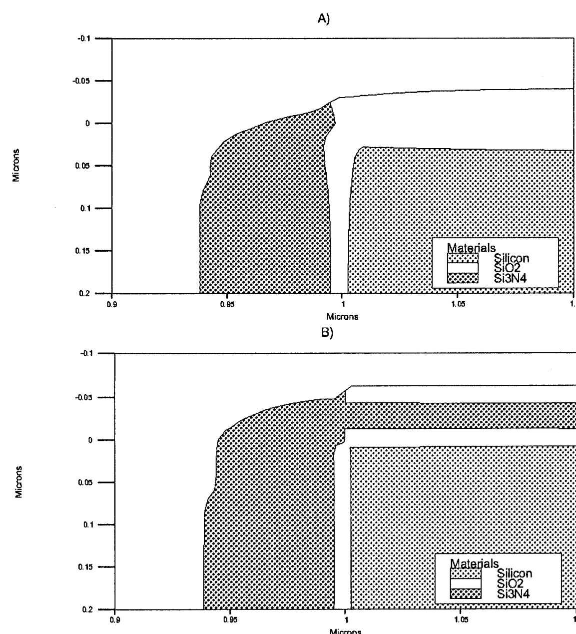

Fig. 11. Cross section of the FILOX process as simulated by Athena for pillars with different protection using the calibrated values derived from Fig. 4: (a) thermal oxide and (b) thermal oxide-nitride-LTO stack. The oxidation at the bottom is identical to that shown in Fig. 4.

B. Capacitors

In the previous section it has been shown that the oxide encroachment at the top of the pillar can be beneficial in reducing the overlap capacitance between source and gate. However, the source capacitance on the side can also be reduced by over etching of the gate spacer, Furthermore, precise control of the gate oxide thickness on the sidewalls is of paramount importance and it is probably required to minimize this encroachment. Complete suppression of the FILOX oxide encroachment at the top of the pillar can be achieved by depositing a protective layer on the wafer before the pillar etch. The top of the pillar is then protected against oxidation by this layer. The calibrated process simulations in Fig. 11 in combination with Fig. 4 show that an oxide protection is insufficient to completely suppress encroachment at the top of the pillar. Complete protection can only be realized when a nitride layer is used to prevent penetration of the oxidation. In the simulation shown in Fig. 11(b) an oxide/nitride/oxide stack has been used with the bottom oxide acting as a stress relief oxide and the top low temperature oxide (LTO) as a protection during the anisotropic etch of the nitride spacers.

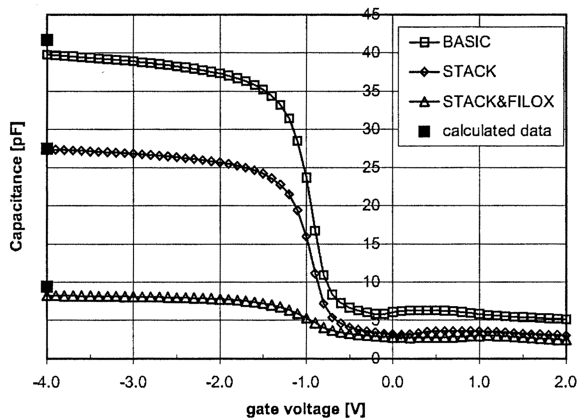

Fig. 12. C–V measurements for the three different pillar structures: basic pillar without protection, with oxide-nitride-oxide stack on top, and with oxide-nitride-oxide stack on top and FILOX process at the bottom.

To test this idea, capacitors were fabricated by using the latter process of having a thermal oxide/CVD nitride/LTO stack grown before the pillar etch. After the FILOX oxidation and the removal of the nitride spacers, a short HF dip removed the sacrificial oxide. A 4 nm gate oxide was grown at 800 °C, immediately followed by CVD polySi deposition. The capacitor structures consisted of 40 pillar elements of 300 nm height that were etched anisotropically into the silicon. The width of the pillar and the trenches corresponds to the lithography definition of 1.5 μm. The length of the pillars was 94.5 μm. Three different type of capacitors were fabricated: A) basic pillars B) pillars with a 20 nm thermal oxide-130 nm CVD nitride and 50 nm LTO stack, and C) pillars with both the oxide-nitride-oxide stack and a 80 nm FILOX oxidation. C–V measurements were performed on a HP4280A at 1 MHz. Fig. 12 compares the C–V characteristics of these three pillar structures. A strong decrease in the total capacitance in accumulation has resulted from the application of the oxide-nitride-oxide stack and the FILOX process. The oxide-nitride-oxide stack reduces the capacitance by 30% and the FILOX process gives a reduction of a factor of five for a 4.0 nm gate oxide compared to a basic pillar.

IV. Conclusion

A simple self-aligned process has been developed to reduce the parasitic gate capacitance in vertical MOSFETs using nitride spacers on the sidewalls of the trench or pillar and a local oxidation (FILOX). This results in an oxide layer on all exposed planar surfaces, but no oxide layer on the protected vertical channel area. A TEM cross-section was used to calibrate the nitride viscosity in the process simulator. This viscosity value was used in the calibrated process and device simulations to demonstrate a total reduction in the overlap capacitance by a factor of 3 in a surround gate vertical MOSFET. Surround-gate vertical transistors incorporating the spacer oxidation have been fabricated, and those transistors show excellent subthreshold slope and drive current and no degradation of the electrical or structural characteristics due to the FILOX process. Encroachment of the FILOX oxide adjacent to the top electrode is seen in the completed transistors. This encroachment is advantageous for the reduction of gate to top electrode capacitance. To control the oxide encroachment on top of the pillar, the calibrated process simulations show that a nitride layer on top completely suppresses the encroachment.

Acknowledgment

After the submission of the paper, the authors learned that a similar idea has been touched upon in the Ph.D. dissertation "Physics and Technologies of Vertical Transistors" by Sang-Hyun Oh, Stanford University, Stanford, CA, in 2001.

References

[1] J. Moers, D. Klaes, A. Toennesmann, L. Vescan, S. Wickenhaeuser, T. Grabolla, M. Marso, P. Kordos, and H. Lueth, "Vertical p-MOSFETs with gate oxide deposition before selective epitaxial growth," *Solid-State Electron.*, vol. 43, pp. 529–535, 1999.

[2] K. De Meyer, M. Caymax, N. Collaert, R. Loo, and P. Verheyen, "The vertical heterojunction MOSFET," *Thin Solid Films*, vol. 336, pp. 299–305, 1998.

[3] K. Mori, A. Duong, and W. F. Richardson, "Sub 100 nm vertical MOSFET with threshold voltage adjustment," *IEEE Trans. Electron Devices*, vol. 49, pp. 61–66, Jan. 2002.

[4] K. C. Liu, S. K. Ray, S. K. Oswal, and S. K. Banerjee, "A deep submicron Si_{1-x} Ge_x/Si vertical pmosfet fabricated by Ge ion implantation," *IEEE Electron Device Lett.*, vol. 19, pp. 13–15, Jan. 1998.

[5] J. M. Hergenrother *et al.*, "The vertical replacement-gate (VRG) MOSFET: A 50-nm vertical MOSFET with lithography-independent gate length," *IEDM Tech. Dig.*, pp. 75–78, 1999.

[6] T. Schulz, W. Roesner, L. Risch, A. Korbel, and U. Langmann, "Short channel vertical sidewall MOSFETs," *IEEE Trans. Electron Devices.*, vol. 48, p. 1783, Aug. 2001.

[7] Y.-K. Choi, T.-J. King, and C. Hu, "Nanoscale CMOS spacer FINFET for the terabit era," *IEEE Electron Device Lett.*, vol. 23, pp. 25–27, Jan. 2002.

[8] M. Kumar, H. Liu, and J. K. O. Sin, "A high-performance five-channel NMOSFET using selective epitaxial growth and lateral solid phase epitaxy," *IEEE Electron Device Lett.*, vol. 23, pp. 261–263, May 2002.

[9] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 18, pp. 74–76, Feb. 1997.

[10] D. C. Donaghy, S. Hall, V. D. Kunz, C. H. de Groot, and P. Ashburn, "Investigating 50 nm channel lenght vertical MOSFETs containing a dielectric pocket, in a circuit environment," in *Proc. ESSDERC Conf.*, 2002, pp. 499–502.

[11] M. Jurczak, E. Josse, R. Gwoziecki, M. Paoli, and T. Skotnicki, "Investigation on the suitability of vertical MOSFETs for high speed (RF) CMOS applications," *in Proc. ESSDERC*, pp. 172–175, 1998.

[12] C. K. Lau, H. Shibata, M. Saitoh, T. Matsuno, S. Samata, H. Itoh, H. Sasaki, and K. Hashimoto, "A super self-aligned source/drain MOSFET," *IEDM Tech. Dig.*, pp. 358–361, 1987.

[13] V. D. Kunz, C. H. de Groot, and P. Ashburn, "Method for local oxidation in vertical semiconductor devices using fillets," U.K. Patent 0 128 414.0, Nov. 2001.

[14] B. Goebel, D. Schumann, and E. Bertagnolli, "Vertical n-channel MOSFETs for extremely high density memories: The impact of interface orientation on device performance," *IEEE Trans. Electron Devices*, vol. 48, pp. 897–906, May 2001.

[15] Silvaco International. (1995) Analysis and calibration of LOCOS simulation using VWF. Tech. Rep.. [Online]. Available: http://www.silvaco.com/applications/archive/-aug95a3/aug95a3.html

[16] P. Ferreira, V. Senez, D. Collard, and B. Baccus, "Study of local silicon oxidation with calibrated nitride model," in *Proc. ESSDERC'94*, 1994, pp. 259–262.

[17] S. M. Hu, "Stress-related problems in silicon technology," *J. Appl. Phys.*, vol. 70, pp. r53–r80, 1991.

[18] H. Matsumoto and M. Fukuma, "Numerical modeling of nonuniform si thermal oxidation," *IEEE Trans. Electron. Devices*, vol. ED-32, pp. 132–140, Feb. 1985.

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