

Hot-Carrier Stressing of NPN Polysilicon Emitter Bipolar Transistors Incorporating Fluorine

S. R. Sheng, W. R. McKinnon, S. P. McAlister, C. Storey, J. S. Hamel, and P. Ashburn

Abstract—The effects of fluorine on the hot-carrier induced degradation in low-thermal-budget polysilicon-emitter NPN bipolar transistors have been examined. Forward Gummel plots, base-emitter (BE) diode characteristics, and stress currents were measured during reverse BE bias stress. Fluorinated devices behave similarly under stress to nonfluorinated devices retaining the initial improvement observed in the forward-bias base current, which is due to suppression of recombination in the BE junction depletion regions at the oxide/silicon interface. The benefits of fluorination, and particularly the reduction in base current in fluorinated devices, appear to be robust—that is, there is no evidence that the defects passivated by fluorine are reactivated during stressing, or that fluorination introduces additional defects that are activated under stressing.

Index Terms—Fluorination, hot carriers, polysilicon bipolar junction transistor (BJT), reliability.

I. INTRODUCTION

Hot-carrier induced degradation is one of the most serious problems in the reliability of bipolar junction transistors (BJTs). The reliability issue arises when the base-emitter (BE) junction is reverse biased, as in the normal BiCMOS circuit operation [1]. Extensive investigations of the effect [2] have identified that this degradation is mainly caused by injection of energetic holes and/or electrons into the oxide surrounding the BE junction and at the oxide/silicon interface. This leads to the generation of interface traps and damage at the oxide/silicon interface near the high field BE junction.

The interface traps are believed to be generated by hot carriers, through the breaking of weak interface bonds. The breaking of Si–H bonds has been suggested [3] as one of the important mechanisms for the trap generation, because hydrogen is weakly bonded to silicon and has relatively high mobility at the oxide/silicon interface. One approach to improving resistance to stressing is to replace the weakly bonded hydrogen with an element that forms stronger bonds to silicon. Fluorine, being the most electronegative of the elements, is a good candidate, and so has been incorporated into unipolar (e.g., CMOS) devices to improve the device reliability [4]–[6]. Overall, fluorine has a positive effect. An appropriate amount of fluorine can passivate hydrogen-related sites that are precursors to interface trap generation [4]. Fluorination replaces the weak Si–H bonds by Si–F bonds and relaxes strain at the oxide/silicon interface, reducing generation of interface traps and oxide trapped charges during hot-carrier injection or ionizing radiation [5]. Detrimental effects of the fluorine incorporation, however, have also been observed. These include enhancement of boron diffusion in oxide [7] and negative charge trapping at high electric fields [8], as well as generation of additional traps for Si interstitials [7]—all of which may lead to poor dielectric quality and device reliability [4], [7], [8].

Manuscript received October 10, 2002. The review of this paper was arranged by Editor J. N. Burghartz.

S. R. Sheng, W. R. McKinnon, S. P. McAlister, and C. Storey are with Device Physics, Institute for Microstructural Sciences, National Research Council of Canada, Ottawa, ON K1A 0R6, Canada (e-mail: Shuran.Sheng@nrc.ca).

J. S. Hamel is with the Department of Electrical and Computer Engineering, University of Waterloo, Waterloo, ON N2L 3G1, Canada.

P. Ashburn is with the Department of Electronics and Computer Science, University of Southampton, Southampton, SO9 5NH, U.K.

Digital Object Identifier 10.1109/TED.2003.812502

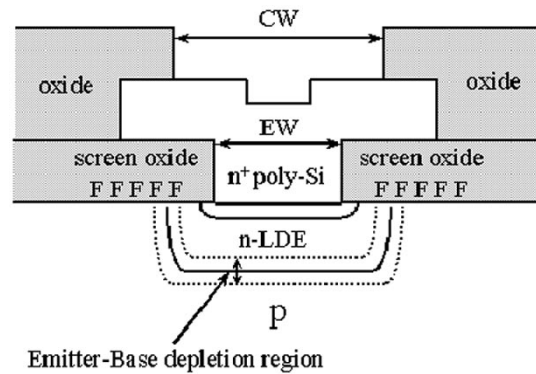


Fig. 1. Schematic cross section of the polysilicon emitters of NPN BJTs.

The effects of fluorine on the reliability of bipolar transistors (e.g., BJTs and HBTs) are not well documented. Recent interest in the impact of fluorine in silicon-based transistors has been mainly focused on two related beneficial effects of fluorine implantation into the polysilicon emitters [9]–[14]: 1) enhancement in break-up of the interfacial oxide layer at a lower temperature; and 2) suppression of recombination in the BE junction depletion regions through passivation of surface states at the oxide/silicon interface. It is the second effect that prompted us to investigate whether fluorination leads to improved resistance to hot-carrier stressing, or whether the initial improvement is lost. Here, we present data of the hot-carrier stressing of polysilicon-emitter NPN BJTs implanted with fluorine, and compare them with nonimplanted devices.

II. DEVICE AND EXPERIMENTAL DETAILS

The devices studied in this paper are self-aligned NPN BJTs with polysilicon emitters, fabricated in a simple conventional procedure [9], [12], [13]. The base and low-doped emitter (LDE) were produced by implanting boron and phosphorus, respectively, into (100) Czochralski n-on-n⁺ epitaxial silicon wafers through an 80 nm screen oxide formed by a thermal oxidation in dry O₂ at 1100 °C. The phosphorus was implanted through an emitter window (EW) in photoresist. After the implant the screen oxide in the EW was removed, and the surrounding screen oxide remained as the isolation oxide at the emitter perimeter. Immediately prior to polysilicon emitter deposition, the wafers were subjected to an HF interface treatment, which leads to a surface oxide layer of ~4 Å thick, and then nominally 200 nm polysilicon was deposited at 610 °C. Fluorine was then implanted at 30 keV in two stages to give two different doses, $1 \times 10^{15} \text{ cm}^{-2}$ and $5 \times 10^{15} \text{ cm}^{-2}$, in opposite quarters of each wafer. Wafers were subjected to an interface anneal for 30 s at 950 °C following 600 nm LPCVD oxide deposition at 400 °C. The polysilicon emitter was completed by implanting with arsenic, and then performing an emitter drive-in at 900 °C for 30 s. The EW is $6 \times 6 \mu\text{m}^2$ in all the devices reported here. The devices available have various sizes of contact window (CW) to the emitter (4×4 – $12 \times 12 \mu\text{m}^2$). Fig. 1 shows a schematic cross section of the polysilicon emitter.

An HP 4155 Semiconductor Parameter Analyzer was used for device characterization, and also for hot-carrier stressing. The devices, fluorine implanted or not, were subjected to a constant reverse-bias BE voltage stress at room temperature with the collector open. During a stress period, the stress current was continuously monitored to integrate the accumulated stress charge passing through the BE junction. This stress was interrupted periodically for measurements, which included forward Gummel plots and BE diode characteristics.

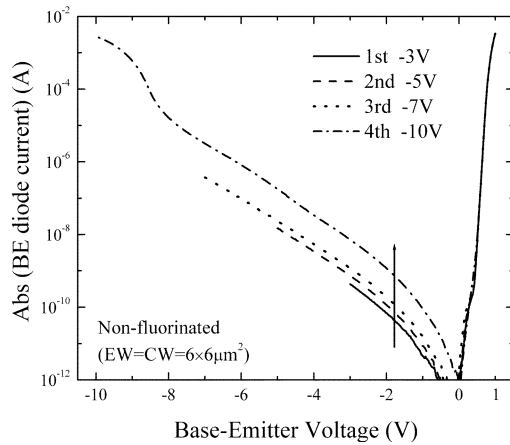


Fig. 2. Typical I - V characteristics of the base-emitter junction at room temperature for a nonfluorinated Si BJT device. The reverse-bias voltage was extended successively from -3 to -10 V for each sweep measurement.

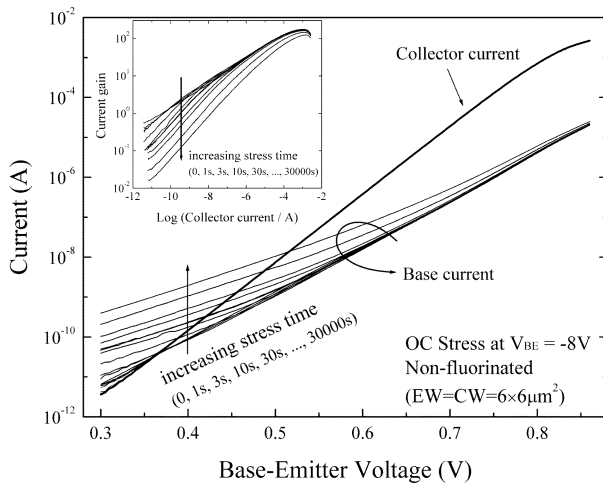


Fig. 3. Typical Gummel plot variations during reverse BE bias stressing at -8 V for a nonfluorinated device. The inset shows stress-induced changes in the collector current dependent gain.

III. RESULTS

Fig. 2 shows typical I - V characteristics of the BE junction at room temperature for a nonfluorinated Si BJT device. The reverse characteristics were measured by extending the reverse-bias limit successively from -3 to -10 V. There is a strong field dependent leakage current in the reverse-bias regime; the avalanche breakdown occurs at approximately -9 V. As each curve is measured, the device appears to be stressed enough during the sweep that the current at a given bias is increased on the subsequent curve. This increase is most noticeable in reverse-bias.

For both nonfluorinated and fluorinated devices, little degradation in device characteristics was observed after stressing at lower than -6 V for up to 3×10^4 s, due to the low reverse BE leakage currents. These currents are low because of the relatively large device dimensions and low doping levels in the base ($10^{17} \sim 10^{18} \text{ cm}^{-3}$), leading to lower perimeter electric fields than found in state-of-the-art small emitter Si BJTs. A higher reverse-bias voltage of -8 V was, therefore, applied for the hot-carrier stressing studies.

Fig. 3 shows typical Gummel plot variations during reverse bias stressing at -8 V for a nonfluorinated Si BJT device. With increasing stress time, the base current, particularly in the low-bias region, in-

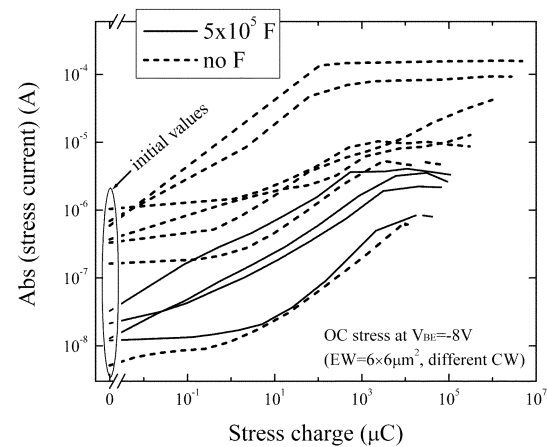


Fig. 4. Impact of fluorine on stress currents I_{ST} at -8 V versus stress charge Q_{ST} . All the nonfluorinated and fluorinated devices have the same EW dimension ($6 \times 6 \mu\text{m}^2$), some of them have different CW dimensions, ranging from $4 \times 4 \mu\text{m}^2$ to $12 \times 12 \mu\text{m}^2$, as shown in the figure.

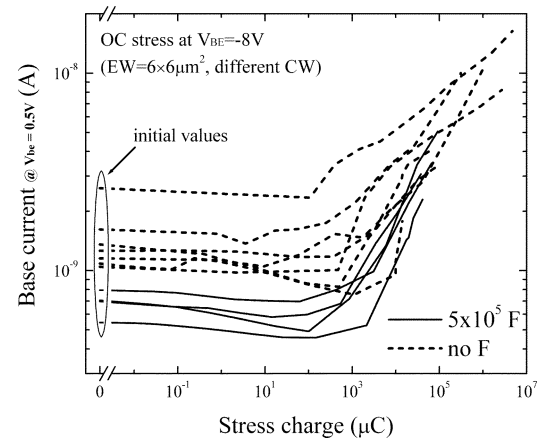


Fig. 5. Impact of fluorine on the base currents I_B at low bias (0.5 V) versus Q_{ST} for the same devices shown in Fig. 3.

creases considerably, whereas the collector current is not affected. This gives rise to a drop in the current gain at low currents (see the inset), consistent with previous reports [15]. The BE diode characteristics were also degraded by this long-term stressing. The reverse leakage current increases with increasing stress time, similar to the changes in reverse bias shown in Fig. 2. Moreover, the forward leakage current increases too, as is normally observed [15]. Significant increases occur at low reverse- and forward-bias. Since the stress current varies during the constant reverse-bias voltage stressing, the accumulated stress charge Q_{ST} rather than time was used as a measure of stress progression, for comparison of the devices with and without fluorine.

Fig. 4 shows the variation of the stress currents I_{ST} at -8 V versus Q_{ST} . The data points at zero Q_{ST} are the initial values of I_{ST} . The results for $1 \times 10^{15} \text{ cm}^{-2}$ fluorinated devices are not shown, but were similar to those for the nonfluorinated devices. With increasing Q_{ST} , I_{ST} increase for both the nonfluorinated and fluorinated devices, and in most cases reaches saturation after $\sim 5 \times 10^3 \mu\text{C}$. The starting values of I_{ST} vary considerably between the devices, whether the devices are fluorinated or not.

Fig. 5 shows the effect of fluorine on the low-bias base currents I_B at $V_{BE} = 0.5$ V versus Q_{ST} for the same devices shown in Fig. 4. The scatter in I_B between the devices is at least a factor 10 less than the scatter in I_{ST} . The initial values of I_B of all fluorinated devices

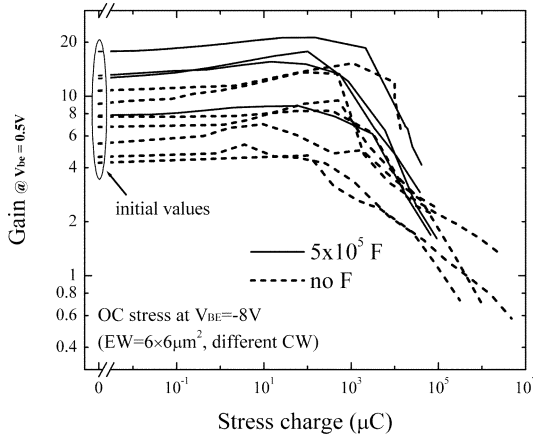


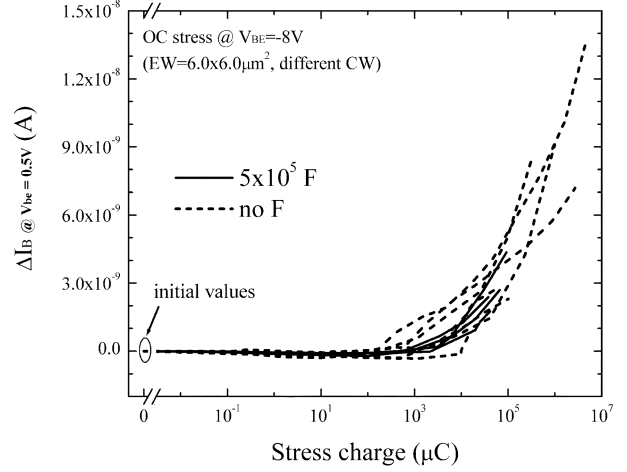
Fig. 6. Impact of fluorine on the gain degradation at low bias (0.5 V).

are lower than those of nonfluorinated devices. This improvement in I_B due to the reduced nonideal base current component was reported for a larger number of samples in [12], [13] than studied here, and was attributed to suppression of recombination in the BE junction depletion regions at the oxide/silicon interface [9]–[14]. This suppression of I_B by fluorine incorporation leads to improved gain, as shown in Fig. 6. In all cases I_B begins to increase for Q_{ST} in the range of 10^2 μC to 10^4 μC , whether the device is fluorinated or not, and then degrades at roughly the same rate with Q_{ST} ($>10^4$ μC). There is no evidence that I_B degrades earlier or more in fluorinated devices than in nonfluorinated ones.

IV. DISCUSSION

Hot-carrier stressing can cause degradation in BJT characteristics by at least two mechanisms [2]. First, it can break weak interface bonds to create defects N_{it} that provide sites for recombination or for trap-assisted tunneling. Second, stressing can inject charge into the oxide surrounding the BE junction, and this charge build-up can modify the depletion region, changing both the field and depletion width [16]. Oxide charge build-up is negligible for low values of Q_{ST} in tunneling regime stress [17], whereas the degradation is driven by generation of fast interface traps. Only for a large amount of Q_{ST} , or in avalanche regime stress, are the capture cross sections larger and the average energy of hot carriers higher. This can lead to significant positive charge trapping into the oxide close to the silicon interface. Consequently, it seems unlikely that changes in the field due to charge trapping are enough to account for an increase in the stress current I_{ST} by several orders of magnitude within low Q_{ST} ($\sim 10^4$ μC), so it is likely that trap-assisted tunneling dominates I_{ST} [18], [19]. For the low-bias base current in the Gummel plot, it likely results from Shockley–Read–Hall (SRH) recombination in the depletion region via trap states. The defects responsible for increasing I_{ST} and I_B are often attributed to be located at the oxide/silicon interface, where the stress is expected to produce damage [2].

The stress current I_{ST} varies during stress progression differently than the changes in I_B . With increasing Q_{ST} , I_{ST} increases, then saturates, while I_B does not saturate up to the maximum Q_{ST} measured. The difference in the behaviors of I_{ST} and I_B implies that the defects involved in determining I_{ST} may be not the same defects as those involved in determining I_B . The other possibility is that after I_{ST} reaches saturation for $Q_{ST} > 5 \times 10^3$ μC , the charge trapping becomes appreciable so that the surface potential ψ_s is raised significantly, leading to further increase in I_B that is a function of both N_{it} and ψ_s [2].

Fig. 7. Impact of fluorine on the rate of degradation in the base current ΔI_B .

Here, we are interested in the defects associated with increasing I_B , since they result in a degraded gain. The contributions to I_B can be written as follows:

$$I_B^{NF} = I_{B0}, \quad \text{nonfluorinated device before stressing} \quad (1)$$

$$I_B^{NF} = I_{B0} + I_{BS} \quad (2)$$

nonfluorinated device after stressing

$$\Delta I_B^{NF} = I_{BS} \quad (3)$$

stress-induced changes for nonfluorinated device

$$I_B^F = I_{B0} - I_{BF}, \quad \text{fluorinated device before stressing} \quad (4)$$

$$I_B^F = I_{B0} - I'_{BF} + I'_{BS} \quad (5)$$

fluorinated device after stressing

$$\Delta I_B^F = I'_{BS} + (I_{BF} - I'_{BF}) \quad (6)$$

stress-induced changes for fluorinated device

where I'_{BF} accounts for the possibility that stressing could remove the benefits of the fluorine (and hence change the value of I_{BF}), and I'_{BS} accounts for the possibility that the effects of stressing may be different in fluorinated and nonfluorinated devices. Expressions (5) and (6) indicate the two ways that fluorination and stressing can interact. First, stressing could remove the benefits of fluorine, reducing I_{BF} before stressing to I'_{BF} after stressing. For instance, some Si–F bonds resulting from the defects passivated by F may be strained and weakened due to poor fluorine microstructure, such as a clustered fluorine phase. These strained Si–F bonds might be unstable under stressing. Second, fluorination can change the resistance of the device to stressing, making I'_{BS} either smaller or larger than I_{BS} . Since only a small fraction (1 : 100) of the incorporated fluorine play a role of terminating the silicon dangling bonds (also known as P_b centers) at the SiO_2/Si interface [20], the rest of the fluorine can passivate other defects (e.g., hydrogen-related sites and oxygen vacancies) and relax the strain at the oxide/silicon interface through breaking weak or strained bonds to form much stronger Si–F bonds with different configurations [5]. This consequently could result in lower densities of both the interface traps and their precursors, and hence, improved hot-carrier resistance for appropriately fluorinated devices (i.e., $I_{BS} < I'_{BS}$). However, when excess fluorine is incorporated, the device reliability is expected to get worse

again ($I'_{BS} > I_{BS}$) due to too many nonbridging oxygen bonds and poor fluorine microstructure created [5], which is known to be harmful to the oxide reliability.

For clarity, ΔI_B^{NF} and ΔI_B^F versus Q_{ST} are shown in Fig. 7. From Figs. 5 and 7, we see that at low Q_{ST} , the terms I_{BS} and I'_{BS} are much smaller than the term I_{BF} . No evidence was found for any reduction in I_{BF} to I'_{BF} at low Q_{ST} , because the fluorinated devices begin to degrade at about the same value of Q_{ST} as the nonfluorinated devices do. Therefore, we can conclude that the reduction in I_B due to fluorination is robust enough to resist stressing at low Q_{ST} . At large Q_{ST} , however, the situation is more complicated because the terms I_{BS} and I'_{BS} become larger and dominate I_B . Within the scatter in the results, there is no evidence that ΔI_B^F (or I'_{BS}) differs from ΔI_B^{NF} (or I_{BS}), neither is it clear whether there is any change in I_{BF} at large Q_{ST} since it would be masked by the dominating components I_{BS} and I'_{BS} . It appears that fluorination at the levels used does not improve the resistance to stressing in the devices studied here, but neither does it make the devices degrade more easily under stressing.

In summary, it appears that the defects passivated by fluorine are not reactivated under electrical stressing. The fluorine incorporation in our devices seems not to introduce additional defects that are activated under stressing, indicating no adverse effect is imposed by fluorination on device reliability. Detailed measurements on devices with smaller emitters and high base doping levels are required to confirm whether the advantages of fluorine would extend to state-of-the-art devices with emitter widths $< 1 \mu\text{m}$ and base doping over 10^{19} cm^{-3} . Furthermore, we suspect that the lack of improved resistance to hot-carrier stressing in fluorinated BJT devices is related to the fluorine microstructure and distribution at the silicon/oxide interface.

REFERENCES

- [1] D. Burnett and C. Hu, "Modeling hot-carrier effects in polysilicon emitter bipolar transistors," *IEEE Trans. Electron Devices*, vol. 35, pp. 2238–2244, Dec. 1988.
- [2] L. Vendrame, P. Pavan, G. Corva, A. Nardi, A. Neviani, and E. Zanoni, "Degradation mechanisms in polysilicon emitter bipolar junction transistors for digital applications," *Microelectron. Reliab.*, vol. 40, pp. 207–230, Feb. 2000 and references therein.
- [3] C. Hu, S. C. Tam, F. C. Hsu, P. K. Ko, T. Y. Chan, and K. W. Terrill, "Hot-electron-induced MOSFET degradation-model, monitor, and improvement," *IEEE Trans. Electron Devices*, vol. ED-32, pp. 375–385, Feb. 1985.
- [4] T. B. Hook, E. Adler, F. Guarini, J. Lukaitis, N. Rovedo, and K. Schroefer, "The effects of fluorine on parametrics and reliability in a 0.18- μm 3.5/6.8 nm dual gate oxide CMOS technology," *IEEE Trans. Electron Devices*, vol. 48, pp. 1346–1353, July 2001.
- [5] T. P. Ma, "Metal-oxide-semiconductor gate oxide reliability and the role of fluorine," *J. Vac. Sci. Technol. A*, vol. 10, pp. 705–712, July–Aug. 1992.
- [6] N. Kasai, P. J. Wright, and K. C. Saraswat, "Hot-carrier-degradation characteristics for fluorine-incorporated nMOSFET's," *IEEE Trans. Electron Devices*, vol. 37, pp. 1426–1431, June 1990.
- [7] H.-H. Vuong, H.-J. Gossmann, C. S. Rafferty, H. S. Luftman, F. C. Unterwald, D. C. Jacobson, R. E. Ahrens, T. Boone, and P. M. Zeitzoff, "Influence of fluorine implant on boron diffusion: Determination of process modeling parameters," *J. Appl. Phys.*, vol. 77, pp. 3056–3060, April 1995.
- [8] G. Ghidini, C. Clementi, D. Drera, and F. Murgain, "The impact of F contamination induced by the process on the gate oxide reliability," *Microelectron. Reliab.*, vol. 38, pp. 255–258, Feb. 1998.
- [9] N. Siabi-Shahrivar, W. Redman-White, P. Ashburn, and H. A. Kemhadjian, "Reduction of $1/f$ noise in polysilicon emitter bipolar transistors," *Solid State Electron.*, vol. 38, pp. 389–400, Feb. 1995.
- [10] N. E. Moiseiwitsch and P. Ashburn, "The benefits of fluorine in pnp polysilicon emitter bipolar transistors," *IEEE Trans. Electron Devices*, vol. 41, pp. 1249–1256, July 1994.
- [11] C. R. Bolognesi and M. B. Rowlandson, "Impact of fluorine incorporation in the polysilicon emitter of NPN bipolar transistors," *IEEE Electron Device Lett.*, vol. 16, pp. 172–174, May 1995.
- [12] F. J. W. Schiz, "The effect of fluorine in low thermal budget polysilicon emitters for SiGe heterojunction bipolar transistors," Ph.D. dissertation, Univ. Southampton, U.K., 1999.
- [13] F. J. W. Schiz and P. Ashburn, "Improved base current ideality in polysilicon emitter bipolar transistors due to fast fluorine diffusion through oxide," *Electron. Lett.*, vol. 35, pp. 752–753, April 1999.
- [14] N. Lukyanchikova, N. Garbar, M. Petrichuk, J. F. W. Schiz, and P. Ashburn, "The influence of BF_2 and F implants on the $1/f$ noise in SiGe HBT's with a self-aligned link base," *IEEE Trans. Electron Devices*, vol. 48, pp. 2808–2815, Dec. 2001.
- [15] D. R. Collins, "Excess current generation due to reverse bias p-n junction stress," *Appl. Phys. Lett.*, vol. 13, pp. 264–266, Oct. 1968. " \hbar_{FE} degradation due to reverse bias emitter-base junction stress," *IEEE Trans. Electron Devices*, vol. ED-16, pp. 403–406, Apr. 1969.
- [16] S. L. Kosier, R. D. Schrimpf, R. N. Nowlin, D. M. Fleetwood, M. DeLaus, R. L. Pease, W. E. Combs, A. Wei, and F. Chai, "Charge separation for bipolar transistors," *IEEE Trans. Nucl. Sci.*, pt. 1, vol. 40, pp. 1276–1285, Dec. 1993.
- [17] A. Neviani, P. Pavan, A. Nardi, A. Chantre, L. Vendrame, and E. Zanoni, "Hot-carrier degradation and oxide charge build-up in self-aligned etched-polysilicon npn bipolar transistors," *IEEE Trans. Electron Devices*, vol. 44, pp. 2059–2063, Nov. 1997.
- [18] G. A. M. Hurkx, D. B. M. Klaassen, M. P. G. Knuvers, and F. G. O'Hara, "A new recombination model describing heavy-doping effects and low-temperature behavior," in *IEDM Tech. Dig.*, 1989, pp. 307–310.
- [19] G. A. M. Hurkx, H. C. de Graaff, W. J. Kloosterman, and M. P. G. Knuvers, "A new analytical diode model including tunneling and avalanche breakdown," *IEEE Trans. Electron Devices*, vol. 39, pp. 2090–2098, Sept. 1992.
- [20] Y. Ono, M. Tabe, and Y. Sakakibara, "Segregation and defect termination of fluorine at SiO_2/Si interfaces," *Appl. Phys. Lett.*, vol. 62, pp. 375–377, Jan. 1993.