block coded 4CFPM and 8CFPM are found to significantly outperform the block coded 2FSK/8PSK and 2FSK/16PSK, respectively.

Digital computer simulation was also conducted to investigate the bit error probability characteristics of the considered block coded LCFPM schemes for moderate signal to noise power ratios. Multi-stage soft-decision decoding is adopted in simulation [6]. It was found by the authors that the practical coding gains achieved at the bit error probability of 10^{-5} are around 1–2 decibels less than the corresponding asymptotic coding gains.

Conclusion: Block coding of LCFPM modulated signals is investigated in this Letter. It is analytically shown that the block coded LCFPM is competitive, and in some cases superior, in power efficiency to the block coded 2FSK/2LPSK providing the same bandwidth efficiency.

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5 June 2002
Electronics Letters Online No: 20021096
DOI: 10.1049/el:20021096

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Iterative soft sequential estimation assisted acquisition of *m*-sequences

Lie-Liang Yang and L. Hanzo

A novel iterative soft sequential-estimation (ISSE) method is proposed for the acquisition of *m*-sequences. The ISSE algorithm is designed based on the principle of iterative soft-in-soft-out (SISO) decoding. The employment of the proposed ISSE acquisition scheme is particularly beneficial for the acquisition of long *m*-sequences. Results demonstrate that a chip signal-to-noise ratio reduction of ~10 dB is achievable at an erroneous acquisition probability of 10^{-4}.

Introduction: The sequential estimation acquisition arrangement proposed by Ward [1] constitutes one of the simplest acquisition schemes. In this acquisition scheme S consecutive chips of the received noise contaminated m-sequence have to be correctly estimated, in order to acquire an m-sequence having a period of $N=2^S-1$. This is because the S number of correctly detected consecutive chips uniquely describe the m-sequence of period N and hence are sufficient for the local m-sequence generator to produce a locally synchronised despreading m-sequence replica. In this Letter we invoke the iterative SISO decoding principle originally developed for turbo channel decoding [2, 3] for the sake of improving the reliabilities associated with deciding upon the S consecutive chips.

ISSE acquisition algorithm: The schematic diagram of the proposed ISSE acquisition scheme is shown in Fig. 1, which includes four fundamental building blocks, namely an m-sequence generator, a soft-chip-register, a SISO decoder and a code phase tracking loop. The soft-chip-register has the same S number of delay-units—which we refer to as soft-chip-delay-units (SCDUs)—as the m-sequence generator. The SCDUs store the instantaneous log-likelihood ratio (LLR) values of S consecutive chips. With the aid of these S number of LLR values, S number of consecutive chips can be determined after the thresholding operation of $\lessgtr 0$ of Fig. 1, which are then loaded into the corresponding delay-units of the m-sequence generator of Fig. 1. The SISO decoder estimates the corresponding LLR soft output after receiving a soft channel output sample associated with a given chip of the m-sequence. In addition to the so-called intrinsic information of this chip, which was received from the channel, the SISO decoder also exploits the so-called *a-priori* (extrinsic) information related to the chip considered, which is provided by the previously decoded LLR values stored in the SCDUs of Fig. 1. The extrinsic information related to a chip and provided by the surrounding chips conveys related information, because the generator polynomial of the m-sequence imposes constraints on the consecutive chips in a similar fashion to a convolutional encoder. The soft output of the SISO decoder is then shifted to the left-most position of the SCDUs in the soft-chip-register, while the soft value in the right-most SCDUs is shifted out and discarded.

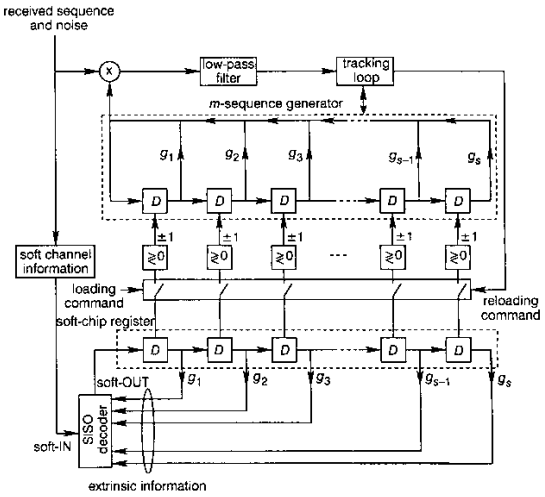

Fig. 1 *Schematic diagram of proposed iterative soft sequential estimator*

In the context of the iterative decoding principle [3], the soft input information is derived from the channel outputs. Let $Z_0, Z_1, Z_2, \ldots$ be the channel outputs, which correspond to the transmitted chips $c_0, c_1, c_2, \ldots$. The soft input information in terms of c_i entered into the SISO decoder is the LLR of c_i conditioned on the channel output Z_i, $i=0, 1, 2, \ldots$, which is given by [3, (15)]

$$L(c_i|Z_i) = L_c \cdot Z_i + L(c_i), \quad i = 0, 1, 2, \ldots, \tag{1}$$

where $L_c = 4\alpha_i \cdot E_c/N_0$, α_i denotes the fading amplitude associated with the transmission of chip c_i over a fading channel, while we have $\alpha_i = 1$ for an AWGN channel. Explicitly, L_c is referred to as the reliability value of the channel. In (1) $L(c_i)$ is the LLR of a random variable c_i, which is defined as [3] $L(c_i) = \log(P(c_i = +1)/P(c_i = -1))$ for $i = 0, 1, 2, \ldots$. $L(c_i) = 0$, if we have no *a-priori* information related to c_i.

Let the previous S number of soft outputs of the SISO decoder be $L(y_{i-1})$, $L(y_{i-2}), \ldots, L(y_{i-S})$. Let us assume furthermore that the m-sequence's generator polynomial is $g(D) = 1 + D^{s_1} + D^{s_2} + \cdots + D^{s_i} + \cdots + D^{s_M = S}$. Then, the extrinsic information used for enhancing the correct decoding probability of c_i can be approximately expressed as [3, (12)]

$$L_e(c_i) \simeq \left[\prod_{m=1}^{M} \operatorname{sign}\left(L(y_{i-s_m})\right)\right] \times \min\{|L(y_{i-s_1})|, \quad |L(y_{i-s_2})|, \ldots, |L(y_{i-(s_M=S)})|\}, \quad i = 0, 1, 2, \ldots, \tag{2}$$

where we assumed that we have $L_e(c_{-\infty}) = \cdots = L_e(c_{-2}) = L_e(c_{-1}) = 0$.

Finally, with the aid of the channel output information of (1) and the extrinsic information $L_e(c_i)$ of (2), the soft output of the SISO decoder

associated with chip c_i can be expressed as

$$L(y_i) = L(c_i|Z_i) + L_e(c_i)$$
$$= L_c \cdot Z_i + L(c_i) + \left[\prod_{m=1}^{m} \text{sign}\,(L(y_{i-s_m}))\right] \times \min\{|L(y_{i-s_1})|, |L(y_{i-s_2})|, \ldots, |L(y_{i-(s_M=S)})|\}, \quad i = 0, 1, 2, \ldots . \quad (3)$$

Eqn (3) represents an iterative equation for estimating the S number of consecutive chips required by the receiver's m-sequence generator for producing the full m-sequence. The typical feature of the ISSE acquisition scheme is that it is capable of observing the reliabilities of the S consecutive chips through observing the amplitudes of the LLR values stored in the SCDUs. Based on these chip-reliabilities, the ISSE acquisition scheme can decide, when it should be in the position to activate the 'loading command' for the loading of reliable initial chips into the m-sequence generator. When the erroneous acquisition probability—which is defined as the probability of the event that the m-sequence generator is loaded with one or more erroneous chips—is sufficiently low, namely it is in the region of for example 10^{-4}, the transmitted m-sequence can be acquired with a high probability after the first loading of the initial chips. Therefore, the total acquisition time of the ISSE acquisition scheme can be approximated by the time duration required by the ISSE for carrying out the iterative SISO decoding, in order to reach a sufficiently low erroneous acquisition probability.

Once the m-sequence generator is loaded with sufficiently reliable initial binary chip values, the received spread-spectrum signal can be de-spread using the locally generated m-sequence replica. The de-spread signal is then low-pass filtered and it is forwarded to the code tracking loop of Fig. 1. If the code tracking loop is capable of tracking the phase, the code acquisition process is completed. By contrast, if the tracking loop is incapable of tracking the phase, the code tracking loop activates a 'reloading command', in order to load another group of S consecutive chips into the delay-units of the m-sequence generator This process can be repeated, until successful code tracking is accomplished.

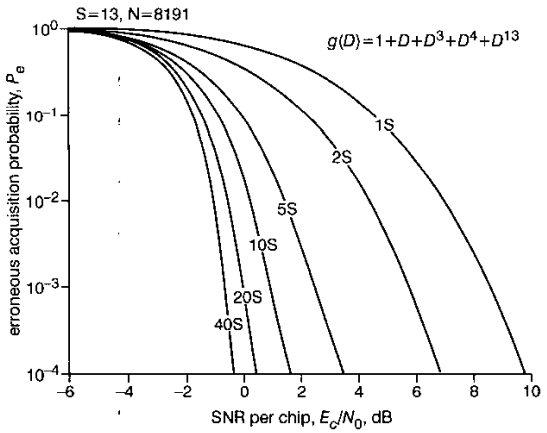

Fig. 2 *Erroneous acquisition probability, P_e, against SNR/chip, E_c/N_0, performance for various numbers of chips invoked into proposed iterative SISO decoder, when transmitting m-sequence generated using generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$ over AWGN channels*

Results: Fig. 2 shows the acquisition performance for a long m-sequence having a period of $N = 8191$ chips, which was generated by a thirteen-stage ($S = 13$) generator using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$. As shown in Fig. 2, the m-sequence can be reliably acquired at an SNR per chip value of $E_c/N_0 = -0.5$ dB by loading about $L = 40S = 40 \times 13 = 520$ chips into the iterative SISO decoder. By contrast, without using any *a-priori* information, i.e. using the conventional sequential estimation acquisition scheme of [1], the acquisition scheme has to operate at the SNR per chip value of $E_c/N_0 = 9.5$ dB, in order to achieve the erroneous acquisition probability of 10^{-4}. Hence, the SNR per chip gain of the proposed ISSE acquisition scheme over the conventional sequential estimation acquisition scheme is about 10 dB at the erroneous acquisition probability of 10^{-4}, when $L = 520$ chips are loaded into the iterative SISO decoder.

© IEE 2002
12 June 2002
Electronics Letters Online No: 20021095
DOI: 10.1049/el:20021095

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Modified belief-propagation algorithm for decoding of irregular low-density parity-check codes

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A modified belief-propagation algorithm is proposed for decoding of irregular low-density parity-check codes. This algorithm effectively reduces the decoding complexity while achieving a BER performance near to or even better than that of the standard belief-propagation algorithm.

Introduction: Irregular low-density parity-check (LDPC) codes have been proven to be capable of transmitting information over noisy channels with a capacity near to the Shannon limit. However, decoding algorithms for LDPC codes, such as the belief-propagation algorithm, still suffer from a huge amount of computations, especially when a code length is long. Thereby, it is of great interest to further reduce the LDPC decoding complexity with a more efficient decoding scheme.

Unequal protection for variable nodes within an irregular LDPC code provides a possibility to improve the efficiency of the belief-propagation decoding algorithm. As shown in [1], during the decoding procedure, high-degree variable nodes are firstly corrected, providing good information to check nodes, which subsequently provide better information to lower-degree variable nodes, resulting in a correction further for variable nodes with slightly smaller degree, and so on. This intuition motivates us to come up with a modified decoding algorithm that successively terminates the iterations for high-degree variable nodes during the decoding, and then yields a hard-decoding result accordingly. By doing so, a BER performance near to or even better than that of the belief-propagation algorithm may be achieved, while the decoding complexity is effectively reduced.

Proposed decoding algorithm for irregular LDPC codes: With reference to the description in [2], assuming that an ensemble of irregular LDPC codes is constructed with a code length of N bits, a variable node degree distribution of $\lambda(x) = \sum_{i=2}^{d_v} \lambda_i x^{i-1}$, where d_v is the maximum variable degree, and a check-node degree distribution of $\rho(x) = \sum_{i=2}^{d_c} \rho_i x^{i-1}$, where d_c is the maximum check degree, the number of variable nodes of degree i can be computed with the following formula:

$$N_i = N \cdot \frac{\lambda_i/i}{\sum_{i=2}^{d_v} \lambda_i/i} = N \cdot \frac{\lambda_i/i}{\int_0^1 \lambda(x)dx}, \quad 2 \le i \le d_v \quad (1)$$

Likewise, the number of check nodes with degree j can be computed by

$$M_j = M \cdot \frac{\rho_j/j}{\sum_{j=2}^{d_c} \rho_j/j} = M \cdot \frac{\rho_j/j}{\int_0^1 \rho(x)dx}, \quad 2 \le j \le d_c \quad (2)$$