Electrical Characteristics of Single, Double & Surround Gate Vertical MOSFETs with Reduced Overlap Capacitance

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Abstract:

The vertical MOSFET structure is one of the solutions for reducing the channel length of devices under 50nm. Surround gate structures can be realized which offer improved short channel effects and more channel width per unit silicon area. In this paper, a low overlap capacitance, surround gate, vertical MOSFET technology is presented, which uses fillet local oxidation (FILOX) to reduce the overlap capacitance between the gate and the drain on the bottom of the pillar. Electrical characteristics of surround gate n-MOSFETs are presented and compared with results from single gate and double gate devices on the same wafer. The devices show good symmetry between the source on top and source on bottom configuration. The short channel effects of the surround gate MOSFETs are investigated.

1. Introduction

Surround gate vertical MOSFET transistors built on the sidewalls of vertical pillars [1] [2] have been developed for four main reasons:

- surround gate or double gate structures allow more channel width per unit of silicon area; this leads to an increase of the drive current per unit area;
- the gate length is controlled by non-lithographic methods; this allows the realization of shorter channel lengths than using photolithography;
- the better control of the substrate depletion region in thin, fully depleted pillars reduces the short channel effects;
- the gate length is decoupled from the packing density; as a result, long channel transistors (with lower off currents) can be produced without decreasing the number of devices per unit area.

One of the main problems inherent to the vertical layout is the position of the gate contact. The gate is composed of polysilicon fillets that surround the pillar. The contact to the surround gate is created via a polysilicon track that overlaps onto the top of the pillar (Fig. 1). As two different masks are needed for the pillar patterning (Fig. 2a) and the active area definition (Fig. 2b), alignment tolerances must be maintained between these two layers. This results in a large overlap capacitance between the gate track and the source-drain electrodes, which are only separated by a thin gate oxide (Fig. 1a).

Several solutions to this problem have been proposed. In one approach the pillar was selectively grown by epitaxial deposition in a well etched in a previously deposited oxide / polysilicon / oxide stack [3]. Another solution is the Vertical Replacement Gate transistor [4]. Both of these solutions are used in devices in which the channel is defined by epitaxial deposition.

The new FILOX process allows the gate overlap capacitance to be reduced in ion implanted devices and hence it is fully CMOS compatible. This is achieved by a thick oxide layer that reduces significantly the overlap between the gate and both the electrode on the top and on the bottom of the pillar (Fig. 1b).

Working n-MOSFET devices with channel lengths down to 100nm and a gate oxide thickness of 3nm have been realized and characterized, which demonstrate the feasibility of this new approach. Three different layouts have been fabricated on the same wafer: surround gate [5] [6] [7] (Fig. 2, e1), double gate [8] (Fig. 2, e2) and single gate (Fig. 2, e3).

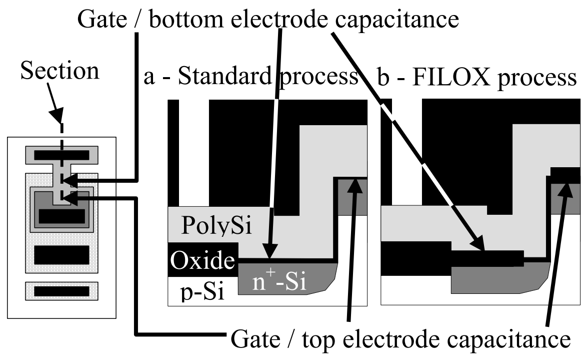

Figure 1. Gate / source-drain overlap capacitance improvement with the FILOX process

2. Device fabrication

The process flow and the mask layout used for the fabrication of the devices are presented in Fig. 2.

Boron-doped (10-33Ωcm) (100) wafers served as the starting material. A p-type body was formed with Boron implantation ($5x10^{14}$ cm^{-2}, 50keV). Then the pillar was defined and patterned by dry etch. A 20nm pad oxide was thermally grown at 900°C to relieve the stress between the ensuing nitride layer and the silicon. Silicon nitride was then deposited to a thickness of 130nm at 740°C (Fig. 2a).

The active area was defined by patterning the nitride layer using an anisotropic dry etch. Then the field oxide was created with a standard LOCOS process, thermally growing a 600nm thick oxide layer at 1000°C (Fig. 2, b1).

At this stage the FILOX (Fillet Local Oxidation) process took place. The nitride layer was dry etched; this resulted in the formation of 130nm wide nitride fillets on the sidewalls of the pillar. Then an oxide layer 60nm thick was thermally grown at 1000°C (Fig. 2, b2). The area protected by the nitride spacers was not affected by the oxide growth; thus a thick oxide layer was formed on the whole active area and on the top of the pillar.

A substrate contact was created with Boron implantation ($5x10^{15}$ cm^{-2}, 47keV). Then the source/drain electrodes were implanted (Arsenic, $6x10^{15}$ cm^{-2}, 150keV); thanks to the presence of the nitride fillets, source and drain were self-aligned to the pillar (Fig. 2c). This was followed by a selective wet etch in orthophosphoric acid in order to remove the nitride fillets. Another wet etch in HF was performed to remove the pad oxide; a precise etch timing removes all pad oxide, leaving an approximately 40nm thick FILOX oxide.

A 3nm gate oxide was thermally grown on the sidewall of the pillar at 900°C. Then a 200nm in-situ doped (Arsenic, $5x10^{19}$ cm^{-3}) polysilicon layer was deposited by LPCVD and patterned by dry etch. In this way polysilicon fillets were created all around the pillar; the polysilicon track connecting the polysilicon fillets to the gate contact was protected from the etch by a resist mask (Fig. 1 and 2d). Another mask was used to selectively remove by isotropic dry etch the remaining polysilicon fillets (Fig. 1e), creating single, double and surround gate devices on the same wafer.

A 600nm thick oxide isolation layer was then deposited and an RTA at 1100°C for 10sec was performed for dopant activation; then contacts were etched and metal deposited and patterned.

3. Pillar Characterisation

The FILOX process provides a gate overlap capacitance that is lower than in the standard process. The reduction in overlap capacitance is achieved by the approximately 40nm thick FILOX oxide layer instead of the 3nm thick gate oxide. Nevertheless this process presents a critical stage. The deposition of a nitride layer on the pillar creates mechanical stress; the pad oxide is essential to reduce this effect.

The SEM cross-section of the active transistor area in Fig. 3 shows that excellent results have been obtained; the gate is clearly separated from the substrate by a thicker oxide layer (see arrows in Fig. 3); this layer begins at a distance of about 130nm from the pillar, corresponding to the nitride fillets thickness. It is possible to distinguish the bird's beaks formed during the FILOX oxidation. These have the advantage of further reducing the overlap capacitance between the top electrode and the gate on the side of the pillar and between the gate and the portion of the bottom electrode beneath the polysilicon fillet at the bottom of the pillar.

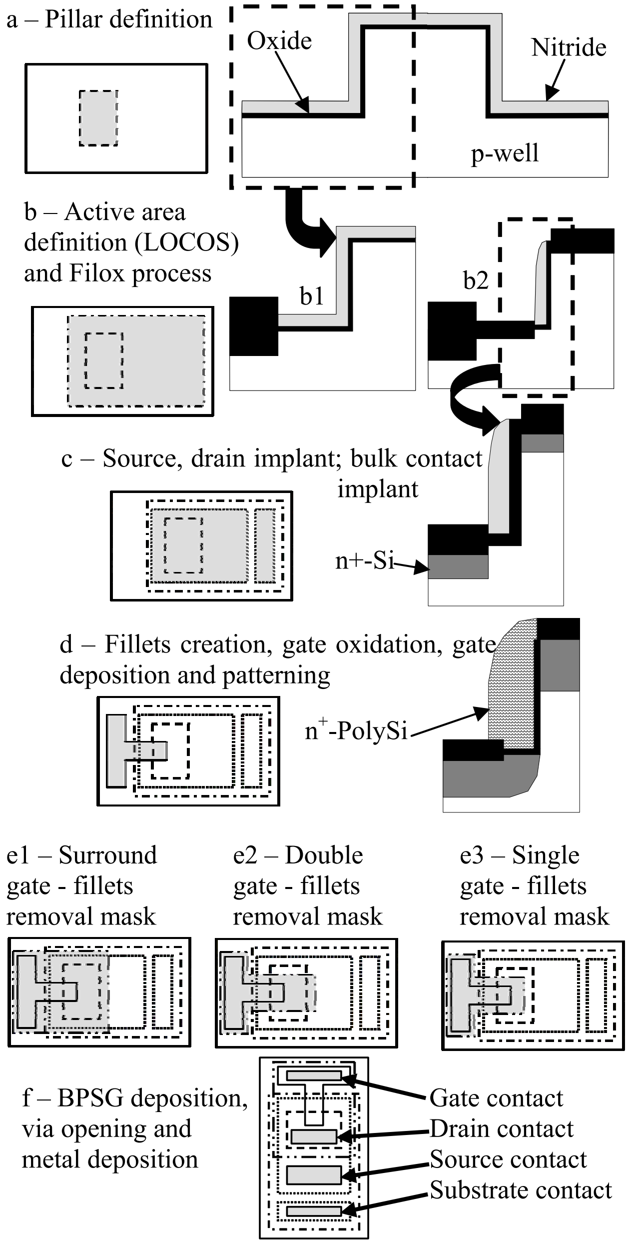

Figure 2. Process flow and layout of the surround gate, double gate and single gate transistors obtained with FILOX process

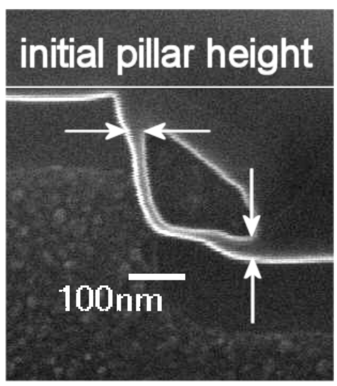

Figure 3. Cross section SEM view of the active transistor area; the pillar was about 290nm in height before the FILOX process; the estimated channel length is 110nm; sample with 6nm gate oxide

4. Electrical Characteristics

Fig. 4, 5 and 6 show the transfer characteristics of surround, double and single gate devices with estimated channel length of 120nm. Fig. 7 shows the output characteristic of the surround gate layout. All results show measurements in both configurations: source on top and source on bottom of the pillar. Very little asymmetry is observed, due to the low series resistances of both electrodes. This is due to the high percentage of activation of the dopants implanted and to the transistor layout that minimises source and drain series resistances.

The best electrical results are achieved with the surround gate layout. This is because in this device the gate fillets cover the whole surface of the pillar and the gate controls the substrate depletion region throughout the pillar perimeter. On the contrary in the double and single gate layouts the areas where the fillets have been removed (Fig. 2, e2 and e3) are not controlled by the gate during the off-state operation of the transistors. This gives rise to an increase of the leakage currents between source and drain.

The subthreshold slopes show a weak dependence on the channel length and on the layout variations; measured values varied between 100 and 120 mV/dec.

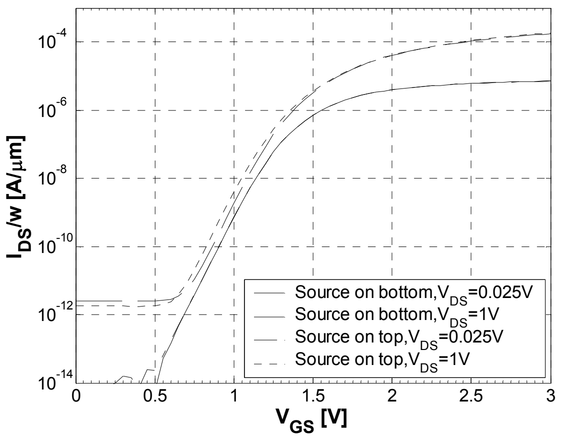

Figure 4. Measured transfer characteristic of a device with a surround gate layout, channel width = 24μm and approximate channel length = 120nm

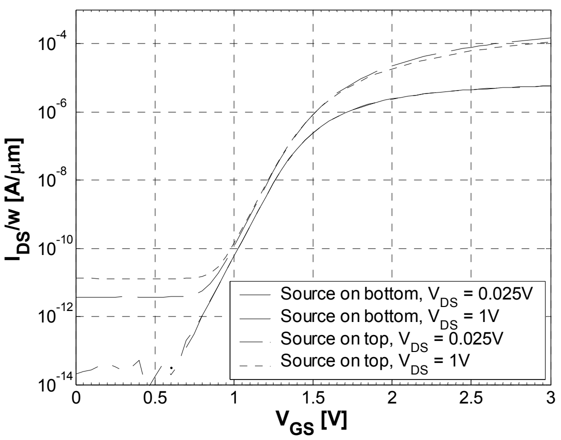

Figure 5. Measured transfer characteristic of a device with a double gate layout, channel width = 9μm and approximate channel length = 120nm

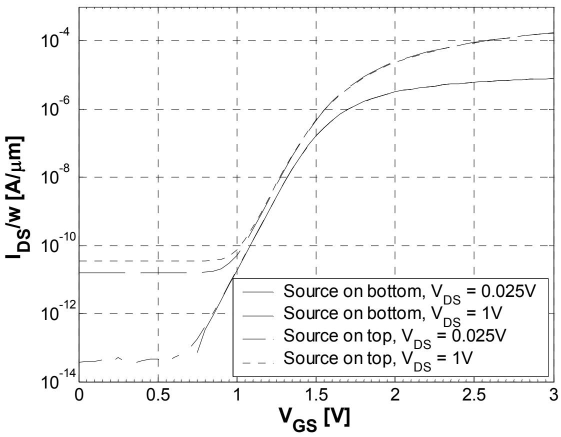

Figure 6. Measured transfer characteristic of a device with a single gate layout, channel width = 4.5μm and approximate channel length = 120nm

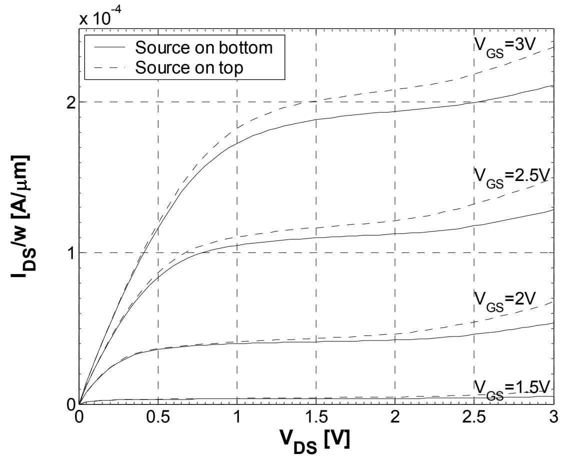

Figure 7. Measured output characteristic of a device with a surround gate layout, channel width = 24μm and approximate channel length = 120nm

5. Short Channel Effects

Due to nonuniformity of the dry etch during the pillar definition process step (Fig. 2a), a distribution of pillar heights has been measured. This results in a variation between 100 and 130nm of the channel length of the devices obtained. An analysis of the short channel effects [9] of the devices has thus been possible.

Fig. 8 shows the measured threshold voltage for the surround gate layout as a function of the channel length. The threshold voltage has been calculated using the Linear Extrapolation method both in the linear (V_{DS} = 0.025V) and in the saturation (V_{DS} = 1V) regions of operation. The results show a decrease in the value of the parameter with decreasing channel length. The difference between the saturation and linear behaviour increases for the shortest channel lengths. This is expected, because for short channel lengths the gate loses control of the substrate depletion region. This short channel effect increases with the drain-source voltage [9].

The measured variation of the on-state drain current for the surround gate layout confirms a strong dependence on the channel length. Fig. 9 shows a decrease of the drain current from 330µA/µm for L = 100nm to 120µA/µm for L = 130nm (current measured with V_{DS}=1V and V_{GS}=3V).

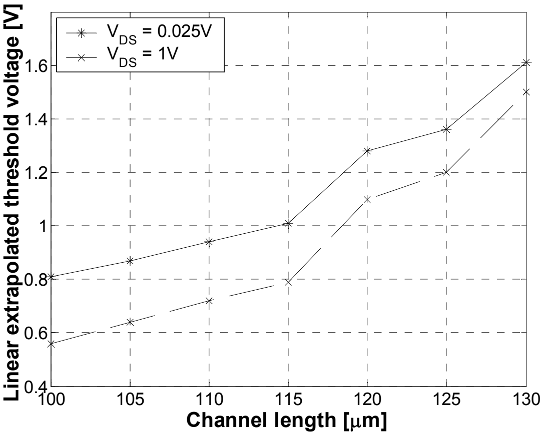

Figure 8. Measured threshold voltage of devices with a surround gate layout and a channel width of 24µm as a function of the estimated channel length

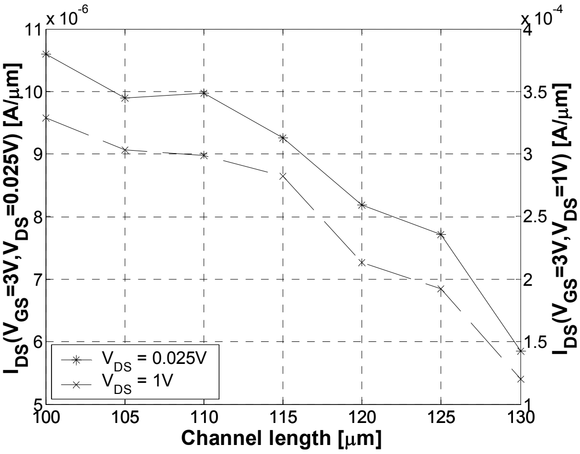

Figure 9. Measured on-state drain current (V_{GS} = 3V) of devices with a surround gate layout and a channel width of 24µm as a function of the estimated channel length

6. Conclusions

Surround, single and double gate vertical MOSFETs have been realized on a single wafer using a new fillet local oxidation (FILOX) process. Channel lengths down to 100nm and a gate oxide 3nm thick have been realized. The FILOX process allows a reduction of the capacitance between the gate and the source/drain of the vertical MOSFET; it has been used with implanted sources and drains and hence is CMOS-compatible.

Electrical results for the single, double and surround-gate layouts have been presented. They show good symmetry between the source on top and source on bottom configuration. The short channel effects of the surround gate MOSFET have been analysed and plots of measured threshold voltage and on-state drain current as a function of the channel length shown. The electrical results demonstrate the feasibility of the FILOX process.

7. Acknowledgements

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8. References

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