Acquisition of m-Sequences Using Recursive Soft Sequential Estimation

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***Abstract*— A novel sequential estimation method is proposed for the initial synchronization of pseudonoise (PN) signals derived from m-sequences. This sequential estimation method is designed based on the principle of iterative soft-in-soft-out (SISO) decoding, and hence we refer to it as the Recursive Soft Sequential Estimation (RSSE) acquisition scheme. The RSSE acquisition scheme exhibits a complexity similar to that of a conventional m-sequence generator, which increases only linearly with the number of stages in the m-sequence generator. Furthermore, our simulation results show that the acquisition time of the proposed RSSE acquisition scheme is also linearly dependent on the number of stages in the m-sequence generator. Hence, the employment of the proposed RSSE acquisition scheme is beneficial for employment in the acquisition of long m-sequences.**

I. Introduction

The sequential estimation acquisition arrangement proposed by Ward [1] constitutes one of the simplest acquisition schemes. The principle of the sequential estimation acquisition scheme is as follows. The acquisition of an m-sequence of length (2^S-1) is deemed successful, provided that S consecutive chips are correctly received by the acquisition device and are loaded into the local m-sequence generator, where successive shifts of the chips in the generator will generate chips that exactly match the forthcoming received chips of the transmitted m-sequence. However, in the presence of noise, one or more of the S consecutive received chips might be in error, potentially resulting in loading erroneous values into the m-sequence generator. In this case a new set of S chips can be processed similarly.

Hence, in sequential estimation [1] the most critical requirement for attaining the successful acquisition of PN sequences is that S consecutive chips of the received noise-contaminated PN sequence have to be correctly estimated. It has been shown that techniques such as majority logic decoding [2] and recursive sequential estimation [3] can be employed for improving the acquisition performance of sequential estimation assisted acquisition schemes. However, all existing sequential estimation based acquisition schemes operate on the basis of hard-decision chips.

In this contribution, we invoke the iterative SISO decoding principle originally developed for turbo channel decoding [4], [5] for improving the reliabilities associated with deciding upon the S consecutive chips loaded into the m-sequence generator. Upon exploiting the inherent properties of m-sequences, a RSSE acquisition scheme is proposed, which estimates S consecutive chips using a recursive SISO decoder. An important feature of the proposed RSSE acquisition scheme is that it exploits the real-time knowledge of the reliabilities associated with the S consecutive chips. This real-time knowledge of the chip-reliabilities increases the probability of successful acquisition of an m-sequence of length (2^S-1), once S consecutive chips have been loaded into the local m-sequence generator. The proposed RSSE acquisition scheme has an algorithmic complexity similar to that of an m-sequence generator. Our simulation results will show that the acquisition time of the RSSE acquisition scheme is a linear function of the number of stages in the m-sequence generator. Therefore, the proposed RSSE acquisition scheme constitutes a promising technique, especially for the acquisition of long m-sequences.

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II. Principle of Sequential Estimation Acquisition

The well-established maximum-length sequences, which are also known as m-sequences are generated using feedback shift registers of the form shown in Fig.1. In Fig.1 D represents a unity time-delay operation, while each of the coefficients, $g_1, g_2, \ldots, g_S$, represents the presence of a connection if it is a 1 or the absence of a connection if it is a 0. Let the output binary sequence be $\ldots, c_{-2}, c_{-1}, c_0, c_1, c_2, \ldots$, where $c_i \in \{+1, -1\}$. Furthermore, we assume that in Fig.1 the coefficients are given by $g_{s_1} = g_{s_2} = \ldots = g_{s_l} = \ldots = g_{s_M=S} = 1$, where s_i is an integer in the range $[1, S]$, while the remaining coefficients are 0. The above configuration corresponds to the generator polynomial of

$$g(D) = 1 + D^{s_1} + D^{s_2} + \ldots + D^{s_l} + \ldots + D^{s_M=S}, \quad (1)$$

where $g(D)$ must be a primitive polynomial [6], i.e., a polynomial that cannot be factorized, in order to generate an m-sequence. Based on the above assumptions, it can be shown that the output symbols of Fig.1 obey the recursive equation expressed as

$$\begin{aligned} c_i &= c_{i-s_1} c_{i-s_2} \cdots c_{i-s_l} \cdots c_{i-(s_M=S)} \\ &= \prod_{m=1}^{M} c_{i-s_m} \text{ for } i = \ldots, -1, 0, 1, \ldots, \end{aligned} \quad (2)$$

where $\prod$ represents the product of the coefficients.

The principle behind the sequential estimation acquisition scheme [1] can be stated as follows. In spread-spectrum communications using m-sequences as spreading sequences, Equation (2) implies that, the chip values c_{i-1}, c_{i-2}, $\cdots$, c_{i-S} can be loaded into the corresponding registers of the m-sequence

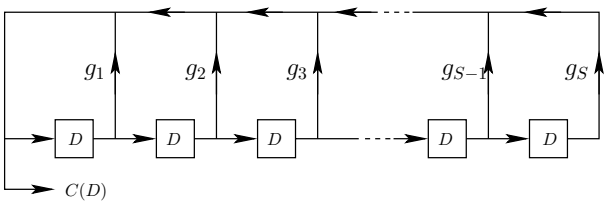

Fig. 1. Maximal-length sequence (m-sequences) generator that outputs binary sequences.

generator at the receiver for generating the forthcoming chips, provided that the receiver has the knowledge of the chip values $c_{i-1},\ c_{i-2},\ \cdots,\ c_{i-S}$ before the transmitter generates the ith chip c_i, on condition that the receiver uses the same m-sequence generator as the transmitter. Consequently, the corresponding replicas of the ith as well as the following chips, namely chip $c_i, c_{i+1}, \ldots$, can be obtained at the receiver, which exactly match the chips received as a result of the transmitted m-sequence. Hence, the de-spreading of the spread transmitted signal can be successfully carried out by correlating it with the m-sequence replica generated at the receiver.

III. Recursive Soft Sequential Estimation Acquisition

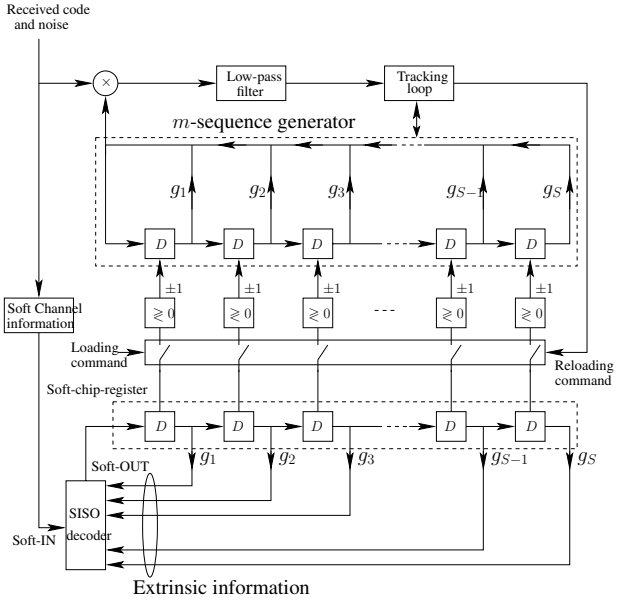

Fig. 2. Schematic diagram of the proposed soft recursive sequential estimator.

A. Description of the RSSE

The schematic diagram of the proposed RSSE acquisition scheme is shown in Fig.2, which includes four fundamental building blocks, namely an m-sequence generator, a soft-chip-register, a SISO decoder and a code phase tracking loop. The soft-chip-register has the same S number of delay-units - which we refer to as soft-chip-delay-units (SCDUs) - as the m-sequence generator. The SCDUs store the instantaneous log-likelihood ratio (LLR) values of S consecutive chips. With the aid of these S number of LLR values, S number of consecutive chips can be determined, which are loaded into the corresponding delay-units of the m-sequence generator of Fig.2. The SISO decoder estimates the corresponding LLR soft output after receiving a soft channel output sample associated with a given chip of the m-sequence. In addition to the so-called intrinsic information of this chip, which was received from the channel, we also exploit the so-called *a-priori* (extrinsic) information related to the chip considered, which is provided by the previous decoded LLR values stored in the SCDUs of Fig.2. The soft output of the SISO decoder is then shifted to the left-most position of the SCDUs in the soft-chip-register, while the soft value in the right-most SCDUs is shifted out and discarded. Note that both the m-sequence generator and the soft-chip-register use the same feedback branches. However, in the m-sequence generator the feedback elements are duo-binary values and the product of these feedback elements is used for generating a binary feedback quantity. By contrast, the feedback elements provided from the soft-chip-register to the SISO decoder consist of the LLR values and the specific operations must be employed in the soft-value domain in order to provide extrinsic information for the SISO decoding.

B. RSSE Acquisition Algorithm

Let $Z_i = \alpha_i c_i + n_i$ represent the received channel output corresponding to chip c_i, where $i = \ldots, -1, 0, 1, \ldots$. When communicating over a fading channel, α_i denotes the fading amplitude, whereas for an Additive White Gaussian Noise (AWGN) channel we set $\alpha_i = 1$. Furthermore, n_i denotes the AWGN having zero mean and a normalized variance of $N_0/2E_c$, where N_0 represents the single-sided power spectral density of the AWGN, E_c represents the transmitted chip-energy and E_c/N_0 represents the signal-to-noise ratio (SNR) per chip. As shown in Fig.2, the SISO decoder requires both soft channel output information and extrinsic information provided by the previous estimates of the SISO decoder, in order to compute the soft output for updating the contents of the soft-chip-register. The soft input information related to chip c_i and entered into the SISO decoder is the LLR of c_i conditioned on the channel output $Z_i,\ i = 0, 1, 2, \ldots$, which is given by [5][Eq.(15)]

$$L(c_i|Z_i) = L_c \cdot Z_i + L(c_i),\ \ i = 0, 1, 2, \ldots, \tag{3}$$

where $L_c = 4\alpha_i \cdot E_c/N_0$, α_i denotes the fading amplitude associated with the transmission of chip c_i over a fading channel, while we have $\alpha_i = 1$ for an AWGN channel. Explicitly, L_c is referred to as the reliability value of the channel. In Equation (3) $L(c_i)$ is the LLR of a random variable c_i, which is defined as [5]

$$L(c_i) = \log \frac{P(c_i = +1)}{P(c_i = -1)},\ \ i = 0, 1, 2, \ldots, \tag{4}$$

where $L(c_i) = 0$, if we have no *a-priori* information related to the chip c_i, which hence assumes the chip value of +1 or -1 with equal probability, i.e., that $P(c_i = +1) = P(c_i = -1)$.

As in Section II we assume that in Fig.2 the generator coefficients are given by $g_{s_1} = g_{s_2} = \ldots = g_{s_l} = \ldots = g_{s_{M=S}} = 1$, while the other coefficients are 0, i.e., that the m-sequence generator obeys a recursive equation described by (2). Consequently, the previous soft outputs of the SISO decoder of Fig.2 obtained at the time-indices of $(i-s_1), (i-s_2), \ldots, (i-(s_M = S))$ are fed back to the SISO decoder, in order to provide extrinsic information for enhancing the correct decoding probability of chip c_i. Let the previous S number of soft outputs of the SISO decoder be $L(y_{i-1}), L(y_{i-2}), \ldots, L(y_{i-S})$. According to (2) the extrinsic information used for enhancing the correct decoding probability of c_i can be approximately expressed as [5][Eq.(12)]

$$L_e(c_i) \approx \left[\prod_{m=1}^{M} \text{sign}(L(y_{i-s_m}))\right] \times \min\left\{|L(y_{i-s_1})|, |L(y_{i-s_2})|, \ldots, |L(y_{i-(s_M=S)})|\right\}, \quad i = 0, 1, 2, \ldots, \quad (5)$$

where we assumed that we have $L_e(c_{-\infty}) = \ldots = L_e(c_{-2}) = L_e(c_{-1}) = 0$.

Finally, with the aid of the channel output information $L_c \cdot Z_i + L(c_i)$ of (3) and the extrinsic information $L_e(c_i)$ of (5), the soft output of the SISO decoder associated with chip c_i can be expressed as

$$L(y_i) = L(c_i|Z_i) + L_e(c_i) = L_c \cdot Z_i + L(c_i) + \left[\prod_{m=1}^{M} \text{sign}(L(y_{i-s_m})\right] \cdot \min\left\{|L(y_{i-s_1})|, |L(y_{i-s_2})|, \ldots, |L(y_{i-(s_M=S)})|\right\}, \quad i = 0, 1, 2, \ldots, \quad (6)$$

where, again, we assumed that we have $L_e(c_{-\infty}) = \ldots = L_e(c_{-2}) = L_e(c_{-1}) = 0$. Note that (6) represents a recursive equation that can be used for estimating the S number of consecutive chips required by the receiver's m-sequence generator for producing the full m-sequence. Provided that the channel's output SNR per chip value of E_c/N_0 is sufficiently high, the LLR values of the S consecutive chips will increase upon increasing the depth of this recursion. In other words, the reliabilities associated with the S consecutive chips increase, while the erroneous loading probability of the generator - which is defined as the probability of the event that the m-sequence generator is loaded with one or more erroneous chips - decreases upon increasing the number of recursions or iterations. Therefore, the acquisition device is capable of observing the reliabilities of the S consecutive chips through observing the amplitudes of the LLR values stored in the SCDUs. If the amplitudes of the LLR values in the SCDUs become sufficiently high after a number of update operations using (6) and they result in a sufficiently low erroneous loading probability, then, as shown in Fig.2, a 'loading command' can be activated for loading the corresponding hard-decision based binary +1 or -1 chip values into the delay-units of the m-sequence generator according to the polarity of the corresponding LLR values stored in the SCDUs.

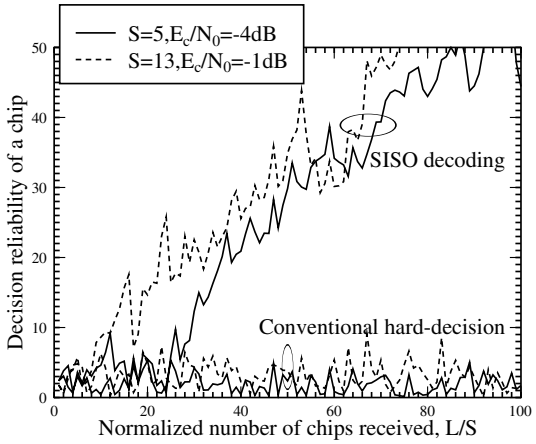

Fig. 3. Decision reliability versus the normalized number of received chips invoked in the recursive SISO decoding, when communicating over an AWGN channel and using an SNR per chip value of $E_c/N_0 = -4$dB for $S = 5$ and $E_c/N_0 = -1$dB for $S = 13$.

Note furthermore that since the acquisition device is capable of observing the reliabilities of the most recent S consecutive chips through observing the amplitudes of the corresponding soft outputs stored in the soft-chip-register of Fig.2, the acquisition scheme has the ability to confidently decide, when it should activate the 'loading command' for loading the initial chips into the m-sequence generator. When the erroneous loading probability is deemed sufficiently low, for example in the region of 10^{-4}, the PN sequence can be acquired with a high probability after the first loading of the initial chips. Therefore, the total acquisition time of the RSSE acquisition scheme can be approximated by the time duration required by the RSSE for carrying out the recursive SISO decoding, in order to reach a sufficiently low erroneous loading probability.

IV. Performance of The RSSE Scheme

In this section we provide a range of simulation results in the context of the proposed RSSE acquisition scheme. Note that the curves were drawn either versus the SNR per chip, namely E_c/N_0 or versus the normalized number of chips received, which also represents the normalized number of chips that the SISO decoder processed. The normalized number of chips L/S was defined as the total number of received chips, L, divided by the number of generator stages, S, of the corresponding m-sequence generator.

Fig.3 shows the reliability associated with correctly deciding upon the polarity of a specific chip of an m-sequence, when the m-sequence was transmitted over AWGN channels. The m-sequence was generated by the generator polynomial of $g(D) = 1 + D^2 + D^5$ using an $S = 5$-stage generator, or by a generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$ employing an $S = 13$-stage generator. The reliability associated with using SISO decoding was defined as the absolute value of the SISO decoder's output evaluated according to (6) in the

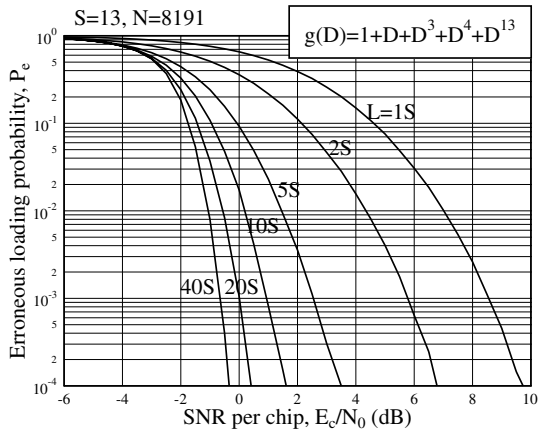

Fig. 4. Erroneous loading probability, P_e, versus the SNR/chip, E_c/N_0, performance for various numbers of chips invoked into the proposed recursive SISO decoder, when transmitting the m-sequence generated using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$ over AWGN channels.

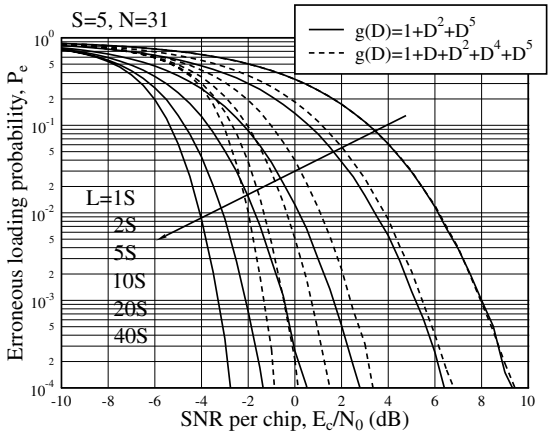

Fig. 5. Comparison of erroneous loading probabilities for the m-sequences having the same length of $N = 31$, but generated by the generating functions of $g(D) = 1 + D^2 + D^5$ and $g(D) = 1 + D + D^2 + D^4 + D^5$, respectively, when communicating over AWGN channels.

context of each chip received. By contrast, for conventional hard-decision the decision reliability associated with the decision concerning the polarity of a specific chip was defined as the absolute value of the channel output corresponding to that chip. From the simulation results of Fig.3 we observe that for the conventional hard-decision based scheme the decision reliability associated with a chip is mainly distributed within the range spanning from 0 to 10 and does not increase as more chips received, since the polarity of each chip is decided separately. By contrast, for the proposed RSSE acquisition scheme the correct decision reliability increases, when receiving more chips from the channel. Furthermore, we observe that the average correct decision reliability increases nearly linearly upon increasing the normalized number of chips received. This is because the proposed recursive SISO decoder is capable of efficiently exploiting the *a-priori* information provided by the previous chips received. Therefore, according to Fig.3 we expect that the RSSE acquisition scheme will outperform the conventional sequential estimation acquisition scheme [1] without exploiting the *a-priori* information provided by the previous chips.

Fig.4 shows the acquisition performance of an m-sequence having a period of $N = 8191$ chips, which was generated by a thirteen-stage ($S = 13$) generator using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$. As shown in Fig.4, the m-sequence can be reliably acquired at an SNR per chip value of $E_c/N_0 = -0.5$dB by invoking about $L = 40 \times S = 40 \times 13 = 520$ chips into the recursive SISO decoder. By contrast, without using any *a-priori* information, i.e., when using the conventional sequential estimation acquisition scheme of [1], the PN code acquisition scheme has to operate at the SNR per chip value of $E_c/N_0 = 9.5$dB, in order to achieve the erroneous loading probability of 10^{-4}. Hence, the SNR per chip gain owing to using the proposed RSSE acquisition scheme instead of using the conventional sequential estimation acquisition scheme at the erroneous loading probability of 10^{-4} is about 10dB, when $L = 520$ chips are loaded into the recursive SISO decoder.

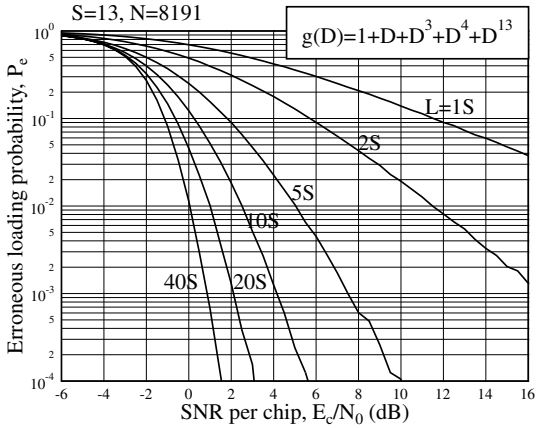

Fig. 6. Erroneous loading probability, P_e, versus the SNR/chip, E_c/N_0, performance for various numbers of chips invoked into the proposed recursive SISO decoder, when transmitting the m-sequence generated using the generator polynomial of $g(D) = 1+D+D^3+D^4+D^{13}$ over Rayleigh fading channels.

It is widely recognised that different m-sequences having the same period can be generated using various generator polynomials. Fig.5 demonstrates the effect of using various generator polynomials on the erroneous loading probability of the m-sequences having the period of $N = 31$, when communicating over AWGN channels. The generator polynomials used were $g(D) = 1 + D^2 + D^5$ and $g(D) = 1 + D + D^2 + D^4 + D^5$, respectively. Explicitly, the generator using the polynomial of $g(D) = 1 + D + D^2 + D^4 + D^5$ has more feedback branches than that using $g(D) = 1 + D^2 + D^5$. According to the re-

sults of Fig.5, it can be observed that given a fixed number of chips invoked during the recursive SISO decoding process, the generator using the polynomial of $g(D) = 1+D^2+D^5$ outperforms that using $g(D) = 1 + D + D^2 + D^4 + D^5$. The reason for these results is that in the context of the generator using the polynomial of $g(D) = 1+D^2+D^5$, the extrinsic information is based on only two feedback branches. By contrast, in the context of the generator using $g(D) = 1+D+D^2+D^4+D^5$, the extrinsic information is based on four feedback branches. However, according to (5) the extrinsic information is determined by the minimum of the LLR values of all the feedback branches. Hence, the generator using a low number of feedback branches has a higher probability of providing high-valued, i.e. reliable extrinsic information to the SISO decoder than that using a high number of feedback branches. Nevertheless, the results of Fig.5 show that regardless of which generator polynomial is used, the proposed RSSE acquisition scheme has a significantly lower erroneous loading probability than the conventional sequential estimation acquisition scheme, provided that a sufficiently high number of received chips are invoked in the recursive SISO decoding process.

In Fig.6 we investigated the acquisition performance of the RSSE acquisition scheme for transmission over Rayleigh fading channels. Specifically, in Fig.6 the m-sequence was generated by a thirteen-stage m-sequence generator using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$. From the results of Fig.6, we observe that at a given SNR per chip value of E_c/N_0, similarly to the results of Fig.4, the erroneous loading probability decreases, when increasing the number of received chips invoked into the recursive SISO decoder. Furthermore, by comparing the results of Fig.6 to those of Fig.4, which were valid when communicating over AWGN channels, it can be shown that for a given number of received chips invoked into the recursive SISO decoder, the achievable SNR gain is significantly higher in the context of Rayleigh fading channels than that over AWGN channels, when using the proposed RSSE acquisition scheme instead of the conventional sequential estimation acquisition scheme. However, for a given number of received chips used by the recursive SISO decoder and for a given SNR per chip value, the acquisition scheme communicating over AWGN channels achieves a lower erroneous loading probability than that encountered, when communicating over Rayleigh fading channels.

Finally, in Fig.7 we show the erroneous loading probability performance versus the normalized number of received chips used by the recursive SISO decoder for an m-sequence generated by an $S = 13$-stage m-sequence generator, which has a period of 8191 chips. The results were generated for transmissions over both AWGN and Rayleigh fading channels at the SNR per chip value of $E_c/N_0 = -1$dB. According to the results of Fig.7 it can be shown that for AWGN channels the RSSE acquisition scheme is capable of achieving an erroneous loading probability of 10^{-3} after receiving approximately $80 \times 13 = 1040$ chips. By contrast, when communicating over Rayleigh fading channels, the RSSE acquisition scheme is capable of achieving the erroneous loading probability of 10^{-3} after receiving approximately $500 \times 13 = 6500$ chips. These results imply that with the aid of the proposed recursive SISO decoder the required target performance can be achieved, regardless of the specific communication environment encountered, when invoking the required number of chips into the SISO decoder.

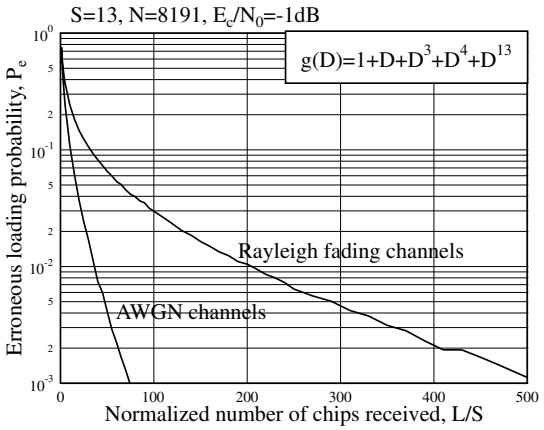

Fig. 7. Erroneous loading probability, P_e versus the normalized number of received chips invoked into the proposed recursive SISO decoder for an m-sequence having a period of 8191, when communicating over AWGN or Rayleigh fading channels and using an SNR per chip value of $E_c/N_0 = -1$dB for $S = 13$.

V. Conclusions

In summary, in this contribution we have proposed a recursive soft sequential estimation (RSSE) acquisition scheme using the principles of iterative SISO decoding. The acquisition performance of the RSSE acquisition scheme has been investigated. It has been shown that the RSSE acquisition scheme has both an implementational complexity and an initial synchronization time, which are linearly dependent on the number of stages in the m-sequence generator. In terms of these characteristics, the RSSE acquisition scheme outperforms both the family of conventional serial search based acquisition schemes and the class of conventional parallel search aided acquisition schemes. These conventional schemes either result in a high mean-acquisition time or impose a high implementational complexity, that are exponentially dependent on the number of stages in the m-sequence generator.

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