Iterative Soft Sequential Estimation Aided Differential Acquisition of m-Sequences

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***Abstract*— In this contribution a novel sequential estimation method is proposed for the acquisition of m-sequences. This sequential estimation method exploits the principle of iterative soft-in-soft-out (SISO) decoding for enhancing the acquisition performance, and that of differential pre-processing for the sake of achieving an enhanced acquisition performance, when communicating over various propagation environments. Hence the advocated acquisition arrangement is referred to as the Differential Recursive Soft Sequential Estimation (DRSSE) acquisition scheme. The DRSSE acquisition scheme exhibits a low complexity, which is similar to that of an m-sequence generator, while achieving an acquisition time that is linearly dependent on the number of stages in the m-sequence generator. Owing to these attractive characteristics, the DRSSE acquisition scheme constitutes a promising initial synchronization scheme, in particular, when acquiring long m-sequences transmitted over various propagation environments.**

I. Introduction

Ward's sequential estimation acquisition arrangement [1] constitutes one of the simplest acquisition schemes. The philosophy behind the sequential estimation acquisition scheme is as follows. The acquisition of an m-sequence of length $(2^S - 1)$ is deemed successful, provided that S consecutive chips are correctly received by the acquisition device and are loaded into the local m-sequence generator, where successive shifts of the chips in the generator will generate chips that exactly match the forthcoming received chips of the transmitted m-sequence. However, in the presence of noise a number of the S consecutive chips might be in error, potentially resulting in erroneous loading of the m-sequence generator. In this case a new set of S chips can be processed similarly.

Clearly, the most critical requirement for attaining the successful acquisition of PN sequences based on sequential estimation [1] is that S consecutive chips of the received and noise contaminated PN sequence have to be correctly estimated. In order to improve the reliabilities associated with deciding upon the value of S consecutive initial chips, Kilgus [2] proposed a majority logic decoding aided scheme for estimating the required S number of consecutive chips. By contrast, in [3] Ward and Yiu have proposed a recursive sequential estimation assisted acquisition scheme. It was shown that both the above schemes are capable of significantly improving the acquisition performance by exploiting the inherent properties of the m-sequences for aiding the estimation of the S consecutive chips. However, all existing sequential estimation based acquisition schemes operate on the basis of hard-decision chips. Furthermore, in the existing sequential estimation based acquisition schemes coherent detection was assumed, which is often unrealistic to achieve, since prior to despreading the SNR is usually insufficiently high for attaining a satisfactory carrier-phase tracking.

In this contribution we invoke the iterative SISO decoding principle - which has originally been developed for turbo channel decoding [4], [5] - for improving the reliabilities associated with deciding upon the S consecutive chips to be loaded into the local m-sequence generator. Upon exploiting the inherent properties of m-sequences, a DRSSE acquisition scheme is proposed. In the DRSSE acquisition scheme the transmitted m-sequence is first mapped to another m-sequence, where the time-varying carrier-phase is removed with the aid of differential pre-processing. Then, S consecutive chips of the resultant m-sequence are estimated using a recursive SISO decoder. An important feature of the proposed DRSSE acquisition scheme is that it exploits the real-time knowledge of the reliabilities associated with the S consecutive chips. By exploiting this real-time knowledge of the chip-reliabilities the acquisition device becomes capable of astutely managing the loading of S consecutive chips into the local m-sequence generator. The proposed DRSSE acquisition scheme has an algorithmic complexity, which is similar to that of an m-sequence generator. Our simulation results will show that the acquisition time of the DRSSE acquisition scheme is a linear function of the number of stages in the m-sequence generator. Furthermore, the DRSSE acquisition scheme is suitable for m-sequence acquisition, when communicating over various propagation environments including AWGN, slow fading and fast fading channels. This is because the differential processing is at the chip-level of the m-sequences and during a chip-interval the fading-induced phase-changes are low, even when the Doppler frequency shift is relatively high.

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II. Principle of Sequential Estimation Acquisition

The well-established maximum-length sequences, which are also known as m-sequences, are generated using feedback shift registers of the form shown in Fig.1. In Fig.1 D represents a unity time-delay operation, while each of the coefficients, $g_1, g_2, \ldots, g_S$, represents the presence of a connection if it is a 1 or the absence of a connection if it is a 0. Let the output binary sequence be $\ldots, c_{-2}, c_{-1}, c_0, c_1, c_2, \ldots$, where $c_i \in \{+1, -1\}$. Furthermore, we assume that, in Fig.1, the coefficients $g_{s_1} = g_{s_2} = \ldots = g_{s_l} = \ldots = g_{s_M=S} = 1$, where s_i is an integer in the range $[1, S]$, while the remaining coefficients are 0. The above configuration corresponds to the generator polynomial of

$$g(D) = 1 + D^{s_1} + D^{s_2} + \ldots + D^{s_l} + \ldots + D^{s_M=S}, \qquad (1)$$

where $g(D)$ must be a primitive polynomial [6], i.e., a polynomial that cannot be factorized, in order to generate an m-sequence. Based on the above assumptions, it can be shown that the output symbols of Fig.1 obey the recursive relationship of

$$\begin{aligned} c_i &= c_{i-s_1} c_{i-s_2} \cdots c_{i-s_l} \cdots c_{i-(s_M=S)} \\ &= \prod_{m=1}^{M} c_{i-s_m} \text{ for } i = \ldots, -1, 0, 1, \ldots, \end{aligned} \qquad (2)$$

where $\prod$ represents the product of the coefficients.

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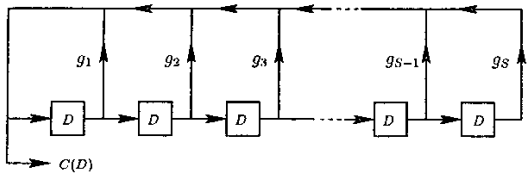

Fig. 1. Maximal-length sequence (m-sequences) generator that outputs binary sequences.

In spread-spectrum communications using m-sequences as spreading sequences, Equation (2) implies that if the receiver has the knowledge of the chip values c_{i-1}, c_{i-2}, $\cdots$, c_{i-S} before the transmitter generates the ith chip c_i, then the chip values c_{i-1}, c_{i-2}, $\cdots$, c_{i-S} can be loaded into the corresponding registers of the m-sequence generator at the receiver for generating the forthcoming chips, provided that the receiver uses the same m-sequence generator as the transmitter. Consequently, the corresponding replicas of the ith as well as the forthcoming chips, namely $c_i, c_{i+1}, \ldots$, can be obtained at the receiver, which exactly match the chips received as a result of the transmitted m-sequence. Hence, the de-spreading of the spread transmitted signal can be successfully carried out by correlating it with the m-sequence replica generated at the receiver. What we have described above constitutes the principle behind the sequential estimation acquisition scheme proposed by Ward [1].

III. DRSSE Acquisition

The motivation of employing a chip-based differential preprocessing operation is two-fold. Firstly, prior to despreading the signal-to-noise ratio (SNR) is usually insufficiently high for attaining a satisfactory performance with the aid of coherent carrier phase estimators based on carrier-phase tracking loops. By contrast, the chip-based differential operation is capable of reducing the effects of the time-varying phase fluctuations imposed by fading and frequency offset. Consequently, chip-based differential pre-processing is capable of significantly enhancing the performance of the subsequent sequential estimation process. Secondly, from the shift-and-add property of m-sequences [7], the product of the spreading waveform and its chip-time delayed phase yields another phase. This indicates that the differential processing of an m-sequence preserves the characteristics of the m-sequences. Specifically, this property can be demonstrated as follows.

The recursive equation of the m-sequence generator using the generator polynomial of (1) is given by (2). We multiply both sides of (2) by c_{i-1} and upon substituting c_{i-1} at the right-hand side of (2) by $c_{i-1} = \prod_{n=1}^{M} c_{i-1-s_n}$, we obtain

$$\begin{aligned} c_i \cdot c_{i-1} &= \prod_{m=1}^{M} c_{i-s_m} \cdot \prod_{n=1}^{M} c_{i-1-s_n} \\ &= \prod_{m=1}^{M} (c_{i-s_m} \cdot c_{i-1-s_m}) \quad \text{for } i = \ldots, -1, 0, 1, \ldots \quad (3) \end{aligned}$$

Let $b_j = c_j \cdot c_{j-1}$ in (3), where j is an integer. Then Equation (3) can be expressed as

$$b_i = \prod_{m=1}^{M} b_{i-s_m} \text{ for } i = \ldots, -1, 0, 1, \ldots. \quad (4)$$

Explicitely, both recursive equations, namely (2) and (4), describe the same m-sequence generator. The m-sequence generated by (4) represents a specifically delayed or phase-shifted version of the m-sequence generated by (2). Consequently, once the m-sequence of (4) has been acquired, the acquisition of the m-sequence generated by (2) can also be achieved. The objective of the DRSSE is to achieve the acquisition of the m-sequence generated by (4) using the proposed soft recursive sequential estimation scheme.

A. Description of the DRSSE Scheme

The schematic diagram of the proposed DRSSE acquisition arrangement is shown in Fig.2, which includes five fundamental building blocks, namely a chip-based differential processor, an m-sequence generator, a soft-chip-register, a SISO decoder and a code phase tracking loop. The chip-based differential processor executes differential processings at the chip level, which requires that the carrier phases between two adjacent chips remain similar. Hence, the DRSSE acquisition scheme is suitable for communicating over fading channels exhibiting a high fading rate. The soft-chip-register of Fig.2 has the same S number of delay-units - which we refer to as soft-chip-delay-units (SCDUs) - as the m-sequence generator. The SCDUs store the instantaneous log-likelihood ratio (LLR) values of S consecutive chips of the m-sequence in the form of (4). With the aid of these S number of LLR values, S number of consecutive chips can be determined, which are loaded into the corresponding delay-units of the m-sequence generator of Fig.2. The SISO decoder estimates the corresponding LLR soft output after receiving a soft output sample from the differential processor associated with a given chip of the m-sequence of (4). In addition to the so-called *intrinsic* information of this chip, we also exploit the so-called *a-priori* (*extrinsic*) information related to the chip considered. This *extrinsic* information is provided by the previously decoded LLR values stored in the SCDUs of Fig.2. The soft output of the SISO decoder is then shifted to the left-most position of the SCDUs in the soft-chip-register, while the soft value in the right-most position of the SCDUs is shifted out and discarded. Note that both the m-sequence generator and the soft-chip-register use the same feedback branches. However, in the m-sequence generator the feedback elements are duobinary values and the product of these feedback elements is used for generating a binary feedback quantity. By contrast, the feedback elements of the soft-chip-register feeding information back to the input of the SISO decoder consist of the LLR values. Hence, the specific operations must be carried out in the soft-value domain for the sake of providing *extrinsic* information for the SISO decoding.

B. DRSSE Acquisition Algorithm

As shown in Fig.2, the SISO decoder requires both *intrinsic* information conveyed to the input of the SISO decoder by the differential processor as well as *extrinsic* information provided by the previous estimates of the SISO decoder, in order to generate the soft output required for updating the contents of the soft-chip-register. Let us now consider these sources of information. Let $Z_i = \alpha_i e^{j\phi_i} c_i + n_i$ represent the received channel output sample corresponding to chip c_i, where $i = 0, 1, 2, \ldots$. The parameter α_i denotes the fading amplitude, while ϕ_i represents the phase shift due to carrier modulation and channel fading. Note that when communicating over Additive White Gaussian Noise (AWGN) channels, the term of $\alpha_i e^{j\phi_i}$ is set to one. Furthermore, n_i denotes the complex AWGN having zero mean and a normalized variance of N_0/E_c, where N_0 represents the single-sided power spectral density of the AWGN, E_c represents the transmitted

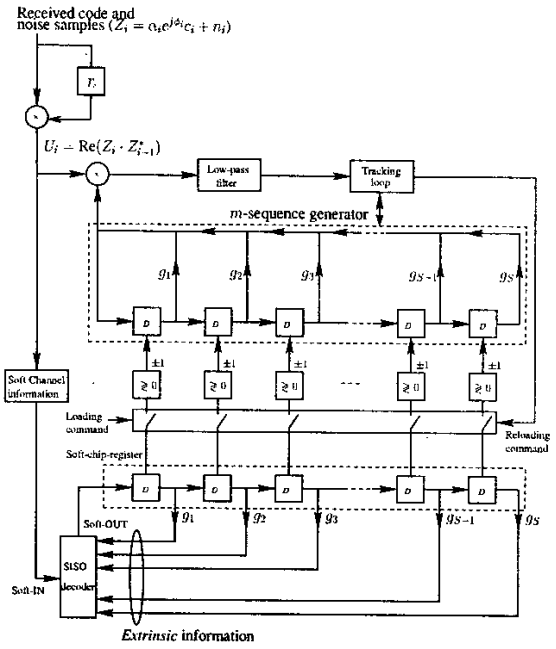

Fig. 2. Schematic diagram of the proposed differential soft recursive sequential estimator.

chip energy and E_c/N_0 represents the signal-to-noise ratio (SNR) per chip. Assuming that the channel-induced fading and phase-rotation remain constant over two adjacent chip time-durations, i.e., that we have $\alpha_i = \alpha_{i-1}$ and $\phi_i = \phi_{i-1}$, the differential processor's output can be expressed as:

$$\begin{aligned} U_i &= \mathrm{Re}(Z_i \cdot Z_{i-1}^*) \\ &= \alpha_i^2 c_i \cdot c_{i-1} \\ &+ \mathrm{Re}(\alpha_i e^{j\phi_i} c_i n_{i-1}^* + \alpha_i e^{-j\phi_i} c_{i-1} n_i + n_i n_{i-1}^*), \end{aligned} \quad (5)$$

where * represents the complex conjugate operation. When using $b_i = c_i \cdot c_{i-1}$ and, without changing the associated statistical properties, we absorb the terms of $e^{j\phi_i} c_i$ and $e^{-j\phi_i} c_{i-1}$ in the Gaussian noise components n_{i-1}^* and n_i, Eq. (5) can be written as

$$U_i = \alpha_i^2 b_i + \alpha_i \cdot \mathrm{Re}(n_{i-1}^* + n_i) + \mathrm{Re}(n_i n_{i-1}^*). \quad (6)$$

It was shown in [8] that at the SNRs of practical interest the term $n_i n_{i-1}^*$ is small relative to the dominant noise term of $\alpha_i(n_{i-1}^* + n_i)$. Consequently, if we neglect the term $n_i n_{i-1}^*$, then U_i can be described as a Gaussian variable having a mean given by $\alpha_i^2 b_i$ and a variance given by $\Omega N_0/E_c$, where $\Omega = \overline{\alpha_i^2}$ represents the ensemble average of α_i^2. Hence, the probability density function (PDF) of U_i can be approximated as

$$p_{U_i}(y|b_i) \approx \frac{1}{\sqrt{2\pi\Omega N_0/E_c}} \exp\left(-\frac{E_c}{2\Omega N_0}(y - \alpha_i^2 b_i)^2\right). \quad (7)$$

The *intrinsic* information is derived from the LLR of b_i conditioned on the channel-related variable U_i, which can be expressed as

$$\begin{aligned} L(b_i|U_i) &= \log \frac{p_{U_i}(b_i = +1|y = U_i)}{p_{U_i}(b_i = -1|y = U_i)} \\ &= \log\left(\frac{p_{U_i}(y = U_i|b_i = +1)}{p_{U_i}(y = U_i|b_i = -1)} \cdot \frac{P(b_i = +1)}{P(b_i = -1)}\right). \end{aligned} \quad (8)$$

Upon substituting $p_{U_i}(y = U_i|b_i)$ of (7) associated with $b_i = +1$ and $b_i = -1$ into (8), finally, we obtain

$$\begin{aligned} L(b_i|U_i) &= \log \frac{\exp\left(-\frac{E_c}{2\Omega N_0}(U_i - \alpha_i^2)^2\right)}{\exp\left(-\frac{E_c}{2\Omega N_0}(U_i + \alpha_i^2)^2\right)} + \log \frac{P(b_i = +1)}{P(b_i = -1)} \\ &= L_c \cdot U_i + L(b_i), \quad i = 0, 1, 2, \ldots, \end{aligned} \quad (9)$$

where we have $L_c = 2\alpha_i^2 E_c/\Omega N_0$, which is referred to as the reliability value of the channel, while $L(b_i)$ is the LLR of a random variable b_i, which is defined as [5] $L(b_i) = \log \frac{P(b_i = +1)}{P(b_i = -1)}$. Furthermore, we set $L(b_i) = 0$, if we have no *a-priori* information related to b_i, which corresponds to assuming a chip value of +1 or -1 with equal probability, i.e., that we have if $P(b_i = +1) = P(b_i = -1)$.

Note that at the initial synchronization stage the estimation of the channel parameters might be unreliable. If we have no prior knowledge concerning the channel parameters, we can simply set $L_c = 2E_c/N_0$. However, our simulation results in Section IV will show that the acquisition performance degrades in the absence of perfect knowledge of the channel. Furthermore, for transmission over AWGN channels the reliability value of the channel is set to $L_c = 2E_c/N_0$.

In the context of the *extrinsic* information, as in Section II, we assume that in Fig.2 the generator coefficients are given by $g_{s_1} = g_{s_2} = \ldots = g_{s_l} = \ldots = g_{s_M = S} = 1$, while the other coefficients are 0s, i.e., the m-sequence generator obeys the recursive equation (2) or (4). Consequently, the previous soft outputs of the SISO decoder of Fig.2 obtained at the time instants of $(i - s_1), (i - s_2), \ldots, (i - (s_M = S))$ are fed back to the input of the SISO decoder, in order to provide *extrinsic* information for enhancing the correct decoding probability of chip b_i. Let the previous S number of soft outputs of the SISO decoder be $L(y_{i-1}), L(y_{i-2}), \ldots, L(y_{i-S})$. According to (2) the *extrinsic* information used for enhancing the correct decoding probability of b_i can be approximately expressed as [5][Eq.(12)]

$$\begin{aligned} L_e(b_i) \approx &\left[\prod_{m=1}^{M} \mathrm{sign}(L(y_{i-s_m}))\right] \\ &\times \min\left\{|L(y_{i-s_1})|, |L(y_{i-s_2})|, \ldots, |L(y_{i-(s_M=S)})|\right\}, \\ &i = 0, 1, 2, \ldots, \end{aligned} \quad (10)$$

where we assumed that we have $L_e(b_{-\infty}) = \ldots = L_e(b_{-2}) = L_e(b_{-1}) = 0$.

Finally, with the aid of the *intrinsic* information $L_c \cdot U_i + L(b_i)$ of (9) and the *extrinsic* information $L_e(b_i)$ of (10), the soft output of the SISO decoder associated with chip b_i can be expressed as

$$\begin{aligned} L(y_i) &= L(b_i|Z_i) + L_e(b_i) \\ &\approx L_c \cdot U_i + L(b_i) + \left[\prod_{m=1}^{M} \mathrm{sign}(L(y_{i-s_m})\right] \\ &\quad \cdot \min\left\{|L(y_{i-s_1})|, |L(y_{i-s_2})|, \ldots, |L(y_{i-(s_M=S)})|\right\}, \\ &\quad i = 0, 1, 2, \ldots, \end{aligned} \quad (11)$$

where, again, we assumed that we have $L_e(b_{-\infty}) = \ldots = L_e(b_{-2}) = L_e(b_{-1}) = 0$. Note that (11) represents a recursive equation that can be used for estimating the S number of consecutive chips

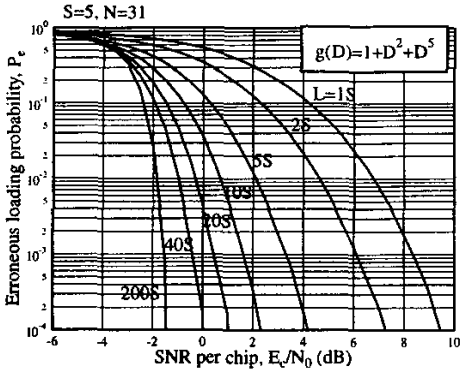

Fig. 3. Erroneous loading probability, P_e, versus the SNR/chip, E_c/N_0, performance for various numbers of chips invoked by the proposed recursive SISO decoder, when transmitting the m-sequence generated using the generator polynomial of $g(D) = 1 + D^2 + D^5$ over AWGN channels.

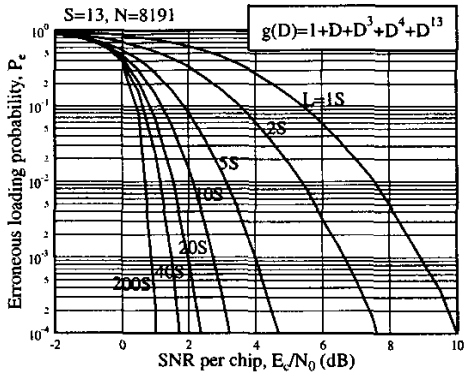

Fig. 4. Erroneous loading probability, P_e, versus the SNR/chip, E_c/N_0, performance for various numbers of chips invoked by the proposed recursive SISO decoder, when transmitting the m-sequence generated using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$ over AWGN channels.

required by the receiver's m-sequence generator for producing the full m-sequence of (4). Provided that the channel's output SNR per chip value of E_c/N_0 is sufficiently high, the LLR values of the S consecutive chips will increase upon increasing the depth of this recursion. In other words, the reliabilities associated with the S consecutive chips increase, while the erroneous loading probability of the m-sequence generator - which is defined as the probability of the event that the m-sequence generator is loaded with one or more erroneous chips - decreases upon increasing the number of recursions or iterations. Therefore, the acquisition device is capable of observing the reliabilities of the S consecutive chips through observing the amplitudes of the LLR values stored in the SCDUs. If the amplitudes of the LLR values in the SCDUs become sufficiently high after a number of update operations using (11) and they result in a sufficiently low erroneous loading probability, then, as shown in Fig.2, a 'loading command' can be activated for loading the corresponding hard-decision based binary +1 or -1 chip values into the delay-units of the m-sequence generator according to the polarity of the corresponding LLR values stored in the SCDUs.

IV. Performance Results

In this section we provide a range of simulation results for characterizing the proposed DRSSE acquisition scheme. Note that the curves were drawn either versus the SNR per chip, namely E_c/N_0 or versus the normalized number of chips received, which also represents the normalized number of chips that the SISO decoder processed. The normalized number of chips L/S was defined as the total number of received chips, L, divided by the number of generator stages, S, of the corresponding m-sequence generator.

In Fig.3 we show the erroneous loading probability, P_e, versus the SNR per chip, E_c/N_0 performance for an m-sequence generated using the generator polynomial of $g(D) = 1 + D^2 + D^5$ and transmitted over AWGN channels. Note that in Fig.3 the curve corresponding to the parameter of $L = 1 \times S$ represents the erroneous loading probability of the DRSSE acquisition scheme using no recursive SISO decoding. From the results we can see that when more channel output chips are involved in the recursive SISO decoding process, a higher correct detection reliability and hence a lower erroneous loading probability can be achieved. For the sake of illustration, let us assume that the transmitted m-sequence can be reliably acquired, once the erroneous loading probability is lower than 10^{-4}. Then, from the results of Fig.3 we can observe that the m-sequence can be reliably acquired at an SNR per chip value of $E_c/N_0 = 0$dB by invoking about $L = 40 \times S = 40 \times 5 = 200$ chips into the recursive SISO decoding scheme. By contrast, without exploiting the power of recursive SISO decoding, the DRSSE acquisition scheme has to operate at an SNR per chip value of $E_c/N_0 = 9.5$dB, in order to achieve the same erroneous loading probability of 10^{-4}. Explicitly, at the erroneous loading probability of 10^{-4} the SNR per chip gain is about 9.5dB, when $L = 200$ chips are invoked by the recursive SISO decoding scheme. In general, it is expected that when more chips can be used during the recursive SISO decoding process, an increased gain can be achieved by the proposed DRSSE acquisition scheme. For example, when invoking $L = 200 \times S$ instead of $L = 40 \times S$ chips into the recursive SISO decoder, another 1.7dB SNR per chip gain can be achieved at the erroneous loading probability of 10^{-4}.

Fig.4 shows the acquisition performance for an m-sequence having a period of $N = 8191$ chips, which was generated by a thirteen-stage ($S = 13$) generator using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$. As shown in Fig.4, the m-sequence can be reliably acquired at an SNR per chip value of $E_c/N_0 = 1.7$dB, when invoking about $L = 40 \times S = 40 \times 13 = 520$ chips in the recursive SISO decoder. This m-sequence can also be reliably acquired at a reduced SNR per chip value of $E_c/N_0 = 1$dB by invoking about $L = 200 \times S = 200 \times 13 = 2600$ chips in the recursive SISO decoder. By contrast, in the absence of the recursive SISO decoding, the PN code acquisition scheme has to operate at the SNR per chip value of $E_c/N_0 = 10$dB, in order to achieve the erroneous loading probability of 10^{-4}. Hence, the SNR per chip gain recorded at the erroneous loading probability of 10^{-4} is about 8.3dB or 9dB, respectively, when $L = 520$ or $L = 2600$ chips are invoked by the recursive SISO decoder. Note that even though $L = 2600$ chips are invoked

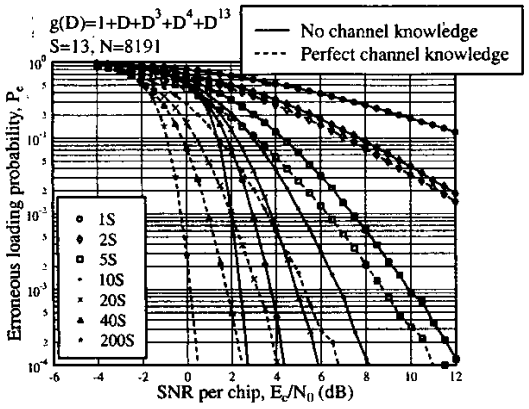

Fig. 5. Erroneous loading probability, P_e, versus the SNR/chip, E_c/N_0, performance for various numbers of chips invoked by the proposed recursive SISO decoder, when transmitting the m-sequence generated using the generator polynomial of $g(D) = 1+D+D^3+D^4+D^{13}$ over Rayleigh fading channels.

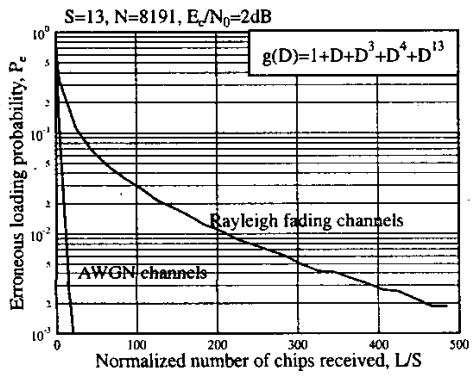

Fig. 6. Erroneous loading probability, P_e versus the normalized number of received chips invoked by the proposed recursive SISO decoder for an m-sequence having a period of 8191, when communicating over AWGN or Rayleigh fading channels and using an SNR per chip value of $E_c/N_0 = 2$dB for $S = 13$.

by the recursive SISO decoder for achieving reliable acquisition at the SNR per chip value of $E_c/N_0 = 1$dB, the associated acquisition time of $L = 2600$ chip durations is still significantly lower than that of any conventional serial search acquisition scheme, which requires a mean acquisition time on the order of the period of the m-sequences considered, i.e., 8191 chips in this example.

In Fig.5 we investigated the acquisition performance of the DRSSE acquisition scheme for transmission over Rayleigh fading channels. As we analysed in Section III, when communicating over fading channels, depending on whether the recursive SISO decoder employs perfect knowledge or no knowledge of the fading channel, the term L_c in the *intrinsic* information of (9) can be set to $L_c = 2\alpha_i^2 E_c/\Omega N_0$ or to $L_c = 2E_c/N_0$. In Fig.5 we also compared the acquisition performance recorded in the context of these two cases. In Fig.5 the m-sequence was generated by a thirteen-stage m-sequence generator using the generator polynomial of $g(D) = 1 + D + D^3 + D^4 + D^{13}$. From the results of Fig.5 we observe that the acquisition performance improves in both cases, when increasing the number of received chips invoked by the recursive SISO decoder. However, compared to the acquisition performance achieved, when using no recursive SISO decoding (the curve marked with circles), for a given number of received chips, the recursive SISO decoder using perfect channel knowledge provides a higher SNR per chip gain than that attained without using any channel knowledge. This observation can be explained with the aid of (11). When perfect knowledge of the channel is employed, Equation (11), in fact, is processed based on the 'maximal-ratio combining (MRC)' principle. By contrast, without the knowledge of the channel, Eq.(11) is processed based on the 'equal-gain combining (EGC)' principle. It is well-known that the MRC scheme outperforms the EGC scheme in multipath fading channels.

Finally, in Fig.6 we show the erroneous loading probability performance versus the normalized number of received chips used by the recursive SISO decoder for an m-sequence generated by an $S = 13$-stage m-sequence generator and hence having a period of 8191 chips. The results were generated for transmissions over both AWGN and Rayleigh fading channels at the SNR per chip value of $E_c/N_0 = 2$dB. Observe in Fig.6 when communicating over AWGN channels, the DRSSE acquisition scheme is capable of achieving an erroneous loading probability of 10^{-3} after receiving approximately $20 \times 13 = 260$ chips. By contrast, when communicating over Rayleigh fading channels, the DRSSE acquisition scheme is capable of reaching the erroneous loading probability of 10^{-3} after receiving approximately $500 \times 13 = 6500$ chips. These results imply that with the aid of the proposed recursive SISO decoder the required target performance can be achieved, regardless of the specific communication environment encountered upon invoking a sufficiently high number of chips in the SISO decoder. The results of Fig.6 indicate that successful acquisition can be achieved by the proposed DRSSE acquisition scheme, when communicating over Rayleigh fading channels at $E_c/N_0 = 2$dB within about 6500 chip durations, which is lower than the 8191-chip period of the transmitted m-sequence.

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