Switched-Current Wave Group Delay Equalizers

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Abstract: To improve the elliptic filters step response, group delay equalizers are often cascaded with the filters. This paper describes the design of switched-current (SI) group delay equalizer using wave synthesis technique. This design is based on a new all-pass circuit, where the poles are generated using wave structures. Simulation results are included demonstrating that the 3rd-order SI group delay equalizer can reduces the amount of overshoot in 100kHz elliptic low-pass filter step response by $\geq 50\%$. This is as a result of reducing the filter group delay variation from 2.29 μs to 0.32 μs when the group delay equalizer is employed

1. Introduction

Switched-current (SI) is becoming a viable alternative to switched-capacitor particularly in low voltage analog circuit design [1]. Numerous design methods for SI filters have been reported [2-6]. Communications applications often call for filters with high stop-band attenuation and linear phase or flat group delay (derivate of phase with respect to frequency) response in the pass-band. To design sharp filters with low component count, elliptic approximation is normally used. However, elliptic filters have non-linear phase and non-flat group delay response resulting in excessive overshoot in the filters step response. For example, it was reported in [7] that the step response of 7th-order elliptic low-pass filter with stop-band attenuation of >45dB has >30% overshoot when it is driven by 100kHz square waveform. Such an overshoot is often unacceptable in most communication applications. An approach to improve the filter step response (i.e. reduce the overshoot) is to cascade filter with group delay equalizer or an all-pass

circuit. The function of the all-pass circuit is to flatten the filter group delay response without changing the magnitude of the filter characteristics.

While much research has been carried out in SI filter designs [2-6], very little work has been reported on the design of group delay equalizers using SI technology. In order to realize the full potential of SI technology in analog signal processing, design methods for SI group delay equalizations are needed. Recently, an integrator-based design method for SI group delay equalizers derived from LC prototypes was reported [8]. However, the application of wave synthesis technique [9] to design SI filters provides circuits that can be easily implemented [5,6], when compared with integrator-based filters [2,3]. This is because SI wave filters consist of only delay cells and wave adaptors, which are readily available in SI technology. The aim of this paper is to investigate the design of SI group delay equalizers based on wave synthesis technique.

2. New all-pass wave circuit architecture

The general z-domain transfer function of *Nth*-order group delay equalizer is [10]:

$$H(z) = \pm \frac{a_N z^N + a_{N-1} z^{N-1} + \cdots + a_1 z + 1}{z^N + a_1 z^{N-1} + \cdots + a_{N-1} z + a_N} = \pm \frac{\sum_{k=0}^{N} a_k z^k}{\sum_{k=0}^{N} a_k z^{N-k}}, \; a_0 = 1 \qquad (1)$$

where the poles and zeros of *H(z)* are reciprocals of one another. According to ladder-based realization of all-pass filter [11], the general z-domain transfer function *H(z)* can be rearranged as:

$$H(z) = 1 - \frac{2}{1 + Y(z)} \qquad (2)$$

where *Y(z)* is polynomial function, which can be expanded into continued fraction [11].

Numerous implementations of Eq.(2) have been reported, including OTA-C [7] and switched-capacitor realization [10]. In this paper, SI implementation of Eq.(2) is proposed as shown in Fig.1. The circuit operates as follows:

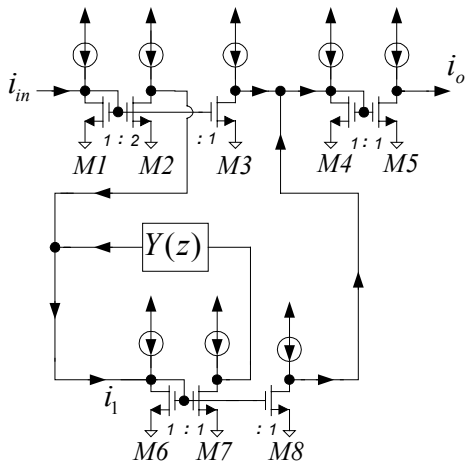

Fig.1 SI wave all-pass circuit architecture

The circuit input current i_{in} is inverted and multiplied by a gain of 2 through current mirror (*M1~M2*). This amplified current is summed with output of block *Y(z)* and fed into the current mirror *M6*, *M7* and *M8*. One inverted current copy of this current mirror is sent to the input of block *Y(z)*, whose output is fedback into current mirror *M6*, *M7* and *M8*. Another inverted current copy is summed with the inverted current copy of i_{in} and sent to current mirror (*M4~M5*), whose output is current i_o. The architecture operation can be summarized by the following equations:

$$-2i_{in} - i_1 Y(z) = i_1 \tag{3}$$

From which, we obtain

$$i_1 = -2i_{in} /(1 + Y(z)) \tag{4}$$

The circuit output current is:

$$i_o = i_{in} + i_1 \tag{5}$$

Substituting Eq.(3) into Eq.(5) produce the all-pass transfer function Eq.(2), confirming that Fig.1 realizes Eq.(2).

Since *Y(z)* can be expanded into continued fraction [8,10,11], Eq.(6), it is analogous to a driving-point admittance, which can be synthesized as LC ladder circuit, Fig.2.

$$Y(z) = C_1\lambda + \cfrac{1}{L_2\lambda + \cfrac{1}{\vdots + \cfrac{1}{C_N\lambda}}} \qquad (6)$$

where $\lambda = (2/T)\cdot(1-z^{-1})/(1+z^{-1})$ and $C_i,\ L_i > 0\ \ i = 1,2,\cdots N$

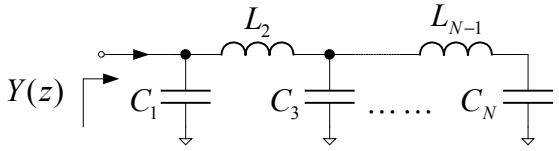

Fig.2 *Nth*-order LC ladder network

The circuit in Fig.1 realizes an all-pass function, where the order and pole positions are determined by *Y(z)*. In this paper, we propose to convert the *LC* ladder network of Fig.2 to SI circuit using wave synthesis technique. This is because the resultant SI circuit has the benefits of implementation simplicity and the elimination of integrators as outlined in [5,6]. The wave synthesis technique simulates the behavior of *LC* networks through the use of wave quantities instead of port voltages and current. The wave variables A_k (incident wave) and B_k (reflected wave) are defined as linear combinations of the corresponding port current, I_k and voltage, V_k:

$$A_k = V_k + I_k \cdot R_k \qquad (7a) \qquad\qquad B_k = V_k - I_k \cdot R_k \qquad (7b)$$

where R_k is the port resistance, and is chosen arbitrarily to simplify the wave model. For the passive component: *R*, *L* and *C*, their port resistances are *R*, *2L/T* and *T/2C*, respectively.

Wave adaptors model the reflections caused by the parallel or series connections of the passive components within the prototype filter. Fig.3 shows the *Nth*-order equivalent wave structure of LC ladder network in Fig.2. (reader can refer to [9] for more details on wave filter design).

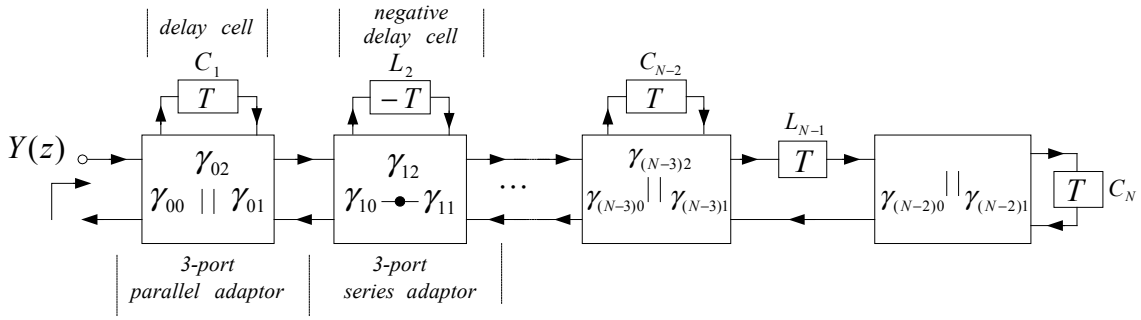

Fig.3 *Y(z)* realization using wave synthesis technique

This wave structures consist of delay cells, series and parallel adaptors, where γ_{ij} is coefficient of port j in adaptor i. The wave adaptor coefficients γ are calculated using the following expressions, which must be satisfied for each M-port adaptor:

$$\sum_{k=0}^{M-1} \gamma_k = 2 \tag{8}$$

M-port series adaptors: $\frac{\gamma_0}{R_0} = \frac{\gamma_1}{R_1} = \cdots = \frac{\gamma_{M-1}}{R_{M-1}}$ (9a)

M-port parallel adaptors: $\frac{\gamma_0}{G_0} = \frac{\gamma_1}{G_1} = \cdots = \frac{\gamma_{M-1}}{G_{M-1}}$ (9b)

where R_k and G_k are the port resistance and conductance of port k.

3. Design of SI wave group delay equalizers

The design flow of the SI wave group delay equalizers is shown in Fig.4. It consists of four steps.

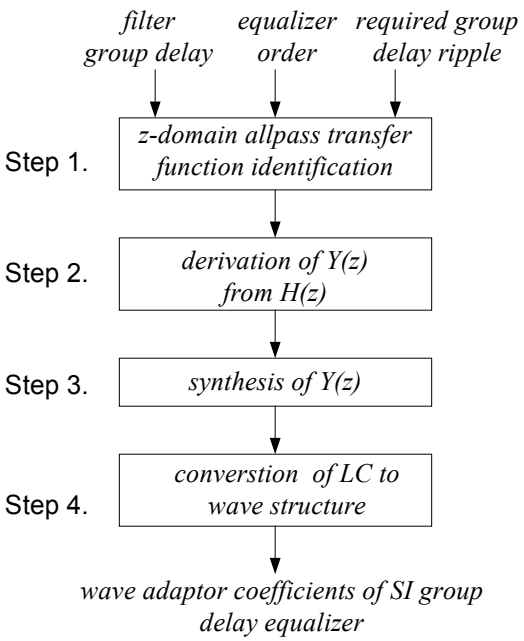

Fig.4 Design flow for SI wave group delay equalizer

The first step involves finding an all-pass circuit transfer function, *H(z)* given by Eq.(1), whose delay response equalizes the filter group delay variation by minimizing the group delay ripple of the combined filter and group delay equalizer. The inputs of first step are: filter group delay variation to be equalized specified in the form of data points (frequency, delay), the order of equalizer *N*, and the required final group delay ripple. The transfer function of the all-pass circuit is produced using an optimization algorithm based on curve-matching approximation as outlined in [7]. To facilitate the optimization process, the all-pass transfer function is expressed in terms of magnitude *R* and phase θ, and then rearranged into the form of Eq.(1). For the 1st-order and 2nd order all-pass section, the group delay expressions are:

$$\tau_1(\omega) = \frac{T(1-R^2)}{1+2R\cos(\omega T)+R^2} \tag{10a}$$

$$\tau_2(\omega) = \frac{T(1-R^2)}{1-2R\cos(\omega T-\theta)+R^2} + \frac{T(1-R^2)}{1-2R\cos(\omega T+\theta)+R^2} \tag{10b}$$

where T is sampling period and $R<1$.

The group delay of the equalizer is the sum of the individual group delay in Eq.(10):

$$\tau(\omega) = \tau_1(\omega) + \sum_{i=1}^{k} \tau_{2i}(\omega)\text{, where the order of } H(z) \text{ is } N=2k+1 \qquad (11)$$

The second step involves obtaining *Y(z)* from *H(z)* according to Eq.(2), whilst the third step carries out the synthesis of *Y(z)* to obtain the *LC* values of the ladder network (C_1, L_2,..C_N), Eq.(6). The final step of design flow derives the wave adaptor coefficients of the SI wave equalizer using Eq.(9) from the *LC* component values produced by step three. To automate the design process of SI wave group delay equalizers, the design flow of Fig.4 has been incorporated into *MATLAB*.

To demonstrate the design flow, three different group delay equalizers have been designed to equalize the group delay variation of the 3rd-order normalized low-pass elliptic SI filter. The group delay and frequency data of the low-pass filter is fed into step one of the design process. Table.1 shows the optimization result of different group delay equalizers. It can be seen the combined ripple of the filter and group delay equalizer reduces as the order of equalizer increase, as expected.

Table.1 Optimization result of different order equalizers

3rd-order low-pass elliptic SI filter, cutoff freq. = 0.1Hz, normalized (*T=1s*) group delay ripple = 2.294s (DC to cutoff frequency)	
3rd-order equalizer	combined filter and equalizer ripple = 0.275s
5th-order equalizer	combined filter and equalizer ripple = 0.193s
7th-order equalizer	combined filter and equalizer ripple = 0.162s

As an example of the z-domain transfer function *H(z)* of the group delay equalizer, Eq.(12) shows the transfer function of the 7th-order equalizer is:

$$H(z) = \frac{z^{-7} + a_1 z^{-6} + a_2 z^{-5} + a_3 z^{-4} + a_4 z^{-3} + a_5 z^{-2} + a_6 z^{-1} + a_7}{a_7 z^{-7} + a_6 z^{-6} + a_5 z^{-5} + a_4 z^{-4} + a_3 z^{-3} + a_2 z^{-2} + a_1 z^{-1} + 1} \qquad (12)$$

Where $a_1 = -2.7$, $a_2 = 3.684$, $a_3 = -3.378$, $a_4 = 2.176$, $a_5 = -0.921$, $a_6 = 0.226$, $a_7 = -0.024$

Fig.5 gives z-domain pole-zero plot of this equalizer. As can be seen, the poles and zeros are reciprocal of one another, confirming the correct theoretical design of the group delay equalizer. The wave adaptor coefficients of group delay equalizer are derived from the obtained *H(z)* according to the design flow. The results are given in Table.2.

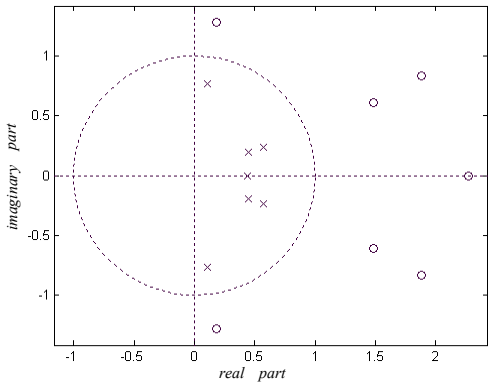

Fig.5 z-plane pole-zero plot of 7th-order group delay equalizer

$\gamma_{00} = 0.8$	$\gamma_{01} = 0.8$	$\gamma_{02} = 0.4$
$\gamma_{10} = 0.6$	$\gamma_{11} = 0.6$	$\gamma_{12} = 0.8$
$\gamma_{20} = 0.533$	$\gamma_{21} = 0.533$	$\gamma_{22} = 0.934$
$\gamma_{30} = 0.51$	$\gamma_{31} = 0.51$	$\gamma_{32} = 0.98$
$\gamma_{40} = 0.5$	$\gamma_{41} = 0.1$	$\gamma_{42} = 1.4$
$\gamma_{50} = 0.054$	$\gamma_{51} = 1.946$	

Table.2 Adaptor coefficients of 7th-order group delay equalizer

4. Simulation examples

Elliptic filters step response often has excessive overshoot mainly due to the fact that such filters have large variations (ripple) in their group delay response. To demonstrate the effectiveness of the design method outlined in section 3, consider reducing the group delay ripple of 3rd-order 100kHz low-pass elliptic SI filter (1MHz sampling frequency) from >2μS to <0.35μS when a suitable group delay equalizer is cascaded with the filter. Using the presented design flow in section 3, it is found that 3rd-order group delay equalizer is needed to achieve the required delay ripple. The equalizer transfer function is:

$$H(z) = \frac{z^{-3} + a_1 z^{-2} + a_2 z^{-1} + a_3}{a_3 z^{-3} + a_2 z^{-2} + a_1 z^{-1} + 1}, \text{ where } a_1 = -0.3314,\ a_2 = -0.686,\ a_3 = 0.38 \qquad (13)$$

From which the adaptor coefficients of the wave structure are calculated as: γ_{00}= 1.0536, γ_{01}=0.838, γ_{02}= 0.1084, γ_{10}= 0.1314, γ_{11}= 1.8686. Fig.6(a) shows the block diagram of the

equalizer, where the block '*CM(-1)/(-2)*' means current mirror with two output: *(-1)* and *(-2)*, corresponding to Fig.1 .

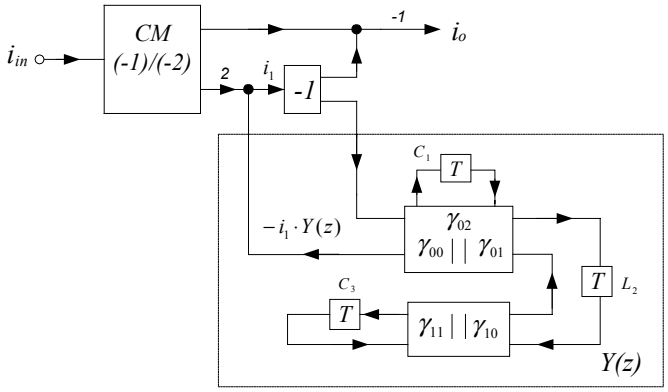

Fig.6(a) block diagram of 3rd-order SI wave equalizer

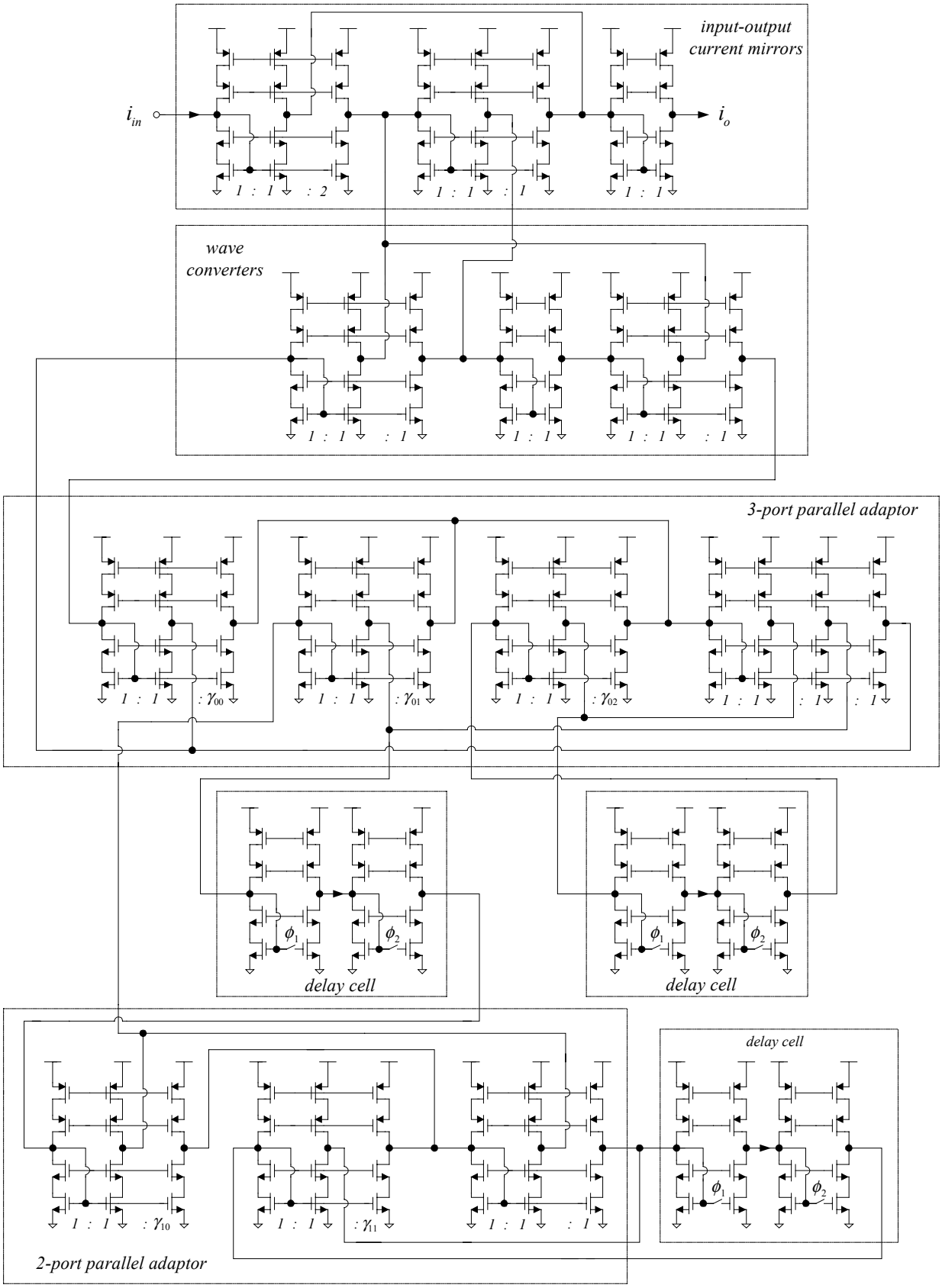

Fig.6(b) Transistor level circuit of 3rd-order SI wave equalizer

Based on 1st-generation delay cells [12] and wave adaptors in [13], Fig.6(b) gives the SI realization of the 3rd-order wave equalizer. The input to wave block *Y(z)* is characterized by wave quantities (A_k and B_k). However, as Fig.1 shown, the all-pass circuit architecture requires current signal input to the block *Y(z)*. So the wave converter is added to Fig.6(b) for converting the current signal to the wave quantities of block *Y(z)*. To improve the equalizer performance, cascode current mirrors were employed throughout the equalizer SI design. Fig.7(a) shows a cascode current mirror, while Fig.7(b) shows a cascode based 1st-generation delay cell. To reduce clock-feedthrough effects in the SI equalizer, CMOS switches were used. Fig.7(c) shows the circuit used for the switches in the transistor-level circuit of 3rd-order group delay equalizer, Fig.6(b). The wave adaptor coefficients are implemented through the ratio aspects (*W/L*) of the current mirrors as shown in Table.3.

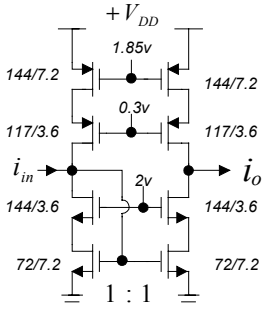

Fig.7(a) Cascode current mirror

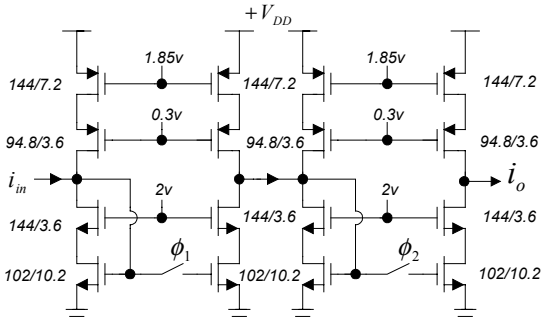

Fig.7(b) Current delay cell

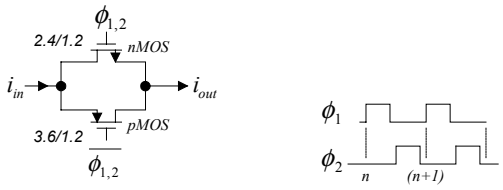

Fig.7(c) CMOS switch and clock phase

Table.3 Coefficients and *W/L* of 3rd –order SI wave equalizer

Port	γ_{ij}	*W/L*
γ_{00}	1.0536	76/7.2

γ_{01}	0.838	60.3/7.2
γ_{02}	0.1084	7.8/7.2
γ_{10}	0.1314	9.5/7.2
γ_{11}	1.8686	134.5/7.2

Other transistors in current mirror have *W/L=72μm/7.2μm*

Fig.8 shows SCNAP4 [14] simulation of the group delay response of the filter, equalizer, and combined filter and equalizer. As can be seen the filter alone has group delay variation of almost 2.29μs between DC and 100kHz. Cascading the filter with the individual equalizers show that the combined filter and equalizer group delay ripple reduces to 0.32 μs. Note the simulated filter was designed using the SI technology outlined in [6].

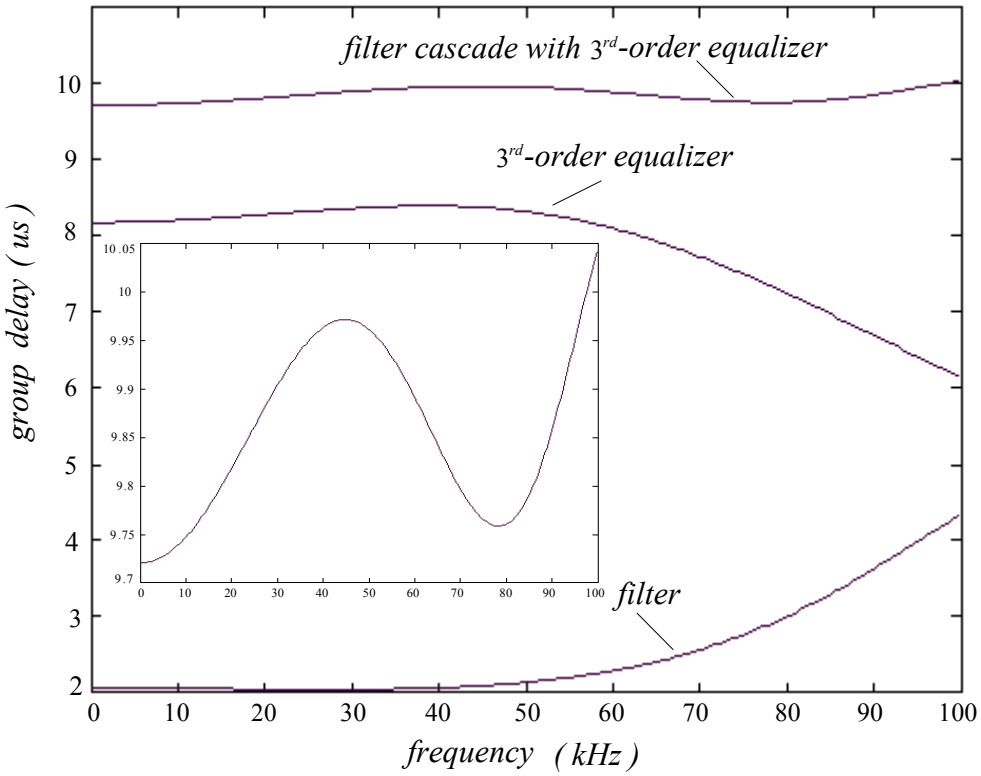

Fig.8 Group delay response of filter, equalizer and filter cascade with 3rd-order equalizer

It has been demonstrated that group delay equalizers derived from ladder-based structure have low amplitude sensitivity [10]. Since the design method given in this paper starts with ladder-

based circuits, it is expected that the group delay wave equalizer has similar low amplitude sensitivity to that reported in [10]. Filters with large group delay variations or non-linear phase lead to waveform distortion in the form of overshoot in the step response. Using typical 1.2μm CMOS process parameters provided by AMS, SPICE level 2 transistor models, bias current of 100μA, and V_{DD}=3.3v, Fig.9, trace (a) shows PSPICE step response of the 3rd-order elliptic SI filter when it is driven by 10 μA input step signal. The response has almost 15% overshoot in this case. Trace (b) shows the same filter step response but in this case the 3rd-order equalizer circuit discussed earlier has been cascaded with the filter. It can be seen that the equalizer has resulted in reducing the amount of overshoot present in the filter step response by more than 50%.

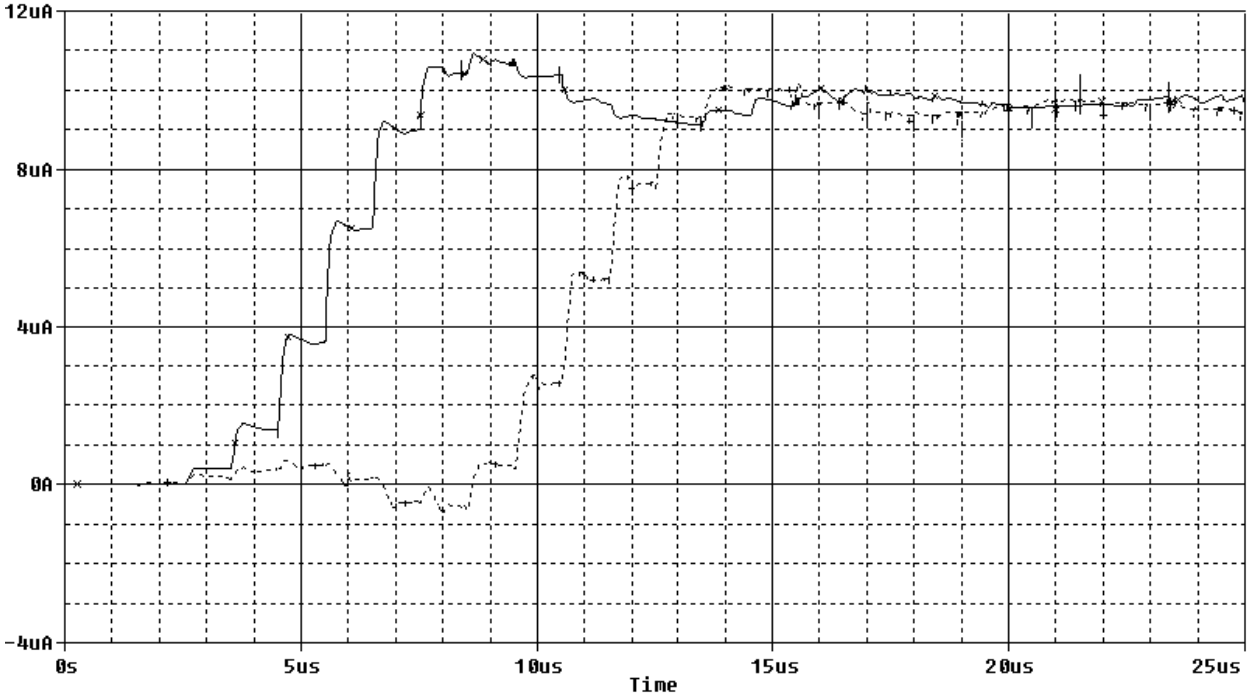

Fig.9 Step response of the filter and filter cascaded with 3rd –order equalizer

(trace *a*: ———— trace *b*: .....)

A. High order group delay equalizers

To obtain higher order SI equalizers using the proposed all-pass circuit architecture (Fig.1) than the third order considered, only requires replacing the driving-point admittance *Y(z)* of Fig.3 with the required order of wave structure generated as outlined in Fig. 4. Expanding *Y(z)* into 5th and

7^{th}-order wave structure, the circuit of 5^{th} and 7^{th}-order SI wave equalizers are designed and simulated, as shown in Fig.10. It can be seen the combined group delay variation is reduced to 0.196 μs and 0.164 μs for the 5^{th} and 7^{th}-order SI wave equalizer, respectively. Note that the inclusion of group delay equalizer with filter increases the propagation delay of the filter, for example the filter propagation delay is approximately 15.4μs when 7^{th}-order equalizer is connected (Fig.10, compared to 2.1 us when no equalizer is connected (Fig.8). This increase in propagation delay needs to be considered carefully in certain applications, and may be reduced during step one of the design flow of Fig.4, if the delay is input as a constraint in the optimization process.

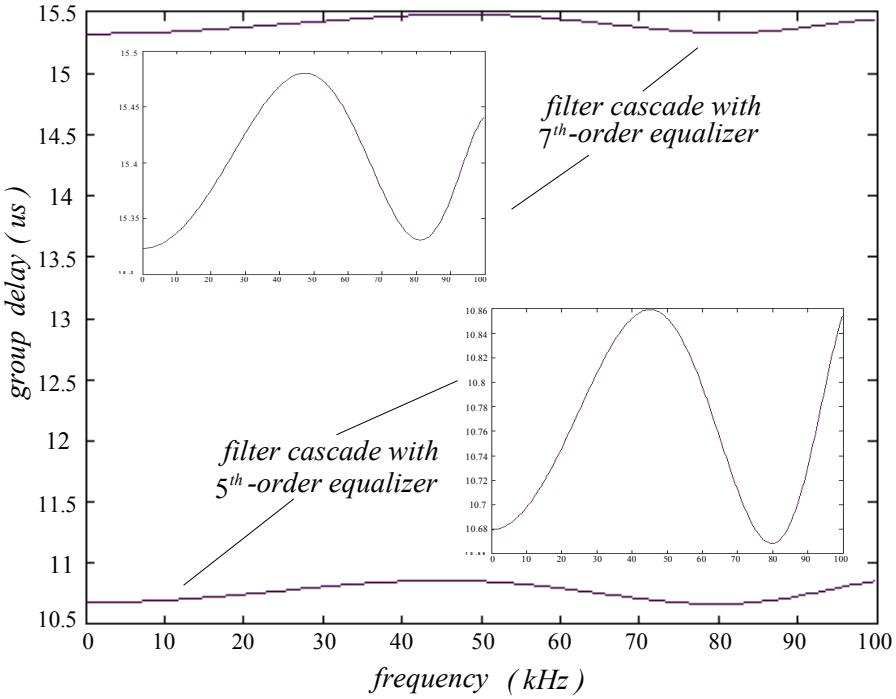

Fig.10 Group delay response of filter cascade with 5^{th} and 7^{th}-order equalizer

To give insight into the complexity of SI equalizers obtained from the proposed all-pass circuit, expressions for predicting the transistor count of a given order equalizer have been developed. The SI circuit complexity depends on the order of equalizer, *N*, and the details is given in Table.4.

Table 4. Complexity of SI wave equalizer for order N

SI element		even	odd	Transistor count
Y(z)	positive delay	N/2	(N+3)/2	16
	negative delay	N/2	(N-3)/2	24
	3-port series adaptor	N/2-1	(N-3)/2	76
	3-port parallel adaptor	N/2-1	(N-1)/2	52
	2-port parallel adaptor	1	1	36
input-output current mirror		1	1	32
wave converter		1	1	32

This table shows the input-output current mirror block and wave converter are required for the all-pass circuits. As outlined in section 4, one positive delay cell, implemented with the 1st-generation cascode structure, has 16 transistors. The transistor numbers of one negative delay cell, 3-port series adaptor, 3-port parallel adaptor and 2-port series adaptor are 24, 76, 52 and 36, respectively. It can be calculated that the number of transistors in an even order SI equalizer is *(84N-28)*. Similarly, the number of transistors in an odd order SI equalizer is *(84N-52)*. For example, if the order of SI wave equalizer is 6, its total transistor count is 476. The power consumption of this simulated 3rd-order SI equalizer circuit is 18.6mW.

5. Conclusions

This paper has presented a design method for group delay equalizers derived from all-pass ladder circuit using wave synthesis technique and implemented in SI technology. This method is based on introducing a new all-pass circuit, where wave structures are employed to generate circuit transfer function. Detailed simulation results based on cascode SI delay cells and wave adaptors for different equalizer orders have been included confirming the presented design method effectiveness in improving the step response of low-pass elliptic filters.

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