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## Design of a 3 $\mu\text{m}$ pixel linear CMOS sensor for earth observation

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### Abstract

A visible wavelength linear photosensor featuring a pixel size of 3  $\mu\text{m}$  has been designed for fabrication using commercial 0.25  $\mu\text{m}$  CMOS technology. For the photo-sensing element, the design uses a special “deep N-well” in P-epi diode offered by the foundry for imaging devices. Pixel reset is via an adjacent p-FET, thus allowing high reset voltages for a wide pixel voltage swing. The pixel voltage is buffered using a voltage-follower op-amp and a sampling scheme is used to allow correlated double sampling (CDS) for removal of reset noise. Reset and signal levels are buffered through a 16:1 multiplexer to a switched capacitor amplifier which performs the CDS function. Incorporated in the CDS circuit is a programmable gain of 1–8 for increased signal-to-noise ratio at low signal levels. Data output is via 4 analogue output drivers for off-chip conversion. Each driver supplies a differential output voltage with a  $\pm 1\text{ V}$  swing for improved power supply noise rejection. The readout circuitry is designed for 12 bit accuracy at frame rates of up to 6.25 kHz. This gives a peak data rate at each output driver of 10 M samples/s. The device will operate on a 3.3 V supply and will dissipate approximately 950 mW. Simulations indicate an equivalent noise charge at the pixel of 66.3  $\text{e}^-$  for a full well capacity of 255,000  $\text{e}^-$ , giving a dynamic range of 71.7 dB.

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### 1. Introduction

As satellite imaging moves out of the realms of governments and into the commercial arena, the need for smaller, cheaper and more numerous satellites is growing. A key step towards meeting this goal is reducing the size of the camera optics

itself. The focal length of the camera is determined by the desired ground resolution, the height of the satellite's orbit, and the pixel size of the imaging device used. Given the many constraints on available orbits, the logical place for improvement is in the image sensor. To this end we are developing a prototype linear photosensor using a pixel size of 3  $\mu\text{m}$ , intended for use in a push-broom satellite imaging system operating in the visible spectrum. Push-broom imagers operate by using a linear sensor oriented perpendicular to the

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direction of travel of the satellite, building up a two-dimensional image one line at a time as the satellite passes over the ground. This system would operate on a principle similar to the British TOPSAT camera system [1], and would enable a ground resolution of 1 m to be achieved. Since a  $3\text{ }\mu\text{m}$  pixel size is beyond the capabilities of most commercial CCD processes, and due to its potential for a high level of systems integration, the sensor will be manufactured using a commercial  $0.25\text{ }\mu\text{m}$  CMOS technology with adaptations for image sensing. The densities of signal routing and components made possible by the use of this technology are essential in meeting the challenge of implementing low noise readout for a pixel pitch of  $3\text{ }\mu\text{m}$ .

## 2. Chip overview

The prototype chip under development consists of a linear array of 4096 square pixels of  $3\text{ }\mu\text{m} \times 3\text{ }\mu\text{m}$ . Each pixel has its own reset transistor, voltage buffers and sampling capacitors. Fig. 1 shows a block diagram of the chip. These are arranged in a scheme to allow both the use of correlated double sampling (CDS) and pipelined readout. This removes the potentially dominating kTC reset noise source and allows for operation with a minimum of dead time. Signals from the pixel level electronics are then multiplexed on a 16:1 basis to a fully differential switched capacitor amplifier which performs the CDS function. A programmable gain of 1–8 is available at this stage by altering the size of the input capacitors to the CDS amplifier. Once the output of the CDS-gain amplifier has settled, the output is passed through a 64:1 multiplexer via a differential buffer to one of 4 high-speed output drivers. These drivers are also fully differential and are capable of driving an external ADC input channel plus tracking capacitance.

For ease of layout the readout structure is split into odd and even pixels and mirrored about the pixel array. Odd pixels are therefore read out on one side and even pixels on the other, allowing pixel level buffers and capacitors to be laid out on a more benign  $6\text{ }\mu\text{m}$  pitch. The four output drivers

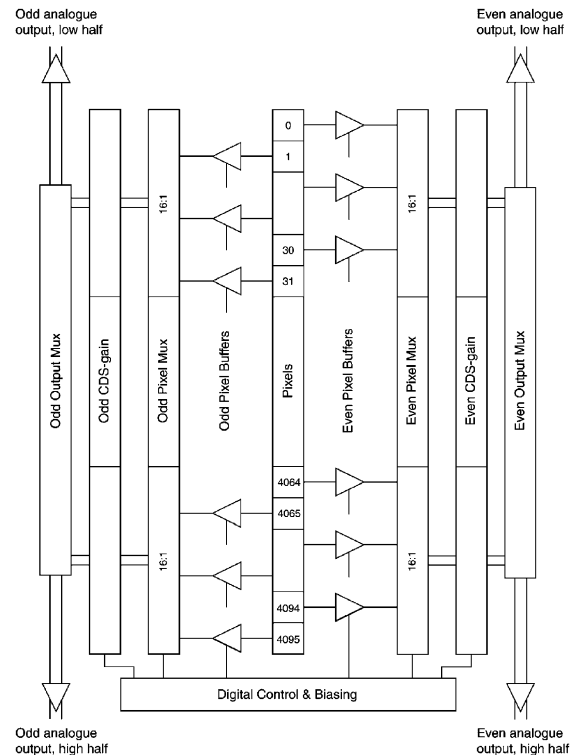


Fig. 1. Block diagram of prototype chip.

are positioned with one in each corner of the chip, each serving half the pixels on a side. Power supplies and biases are brought in at the ends of the array due to the tight layout pitch of the pixel channels, resulting in a need for low wiring resistances.

### 2.1. Photodiode structure

The structure of the photosensor itself is very simple, as can be seen in Fig. 2. The charge collection element is an N-well in P-epi diode measuring  $3\text{ }\mu\text{m} \times 2.4\text{ }\mu\text{m}$ . The manufacturing process to be used is the  $0.25\text{ }\mu\text{m}$  CIS CMOS process operated by TSMC and offers a specially modified N-well implant intended for use in image sensors [2]. This is a low doped well which is driven deeper into the epitaxial layer ( $0.8\text{--}1.0\text{ }\mu\text{m}$ ) than would normally be the case. This has the dual benefit of reducing junction leakage currents (due to lower junction fields) and improving sensitivity to long

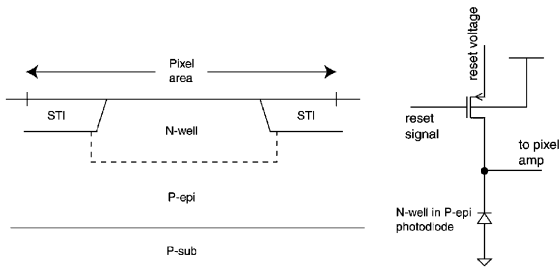


Fig. 2. Structural and schematic design of pixel.

wavelength light, which penetrates further into the silicon. The diode dimensions are selected to be the largest that will fit in the pixel area. This is to reduce charge sharing due to diffusing carriers generated in the silicon below the diodes.

Between integration periods the photodiode voltage is reset using a small p-MOSFET positioned just outside the pixel area. Since there is only a single strip of pixels this can be performed without serious area penalties, as opposed to two-dimensional Active Pixel Sensor (APS) arrays where the reset device is traditionally an n-MOSFET and must be placed inside the pixel. The advantage of using a p-type reset transistor is the higher range of reset voltages it makes available, as the device will effectively pass voltages of within a few 100 mV of the power rails. Due to the nature of the elements contributing to the collection node capacitance, the linearity of the pixel response improves as the reset voltage increases. Using a reset voltage as high as possible will give the best linearity performance; however, this will be limited by the finite operating voltage range of the readout electronics.

## 2.2. Pixel buffering and sampling

Reset and signal voltages on the photodiode node are buffered before being fed to the rest of the readout circuit. The buffering arrangement serves two purposes, firstly it isolates the charge collection node from the rest of the circuit, and secondly it allows for a pipelined readout architecture to be implemented with CDS. The structure of this scheme is shown in Fig. 3.

In this arrangement the pixel amplifier provides the required isolation of the photodiode and the

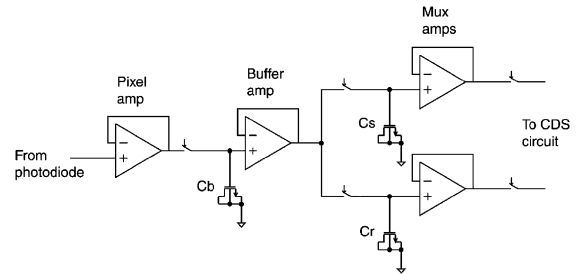


Fig. 3. Pixel buffering and sampling scheme.

drive strength to enable writing to the sampling capacitors. The remaining 3 buffers are present to perform the same function for signals stored on capacitors  $C_b$ ,  $C_r$ , and  $C_s$ . Due to the space limitations involved, these capacitors are realised using n-MOSFET gate capacitances. Operation of the circuit takes place as follows: At the beginning of a frame all pixels are reset to the desired voltage and this level, including kTC noise, is sampled onto  $C_b$  through the pixel amplifier. At this point the integration period begins and charge builds up on the diode capacitance. Towards the end of the integration period the sampled reset voltage is transferred from  $C_b$  to  $C_r$  via the buffer amplifier. Once integration is complete, the signal voltage on the diode is written straight to  $C_s$  through the pixel and buffer amplifiers. Since the reset level has been transferred to  $C_r$ , the capacitor  $C_b$  is ready to accept a new reset level. This sequence means that the only dead time in the system is the time required for the pixels to reset.

As can be seen from Figs. 3 and 4 the buffers used are voltage-followers with the op-amps implemented as cascoded differential pairs. While this method uses considerably more space than a traditional APS source-follower, it confers benefits in terms of gain and linearity. A source-follower in this situation would need to be an n-MOSFET due to the high reset voltage used on the pixel. This will then suffer from sub-unity gain caused by a changing threshold voltage due to the body effect [3]. The voltage-followers used in this case give a gain of around 0.995, in contrast to the source-follower with a gain of around 0.86. Linearity nearly an order of magnitude better at  $\pm 0.25\%$  is also provided by this implementation. While the

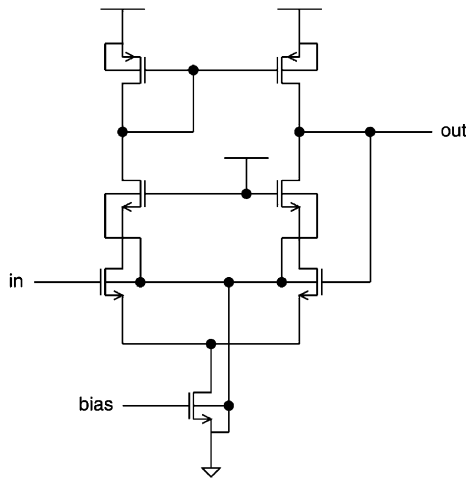
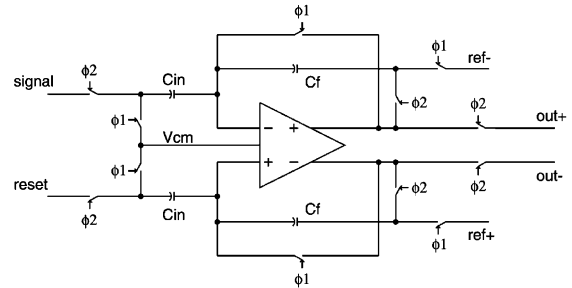


Fig. 4. Voltage-follower buffer architecture.

source-follower generates less noise than the voltage-follower, the low gain negates most of this advantage while also magnifying the effect for noise sources further down the readout chain. It is also worth noting that since both the source and drain of the voltage-follower input device track the gate voltage, as opposed to just the source of the source-follower, the input device contributes less capacitance to the conversion node. This allows a larger device to be used without compromising conversion gain or linearity, improving the noise performance of the buffer.

### 2.3. Correlated double sampling and gain amplifier

Due to the relatively large capacitance of the charge collection node (approximately 20.7 fF), kTC noise from the reset would be very large in this circuit. For this reason a CDS circuit has been included to remove this noise component, although as with all CDS circuits, this gives a  $\sqrt{2}$  increase in noise from the proceeding stages because of the double sample. Given that the two sampling capacitors and buffers are included at the pixel level no extra circuitry is required to perform the CDS function, all that is needed is already present in the switched capacitor gain stage and the fully differential op-amp. Fig. 5 shows the structure of the CDS-gain amplifier feedback network. The gain function is implemented with

Fig. 5. CDS-gain circuit. Switches  $\phi 1$  are closed during reset,  $\phi 2$  during signal processing.

the use of a selectable capacitor bank on the amplifier inputs. The size of the input capacitance can then be controlled to give a particular gain.

Two features of interest are present in the reset configuration of the circuit (switches  $\phi 1$  in Fig. 5). The first is input offset cancellation as the offset is stored across the input and feedback capacitors during reset. In this manner the circuit can remove an amplifier input offset of up to 300 mV without impacting the closed-loop performance of the op-amp. The second involves the introduction of an output offset by charging the output side of the feedback capacitors to reference voltages. Due to the nature of N-in-P photodiodes, the diode capacitance will always be reset to a high voltage which is then reduced by the negatively charged electrons as they are collected. Therefore the signal voltage will always be lower than or equal to the reset voltage. In a fully differential circuit this wastes half the output range of the system. To address this problem offsets are applied during reset so that a zero value differential input signal results in a negative output signal. The magnitude of this output is determined by the difference between the offset reference voltages applied (ref+ and ref- in Fig. 5) and is independent of gain. Offsets of up to  $\pm 1$  V can be accommodated, although only negative offsets are useful. In this manner the full output range of the differential circuit can be utilised.

### 2.4. Output multiplexer

Once the CDS-gain circuit has processed the reset and signal voltages, the data must be brought

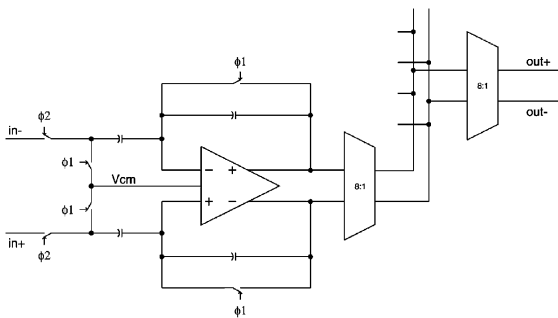


Fig. 6. Mux driver and output multiplexer.

off chip. This is carried out via one of 4 output drivers, and therefore a multiplexer must be placed between the 256 CDS circuits and the output drivers. This multiplexer is broken down into four sections, one for each driver. The multiplexer itself consists of 2 levels of 8:1 multiplexers, which gives an effective trade off between loading and excessive complexity. Due to the necessarily higher speed of the output drivers and multiplexer, a high-speed unity gain buffer is placed after each CDS-gain stage to drive the rapidly changing load to the output. This buffer is a fully differential op-amp in a switched capacitor configuration, as shown in Fig. 6.

The multiplexer itself is controlled by a 2-level shift register. This is designed to increment the register controlling each 8:1 sub-multiplexer as soon as it has been read. The result is that the mux driver can charge the capacitive load of the multiplexer in stages, rather than all at once. This is performed to reduce slewing and ease settling time requirements.

The design of the multiplexer buffer is a traditional three-stage amplifier design with second-stage Miller compensation [4]. The third-stage source-followers are added to isolate the load capacitance from the second gain stage. Speed performance for this circuit is limited by the input capacitance of the output drivers as the source-follower stage slews across much of the output range. Internal biasing gives a slew rate of 66.7 V/ $\mu$ s, and allowing recovery and settling time this restricts the data rate through driver/multiplexer circuit to a maximum of 10MSPS.

## 2.5. Output driver

Data are passed off chip via analogue output drivers at the corners of the chip. Each driver is a unity gain fully differential op-amp capable of driving up to 15 pF of tracking capacitance and 15 pF of ADC input capacitance. A 50  $\Omega$  series resistor is required between each chip output and the external ADC inputs to help isolate the driver from the ADC load. The drivers themselves consist of a differential folded cascode circuit with extra common source output stages to provide the required drive strength.

## 3. Simulated performance

Performance issues for this design can be subdivided into two categories: those associated with the pixel structure and those associated with the readout chain.

The exact performance of the pixel itself is strongly dependent on the details of the fabrication process. Since many of these details such as doping levels, well and diffusion depths, and junction profiles are not made available to users detailed simulation of the pixel (i.e. finite element analysis) is unlikely to yield any meaningful results. However, the chosen process has demonstrated a frequency response suitable for the application [2], and Hspice models provided for the diode structures are available for electrical circuit simulations.

The design of the pixel itself, with the absence of any metal routing, will allow for a fill factor of 100%. This will improve the sensitivity of the device, but may lead to increased charge sharing between neighbouring pixels. The diode has been laid out in such a way as to minimise this effect, but the small pixel pitch and thick epitaxial layer (8  $\mu$ m on  $\sim$ 720  $\mu$ m substrate) employed in the process suggest more serious problems than are encountered with 3.3 and 4  $\mu$ m pixels [2,5]. The large diode size increases the leakage or dark current across its depletion region; however, models for the diode used predict dark current to be around 1.24 fA for a reset voltage of 3 V at 40°C.

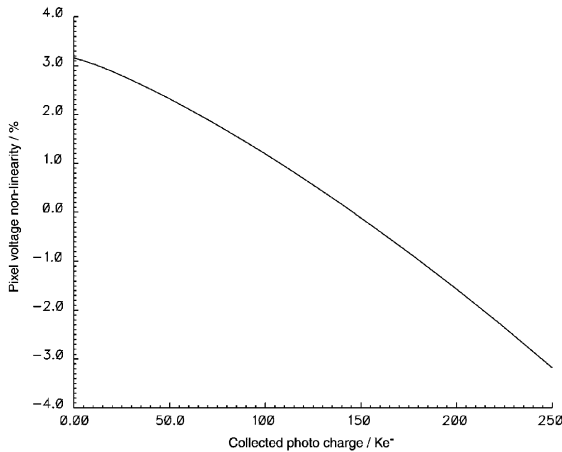


Fig. 7. Pixel node capacitance as a function of charge collected. Reset voltage is 3 V.

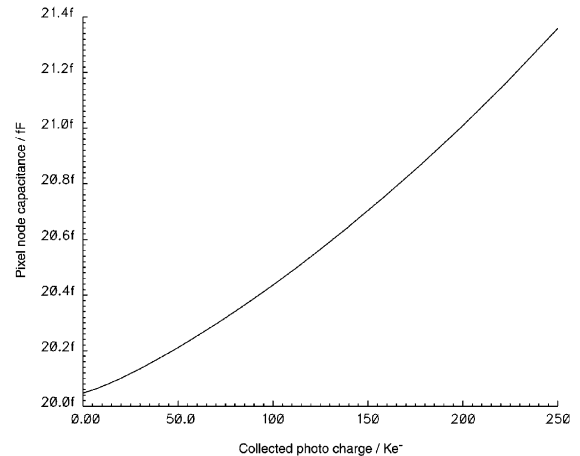


Fig. 8. Pixel node voltage linearity as a function of charge collected. Reset voltage is 3 V.

The linearity of the system is dominated by the voltage dependency of the pixel capacitance. Due to its makeup of depletion regions and an n-MOSFET gate the capacitance of the charge collection node can change substantially over the wide 2 V voltage range employed in this circuit. The change in pixel capacitance can be seen in Fig. 7.

The percentage error graph in Fig. 8 shows the deviation from a nominal equivalent capacitance, in this case of 20.7 fF. Over the full 2 V pixel swing this is  $\pm 3.2\%$ . This gives a conversion gain at the pixel of  $7.75 \mu\text{V}/\text{e}^-$ , and a full well capacity of  $250 \text{ ke}^-$ .

Compared to the pixel characteristics, the errors resulting from the linearity of the amplifiers are almost negligible, being in the range of  $\pm 0.25\%$ . This may be further reduced by using a photo-diode reset voltage below the design maximum of 3 V. This is due to the voltage-follower used for pixel buffering and sampling having an optimal input range of 1–2.5 V range. However, this will have a negative impact on the pixel linearity which may outweigh any benefit gained.

Noise generated in the readout circuit is not dominated by any one source, with the magnitudes of all major sources falling in a narrow range. Noise sources were estimated using Hspice AC simulations, integrating from 1 Hz to 1 GHz. The

Table 1

Noise sources listed by component. Simulated using Hspice, integrating from 1 Hz to 1 GHz

Noise source	Output noise ( $\mu\text{V rms}$ )	Gain to pixel	ENC ( $\text{e}^-$ )
Pixel amp	131.8	0.994	17.11
Buffer amp	89.8	0.990	11.71
Mux amp	87.4	0.986	11.44
CDS gain amp	154.0	0.986	20.15
Mux driver	203.4	0.986	26.65
Output driver	112.1	0.986	14.67
CDS gain amp (reset)	132.6	0.986	17.35
Mux driver (reset)	223.9	0.986	29.30
Output driver (reset)	60.4	0.986	7.90
$C_b$ kT/C	71.3	0.994	9.25
$C_r, C_s$ kT/C	71.3	0.990	9.29
$C_{\text{CDS}}$ kT/C at gain = 1	69.3	0.986	9.07
$C_{\text{mux}}$ at $C_{\text{O/p}}$ kT/C	58.8	0.986	7.69

lower limit was chosen since the noise power in the sub 1 Hz band of the simulated circuits is insignificant relative to that over higher frequencies. The upper limit is a result of specified accuracy limits on the Hspice models provided by the foundry. Table 1 shows the noise contribution from each

Table 2  
Noise sources listed as steps in the readout process

Operation	Output noise ( $\mu\text{V rms}$ )	Gain to pixel	ENC ( $e^-$ )
Write $V_r$ to $C_r$	131.8	0.994	17.11
Transfer $V_r$ to $C_r$	90.7	0.990	11.83
Transfer $V_s$ to $C_s$	149.8	0.990	19.52
$V_r - V_s$ to output	238.1	0.986	31.16
CDS gain amp (reset)	132.6	0.986	17.35
Mux driver (reset)	223.9	0.986	29.30
Output driver (reset)	60.4	0.986	7.90
$C_b$ kT/C	71.3	0.994	9.25
$C_r, C_s$ kT/C	71.3	0.990	9.29
$C_{\text{CDS}}$ kT/C at gain = 1	69.3	0.986	9.07
$C_{\text{mux}}$ and $C_{\text{o/p}}$ kT/C	58.8	0.986	7.69
Total	513.8	0.986	66.30

Simulated using Hspice, integrating from 1 Hz to 1 GHz.

circuit element when simulated in isolation, given as the integrated output noise and equivalent noise charge (ENC) at the pixel. Note that summing these noise contributions to give a total is something of an oversimplification since noise generated in one amplifier is subject to the transfer functions, and hence filtering, of subsequent stages. Table 2 shows integrated noise values when the circuit elements are simulated together. The results have been broken down to reflect the various steps in the readout process of the circuit to take this filtering effect into account. In both cases noise figures are estimates only since filtering due to finite sampling periods is not taken into account.

As can be seen in Table 1, the two main contributors are the low power differential amplifiers used in the CDS-gain circuit and the multiplexer driver. In both cases, these amplifiers produce considerable noise during both reset and sampling phases of their operation. Noise performance in both cases is hampered by the requirement for high bandwidth and low current consumption, since in both cases the circuit is instantiated 256 times on the chip. Following behind these is the pixel voltage buffer amplifier,

Table 3  
Current usage by amplifier

Amplifier	Supply current ( $\mu\text{A}$ )	Instances in design
Pixel amp	10	4096
Buffer amp	10	4096
Mux amp	5	8192
CDS gain diff amp	60	256
Mux driver diff amp	480	256
Output driver diff amp	5000	4

which contributes to the noise twice because of the CDS technique employed. As with the fully differential amplifiers, this circuit cannot be optimised for noise due to constraints placed on it. In this case the contribution of the input n-MOSFET connected to the photodiode towards the conversion capacitance means the gate area must be kept small. The use of a large MOSFET for optimal noise performance would therefore adversely affect both the linearity and the conversion gain of the pixel.

Power consumption and maximum frame rate go hand in hand since the frame rate determines the bandwidth requirements for the amplifiers, and hence their power supply needs. This prototype chip is designed for a minimum frame time of  $160 \mu\text{s}$ , which corresponds to a frame rate of 6.25 kHz. The CDS, multiplexer driver and output driver amplifiers are all designed with sufficient bandwidth and gain to settle to 12-bit accuracy in the time allowed by this frame rate. Operation at  $160 \mu\text{s}$  results in a CDS rate of 100 k samples/s, with the multiplexer driver and output driver running at a burst rate of 10 M samples/s. For every amplifier in the design, the current usage has been kept to the minimum, which coupled with the need for large sampling capacitors to reduce kT/C noise, inevitably leads to problems with output slewing. Amplifiers therefore have bandwidths that are sufficient to settle in an appropriate time once slewing has ceased. Table 3 shows the current requirements of each amplifier and the number of instances in the design. The total current usage for the prototype chip will be 281 mA at a supply voltage of 3.3 V, giving a power dissipation of approximately 930 mW.



#### 4. Conclusions

We have designed a prototype linear photo-sensor using  $3\mu\text{m}$  pixels for use in visible wavelength satellite-based Earth observation. The small pixel size allows for high-resolution imaging with compact camera designs, reducing instrument costs. On-chip CDS removes pixel reset noise while programmable gain allows users to maintain a reasonable signal-to-noise ratio at low signal levels. The feasibility of the device has been demonstrated by simulation, showing good noise performance with a large full well capacity.

The prototype is being fabricated on a commercial  $0.25\mu\text{m}$  CMOS process adapted for image sensors. Successful operation of the prototype would allow for scaling of the concept to more complex devices. Such devices could feature one or more arrays of up to 8096 pixel for larger scale, high-resolution colour imaging. Integrating further systems into the design, such as on-chip

ADCs and advanced control logic, would allow for the construction of a camera-on-a-chip system.

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