

The Influence of BF_2 and F Implants on the $1/f$ Noise in SiGe HBTs With a Self-Aligned Link Base

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Abstract—A study is made of $1/f$ noise in SiGe heterojunction bipolar transistors (HBTs) fabricated using selective growth (SEG) of the Si collector and nonselective growth (NSEG) of the SiGe base and Si emitter cap. The transistors incorporate a self-aligned link base formed by BF_2 implantation into the field oxide below the p^+ polysilicon extrinsic base. The influence of this BF_2 implant on the $1/f$ noise is compared with that of a F implant into the polysilicon emitter. Increased base current noise S_{IB} and base current are seen in transistors annealed at 975°C , compared with transistors annealed at 950 or 900°C . At a constant collector current, both the BF_2 and F implants reduce S_{IB} , whereas at a constant base current, only the BF_2 implant reduces S_{IB} . This result indicates that the BF_2 implant decreases the intensity of the base current noise source whereas the F implant decreases the base current. The proposed explanation for the increased $1/f$ noise is degradation of the surface oxide by viscous flow at 975°C under the influence of stress introduced during selective Si epitaxy. The influence of the BF_2 implant on the noise is explained by the relief of the stress and hence the prevention of viscous oxide flow.

Index Terms— $1/f$ noise, heterojunction bipolar transistors (HBTs), SiGe, stress.

I. INTRODUCTION

OPTIMIZATION of Si bipolar technologies is achieved by a combination of vertical profile design and minimization of parasitic capacitance and resistance, particularly C/B capacitance and base resistance. Minimization of C/B capacitance is generally achieved by using a self-aligned double polysilicon bipolar process [1]. Base resistance is optimized by minimizing the distance between the p^+ polysilicon extrinsic base and the polysilicon emitter, and by silicidating the p^+ polysilicon [2], [3]. More recently, a metallic extrinsic base has been reported, which has delivered an ECL gate delay of just 12 ps in a Si bipolar technology [4].

SiGe adds a new degree of freedom to the vertical profile design through bandgap engineering, but minimization of C/B capacitance and base resistance is equally important. Here the critical issue is the fabrication of the link base region between the intrinsic SiGe base and the p^+ extrinsic polysilicon base. The size of the link base determines the difference in collector and emitter areas and hence impacts both the C/B capacitance and the base resistance. In SiGe technologies employing differential epitaxy [5]–[7], the link base is formed at the perimeter

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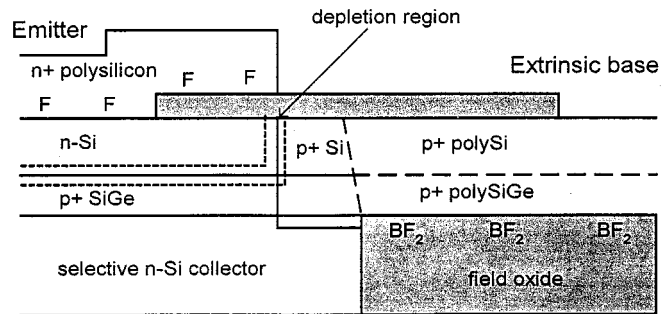


Fig. 1. Schematic illustration of the link base formation and the locations of the F and BF_2 implants in the transistors.

of the active area where the single-crystal base intersects the polycrystalline extrinsic base over the field oxide. In SiGe technologies employing selective growth (SEG) [8]–[11], the link base is formed by the growth of polycrystalline material on a predefined, overhanging p^+ polysilicon extrinsic base. In both approaches, the collector is typically larger than the emitter area by at least an alignment tolerance and some process leeway to allow good linkage of the intrinsic and extrinsic base.

While $1/f$ noise is generally very low in SiGe heterojunction bipolar transistors (HBTs), there is some evidence to suggest that the link base can be a source of $1/f$ noise if it is not correctly optimized [12], [13]. Tang *et al.* [12] showed that recombination centres at the interface between the SiGe intrinsic base and the extrinsic polysilicon base were a source of $1/f$ noise and could be passivated by boron. Sandén *et al.* [13] also showed that the dominant noise source varied strongly with the extrinsic base design. In this paper, a study is made of the influence of a novel self-aligned BF_2 implanted link base on $1/f$ noise in SiGe HBTs produced using SEG of the collector in the same growth step as NSEG of the SiGe base and Si cap. Dramatically increased $1/f$ noise is seen in transistors annealed at 975°C compared with similar transistors annealed at 950 and 900°C . The BF_2 link base implant is shown to eliminate this increased $1/f$ noise. Mechanisms are proposed to explain this behavior.

II. EXPERIMENTAL

Fig. 1 shows a schematic cross-sectional view of the structure of the SiGe HBT. The self-aligned link base was fabricated by implanting 60 keV , $5 \times 10^{15}\text{ cm}^{-2}$ BF_2 into the field oxide over half of the wafer. This scheme allows a direct comparison of transistors with and without the BF_2 implant on the same wafer. The active area was defined by etching through the field oxide down to the underlying silicon. The Si collector was produced

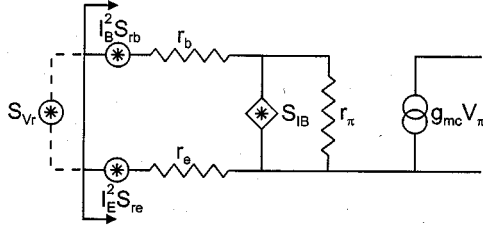


Fig. 2. Small signal equivalent circuit of the bipolar transistor used for $1/f$ noise analysis.

using SEG Si epitaxy [14] in the active area at a pressure of 72 mTorr and a temperature of 800 °C using SiH_4 and PH_3 . The growth conditions were then changed to NSEG epitaxy by changing the pressure and a p-type SiGe base layer (with 7.8% Ge and $\approx 10^{19} \text{ cm}^{-3}$ B) and an n-type Si low-doped emitter grown. The NSEG gives single-crystal material in the active area and polycrystalline material over the field oxide, as illustrated in Fig. 1. The link base was completed by out-diffusion of boron from the field oxide during later high temperature annealing and was self-aligned to the edge of the active area.

A polysilicon emitter was produced by depositing a 200-nm polysilicon layer at 610 °C. At this point, a $5 \times 10^{15} \text{ cm}^{-2}$, 30 keV fluorine implant was made into the polysilicon emitter over half the wafer, orthogonal to the earlier BF_2 implant. As a result, four different types of transistor were created, namely: 1) no F, no BF_2 ; 2) F, no BF_2 ; 3) BF_2 , no F; and 4) F + BF_2 . Fluorine has been shown to give passivation of trapping states at the polysilicon/silicon interface and promotes interfacial oxide breakup [15] and hence would be expected to influence the $1/f$ noise. The polysilicon emitter contact was then implanted with $1 \times 10^{16} \text{ cm}^{-2}$, 70 keV As and patterned, as shown in Fig. 1. The extrinsic base was doped by implanting $5 \times 10^{15} \text{ cm}^{-2}$, 80 keV B into the polysilicon over the field oxide, using the polysilicon emitter contact as a mask. A heat treatment of 60 s at either 900, 950, or 975 °C was used to diffuse the As to the polysilicon/silicon interface and the BF_2 from the buried field oxide.

The noise measurements were carried out on-wafer in the frequency range $f = 1 \text{ Hz}$ to 100 KHz in a common emitter configuration. The C/B voltage was 1.3 V. The base and collector currents were varied from $I_B = 0.01 \mu\text{A}$ to $25 \mu\text{A}$ and $I_C = 0.1 \mu\text{A}$ to 2.5 mA. Measurements were made on devices with an emitter polysilicon area $A_{\text{EFP}} = 14 \times 14 \mu\text{m}^2$, an emitter window area $A_{\text{EWF}} = 6 \times 6 \mu\text{m}^2$ and an active area $A_{\text{AA}} = 14 \times 14 \mu\text{m}^2$ to $22 \times 22 \mu\text{m}^2$.

The noise results were analyzed using the equivalent low-frequency noise circuit of a bipolar transistor shown in Fig. 2, where the noise observed is described by the equivalent input noise current generator and the equivalent input noise voltage generator. The $1/f$ noise of the base current as well as the $1/f$ fluctuations of the internal series emitter resistance r_e and of the internal series base resistance r_b are taken into account in Fig. 2, where the following notations are used: S_{Vr} and S_{IB} are spectral densities of the input $1/f$ noise voltage generator and the input $1/f$ noise current generator (corresponding to the base current $1/f$ noise), respectively; S_{rb} and S_{re} are spectral densities of $1/f$ noise for r_b and r_e , respectively; $r_\pi = dV_{BE}/dI_B$ is the input resistance, $g_{mc} = dI_C/dV_{BE}$ is the collector transcon-

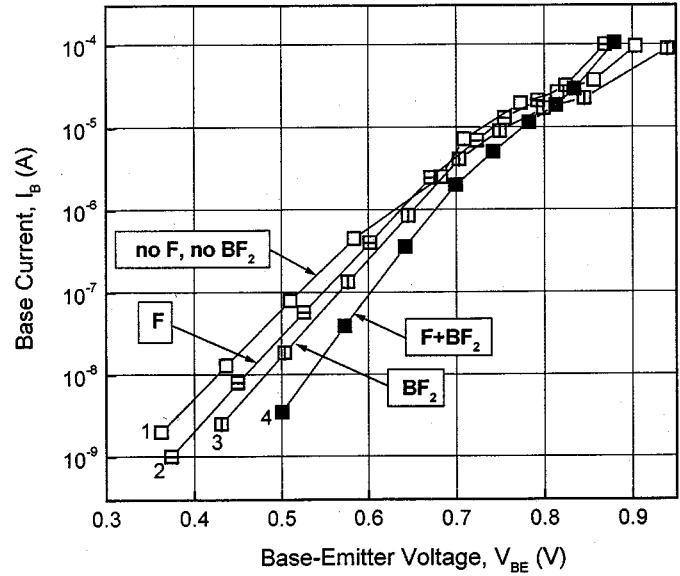


Fig. 3. Base current as a function of base-emitter voltage in SiGe HBTs annealed at 975 °C. Results are shown for transistors 1) without F and BF_2 implants; 2) with a F implant into the polysilicon emitter only; 3) with a BF_2 implant into the buried field oxide only; and 4) with both F and BF_2 implants; $A_{\text{AA}} = 16 \times 16 \mu\text{m}^2$.

ductance, I_E is the emitter current and V_{BE} is the base-emitter voltage. It follows from Fig. 2 that

$$S_{Vr} = I_B^2 S_{rb} + I_E^2 S_{re} + S_{IB}(r_b + r_e)^2. \quad (1)$$

To find the values of S_{IB} and S_{Vr} , the spectral density of the collector current noise S_I under conditions of an open-circuited input (S_I^H) and a short-circuited input (S_I^L) as well as the transistor current gain h_{FE} and the collector transconductance g_{mc} were measured and then the following formulae were used [16]: $S_{IB} = (S_I^H - S_{Vr}/R_B^2)/h_{FE}^2$ and $S_{Vr} = S_I^L/g_{mc}^2$ where R_B is the value of the input load resistor that was used when S_I^H was measured.

III. RESULTS

A. Base Current and $1/f$ Base Current Noise

Fig. 3 shows the base current as a function of base/emitter voltage for the four types of transistor given an anneal at 975 °C. Both the F and BF_2 implants decrease the base current at low base/emitter voltage, but the biggest decrease is obtained when both the F and BF_2 implants are present. The F and BF_2 implants affect the slope of the exponential portion of the base characteristic, changing it from 24 V^{-1} in the case of no implants or only the F implant to 27.1 V^{-1} in the case of the BF_2 implant and to 33.7 V^{-1} in the case of both F and BF_2 implants. The corresponding ideality factors n_B change from 1.65 to 1.18, as summarized in Table I. Such values of n_B point to recombination in the emitter/base depletion region as a significant contribution to the base current. Table I also summarizes the values of collector current at base/emitter voltages of 0.6 and 0.84 V. The collector current is not affected by the F and BF_2 implants in the exponential portion of the characteristic ($V_{BE} = 0.6 \text{ V}$), but the F implant increases the value of I_C at high base/emitter voltage ($V_{BE} = 0.84 \text{ V}$) where the characteristics are determined by

TABLE I
BASE AND COLLECTOR CURRENTS AND BASE CURRENT IDEALITY FACTORS η_B MEASURED AT $V_{BE} = 0.6$ V AND $V_{BE} = 0.84$ V IN SiGe HBTs: 1) WITHOUT F AND BF₂ IMPLANTS; 2) WITH A F IMPLANT ONLY; 3) WITH A BF₂ IMPLANT ONLY; AND 4) WITH BOTH F AND BF₂ IMPLANTS

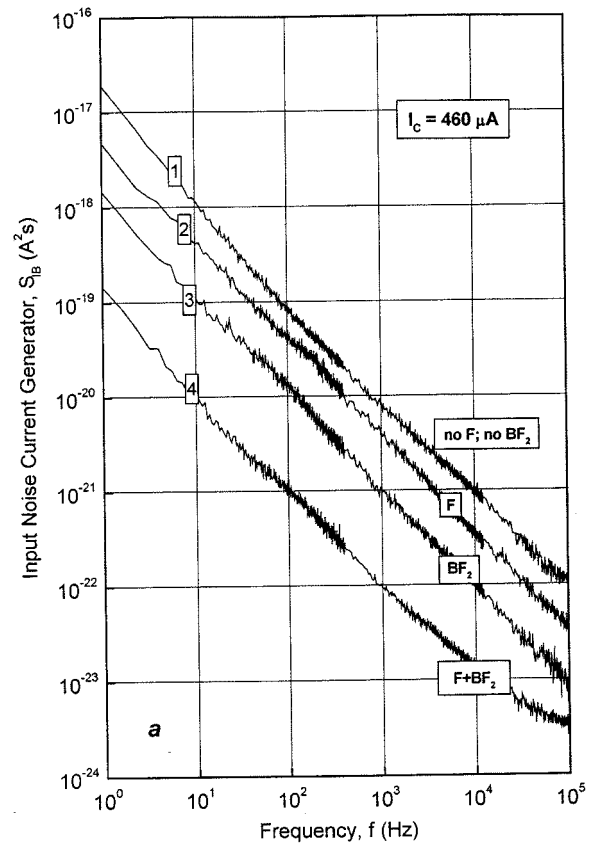
		I m p l a n t			
		no F, no BF ₂	F	BF ₂	F and BF ₂
$V_{BE} = 0.6$ V	I_B , μ A	0.6	0.4	0.24	0.1
	I_C , μ A	1.5	1.5	1.5	1.5
	η_B	1.65	1.65	1.48	1.18
$V_{BE} = 0.84$ V	I_B , mA	0.025	0.05	0.023	0.03
	I_C , mA	1.3	2.5	1.0	2.2

the effects of internal series emitter resistance and/or base resistance, as shown in Table I. A small increase in the value of I_B due to the F implant is also observed in this region.

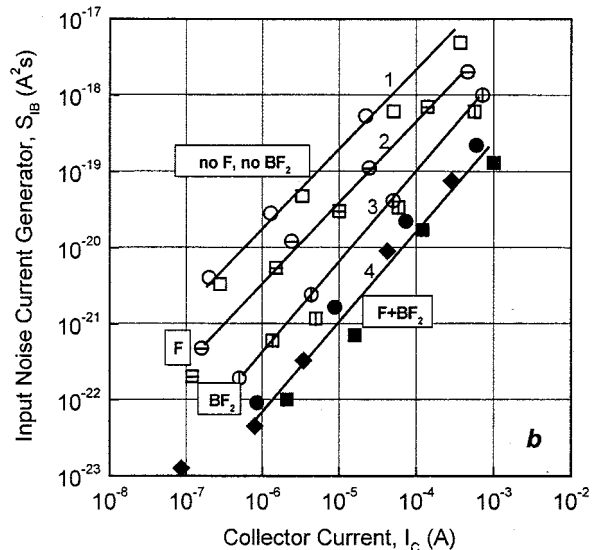
Fig. 4(a) shows the spectra of the base current noise, $S_{IB}(f)$, at a constant collector current $I_C = 460 \mu$ A for the four types of transistor given an anneal at 975 °C. The four spectra are all of $1/f$ type. At a given frequency, both the F and BF₂ implants significantly decrease the base current noise, but the biggest decrease is obtained when both the F and BF₂ implants are present. Fig. 4(b) shows the base current noise $S_{IB}(f)$ measured at a frequency of 2 Hz as a function of collector current. This figure demonstrates that the decrease in base current noise takes place over the whole range of I_C values investigated. At first sight, a comparison of Fig. 3 and Fig. 4(b) suggests that the reason for this effect could be the decrease in base current due to F and/or BF₂ implants, because the base current noise follows a similar trend as the base current. However, the results below show that this is not the case.

Fig. 5(a) shows the spectra of the base current noise $S_{IB}(f)$ at a constant base current $I_B = 7 \mu$ A for the four types of transistors given an anneal at 975 °C. Under these conditions, the F implant does not change the base current noise S_{IB} at a given value of I_B . This means that, in spite of the fact that the F implant affects the value of the base current, it does not change the intensity of the base current noise source. At the same time, the BF₂ implant decreases S_{IB} at a given value of I_B by a factor of 7, irrespective of whether or not a F implant is made. Therefore, it can be concluded that only the BF₂ implant influences the base current $1/f$ noise at a constant base current i.e., gives rise to the decrease of the noise source intensity. The intensity of the noise source is therefore different in the devices implanted with F and BF₂. Fig. 5(b) shows that this conclusion is valid over the whole range of base currents investigated. In addition, it follows from Fig. 5(b) that the base current noise follows a dependence of $S_{IB} \approx I_B^{1.7}$.

Similar measurements of base current and $1/f$ base current noise S_{IB} have been made on transistors annealed at 900 and 950 °C and are summarized in Fig. 6, along with the results for the transistors annealed at 975 °C. The $1/f$ base current noise is summarized in Fig. 6(a) and shows that the F and BF₂ implants have no effect on S_{IB} in transistors annealed at 900 and 950 °C. For transistors annealed at 950 °C, the level of noise is similar to that in the transistors annealed at 975 °C after implant with both F and BF₂. For transistors annealed at 900 °C, S_{IB} is slightly lower than that seen for any of the other anneal temperatures. Values of base current ideality factor are summarized in Fig. 6(b). The ideality factors for transistors annealed at 900 and 950 °C are comparable or significantly better than those in the



(a)



(b)

Fig. 4. Base current noise at different collector currents in SiGe HBTs annealed at 975 °C 1) without F and BF₂ implants; 2) with a F implant into the polysilicon emitter only; 3) with a BF₂ implant into the buried field oxide only; and 4) with both F and BF₂ implants. (a) Dependences of input noise current generator S_{IB} on frequency at $I_C = 460 \mu$ A. (b) Dependences of input noise current generator S_{IB} on collector current at $f = 2$ Hz. Measurements were made on transistors with active areas A_{AA} of $22 \times 22 \mu\text{m}^2$ (circles), $16 \times 16 \mu\text{m}^2$ (squares) and $14 \times 14 \mu\text{m}^2$ (diamonds).

best of the transistors annealed at 975 °C i.e., those implanted with both F and BF₂. These results show that the 975 °C anneal degrades the noise and base current and that the combination of a F and a BF₂ implant can remove much of this degradation.

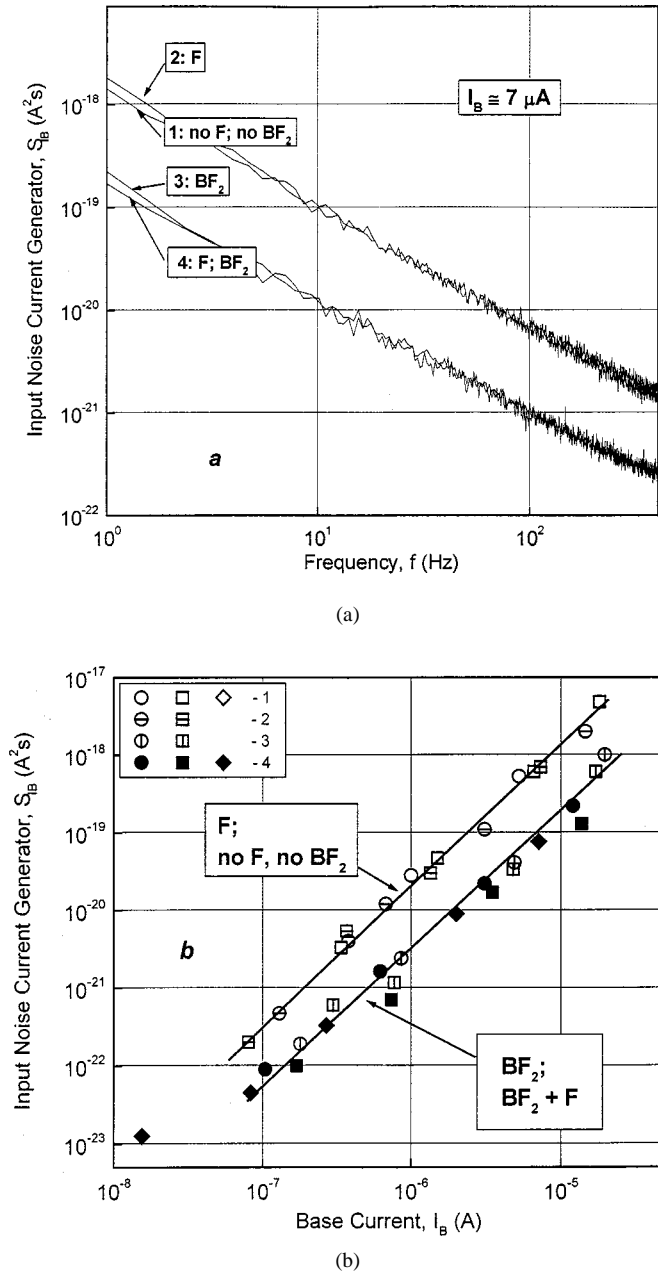


Fig. 5. Base current noise at different base currents in SiGe HBTs annealed at 975 °C 1) without F and BF₂ implants; 2) with a F implant into the polysilicon emitter only; 3) with a BF₂ implant into the buried field oxide only; and 4) with both F and BF₂ implants. (a) Dependences of input noise current generator S_{IB} on frequency at $I_B = 7 \mu A$. (b) Dependences of input noise current generator S_{IB} on base current at $f = 2$ Hz. Measurements were made on transistors with active areas A_{AA} of $22 \times 22 \mu m^2$ (circles), $16 \times 16 \mu m^2$ (squares) and $14 \times 14 \mu m^2$ (diamonds).

B. Input Noise Voltage

Fig. 7 shows the input noise voltage spectra, $S_{V_T}(f)$, measured at $I_E \approx 2$ mA for transistors annealed at 975 °C. As seen, these spectra are also of $1/f$ type and a F implant decreases S_{V_T} by a factor of 16, while an implant of both F and BF₂ decreases S_{V_T} by a factor of 600. In addition, the value of S_{V_T} is found to be unchanged when only the BF₂ implant is made. This can be seen in Fig. 8(a), which shows a graph of S_{V_T} as a function of emitter current, I_E , for the four types of transistors. It can be seen that the data for transistors implanted with BF₂ only (curve 3) and for transistors without

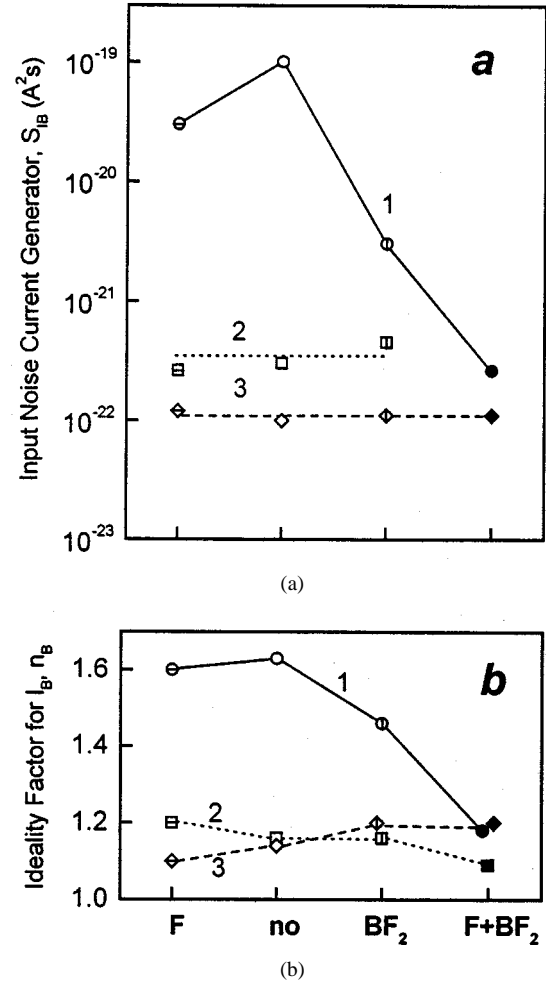


Fig. 6. Effect of anneal temperature on (a) the input noise current generator S_{IB} measured at $V_{BE} = 0.65$ V and $f = 2$ Hz and (b) the values of the base current ideality factor n_B . Results are shown for transistors annealed at 975 °C 1) 950 °C; 2) and 900 °C; and 3) and for transistors without F and BF₂ implants, with a F implant into the polysilicon emitter only, with a BF₂ implant into the buried field oxide only, and with both F and BF₂ implants. Measurements were made on transistors with active areas A_{AA} of $16 \times 16 \mu m^2$.

the F and BF₂ implants (curve 4) fall on a single line. The transistors implanted with F (curve 2) show lower values of S_{V_T} , and the transistors implanted with both F and BF₂ (curve 1) show dramatically lower values of S_{V_T} . For the transistors without the F implant (curves 3 and 4), S_{V_T} follows an emitter current dependence of $S_{V_T} \propto I_E^2$, and for the transistors with the F implant (curves 1 and 2) S_{V_T} follows a dependence of $S_{V_T} \propto I_E^m$ where $m \leq 2$. The base current dependence of S_{V_T} for the transistors implanted with F is shown by curve 2 in Fig. 8(b) and follows a dependence of $S_{V_T} \propto I_B^n$, where $n \approx 1.7$.

IV. DISCUSSION

A. Input Noise Voltage

Considering the input noise voltage results for transistors without the F implant in Fig. 8(a), the emitter current dependence of $S_{V_T} \propto I_E^2$ is typically observed when the $1/f$ noise is due to internal series emitter resistance, as can be seen from the second term on the right-hand side of (1). This observation allows us to conclude that $S_{V_T} = I_E^2 S_{re}$ in the devices without

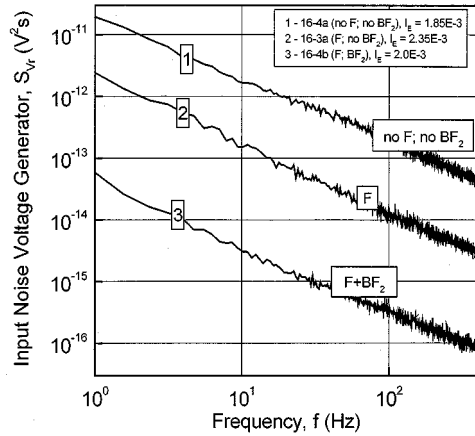


Fig. 7. Dependences of input noise voltage generator S_{Vr} on frequency at $I_E \approx 2$ mA in SiGe HBTs annealed at 975°C 1) without F and BF_2 implants; 2) with a F implant into the polysilicon emitter only; and 3) with both F and BF_2 implants. Measurements were made on transistors with active areas A_{AA} of $22 \times 22 \mu\text{m}^2$.

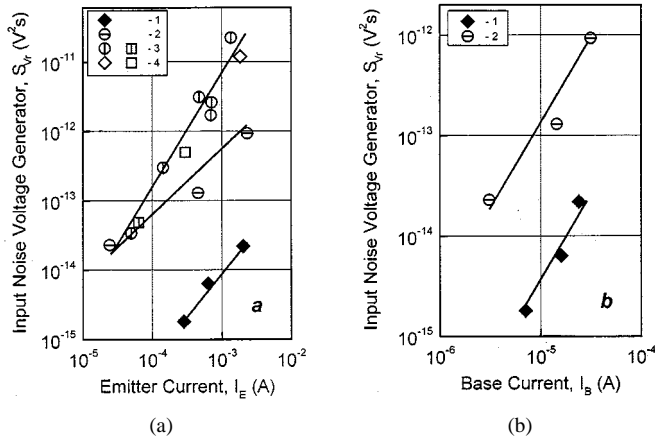


Fig. 8. Input noise voltage generator S_{Vr} as a function of (a) emitter current I_E and (b) base current I_B in SiGe HBTs annealed at 975°C . Results are shown for transistors with 1) both F and BF_2 implants; 2) a F implant into the polysilicon emitter only; 3) a BF_2 implant into the buried field oxide only; and 4) no F and BF_2 implants. Measurements were made at $f = 2$ Hz on transistors with active areas A_{AA} of $22 \times 22 \mu\text{m}^2$ (circles), $16 \times 16 \mu\text{m}^2$ (squares) and $14 \times 14 \mu\text{m}^2$ (diamonds).

the F implant. This means that the fluctuations of the emitter series resistance manifest themselves in the input noise voltage of such devices. The most probable source of these fluctuations is the resistance r_{ox} of the interfacial oxide layer [17]–[20]. That is, we can write $S_{re} = S_{rox}$, where S_{rox} is the spectral density of $1/f$ fluctuations of this resistance. The significant reduction in the value of S_{Vr} observed in the devices implanted with F [Fig. 8(a), curves 1 and 2] indicates that F implantation significantly decreases the value of S_{rox} . Since $S_{rox} \propto r_{ox}^2$ [20], this decrease in S_{rox} indicates that the F decreases the resistance of the interfacial oxide. Hence, these noise results can be regarded as evidence that F promotes interfacial oxide breakup [15] and hence reduces $1/f$ noise, as has been reported previously [17]. It should also be noted that the decrease of r_{ox} explains the increase of both the collector current and the base current observed in the F implanted devices at high base-emitter voltages (Table I).

Considering the input noise voltage of the devices with the F implant, Fig. 8(a) gives an emitter current dependence of $S_{Vr} \propto I_E^m$ where $m \leq 2$. Hence, it is unlikely that the value of $I_E^2 S_{re}$ in (1) is the main contribution to S_{Vr} in this case. On the other hand, the results in Fig. 8(b) give a base current dependence of $S_{Vr} \propto I_B^{1.7}$. Then, bearing in mind that $S_{IB} \propto I_B^{1.7}$ from Fig. 5(b), the conclusion could be drawn that $S_{Vr} \propto S_{IB}$. This suggests that in transistors implanted with F, the input noise voltage generator is given by $S_{Vr} = S_{IB}(r_b + r_e)^2$ in which case, the lower values of S_{Vr} seen in Fig. 8(b) in the devices with both F and BF_2 as compared to devices implanted with just F could be explained by the lower values of S_{IB} in these former devices. This conclusion is supported by the fact that the experimental values of the ratio S_{Vr}/S_{IB} in these transistors appear to be close to the value of $(r_b + r_e)^2$ determined experimentally from measurements of the thermal voltage noise in the base and emitter internal series resistances [16]. Therefore, the effect of the F implant in decreasing S_{Vr} appears to be so strong that the $1/f$ noise of the base current becomes responsible not only for the value of S_{IB} but also for the value of S_{Vr} .

B. Base Current Noise

When developing a model to describe the behavior of the base current and its noise, the following results have to be taken into account:

- 1) For transistors annealed at 975°C the base current is decreased by the F implant and also by the BF_2 implant (Fig. 3).
- 2) For transistors annealed at 975°C , the base characteristics of transistors without F and BF_2 , with F only and with BF_2 only are nonideal ($n = 1.65$ – 1.48), whereas those of transistors with both F and BF_2 are near-ideal ($n = 1.18$).
- 3) For transistors annealed at 975°C , the base current noise is not influenced by the F implant under conditions of constant base current (Fig. 5).
- 4) For transistors annealed at 975°C , the base current noise is dramatically decreased by the BF_2 implant (Fig. 5).
- 5) For transistors annealed at 950 and 900°C , the base current noise is not affected by the F and BF_2 implant under conditions of constant base/emitter voltage and is comparable with or lower than that in the transistors implanted with both F and BF_2 and annealed at 975°C (Fig. 6).

The above results clearly indicate that the 975°C anneal introduces additional base current and noise that is not seen in the transistors annealed at 950 and 900°C . It is also clear that the F and BF_2 implants influence the base current and its noise in different ways.

In order to interpret the different effects of the F and BF_2 implants on the noise, let us suppose that the base current noise can be written as: $S_{IB} = I_B^2 S_X$, where S_X is the noise source present in the transistors annealed at 975°C . Point 4 suggests that the noise source S_X is strongly influenced by the BF_2 implant and point 3 that S_X is not influenced by the F implant. Considering the effect of the F implant on the base current I_B , point 1 indicates that both the F and BF_2 implants influence I_B . In addition, point 2 implies that the base current is due to recombination in

the E/B depletion region in transistors without F and BF_2 , with F only and with BF_2 only.

Recombination in the E/B depletion region can occur at defects, such as misfit dislocations, or at interface states where the E/B depletion region intersects the oxide at the perimeter of the emitter. TEM studies have been made on these transistors and no evidence of misfit dislocations found [14], which implies that the most likely explanation is recombination at interface states. The best candidate for the noise source S_X in the case where I_B is due to recombination at the oxide/silicon interface is surface noise. A model of such a noise has been proposed by McWhorter [21]. The source of the $1/f$ noise in this model is considered to be charge fluctuations at slow oxide traps within the oxide that can modulate the recombination velocity at the interface.

The effect of the F implant on the base current could then be explained by passivation of the interface states by the F, as has been reported previously [15]. This passivation is likely to have occurred by F diffusion through the polysilicon and deposited oxide where the polysilicon overlaps onto the deposited oxide [22]. This is possible because F readily diffuses through polysilicon [23] and silicon dioxide [24]. The absence of any effect of the F implant on S_X suggests that the F implant has no effect on the concentration of slow traps. This would then explain why the F implant has no effect on the base current noise when measurements are made under conditions of constant base current (Fig. 5).

To explain the effect of the BF_2 implant on the base current and its noise, we need to find a mechanism that enables the BF_2 implant into the buried field oxide to influence the oxide/silicon interface at the perimeter of the emitter. In the transistors measured, this distance is several micrometers, and hence the mechanism has to involve action-at-distance. Boron diffusion from the buried field oxide can be discounted because of the low anneal temperatures and the low diffusion coefficient of boron in silicon. Diffusion of fluorine from the buried field oxide to the emitter/base junction might be possible because of the high diffusivity of fluorine in oxide and polysilicon [23], [24]. However, this explanation is not consistent with the results in Fig. 5, which shows that F has no effect on the base current noise when the measurements are made under conditions of constant base current.

One mechanism that does satisfy the criterion of action-at-distance is stress. There is some evidence of the presence of stress in our devices resulting from the selective silicon epitaxy used to grow the collector. TEM micrographs show fringes originating from the buried field oxide [25], indicating that the thin TEM foil is distorted due to the presence of stress between the buried field oxide and the silicon collector. There is considerable evidence in the literature that stress gives rise to increased $1/f$ noise. For example, early work by Brophy [26] showed that the deformation of germanium led to increased $1/f$ noise. More recently, work on nitrided MOSFETs [27], [28] has shown that high surface $1/f$ noise is measured due to stress created by the nitrided gate oxides and that stress relief decreases this noise. These results would be consistent with the results in this work.

To explain the reduction of noise in the BF_2 implanted transistors annealed at 975°C , the BF_2 implant would have to reduce the stress at the oxide/silicon interface. It is possible that

fluorine bubbles introduced into the buried field oxide during the BF_2 implant might provide such a stress relief mechanism. Several researchers [29], [30] have shown the presence of inclusions when BF_2 or F is implanted into polycrystalline silicon. These inclusions are related to the presence of the fluorine and it is postulated that they could contain gaseous [29], liquid, or solid material [30]. To the authors' knowledge, no work has been reported on the properties of fluorine implanted into silicon dioxide. However, it is highly likely that analogous bubbles or voids would be created. Such defects in the buried field oxide could provide a possible mechanism for strain relief during the 975°C anneal. There is some evidence in the literature to suggest that stress relief can occur as a result of the implant of a gas. For example, an argon implant into the back of a silicon wafer has been found to reduce the stress at the front surface of the wafer and reduce $1/f$ noise [27], [28].

Finally, it is necessary to consider why an anneal at 975°C gives increased $1/f$ noise, whereas anneals of 950°C and 900°C do not. The temperature of 975°C is coincidentally very close to the temperature at which viscous flow of oxide would be expected to occur. Eer Nisse [31] showed that viscous flow of oxides occurred at a temperature of 960°C . Based on this information, we would expect viscous oxide flow to occur in the transistors annealed at 975°C , but not in the transistors annealed at 950°C and 900°C . The stress due to the selective collector epitaxy might provide the driving force for the viscous flow in the transistors annealed at 975°C . In addition, the reduction of the stress by the BF_2 implant into the buried field oxide might be expected to reduce the viscous flow. Based on these arguments we propose that viscous flow of the deposited surface oxide during the 975°C anneal could have degraded the oxide quality, introducing interface states and slow oxide states that give rise to the high values of I_B and S_X , respectively.

V. CONCLUSIONS

A study has been made of $1/f$ noise and base current in SiGe HBTs fabricated using selective epitaxy for the silicon collector and NSEG epitaxy for the SiGe base and the n-Si cap. Two noise sources have been identified in transistors annealed at 975°C . The first is an intense noise source due to recombination base current at the oxide/silicon interface where the emitter/base depletion region intersects a deposited oxide. This source is absent in transistors annealed at 950°C and 900°C . The second is due to the resistance of the polysilicon emitter interfacial oxide layer. The intensity of the first source is decreased significantly when a BF_2 implant is made into the buried field oxide to create a link-base. The intensity of the second noise source is decreased significantly when a F implant is made into the polysilicon emitter. In addition, both implants decrease the recombination base current.

The influence of the BF_2 implant on the noise is attributed to the relief of stress created by the selective epitaxial growth of the silicon collector. It is proposed that the stress induces viscous flow of the deposited surface oxide during the 975°C anneal, and hence increases the density of fast interface traps and slow oxide traps. The relief of the stress by the BF_2 implant

into the buried field oxide removes the driving force for the viscous oxide flow and hence reduces the oxide degradation and the resulting $1/f$ noise. Viscous oxide flow does not occur at temperatures of 900 and 950 °C and hence increased $1/f$ noise is not seen for these anneal temperatures. The influence of the F implant on the noise is attributed to the decrease of the resistance of the emitter interfacial oxide layer by the breakup of the interfacial layer, induced by the F.

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