Impact of *Ex-Situ* and *In-Situ* Cleans on the Performance of Bipolar Transistors With Low Thermal Budget *In-Situ* Phosphorus-Doped Polysilicon Emitter Contacts

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***Abstract*—This paper investigates the effects of an *in-situ* hydrogen bake and an *ex-situ* hydroflouric acid (HF) etch prior to polysilicon deposition on the electrical characteristics of bipolar transistors fabricated with low thermal budget *in-situ* phosphorus-doped polysilicon emitter contacts. Emitter contact deposition in a UHV-compatible low pressure chemical vapor deposition (LPCVD) cluster tool is also compared with deposition in a LPCVD furnace. Transmission electron microscopy (TEM) and secondary ion mass spectroscopy (SIMS) are used to characterize the emitter contact material and the interface structure and a comparison is made with Gummel plots and emitter resistances on bipolar transistors. The SIMS results show that an *in-situ* hydrogen bake in a cluster tool gives an extremely low oxygen dose at the interface of 6.3×10^{13} cm^{-2}, compared with 7.7×10^{14} and 2.9×10^{15} cm^{-2} for an *ex-situ* HF etch and deposition in a cluster tool or a LPCVD furnace, respectively. TEM shows that the *in-situ* hydrogen bake results in single-crystal silicon with a high density of defects, including dislocations and twins. The *ex-situ* HF etch gives polycrystalline silicon for deposition in both a cluster tool and a LPCVD furnace. The single-crystal silicon emitter contact has an extremely low emitter resistance of 21 $\Omega.\mu$m^2 in spite of the high defect density and the light emitter anneal of 30 s at 900 °C. This compares with emitter resistances of 151 and 260 $\Omega.\mu$ m^2 for the polycrystalline silicon contacts produced using an *ex-situ* HF etch and deposition in a cluster tool or a LPCVD furnace, respectively. These values of emitter resistance correlate well with the interface oxygen doses and the structure of the interfacial oxide layer. The high defect density in the single-crystal silicon is considered to be due to the high concentration of phosphorus ($>5 \times 10^{19}$ cm^{-3}) in the as-deposited layers.**

***Index Terms*—Bipolar transistor, cluster tool, *in-situ* doped polysilicon, polycrystalline silicon, polysilicon, polysilicon emitter.**

I. Introduction

POLYSILICON emitter contacts [1] have become a vital part of today's bipolar and BiCMOS technologies because they provide a means of realizing an exceptionally shallow emitter/base junction while maintaining a reasonable peripheral emitter/base capacitance. In polysilicon emitter contacts, an interfacial oxide layer is invariably present at the polysilicon/silicon interface, which has the advantage of increasing the current gain [2], [3] but the disadvantage of increasing the emitter resistance of the transistor [4]–[7]. A considerable amount of work has been published in the literature on the effects of the interfacial oxide on the base current [8]–[11] and emitter resistance [4]–[7], [12], [13] of polysilicon emitter contacts. It has been found that the nature of the interfacial oxide is significantly influenced by a number of factors, including the type of *ex-situ* clean (typically an HF etch) used prior to polysilicon deposition [9], [14], the polysilicon deposition conditions [15], [16], and the subsequent annealing conditions [8]. A common requirement in all the work mentioned above is the need to achieve a well controlled interfacial oxide that gives low values of emitter resistance.

The use of a cluster tool for polysilicon deposition is one approach that has been used to achieve good control over the interfacial oxide. Cluster tools are designed to integrate several process steps in one system, so in the context of polysilicon emitter contacts a cluster tool can be used to carry out an *in-situ* interface clean prior to the deposition of *in-situ* doped polysilicon [17]–[25]. Berthold *et al.* [23], using an *ex-situ* HF dip etch and reoxidation in a cluster tool, showed that the interfacial oxide can be varied in a controlled manner from 0.2–1.0 nm. This approach allows the interfacial oxide thickness to be optimized to give an improved gain and an acceptable value of emitter resistance [17], [19]–[23]. For example, Decoutere *et al.* [19] and Simeon *et al.* [20] showed that an interfacial oxygen dose of 2.6×10^{15} cm^{-2} (equivalent to a uniform layer of thickness $\approx$ 0.5 nm, assuming that the oxide is stoichiometric SiO_2) gave an emitter resistance of 170–200 $\Omega \cdot \mu$m^2 and at the same time a current gain enhancement by a factor of two. This was achieved by carrying out an *in-situ* HF vapor etch followed by dry reoxidation in a cluster tool. Similar results were obtained by Hendriks [17], who grew interfacial oxides with thicknesses of 0.5–1.0 nm, and obtained an emitter resistance of 100 $\Omega \cdot \mu$m^2 and a gain improvement by a factor of two. Other authors have used an *in-situ* HF vapor etch [17]–[21] in a cluster tool and obtained emitter resistances of 90 [17], 74–80 [22] and 106 $\Omega \cdot \mu$m^2[19], [20]. However, for deep submicron polysilicon emitters, lower emitter resistance values are required.

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A related area of research where surface cleaning techniques are of paramount importance is low temperature epitaxy [26]–[32]. Two alternative approaches have been used to generate a clean surface prior to epitaxy. In the first approach, an *ex-situ* HF etch is used to give a hydrogen-passivated, hydrophobic silicon surface. This hydrogen passivated surface is air-stable and remains oxide-free for around 10 min [33]. Using this method, device quality Si and SiGe epi-layers were obtained at 550 °C or lower without employing any *in-situ* surface cleaning process. In the second approach, an *in-situ* hydrogen bake is used to desorb the surface oxide prior to growth [34]. The surface oxide is generally removed by thermal desorbtion at a temperature above 800 °C in hydrogen or above 950 °C in ultrahigh vacuum [34].

The use of a cluster tool for emitter contact deposition offers the prospect of achieving very low values of emitter resistance as a result of the clean growth environment and the ability to carry out an *in-situ* clean immediately prior to growth of the emitter contact material. However, to date, little has been published on the best combination of *ex-situ* and *in-situ* cleans needed to achieve this goal, particularly under conditions where low thermal budget emitter anneals are used. In this paper, a comparison is made of the effects of an *ex-situ* HF etch and an *in-situ* hydrogen bake emitter contact clean on the performance of bipolar transistors given low thermal budget emitter anneals. The deposited layers are *in-situ* doped with phosphorus rather than arsenic, because it has a higher diffusivity and hence, is potentially a better candidate for low thermal budget polysilicon emitters. A comparison is made between the *in-situ* phosphorus doped and conventional arsenic implanted emitter contacts. TEM images show that the *in-situ* hydrogen bake results in an emitter contact that is single-crystal silicon with a high density of defects, including dislocations and twins. Bipolar transistors fabricated using this high defect density silicon emitter contact have an emitter resistance as low as 21 $\Omega.\mu m^2$ even after a light emitter anneal of only 30 s at 900 °C.

II. Experimental Procedure

A very light emitter anneal of 30 s at 900 °C was chosen for this work in order to investigate the properties of low thermal budget polysilicon emitter contacts of the type that may be required in future deep submicron technologies or SiGe HBT technologies. This thermal budget is considerably lighter than that currently used for production polysilicon emitter contacts, where the emitter anneal is generally carried out at a temperature in the range 1000–1055 °C [25], [35]–[39]. With a thermal budget as low as 30 s at 900 °C, it is difficult to obtain sufficient out-diffusion of dopant from the polysilicon to push the emitter/base depletion region away from the polysilicon/silicon interface. This is particularly problematic for the arsenic implanted control devices, because of the lower diffusion coefficient of arsenic than phosphorus. In order to facilitate the comparison of *in-situ* doped phosphorus emitters with ion implanted arsenic emitters, a low doped emitter was fabricated by ion implantation prior to emitter fabrication. The doping was chosen to be low enough to minimize Auger recombination, so that the low-doped emitter was transparent to minority carriers injected from the base [40]. This has the effect of making the base current very sensitive to the properties of the interface.

The starting material used for this work was (100) n on n+ material with an epitaxial resistivity of 0.5 Ω·cm. The base was fabricated by implanting 2.5×10^{13} cm^{-2} boron at 80 keV through an 80 nm thermal oxide layer and then annealing for 150 min at 1025 °C in nitrogen. The low-doped emitter was used in all the devices and was formed by implanting 70 keV, 5×10^{14} cm^{-2} phosphorus through an 80 nm screen oxide and annealing for 120 minutes at 950 °C in nitrogen. SIMS profiles indicate that this process delivers a low-doped emitter with a width of 220 nm and a peak doping concentration of 1×10^{19} cm^{-3}.

Two interface cleans carried out prior to growth were investigated. The first was a clean which is commonly used in polysilicon emitter contacts, namely an *ex-situ* etch in 7 : 1 buffered HF for 15 s. The second was a clean that is commonly used in low temperature epitaxy [26]–[34] and is a combined *ex-situ* and *in-situ* clean. The *ex-situ* clean comprised an RCA clean plus a 100 : 1 HF dip etch for half the time taken for the wafer to become hydrophobic. The *in-situ* clean consisted of a 5 min *in-situ* hydrogen bake at 900 °C in 100 sccm of hydrogen at 1 Torr. The purpose of the hydrogen bake was to remove the interfacial oxide remaining after the RCA clean and the 100 : 1 HF dip etch. *In-situ* phosphorus doped polysilicon was deposited in a Thermo VG Semicon CV 200 System [41], which consists of two identical growth chambers linked by a load lock. The deposition time was 13 min and used a mixture of 100% SiH_4 and 0.01% PH_3 with flow rates of 100 and 50 sccm at a temperature of 750 °C and a pressure of 1 torr.

For comparison purposes, a conventional arsenic implanted polysilicon emitter contact was also fabricated. This was given an *ex-situ* HF etch, and 200 nm of polysilicon was deposited in a conventional ASM LPCVD furnace in 25%, 200 sccm of SiH_4 at 610 °C and 0.39 Torr. The polysilicon was doped by implanting a dose of 1×10^{16} cm^{-2} arsenic at 45 keV. A low temperature oxide was deposited at 400 °C on all devices to prevent dopant loss during the 30 s emitter anneal at 900 °C. An unpatterned *in-situ* phosphorus doped test wafer (i.e., not a device wafer) was also produced. This wafer was given a hydrogen bake, a 20 min deposition using the same growth conditions as the device wafers and was not given an emitter anneal.

Electrical characterization in the form of Gummel plots and emitter resistance measurements of the transistors were performed on a HP 4145 parameter analyzer attached to an HP 9133 personal computer. TEM and SIMS analysis were performed on the same wafers as the devices to determine the micro-structure and the phosphorus and oxygen profiles. The TEM analysis was carried out using $\langle 110 \rangle$ cross-sections and $\langle 110 \rangle$ on-axis images were obtained.

III. Results

A. Material and Interface Characterization

Fig. 1 shows cross-section TEM images of the three types of sample after completion of device processing (i.e., after the emitter anneal). Fig. 1(a) shows the sample given an *ex-situ* HF etch prior to the deposition of *in-situ* phosphorus doped polysilicon. The layer is 350 nm thick and TEM selected area diffraction

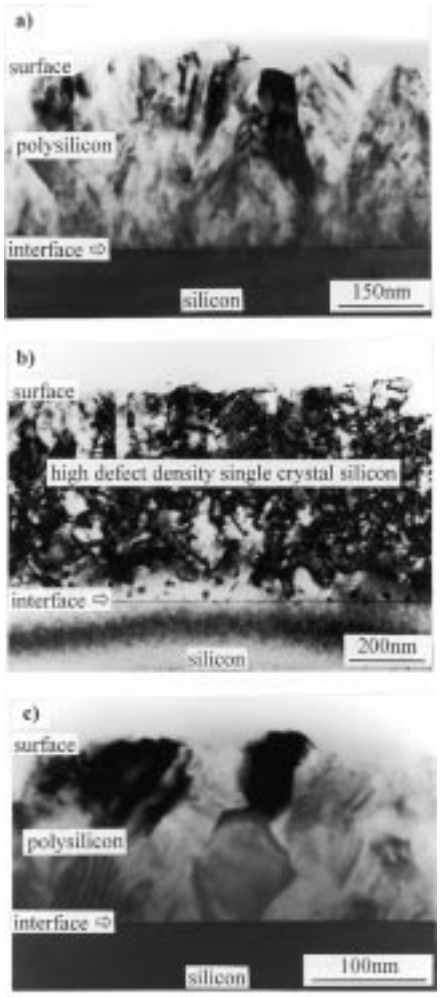

Fig. 1. Cross-section of TEM images of the device samples after the emitter anneal of 30 s at 900 °C. (a) *Ex-situ* HF etch and *in-situ* phosphorus doped deposition. (b) *In-situ* hydrogen bake at 900 °C and *in-situ* phosphorus doped deposition. (c) *Ex-situ* HF etch and arsenic implanted LPCVD deposition.

patterns (not shown) show that it is polycrystalline. There is no significant epitaxial regrowth of the polysilicon, though there is some evidence of roughening at the polysilicon/silicon interface that is indicative of small holes in the interfacial oxide and local epitaxial regrowth. Fig. 1(b) shows the sample given an *in-situ* hydrogen bake prior to the deposition of *in-situ* phosphorus doped material. The layer is 570 nm thick and TEM selected area diffraction patterns (not shown) show that it is single-crystal silicon. The dark line in the micrograph is due to small discrete balls of interfacial oxide at the position of the original interface. The single-crystal layer contains different types of defects, including dislocations and twins. The defect density increases with distance from the interface up to a depth of ~300 nm, and between this depth and the surface the layer contains a high density of defects. Fig. 1(c) shows the arsenic implanted control device. This layer is 160 nm thick and TEM selected area diffraction patterns indicate that it is polycrystalline, as expected. The polysilicon/silicon interface is smooth, indicating that there is little or no interfacial oxide break up or epitaxial regrowth.

The *in-situ* phosphorus doped layers given the hydrogen bake are single-crystal silicon even after deposition. This is illustrated

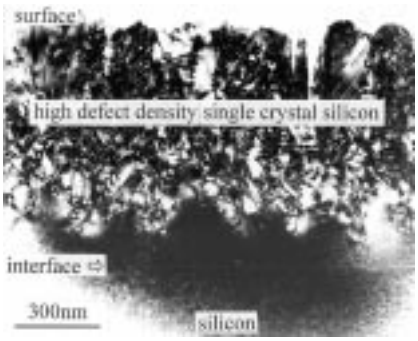

Fig. 2. Cross section TEM image of an unpatterned sample after deposition. The sample was given an *in-situ* hydrogen bake prior to *in-situ* phosphorus-doped deposition.

in Fig. 2, which shows a TEM image of an unpatterned wafer immediately after deposition. The wafer was given a hydrogen bake at 900 °C prior to deposition of the *in-situ* phosphorus doped layer and not given an emitter anneal. The layer is 850 nm thick and shows a 90-nm-wide region immediately above the interface that is relatively defect-free below a region that contains a high density of defects. The fact that the layer is single-crystal, i.e., epitaxial growth has occurred, suggests that the interfacial oxide was not continuous after the hydrogen bake. The thicker layer in this sample compared to that in Fig. 1(b) is due to the use of a longer growth time.

Fig. 3 shows SIMS profiles for layers after the emitter anneal. Fig. 3(a) shows the phosphorus SIMS profiles for the *in-situ* doped layers given either an *in-situ* hydrogen bake or an *ex-situ* HF etch. The phosphorus concentration is between 5 and 8 $\times$ 10^{19} cm^{-3} for both layers over the majority of the thickness of the layer. However, for the layer given a hydrogen bake, the phosphorus concentration decreases to a value of 3.5 $\times$ 10^{19} cm^{-3} immediately adjacent to the interface. Interface peaks occur for both layers, which are presumably due to segregated phosphorus at the original silicon surface. The *ex-situ* HF etch sample is 350 nm thick, and the *in-situ* hydrogen bake sample is 570 nm thick. The deposition time was the same for the two layers, so the difference in thickness suggests either a difference in incubation time for layers grown after an *ex-situ* HF etch and an *in-situ* hydrogen bake or a difference in growth rate for polysilicon and single-crystal silicon.

Fig. 3(b) shows oxygen SIMS profiles for the phosphorus *in-situ* doped layers and the arsenic implanted control layer. For the arsenic implanted control sample there is a large oxygen interface peak with an integrated dose of 2.9 $\times$ $10^{15}/cm^2$. For the *in-situ* phosphorus-doped layer given an HF etch, there is a similar peak with a dose of 7.7 $\times$ $10^{14}/cm^2$, i.e., 3.8$\times$ smaller. For the *in-situ* phosphorus-doped layer given a hydrogen bake, there is a similar peak with a dose of 6.3 $\times$ $10^{13}/cm^2$, i.e., a further 12$\times$ smaller. These three oxygen doses correspond to equivalent oxide layer thicknesses of 0.66, 0.17 and 0.014 nm respectively. The latter thickness for the *in-situ* phosphorus doped layer given a hydrogen bake corresponds to significantly less than a monolayer of silicon dioxide. Hence, the SIMS results also indicate that when the layer deposition commenced the interfacial oxide layer was discontinuous.

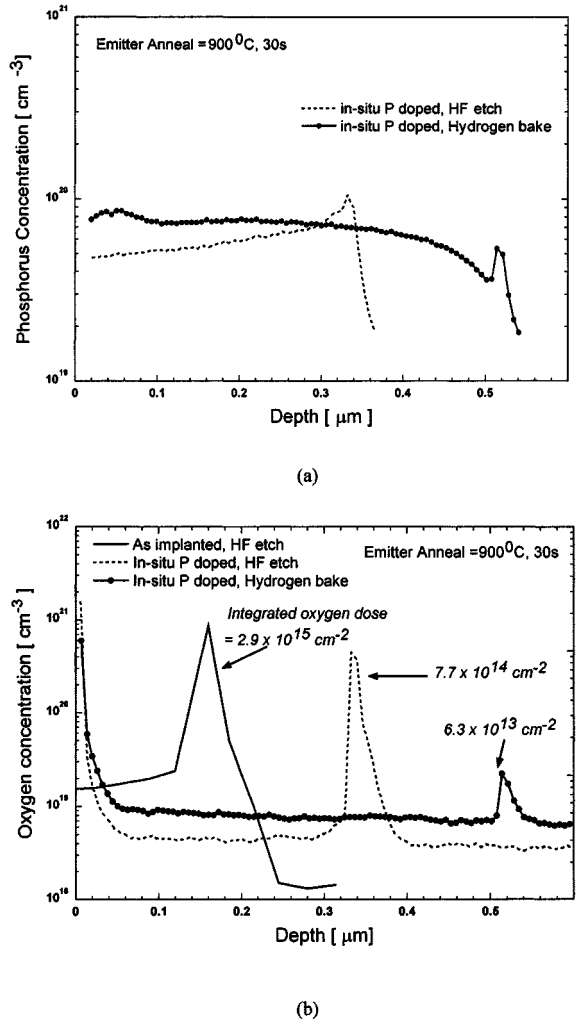

Fig. 3. SIMS profiles of layers produced using the different *ex-situ* and *in-situ* cleans and the different deposition systems: (a) phosphorus profiles and (b) oxygen profiles.

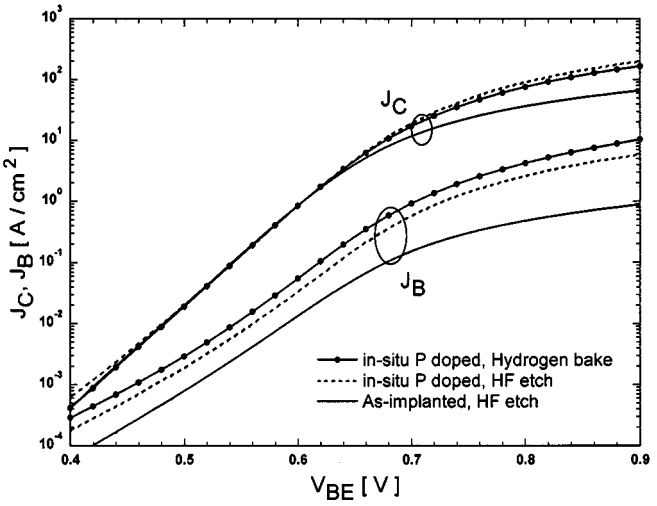

Fig. 4. Gummel plots for transistors produced using the different types of *ex-situ* and *in-situ* cleans and different deposition systems. $T = 300$ K, $V_{CB} = 0$ V, and $A_E = 80 \times 320\,\mu\text{m}^2$.

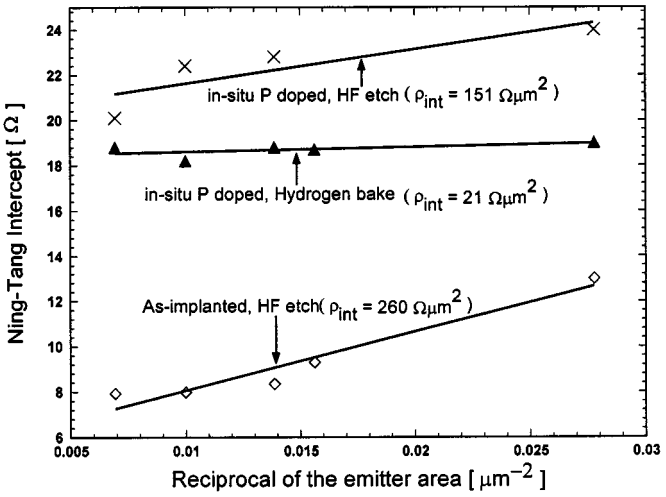

Fig. 5. Ning–Tang intercept [42] as a function of reciprocal emitter area for transistors produced using the different types of *ex-situ* and *in-situ* cleans and different deposition systems. The Ning–Tang intercept was measured on different geometry transistors and the slope of the graph gives the specific interface resistivity [43].

B. Electrical Characterization

Fig. 4 shows Gummel plots for transistors with *in-situ* phosphorus doped layers given an *in-situ* hydrogen bake or an *ex-situ* HF etch, and for comparison, a transistor with a conventional arsenic implanted polysilicon emitter. The lowest values of base current are obtained for the transistor with the arsenic implanted polysilicon emitter and the highest values for the transistor with the *in-situ* phosphorus doped emitter given the hydrogen bake. The difference in base current between these two types of transistor is a factor of 3.8 at a base/emitter voltage of 0.6 V. A comparison of the two *in-situ* phosphorus doped transistors shows that the HF etch gives a lower base current than the hydrogen bake. The difference is a factor of 1.6 at a base/emitter voltage of 0.6 V. A comparison of the Gummel plots with the oxygen SIMS profiles in Fig. 3(b) shows that a decreasing oxygen interface dose correlates with an increasing base current. A comparison with the TEM results in Fig. 1 indicates that the lowest base currents are obtained when the interfacial oxide is intact and the silicon is polycrystalline, and the highest base current when the interfacial oxide is broken up and the silicon is single-crystal. These results are consistent with a base current dominated by hole transport through the interfacial oxide layer when the oxide is intact and through holes in the oxide when the oxide is broken up [1].

Fig. 5 shows the determination of the specific interface resistivity ρ_{int} on the three types of transistor using the Ning–Tang method [42]. For each type of device, the emitter resistance was measured on devices with different geometries and the Ning–Tang intercept [42] plotted as a function of reciprocal emitter area. A linear regression was performed through the data points with the specific interface resistivity ρ_{int} given by the slope of the linear fit [43]. It can be seen that $\rho_{int} = 21\,\Omega \cdot \mu\text{m}^2$ for the *in-situ* phosphorus-doped transistors given the hydrogen bake and $\rho_{int} = 151\,\Omega \cdot \mu\text{m}^2$ for the equivalent transistors given the HF etch. This compares with a value of $\rho_{int} = 260\,\Omega \cdot \mu\text{m}^2$ for the transistor with a conventional arsenic implanted polysilicon emitter. A comparison with the oxygen SIMS profiles in

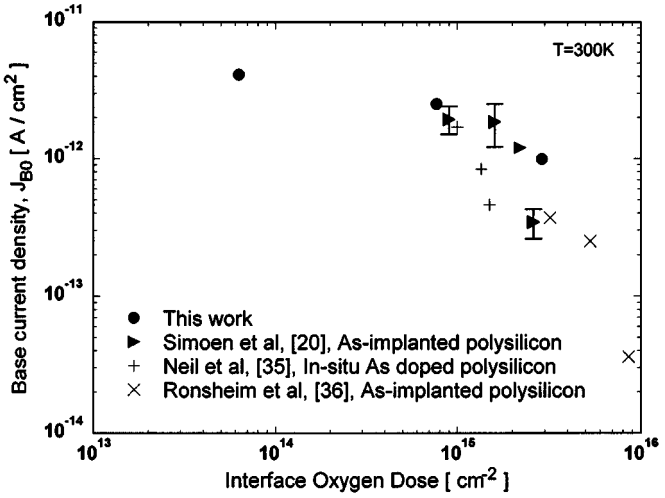

Fig. 6. Comparison of measured and literature values of base saturation current density as a function of interface oxygen dose. $T = 300$ K.

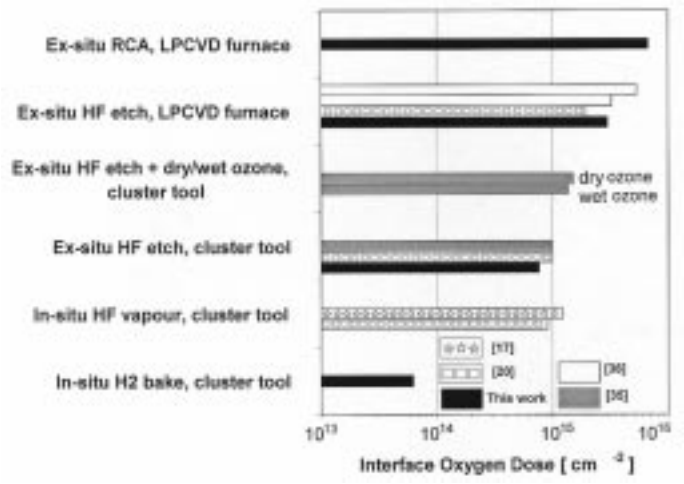

Fig. 7. Comparison of measured and literature values of interface oxygen dose for different *ex-situ* and *in-situ* cleans.

Fig. 3(b) shows that a decreasing interface oxygen dose correlates with a decreasing emitter resistance. A comparison with the TEM results in Fig. 1 indicates that the highest emitter resistances are obtained when the interfacial oxide is intact and the deposited silicon is polycrystalline and the lowest emitter resistances when the interfacial oxide is broken up and the deposited silicon is single-crystal. This is consistent with a current dominated by electron transport through the interfacial oxide layer when the oxide is continuous and through holes in the oxide when the oxide is broken up [1].

IV. Discussion

The values of base saturation current density obtained in this work are compared with those reported in the literature in Fig. 6, where they are plotted against integrated interface oxygen dose. In cases where the literature data was taken at a temperature other than 300 K, a correction has been applied using the equation $J_B = J_{B0}\exp(qV_{BE}/kT)$, where the symbols have their usual meaning. Fig. 6 shows that the results obtained in this work are in reasonable agreement with those in the literature, although there is a wide spread in the data at interface oxygen doses between 1.3×10^{15} and 3.1×10^{15} cm^{-2}. The data shows that the base saturation current density decreases with increasing interface oxygen dose, with the rate of decrease being slow for low oxygen doses and fast for high oxygen doses. The slow rate of decrease in base saturation current density corresponds to an interfacial oxide that is broken up, and the fast rate of decrease corresponds to an interfacial oxide that is continuous. This result indicates that the base saturation current is dominated by hole transport through the interfacial oxide layer [1]. When the interfacial oxide is broken up, there is little impediment to the flow of holes across the interface, so a high base saturation current is obtained. In contrast, when the interfacial oxide layer is continuous, there is a barrier to hole transport across the interface, and the base saturation current is limited by mechanisms such as tunneling [2] and thermionic emission [44].

Fig. 7 compares the interface oxygen doses obtained in this work for the different *ex-situ* and *in-situ* cleans with those reported in the literature [17], [20], [35], [36]. In general, this figure shows that the cluster tool delivers lower values of oxygen dose than the LPCVD furnace, by a factor of typically three. Similar results have been reported by Simeon *et al.* [20], where it was found that the cluster tool produces typically a factor of 1.9 lower values of oxygen dose than the LPCVD furnace. For the *ex-situ* HF etch followed by polysilicon deposition in the LPCVD furnace, the interface oxygen dose of 3×10^{15} cm^{-2} obtained in this work is in the middle of the reported range of 2 to 5×10^{15} cm^{-2}. For the HF dip followed by polysilicon deposition in the cluster tool, our interface oxygen dose of 7.7×10^{14} cm^{-2} is at the bottom of the range of reported values, but nevertheless close to the reported values of 1.0×10^{15} cm^{-2}. The interface oxygen doses for an *in-situ* HF vapor etch in a cluster tool are similar to those for an *ex-situ* HF dip etch. This result indicates that the wafer transfer from the *ex-situ* HF etch to the cluster tool is sufficiently rapid to avoid the growth of additional interfacial oxide. This conclusion is consistent with the work of Meyerson *et al.* [33] who showed that the hydrogen passivated surface produced by an HF dip etch was stable in air for 10 minutes. For the hydrogen bake, our interface oxygen dose of 6.3×10^{13} cm^{-2} is 14.3× lower than the lowest value of Simeon *et al.* [20]. This result demonstrates the effectiveness of the hydrogen bake for eliminating the interfacial oxide. Sun *et al.* [45] have also reported the use of an *in-situ* hydrogen bake prior to selective deposition of the polysilicon emitter, but no value of interface oxygen dose was given. For completeness, Fig. 7 also shows the interface oxygen doses for an *ex-situ* RCA clean performed in this work and an *in-situ* dry/wet ozone clean reported in the literature [35]. The latter has a higher interface oxygen dose than the HF etch, but was reported to have the advantages of removing hydrocarbon residues from the silicon surface and of stabilizing the interfacial oxide with time [35].

Fig. 8 compares the values of emitter resistance obtained in this work with those reported in the literature. The values of emitter resistance taken from the literature have been converted into units of $\Omega \cdot \mu$m^2 using the quoted values of emitter area [17], [20]. For the devices (in this work) given an *ex-situ* HF etch (with interface oxygen doses of 7.7×10^{14} using a cluster tool and 3

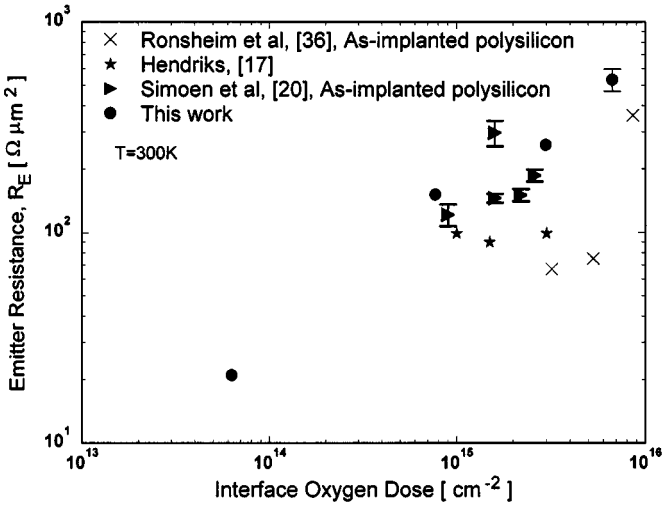

Fig. 8. Comparison of measured and literature values of emitter resistance as a function of interface oxygen dose.

$\times 10^{15}$ cm^{-2} using a LPCVD furnace), the values of emitter resistance are broadly similar to the values in the literature, though there is a large spread in the literature data. In spite of the large spread in emitter resistance values, it can be seen that the *in-situ* hydrogen bake gives a value of emitter resistance that is a factor of three lower than the lowest value reported in the literature. This result clearly demonstrates that the *in-situ* hydrogen bake gives extremely low values of emitter resistance. Sun *et al.* [45] have also used an *in-situ* hydrogen bake prior to the selective deposition of undoped polysilicon. The resulting polysilicon emitter bipolar transistors had emitter resistance values of less than 30 $\Omega \cdot \mu$m^2. This is in good agreement with the value of 21 $\Omega \cdot \mu$m^2 obtained in this work. In contrast with our results, Sun *et al.* [45] reported that the material was polycrystalline after deposition. This may be due to the fact that the layer was undoped or to the use of a H_2/HCl/SiH_2Cl_2 gas mixture, rather than the H_2/SiH_4/PH_3 gas mixture used in this work.

The TEM image in Fig. 2 shows that the *in-situ* phosphorus-doped material given a hydrogen bake was single-crystal after growth with a high density of defects, but the silicon is relatively defect free in a 50-nm-thick region immediately above the interface. A comparison with the phosphorus SIMS profile in Fig. 3(a) shows that the phosphorus concentration decreases from about 5×10^{19} cm^{-3} to 3.5×10^{19} cm^{-3} over a distance of 50 nm above the interface. This result suggests that the high phosphorus concentration may be responsible for the high density of defects in the top part of the silicon layer, with the decrease in phosphorus concentration adjacent to the interface the reason for the lower defect density in this region. SIMS measurements on silicon layers with high phosphorus concentrations tend to confirm this explanation. For example, in layers with a uniform phosphorus concentration above 1×10^{20} cm^{-3}, the high density of defects extends all the way from the surface to the interface. The defects might result from misfit due to the smaller tetragonal radius of phosphorus than silicon [46]. High concentrations of phosphorus in silicon are well known to produce defects, for example dislocation networks in emitters implanted with a high dose of phosphorus [47]. Further work is underway to confirm the origins of the defects.

V. Conclusions

A study has been made of the effects of an *ex-situ* HF etch and an *in-situ* hydrogen bake on the emitter resistance and base current of low thermal budget, *in-situ* phosphorus-doped polysilicon emitter contacts for bipolar transistors. SIMS measurements have shown that an *in-situ* hydrogen bake in a cluster tool gives a very low interface oxygen dose of 6.3×10^{13} cm^{-2}, while an *ex-situ* HF etch gives a dose of either 7.7×10^{14} cm^{-2} when the deposition is performed in a cluster tool or 2.9×10^{15} cm^{-2} when it is performed in a LPCVD furnace. TEM shows that the *in-situ* hydrogen bake results in a material that is single-crystal silicon with a high density of defects, including dislocations and twins. Bipolar transistors fabricated using this high defect density silicon emitter contact have an emitter resistance as low as 21 $\Omega \cdot \mu$m^2 even after a light emitter anneal of 30 s at 900 °C. This is a factor of 7.2× lower than the emitter resistance obtained for cluster tool deposition after an *ex-situ* HF etch and 12.4× lower than that obtained for LPCVD furnace deposition after an *ex-situ* HF etch. The lower value of emitter resistance correlates with an increased base current by a factor of 3.8 for the two extreme cases. The high concentration of phosphorus in the deposited layers is considered to be the cause of the high defect density. In general, the very low value of emitter resistance obtained with the high defect density single-crystal silicon emitter contact suggests that this material could prove useful in future deep submicron Si bipolar or SiGe HBT technologies where the thermal budget is severely constrained.

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