Design of Wave Switched-Current Group Delay Equalizers

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Abstract

This paper describes the design of switched-current group delay equalizers. The design process is based on the pole-zero mirroring technique; with equalizer z-transfer functions generated using an optimization algorithm. To facilitate the systematic implementation of the equalizers, a model describing the design process is developed. A novel feature of the equalizers implementation is that wave structures are employed in realizing the equalizer poles instead of integrators. MATLAB and SI simulation results based on a 6^{th}-order equalizer are included. The results demonstrate that the equalizer can reduce the delay of a 5^{th}-order, 1MHz lowpass SI elliptic filter from 155ns to <20ns over the entire filter bandwidth.

1. Introduction

Group delay equalizers play an important role in video and communications applications where they are normally connected in cascade with filters. Their function is to compensate (flatten) the filter delay (or linear phase) without changing the magnitude of the filter characteristics. This improve the filters time domain response, for example, it was shown in [1], that the step response of an elliptic lowpass filter used in digital PAL video systems has >30% overshoot when no group delay equalizer is used. However, the filter overshoot reduces to <15% when group delay equalization is employed. Switched current (SI) is a relatively new analogue sampled-data technique that has received considerable attention due to its numerous advantages over the switched capacitor technique. This includes implementation simplicity; low-voltage and low power operation and more importantly compatibility with standard digital CMOS processes [2]. Numerous SI filter design methods have been proposed, including [2-4]. Despite the importance of group delay equalization in analog signal processing, little work on their SI design has been reported in the literature until recently [5]. In [5], it was shown how SI equalizers are designed using the CAD tool XFILTER. Different integrator circuits were investigated including LDI, Bilinear, and Euler to improve the equalizer performance. Previous research has shown how SI circuits can also be designed using wave digital theory [6,7], and the synthesis of SI wave filters was reported. The main benefits of using the wave technique is that the resulting SI circuits have no integrators, which often limit the circuit performance. Furthermore, the basic operations in wave theory are delay elements and adaptors, which are easily implemented in SI without performance degradation. The aim of this paper is to show the feasibility of using the wave technique in the design of SI group delay equalizers. Also, the implementation of such equalizers is considered.

2. Design of SI wave group delay equalizers

The presented design method is based on the pole-zero mirroring technique [1,9], where the equalizer poles are derived from the input admittance function of an LC ladder network. These pole positions are mirrored beyond the z-domain unit circle to generate the equalizer zero positions. The general z-domain transfer function of an *Nth*-order group delay equalizer or allpass circuit is:

$$H(z) = \frac{a_N z^N + a_{N-1} z^{N-1} + \cdots + a_1 z + 1}{z^N + a_1 z^{N-1} + \cdots + a_{N-1} z + a_N} = \frac{\sum_{k=0}^{N} a_k z^k}{\sum_{k=0}^{N} a_k z^{N-k}}, \quad a_0 = 1 \qquad (1)$$

where the poles and zeros of the allpass transfer function *H(z)* are reciprocals of one another. If we define the polynomial *A(z)* as: $A(z) = \sum_{k=0}^{N} a_k z^{N-k}$, $a_0 = 1$

Eq.(1) can be expressed as: $H(z) = z^N \frac{A(z^{-1})}{A(z)}$ (2)

To apply the pole-zero mirroring technique to the design of SI equalizers, Eq.(2) needs to be rearranged as [5]:

$$H(z) = 1 - \frac{A(z) - z^N A(z^{-1})}{A(z)} = 1 - \frac{2}{1 + \frac{A(z) + z^N A(z^{-1})}{A(z) - z^N A(z^{-1})}} = 1 - \frac{2}{1 + Y(z)} \quad (3)$$

where $Y(z) = \frac{A(z) + z^N A(z^{-1})}{A(z) - z^N A(z^{-1})}$

Digital wave structure is employed to realize *Y(z)*. Since digital wave circuit is modeled after classical filter, preferably in ladder configuration [8], it is required that *Y(z)* can be expanded in LC ladder form. It was shown in [11], if the *A(z)* has all its zeros inside the unit circle, the following expansion is always possible:

$$Y(z) = b_1 \frac{z-1}{z+1} + \cfrac{1}{b_2 \frac{z-1}{z+1} + \cfrac{1}{\vdots + \cfrac{1}{b_n \frac{z-1}{z+1}}}}$$

where $b_i > 0, i = 1,2,\cdots n$ (4)

This means if all the poles of allpass transfer function *H(z)* is inside the unit circle, *Y(z)* is analogous to a driving-point admittance *Y(s)* which can be synthesized as an LC ladder circuit, Fig.1. The details of realizing *Y(z)* will be discussed in Section.3.

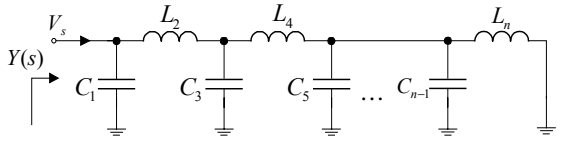

Fig.1 LC ladder network

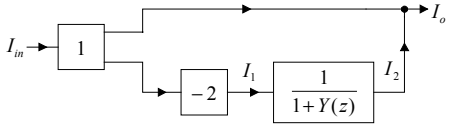

Fig.2 Block-diagram model of Eq.(3)

3. Implementation of SI group delay equalizers

To facilitate the systematic implementation of the equalizers, a block-diagram model representing the pole-zero mirroring design technique is developed as shown in Fig.2. This model describes Eq.(3), where the input and output currents are I_{in} and I_o respectively. To translate this block-diagram into SI circuit, consider first the realization of the term *1/(1+Y(z))*, which is achieved by the circuit shown in Fig.3. The circuit has a unity gain current replicator to produce two identical versions of the input current: *x* and I_2. Due to the presence of the current mirror, $xY(z) = I_1 - x$, and since $x = I_2$, it is readily seen how Fig.3 implements the current ratio of I_2 / I_1. Fig.4 shows the complete SI circuit implementation of the group delay equalizer, marking the circuitry of each section of the group delay equalizer block-diagram (Fig.2).

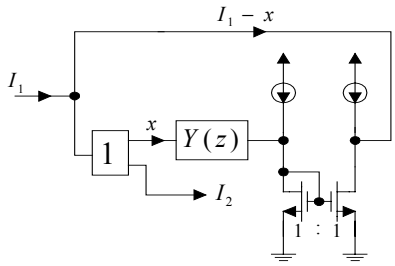

Fig.3. SI implementation of the term, *1/(1+Y(z))*

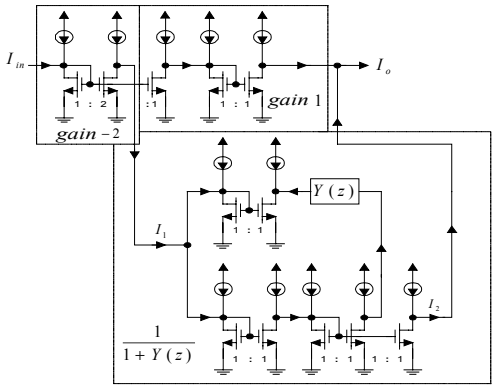

Fig.4. SI realization of Fig.2

There are several techniques for realizing *Y(z)*. In [5], the function of *Y(z)* was realized using various SI integrators. In this paper, *Y(z)* is implemented using wave digital filter technique [8]. The motivation for employing the wave technique is that the resultant equalizers do not require integrators, and more importantly wave structures consists of elements such as delay cells and adaptors which are readily implemented in SI. The wave technique simulates the behavior of passive networks through the use of wave quantities instead of port voltage and current, Fig.5. The wave variables *A* (incident wave) and *B* (reflected wave) are defined as linear combinations of the corresponding port current, *I* and voltage, *V*:

$$I = (A - B)/2R \tag{5}$$

where *R* is the port resistance, and is chosen arbitrarily to simplify the wave model.

Fig.5 Passive network and its wave block

The wave structure consists of delay cells and adaptors (series and parallel), which is used to connect the various wave elements. For the passive component: R, L and C, their port resistance is *R*, *2L/T* and *T/2C*, respectively. Wave adaptors model the parallel or series connections of the passive components in Fig.1. The adaptor coefficients γ are calculated using the following expressions:

series adaptors: $\gamma_i = \dfrac{2R_i}{R_0 + R_1 + \cdots + R_{N-1}}$, parallel adaptors: $\gamma_i = \dfrac{2G_i}{G_0 + G_1 + \cdots G_{N-1}}$ (6)

For each adaptor, the following relation must be satisfied: $\sum_{i=0}^{2} \gamma_i = 2$, $i = 0,1,2$

Prior to convert the circuit of *Y(s)*, Fig.1, into equivalent wave structure, the following modification to the circuit of *Y(s)* is necessary so that it is suitable for SI operation, and hence Fig.4. In order to process current signals, the voltage V_s need to be changed to current which is achieved by introducing voltage source with resistance, *R* into *Y(s)*. However, for *Y(s)* to maintain the same input admittance, a negative resistor $-R$ need to be included as shown in Fig.6. The equivalent wave structure of the modified circuit of *Y(s)* is shown in Fig.7. It should be noted that the block marked "converter" is included to implement Eq.5, assuming R =1.

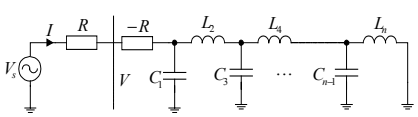

Fig.6 Modified LC ladder network

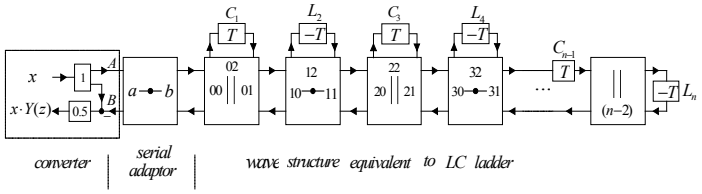

Fig.7 *Y(z)* realization using wave technique

Now, the SI wave group delay equalizer transistor count is considered. Fig. 4 shows the SI design of the group delay equalizer excluding the realization of *Y(z),* where 12 transistors are used. The SI circuit complexity of the wave structure *Y(z)*, Fig.7, depends on the equalizer order, *n*. As outlined earlier, wave structures consists of delay cells, and adaptors. If the equalizers order, *n*, is even, it can be shown that the wave structure has *n/2* positive and negative delay cells, *(n/2-1)* 3-port parallel and series adaptors, and one 2-port parallel adaptor. Using 1st-generation delay cells, and the adaptors reported in [10], it can be shown that the number of transistors in an even-order SI equalizer is *(21n-11)*. Similarly, the number of transistors in an odd-order SI equalizer is *(21n-17)*. Note the theses transistor expressions do not include the transistors count of the two blocks marked "converter" and "serial adaptor" in Fig.7. A transistor realization of these two blocks are shown in Fig.8, Therefore an additional 16 transistors need to be added when calculating the overall equalizer SI complexity. For example, a 6th-order SI equalizer has 131 transistors, assuming positive delay cell has 4 transistors, negative delay cell has 6 transistors, 3-port series adaptor has 13 transistors, 3-port parallel adaptor has 19 transistors, and 2-port parallel adaptor has 9 transistors.

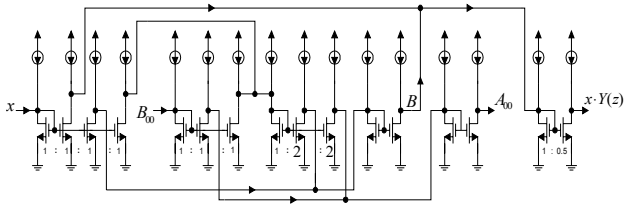

Fig.8 Realization of blocks "converter", and "serial adaptor" (Fig.7)

4. Computer program for designing SI wave group delay equalizers

In this section, a review of a computer program for designing SI wave group delay equalizers based on the pole-zero mirroring technique is given. Due to space limitation, only short discussion of the computer program is included. The design flow of the computer program, which is developed around MATLAB, is shown in Fig.9. The input to the program is the group delay variation of the filter to be equalized specified in the form of data points (frequency, delay), equalizer order, *n*, and required final group delay ripple. The first step of the program generates an allpass z-transfer function, Eq.(1), whose delay response when added with that of the filter can achieve the specified group delay ripple. The generation of the equalizers z-transfer function is achieved using a numerical optimization algorithm. The second step involves obtaining first *Y(z)* from *H(z)* using Eq.(3) and then substituting s for z^{-1} in *Y(z)* with $z^{-1} = (2-s)/(2+s)$ (bilinear transformation, T=1) to produce the driving-point admittance of the LC ladder network *Y(s)*, Fig.1. The third step carries out the synthesis of *Y(s)* to obtain the LC values of the ladder network. The final step of the program derives the wave adaptor coefficients of the SI wave equalizer from the LC component values produced by step three using Eq.(6).

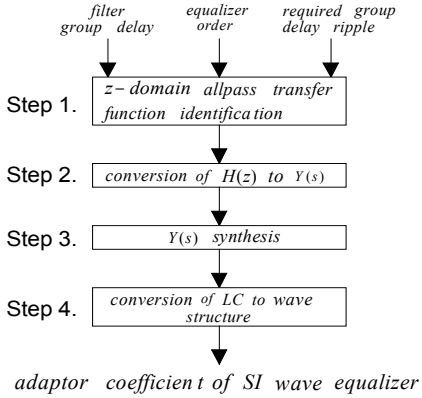

Fig.9 Computer program flow for designing SI equalizer

5. Simulation results

This section demonstrates through the use of an example the effectiveness of the proposed design method in equalizing filter group delay variations. MATLAB and switched current SCANP4 [12] simulation results are presented. Fig.10 shows the normalized delay response of a 5th -order elliptic lowpass filter. This shows that the filter has group delay variation of almost 1s, which is unacceptable in most video and high frequency applications. Using the computer program discussed in Section.4, it was found that a 6th -order group delay equalizer is needed to reduce the group delay variation to 0.1s, when combined with the filter as shown in Fig.10.

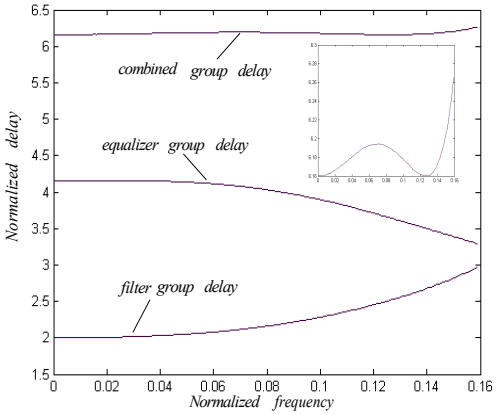

Fig.10 MATLAB simulation of normalized filter delay, equalizer, and their combination

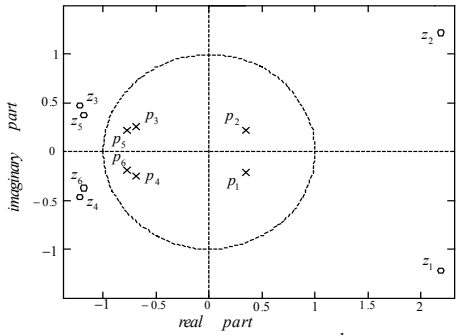

Fig.11 Pole-zero plot of 6th-order delay equalizer

The z-transfer function of the equalizer is: $H(z) = \dfrac{a_6 z^6 + a_5 z^5 + a_4 z^4 + a_3 z^3 + a_2 z^2 + a_1 z + 1}{z^6 + a_1 z^5 + a_2 z^4 + a_3 z^3 + a_4 z^2 + a_5 z + a_6}$

where a_6 =0.0589, a_5 =0.0312, a_4 =-0.0345, a_3 =-0.1066, a_2 =1.521, a_1 =2.2855

Fig.11 shows the pole-zero plot of the equalizer. As can be seen, the poles and zeros are reciprocal of one another, confirming the correct theoretical analysis of z-domain allpass functions. Table.1 give the adaptor coefficients of the wave group delay equalizer.

$\gamma_{00}=0.936$	$\gamma_{01}=1$	$\gamma_{02}=0.064$	$\gamma_a=2$
$\gamma_{10}=0.84$	$\gamma_{11}=1$	$\gamma_{12}=0.16$	$\gamma_b=2$
$\gamma_{20}=0.753$	$\gamma_{21}=1$	$\gamma_{22}=0.247$	$\gamma_{40}=1.635$
$\gamma_{30}=0.915$	$\gamma_{31}=0.717$	$\gamma_{32}=0.368$	$\gamma_{41}=0.365$

Table.1 Adaptor coefficient of SI wave equalizer

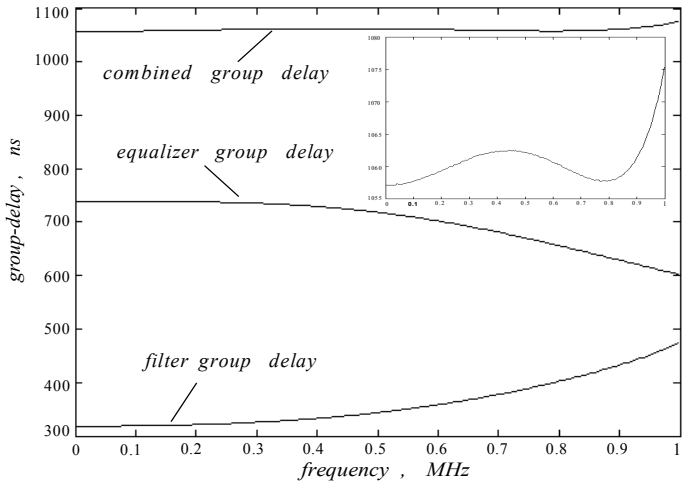

Fig.12 SCNAP4 simulation of filter delay, equalizer, and their combination.

Fig12 shows the transistor-level simulation of the equalizer using the switched-current simulator SCNAP4, assuming a passband frequency of 1MHz, and sampling frequency of 6.25MHz. In SCNAP4, transistors are considered as ideal transconductors with parasitic effects ignored. As can be seen, nearly flat delay has been obtained in the combined response of the filter and group delay equalizer. An enlarged plot of the group delay ripple is included in Fig.12, which shows that the equalizer has reduced the group delay variation of the filter from 155ns to nearly 18ns over the entire filter bandwidth. The presented design method for SI wave equalizers were also used to equalize the delay characteristics of other filtering approximations and found to perform as expected.

6. Concluding remarks

This paper has addressed the synthesis of SI group delay equalizers using the pole-zero mirroring technique. A systematic approach for the equalizers implementation has been presented facilitated by the development of a block-diagram model of the synthesis technique. Expressions predicting the equalizers transistor count have been derived. A novel feature of the implementation process is that wave structures have been used to realize the equalizer poles. A 6^{th}-order group delay equalizer has been designed and simulated, showing that the equalizer can effectively compensate the delay of an elliptic lowpass filter in the passband.

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