JOURNAL OF ELECTRONIC TESTING: Theory and Applications 20, 1–13, 2004

Generation and Verification of Tests for Analog Circuits Subject to Process Parameter Deviations

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Received July 7, 2001; Revised May 15, 2003

Editor: B. Kaminska

Abstract. The paper presents a test stimulus generation and fault simulation methodology for the detection of catastrophic faults in analog circuits. The test methodology chosen for evaluation is RMS AC supply current monitoring. Tests are generated and evaluated taking account of the potential fault masking effects of process spread on the faulty circuit responses. A new test effectiveness metric of probability of detection is defined and the application of the technique to an analog multiplier circuit is presented. The fault coverage figures are therefore more meaningful than those obtained with a fixed threshold.

Keywords: analog test generation, catastrophic faults, fault modeling, fault simulation, supply current monitoring

1. Introduction

The slow and expensive nature of specification testing has motivated research into fault-based or structural testing for analog circuits [3]. The coverage for catastrophic faults of these tests has approached 100%, but the validity of the results is open to question because the setting of the threshold between the faulty and fault free responses has in general been arbitrary, and has not fully taken into consideration the effect of manufacturing process parameter variation [5, 9, 11, 15, 17]. In many publications the tolerance bounds are not stated which makes the comparison of structural based fault detection techniques impossible.

Whilst process variations can be studied in isolation as a failure mechanism, any study of spot defects cannot ignore process spread and the possible fault masking effect it may have. More recent work on structural

testing has used Monte Carlo simulations to produce a tolerance band around the fault-free circuit response [1]. The effect of process variations on circuits under catastrophic fault conditions has also been investigated elsewhere [12]. The effects of parametric variation on system-level behavior have also been studied [16].

Although the success of a test is largely based on the correct choice of stimulus, little effort has been given to generating optimum test stimuli for catastrophic faults [19, 22, 23].

In order to increase confidence in the use of efficient structural tests we present an algorithm that first chooses the best test stimuli using sensitivity analysis, and after fault simulation produces figures of detectability using manufacturing process information to form a realistic tolerance on the fault-free and faulty circuits. The test chosen to demonstrate this algorithm is AC RMS Supply Current Monitoring. Measurement of the RMS value of the AC component of the supply current [25] has many advantages over typical DC [5] and transient based tests [2, 4]. For example it is not necessary to employ complicated post processing techniques to analyze the fault response and an AC stimulus may be propagated though capacitively-coupled analog stages.

The format of this paper is as follows: Section 2 presents our approach to test stimulus generation based on sensitivity analysis but taking account of process variation. In Section 3 we discuss the analog fault models and simulation techniques and in Sections 4 and 5 we consider the prediction of test quality using Monte Carlo simulation and a probabilistic approach. In Section 6 we describe the simulation algorithm that reduces test evaluation time. Section 7 presents an application of the technique and results for an analog multiplier. In the final section we present our conclusions.

2. Test Stimulus Generation

In this work, we have chosen to limit the test stimulus generation problem to that of finding the best set of parameters of a single sinusoid defined by Eq. (1)

$$f(V_{\text{off}}, A, f, t, \varphi) = V_{\text{off}} + A\sin(2\pi f t + \varphi) \quad (1)$$

where V_{off} is the DC offset voltage, A is the amplitude, f is the frequency, t is the current time and ϕ is the phase.

Small signal sensitivity analysis is used to select each test stimulus parameter, avoiding the need for repeated transient simulation of every combination of the stimulus parameters. Sensitivity analysis has previously been used as a means of selecting the optimum frequency to detect parametric component faults at the output of the circuit [21]. Here, we are evaluating RMS supply current test as a test for catastrophic faults. Therefore we use sensitivity analysis to predict how the addition of an extra component, modeling the catastrophic fault, will change the transfer admittance from the input terminal V_{IN} to the supply current I_{DD}.

We obtain this sensitivity information by injecting a high resistance short circuit at each fault site in turn within the circuit. The resistance value is high enough to avoid degradation of functional performance. For the entire input stimuli space, the resultant change in transfer admittance between the faulty and fault free circuit is then calculated using a SPICE-based circuit simulator as

$$S^{IddAC}_{R\text{fault}} = \frac{Idd(f, V_{\text{off}})_{\text{faulty}} - Idd(f, V_{\text{off}})_{\text{faultfree}}}{Idd(f, V_{\text{off}})_{\text{faultfree}}} \quad (2)$$

where, S is the sensitivity of the *Idd* AC transfer function to the catastrophic fault, and $Idd(f, V_{\text{off}})$ is the *Idd* AC response as a function of offset voltage and frequency.

For a fault in a particular component to have the highest chance of detection, the AC supply current though the rest of the circuit must be at a minimum. Since adjustment of the DC offset can change the relative size of the AC supply current that flows though each circuit branch, our input stimuli search space includes DC offsets. However the search must be limited to DC offsets that ensure the AC supply current is as linear as possible so that results from the essentially linear sensitivity analysis are valid. For example we would avoid stimulating an operational amplifier outside the Common Mode input range specification. Therefore we propose a measurement of the extent of the linearity by determining the change in the AC supply current transfer function as the DC offset is incremented between the supply rails. If at a particular offset voltage the gradient of this function exceeds a heuristic limit then this offset voltage is excluded from further analysis.

The best amplitude for fault detection is a compromise between a high signal to noise ratio at the supply terminal and the linearity and predictability of the output response. Here we use one input to excite the fault; two or more inputs could be used in the analysis, in which case the phase relationship between the two would have to be considered. However this would

increase the complexity of the test generation task to and is not implemented here.

Due to variations in process parameters, the spread in values of RMS supply current will not be constant for all frequencies and DC offsets, so the stimulus chosen with sensitivity analysis might also be that at which the circuit is most susceptible to process spread. Therefore for the range of valid DC offsets a Monte Carlo AC frequency sweep is performed on the fault free circuit and the mean and standard deviation of the supply current are calculated for each stimulus. The size of the mean relative to the standard deviation then gives an indication of the effect of process parameter change and acts as a weighting factor on the sensitivity information. The maximum of this weighted sensitivity function is found for each fault, defined by Eq. (3):

$$F(f, V_{\text{off}}) = \text{MAX}\left\| \frac{Idd(f, V_{\text{off}})_{\text{faulty}} - Idd(f, V_{\text{off}})_{\text{faultfree}}}{Idd(f, V_{\text{off}})_{\text{faultfree}}} \times \frac{Idd(f, V_{\text{off}})_{\mu}}{Idd(f, V_{\text{off}})_{\sigma}} \right\| \quad (3)$$

where $Idd(f,V_{\text{off}})_{\mu}$ and $Idd(f,V_{\text{off}})_{\sigma}$ are the mean and standard deviation as a function of DC offset and frequency of the AC *Idd* supply current. From this test stimulus generation technique an input stimuli set of frequencies and offsets is obtained. This set of stimuli is then used in the test evaluation techniques described in the following sections.

3. Fault Modeling and Analog Fault Simulation

It is clear that any research into structural based testing requires a fault simulation methodology in order to evaluate test quality. Several Analog Fault Simulation (AFS) approaches have been developed and are described in the literature [7]. The AFS approach used here, similar to that used in other fault simulators, is to utilize an existing circuit simulator (in this case HSPICE) and modify circuit netlists with a simulation fault model to allow simulation of faulty devices. The ANTICS analog fault simulator that has been developed by the authors is shown in Fig. 1. As analog circuits are subject to process parameter deviations, this must be considered during the analog fault simulation process so Monte Carlo simulations are used for the fault injected and fault-free circuits. The AFS procedure thus contains the steps of random number generation, fault injection, repeated simulation (over a network cluster of workstations) and post-processing analysis. It is the analysis in the final stage of AFS that forms the bulk of the discussion in this paper.

The simulation fault models used (4 catastrophic faults per transistor) are shown in Fig. 2. Only transistor device faults were simulated for this investigation although the technique is not restricted to this fault model. Other approaches have used Inductive Fault Analysis (IFA) in order to generate realistic fault list based on layout and defect information [10, 18]. However, in this case such information was unavailable and the fault list was generated purely from the schematic.

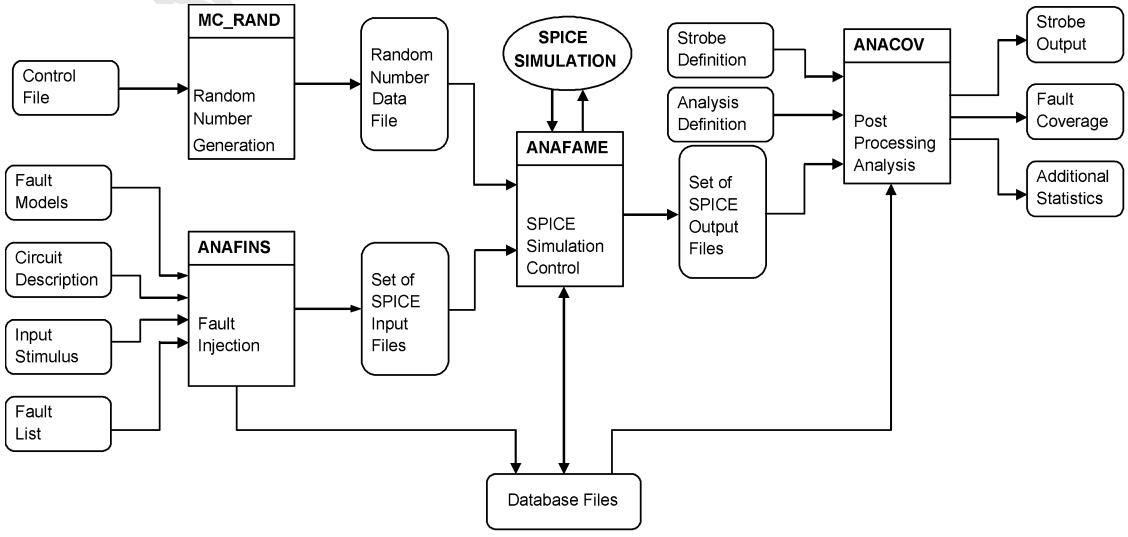

Fig. 1. The ANTICS fault simulation software.

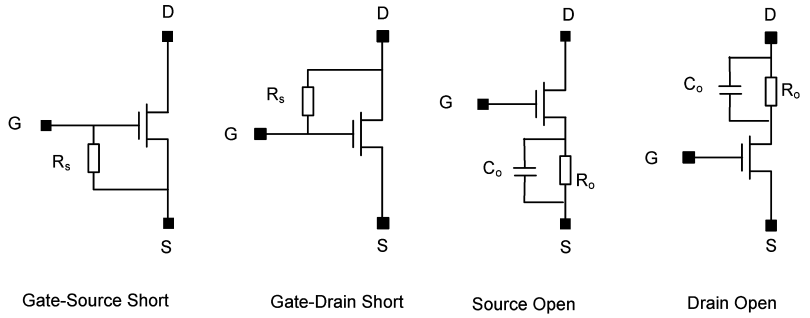

Fig. 2. Catastrophic fault models: Rs = (1 Ω, 500 Ω), Ro = 100 MΩ, Co = 1 fF.

The size of the resistance used to model a bridging defect in previous work [5, 25] was assumed to be 1 Ω. Bruls [20] has investigated the resistance of bridging fault by examining 400 defects on bridging structures specially constructed for the investigation using a standard manufacturing process. Unfortunately a high degree of uncertainty precludes the estimation of an exact distribution of resistance value, and hence the inclusion of the short resistance as one of the parameters varied during the Monte Carlo simulation. The results do however show that the vast majority of bridging defects have a resistance less than 500 Ω although a few "non-catastrophic," soft faults were identified with resistances greater than this and up to 20 KΩ. Since most defects were shown to have a resistance below 500 Ω, some authors have chosen to use this as an upper limit value for modeling spot defects [6, 13]. In this work the effect of bridging resistance value is investigated by comparing the fault simulation results using a 1 Ω and a 500 Ω bridging fault model.

In general, certain faults will be clearly detected, for example those that exhibit changes of several orders of magnitude in the supply current. However, there may be other faults which produce a more subtle effect and these require Monte Carlo simulations in order to correctly classify them. The inclusion of the Monte Carlo simulation post-processing stage within the ANTICS software is considered in the next section.

4. Fault Detection under Process Parameter Deviations

During the HSPICE Monte Carlo simulation, process parameter deviations are simulated by altering the global component models according to manufacturing information. The measurements of the RMS supply current will thus produce a set of output responses that will represent the distributions of the RMS supply current under the simulated process parameter deviations.

An approach for the optimal setting of test limits for DC testing is presented in [24] based on obtaining faulty and fault-free probability distributions. In [18], a statistical test technique is presented based on analyzing the harmonic content of the supply current. In both cases, the quality of tests is presented as Type I and II errors (see below). However, these are obtained using simulation of a number of circuits and recording the percentage number of good and faulty devices misclassified. The approach presented in this paper differs from the other approaches in that the test quality is obtained by considering faulty circuit probability distributions.

Example distribution histograms obtained from a Monte Carlo simulation of the RMS of the AC supply current of the multiplier circuit described in Section 7 under normal and catastrophic short fault conditions are shown in Fig. 3. Two points can be noted from this plot: firstly that the faulty and fault-free circuit spread due to process variations differ and secondly that the histograms overlap each other partially. In general, the measured output distributions obtained should approximately follow the Normal distribution as a consequence of the central limits theorem. The set of distributions obtained can be thought of as conditional probability distributions $p(\phi \mid G)$ and $p(\phi \mid F_N)$ for the fault-free circuit and faulty circuit N, respectively, over the continuous measurement space, ϕ (see Fig. 4). In this case, the measured variable ϕ is the RMS supply current.

We can describe a discrimination function $g(\phi)$ which represents the decision function programmed into the ATE which decides whether a given IC should be passed as good or failed as faulty for a given RMS measurement. Since the final stage of AFS is used to model the ATE, $g(\phi)$ is used in the decision process to decide whether a fault is detectable or undetectable.

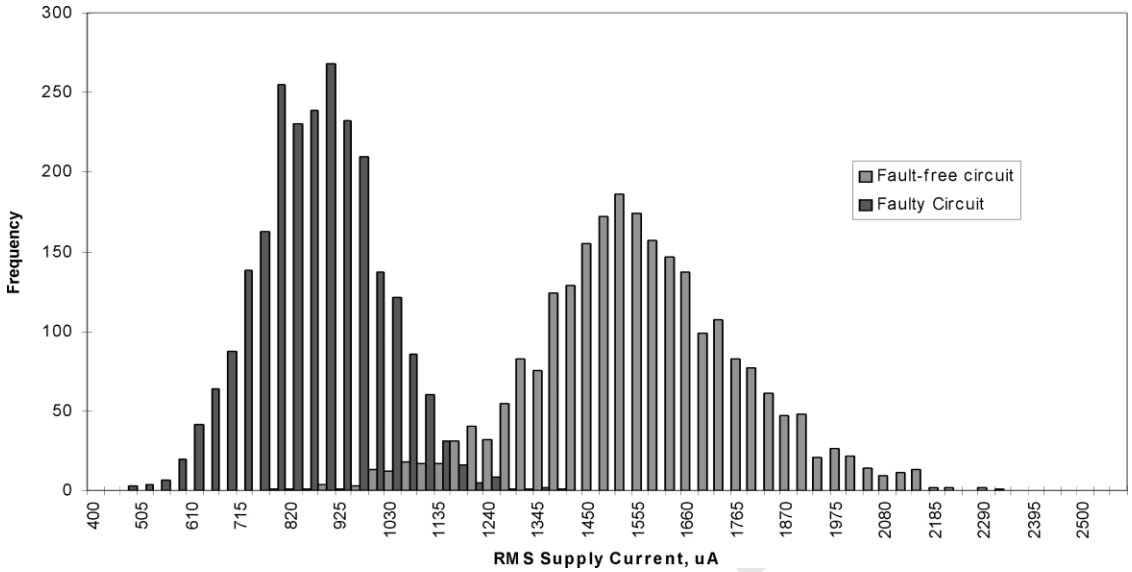

Fig. 3. Histogram of RMS supply currents under process parameter deviations.

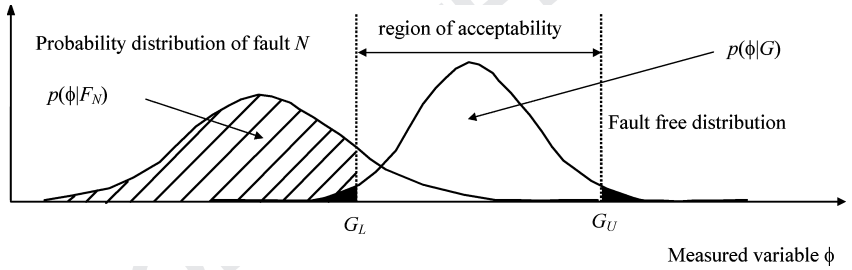

Fig. 4. Probability distributions.

Disk followed.

In this paper we have chosen to define the $g(\phi)$ function using the 3 σ points of the fault-free distribution. From Fig. 4, we have

$$g(\phi) = \begin{cases} 1 \text{ (pass)} & \text{if } G_L < \phi < G_U \\ 0 \text{ (fail)} & \text{otherwise} \end{cases}$$

The AFS post-processing procedure is thus to classify the distribution for a fault (N) using $g(\phi)$. Since we are considering the probability density function of the faulty circuit, we can define the *probability of detection* of a given fault N as:

$$\begin{aligned} P_N &= \int_{-\infty}^{\infty} p(\phi \mid F_N) g(\phi)\, d\phi \\ &= \int_{B}^{\infty} p(\phi \mid F_N)\, d\phi + \int_{-\infty}^{A} p(\phi \mid F_N)\, d\phi \end{aligned} \tag{4}$$

We can also calculate the probabilities of misclassification which are Type I and II errors from standard hypothesis testing. This is shown in Table 1.

Defining α and β as the probabilities of Type I and II errors respectively gives

$$\begin{aligned} \alpha &= \int_{-\infty}^{\infty} p(\phi \mid G) g(\phi)\, d\phi \\ &= \int_{B}^{\infty} p(\phi \mid G)\, d\phi + \int_{-\infty}^{A} p(\phi \mid G)\, d\phi \end{aligned} \tag{5}$$

Table 1. Fault classification.

	Passed	Failed
Good circuit	✓	Type I error
Faulty circuit	Type II error	✓

$$\beta_N = \int_{-\infty}^{\infty} p(\phi \mid F_N)(1 - g(\phi))\, d\phi$$
$$= \int_{A}^{B} p(\phi \mid F_N)\, d\phi = 1 - P_N \qquad (6)$$

The Type I error only depends on the fault-free (good) distribution and is therefore the same for every fault. The Type II error, however, is dependent on the faulty circuit distribution and is thus different for every fault, however it is not a confidence measure in the results since it is simply the probability that the fault in question will be undetected.

5. Goodness of Fit Test

The theory presented in Section 4 is true regardless of the PDF of the distribution obtained. However, in order to calculate the probability of detection for a given fault, we need an estimate of the PDFs of both the faulty and fault free circuits using the Monte Carlo simulation responses. It is expected in general that the distribution PDF will follow the Gaussian normal distribution, as a consequence of the central limit theorem. In order to test the hypothesis that the distribution obtained is Normal, it is possible to use a "goodness of fit test." Several such tests have been developed including the chi-squared test and the Kolmogorov-Smirnov (KS) test [8]. The KS test, which we use here, is generally accepted for continuous data.

The two-sided KS test procedure is as follows (from [8]):

Let $S(\phi)$ be the cumulative distribution function based on a set of random samples taken from distribution $p(\phi)$. (i.e. the values obtained from the Monte Carlo simulation).

Let $p^*(\phi)$ be the hypothesized distribution function (i.e. a Normal distribution with mean and variance obtained from the random samples).

The two sided KS test statistic T_1 is defined as the greatest distance between $S(\phi)$ and $p^*(\phi)$. That is:

$$T_1 = \max_{\phi} \left| p^*(\phi) - S(\phi) \right| \qquad (7)$$

This is shown graphically in Fig. 5. The hypothesis that the samples are sampled from a function $p(\phi) = p^*(\phi)$ is rejected if T_1 is greater than the tabulated KS Test Statistic value at the appropriate significance level. Moreover, the test statistic T_1 can be used as a confidence level in the distribution function.

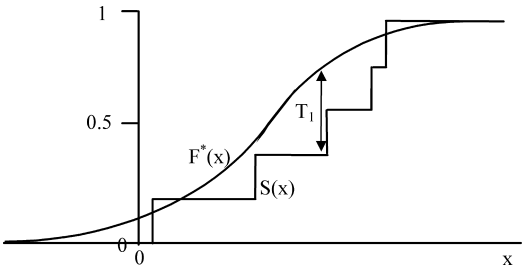

Fig. 5. The KS test statistic.

The significance level of the test governs the level of "Normality" that must be achieved for the distribution to be classed as Normal. The threshold to which this level is set is a compromise between accepting distributions which are not Normal and rejecting distributions which are in fact Normal. A value commonly used in statistical analysis is to test to the 95% significance level, which is used throughout this thesis. Whilst the acceptance of the hypothesis does not prove that the data follows the hypothesized distribution, it indicates that it is not an unsuitable approximation to use.

6. Test Selection and Test Quality Evaluation Algorithm

This section presents the novel algorithm used for test selection and test quality evaluation. Initially the best set of frequencies and DC offsets are chosen with the weighted sensitivity search technique described in Section 2. One approach would then be to use Monte Carlo simulation for each fault and for each stimulus to evaluate the tests. However, this could require a prohibitively large simulation overhead and therefore the fault simulation algorithm described below which reduces Monte Carlo fault simulation time was developed.

Using a single fault simulation run for each stimulus from the set, the best stimulus for detection of each fault is obtained. The *DIST* metric used to determine this is based on the separation of the nominal circuit responses with respect to the fault-free standard deviation in Eq. (8)

$$DIST_{i,j} = \left. \frac{\left| \phi_{F_j} - \phi_G \right|}{\sigma_G} \right|_{\text{stimulus } i} \qquad (8)$$

where ϕ_G and ϕ_{F_j} are the nominal response values of the fault-free and each faulty circuit j respectively and σ_G is the standard deviation of the fault-free circuit obtained by Monte Carlo simulation.

During this stage in the simulation, if the fault current is an order of magnitude greater than the fault free spread used for the region of acceptability then the fault is clearly detectable and is dropped from the fault list. Similarly, totally undetectable faults are marked as undetectable and dropped. For the remaining faults, the best test from the single response simulation (the stimulus with the largest *DIST* value) is selected and a Monte Carlo analysis is performed on the faulty circuit. The distribution of the results is compared to the Normal distribution using the KS test. If the faulty probability distribution is indeed Normal then the probability of detection, POD_j, can be calculated using Eq. (4), if not, the next best test is tried. The whole algorithm is presented below:

```
BEGIN
Obtain initial set of M best input stimuli from analyses:
    • AC analysis for coarse DC offsets and amplitude
    • Noise analysis for input amplitude
    • Monte Carlo AC sweep over frequency and DC offset for process weighting
    • AC sensitivity of each fault
DO FOR each stimulus i = 1 .. M WHILE undropped faults exist
        {
         Perform Monte Carlo simulation on the fault-free circuit with stimulus i to
         get upper and lower pass/fail limits
         DO FOR each fault j = 1 .. N where j not dropped
                {
                 Do single simulation with stimulus i
                 Classify fault j:
                 IF totally detectable ** strike from fault list
                        {
                         Drop fault j from fault list
                         Set POD_j = 100%
                         Set STIM_j = i
                         Continue
                        }
                 ELSE
                         Record DIST_{i,j} distance metric
                }
        }
DO FOR each fault j = 1 .. N where j not dropped
        {
         REPEAT
                {
                 Find i such that DIST_{i,j} = max_i(DIST_{i,j}) ** find best test stimulus
                 IF DIST_{i,j} ≠ 0.0
                        {
                         Do Monte Carlo simulation using stimulus i and record POD_j,
                         Set STIM_j = i
                         Set DIST_{i,j} = 0.0
                        }
                }
         WHILE KS test failed and max_i(DIST_{i,j}) ≠ 0.0
        }
END
OUTPUT POD_j , STIM_j for fault j = 1 .. N
```

where
N = Number of faults on fault list
M = Number of input stimuli
POD_j = Probability of detection for fault $j = 1 .. N$
$STIM_j$ = Best stimulus for fault $j = 1 .. N$
$DIST_{i,j}$ = Distance metric for fault $j = 1 .. N$, stimulus $i = 1..M$

7. Experimental Procedure and Results

This technique was evaluated on a continuous time analog multiplier circuit from a commercial cell library consisting of a series of 4 active attenuators/level shifters, a Gilbert gain cell, a voltage reference and an opamp configured as a current to voltage converter, (see Fig. 6). The inputs are applied to V_{+x} (AC and DC stimuli) and V_{+y} (DC level of input stimulus only) with V_{-x} and V_{-y} grounded. Power supply voltages of $+5$ and -5 volts are applied to VDD and VSS respectively. All Monte Carlo simulations were conducted by varying the level 2 SPICE transistor parameters VTO, TOX, UO, LD and poly resistance using process variation information. For this circuit, an operating point analysis takes about 0.15 s on a 500 MHz Sun UltraSPARC processor. An AC analysis takes about 0.02 s. The marginal cost of AC sensitivity analysis is insignificant. A transient analysis over 10 cycles requires about 0.25 s. This figure applies to fault-free and fault simulations and to each Monte Carlo simulation.

In order to extract the AC component of the supply current at the supply terminal VDD of the circuit under test for these simulations, a behavioral current controlled voltage source (CCVS) converts the total (DC and AC) supply current to a voltage. A capacitor blocks the DC component of the voltage at the output of the CCVS and the steady state AC RMS voltage is measured across a resistance using the HSPICE .measure command, after initial transients in the circuit have died down.

The first part of the test stimulus generation algorithm finds a set of suitable inputs using small signal analysis techniques. The small signal transfer characteristic from the input to the power supply terminal is calculated, defined as the *Idd-tf* response. Fig. 7 shows the *Idd-tf* for all input offsets of the multiplier. It can be seen that *Idd-tf* increases approximately linearly over the range -4 to 5 volts.

The change in *Idd-tf* over the range -4 to 5 V is due to the biasing arrangement used in the attenuators that causes the operating point of the transistors to depend on the DC input voltage. Therefore, if a large

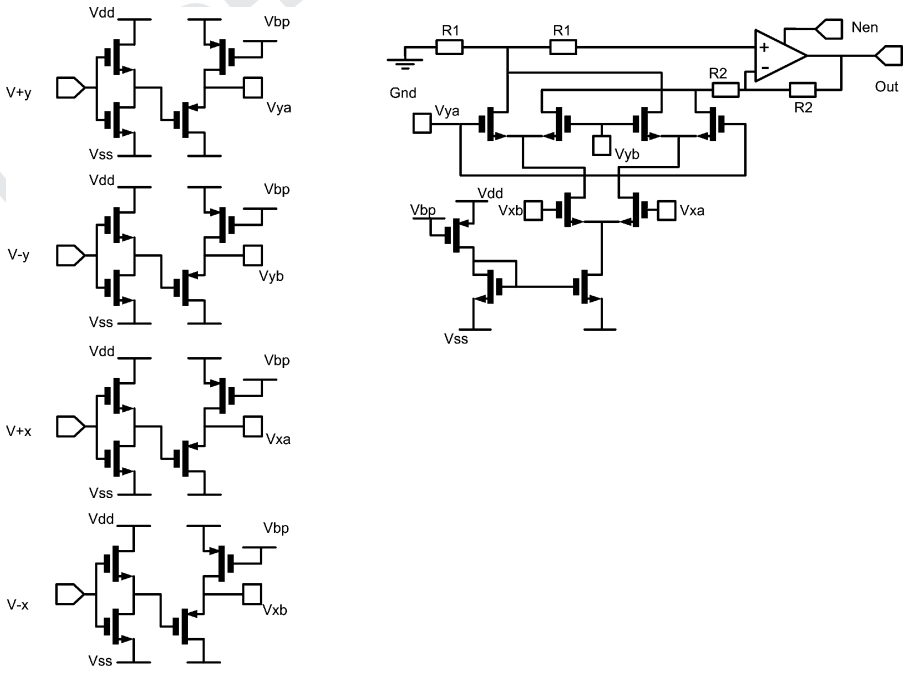

Fig. 6. Multiplier cell.

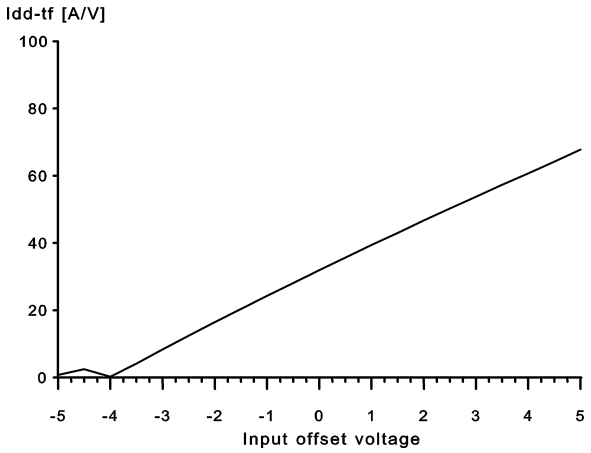

Fig. 7. Small signal input to supply current transfer response *Idd-tf* of the multiplier plotted against DC input offset.

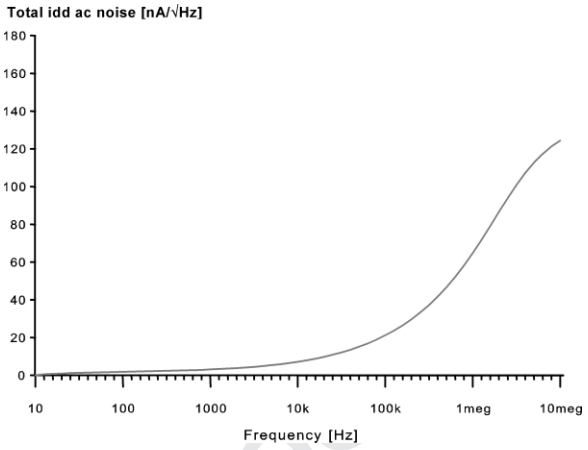

Fig. 8. Total integrated supply current noise with the input of the multiplier held at −3.75 V plotted versus frequency.

amplitude sinusoid is applied to this circuit, the supply current response will contain significant distortion. For the essentially linear AC small signal sensitivity analysis to give predictable results, a small amplitude sinusoid must be used.

The noise (thermal, "1/f", and shot) generated by the circuit must not mask the AC supply current generated by the input stimulus. A signal to noise test is used to determine the smallest amplitude of stimulus we could use. The noise analysis is performed at a DC offset relating to a minimum in the *Idd-tf* response. This is the DC offset voltage that will give the lowest amplitude AC supply current. A minimum in *Idd-tf* near a DC input offset of −4 V is seen in Fig. 7.

The fault free AC RMS supply current at a DC input offset of −3.75 V is approximately 1.5 μV at 1 MHz and 4.5 μV at 10 MHz, (just above the 7.5 MHz passband of the opamp) when stimulated with, for example a 0.25 V amplitude sinusoid. Fig. 8 shows the total noise at these frequencies is 65 nA/$\sqrt{}$Hz and 125 nA/$\sqrt{}$Hz respectively. The signal to noise ratios are 27 dB at 1 MHz and 31 dB at 10 MHz. These figures can be compared to the minimum noise ratios necessary for the transfer of video signals of 20–30 dB. Therefore even at high frequencies the supply current response will not be lost in noise. A 0.25 V amplitude stimulus can thus be used.

The next part of the algorithm consists of finding a set of stimuli and therefore an AC sensitivity analysis was performed for each virtual (10 MΩ resistor) short circuit fault injected into the multiplier at DC offsets of −3.75 volts to +3.75 volts. DC offsets outside this range caused distortion.

The maximum sensitivity for most of the faults considered occurred at the highest frequency 10 MHz and at the lowest DC offset −3.75 volts. However the relative change in fault free RMS supply current due to process variation also showed a maximum of ±90% with these stimuli parameters suggesting a possibility that many of the faults in the attenuators would be undetected. Using the weighted sensitivity measure defined in Eq. (10) the best test for the attenuators was at 3 MHz which has high sensitivity to the fault at this frequency but only ±30% relative deviation. A plot of the weighted sensitivity for a gate source short in one of the transistors of an attenuator is illustrated in Fig. 9.

Faults in the opamp showed a very high sensitivity at 10 MHz, approximately 10 times of that at

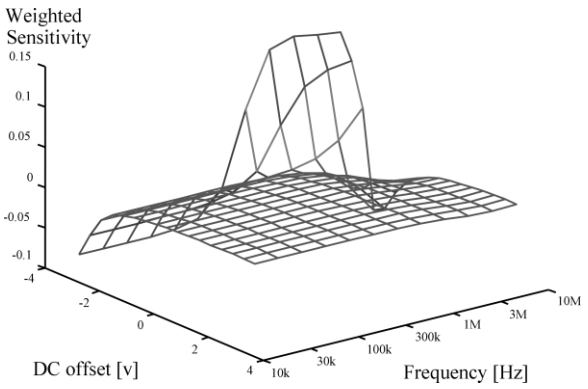

Fig. 9. The variation of process weighted sensitivity measured at the power supply terminal of the multiplier versus DC input offset and frequency of the input stimulus.

3 MHz offsetting the effect of process variation in the weighted sensitivity measure and so the 10 MHz signal at −3.75 V remains the best test. In summary, the four best test frequencies were 3 MHz (27 faults), 10 MHz (22 faults), 1.8 MHz (6 faults) and 560 kHz (4 faults), all at an offset of −3.75 V. These cover 59 out of the 77 short circuit faults considered. Other tests could be considered, for example +3.75 volts offset at a frequency of 10 MHz (1 fault). However these are unlikely to substantially increase the fault coverage the circuit, because these faults are likely to be covered by many different tests.

The algorithm described in Section 6 was then used to obtain the probability of detection and optimum input stimulus for each open and short fault considered. Using the algorithm is was possible to eliminate 28 out of a total of 199 clearly detectable or clearly undetectable faults prior to the Monte Carlo simulation stage. Moreover, since accurate Monte Carlo simulation was (for nearly all faults) only performed at one optimum stimulus, a considerable reduction simulation time was achieved. Tables 2 and 3 show the numbers of simulations required to fault simulate the opamp circuit using a brute force (i.e. simulate everything) approach versus that using the algorithm of Section 6. As can be seen, the number of simulations is reduced by over 5 times.

The results from the fault simulation are shown in Table 4. Many faults have probabilities of detection either towards 100% (totally detectable) or close to 0% (totally undetectable), because some faults have practically no influence on the RMS supply at all and those that do only required a small change in current to be close to 100% detectable. Faults for which the simulation converged were categorized into detectable, undetectable or partially detectable using a threshold of $PD_i = 0.5\%$. This was chosen arbitrarily based on 0.27%, the probability of a type I error (a good circuit classed as faulty), any higher accuracy would not be appropriate, since the cut-off value between faulty and fault free responses was assumed to be 3 standard deviations. 199 faults were considered.

Table 4. Fault coverage.

Classification	Probability of detection range	% number of faults
Detectable faults	$PD_i > 99.5\%$	36
Undetectable faults	$PD_i < 0.5\%$	16
Partially detectable faults	$0.5\% < PD_i < 99.5\%$	42
Simulation did not converge	N/A	6%

The results can also be expressed as an average probability of detection over all convergent faults, which in this case is 65%. The 42% faults classified as partially detectable are of the most interest. It was noted that certain faults produced a variance different to that of the fault free case; an example for a gate-drain short fault is shown in Fig. 5. This confirms the need for a full Monte Carlo simulation on both the faulty and fault free responses in such cases.

It is of particular interest to investigate a suitable value for the DIST test metric which can be used to eliminate clearly detectable faults whilst not incorrectly

Table 2. No. of simulations for "Brute Force" approach.

Simulation stage	Explanation	Total
Good Monte Carlo simulation	Stimuli × Monte Carlo runs: 6 × 30	180
Faulty Monte Carlo simulation	Stimuli × Monte Carlo runs × faults: 6 × 30 × 199	35820
Total		36000

Table 3. No. of simulations for hybrid fault simulation algorithm.

Simulation stage	Explanation	Total
Good Monte Carlo simulation	Stimuli × Monte Carlo runs: 6 × 30	180
Initial single simulation	Stimuli × faults—stimuli for faults that are already detectable: 6 × 199 – 36	1158
Faulty Monte Carlo simulation	(Faults—eliminated faults) × Monte Carlo runs: (199 − (11 + 17 + 8)) × 30	4890
Extra Monte Carlo simulations	Faults which failed KS test × Monte Carlo runs: 6 × 30	180
Total		6408

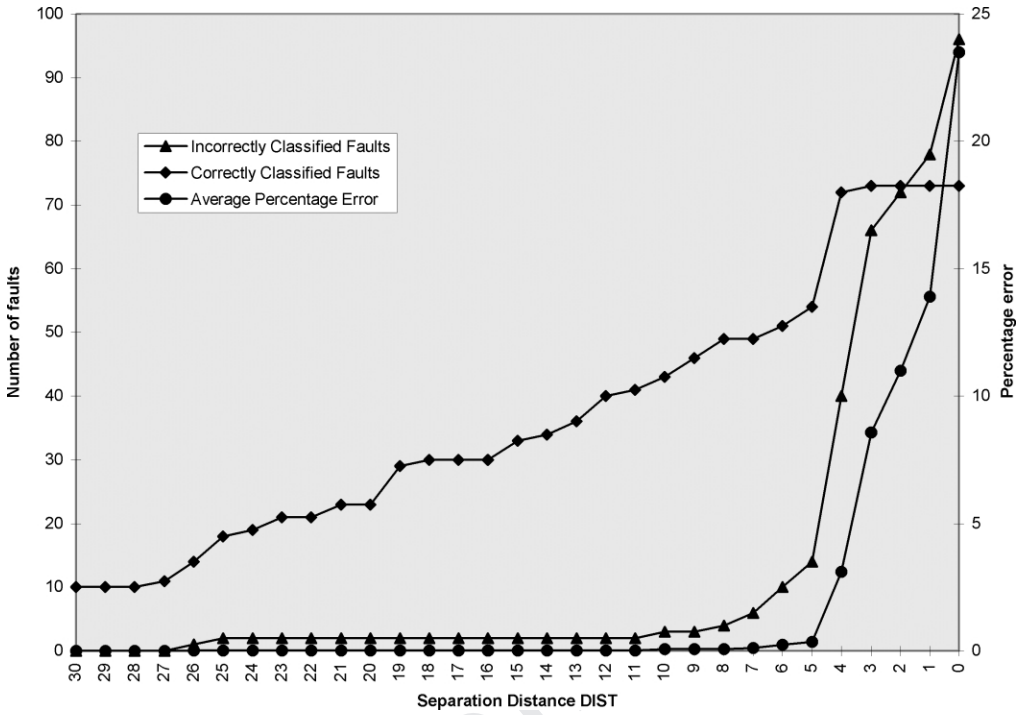

Fig. 10. Fault classification and percentage probability of detection error.

classifying undetectable faults. The problem here is that the process parameter spread effect on each faulty circuit is not known at the stage in the algorithm where clearly detectable faults are eliminated, and the cut-off value must be set at a high value. The graph in Fig. 10 shows the number of incorrectly classified and correctly eliminated faults as a function of the DIST cut-off value. Clearly if the separation distance is reduced then the number of faults dropped increases, which would lead to savings in simulation time, but at the expense of an increased number of incorrectly classified faults. The percentage error in the average probability of detection figure is also plotted because it indicates the effect of the overall error caused by the incorrectly classified faults.

Care must also be taken when considering the error in probability of detection, however, if the relative probabilities of fault occurrence are to be taken into consideration using a technique such as IFA. A small error in a fault which is highly likely to occur will produce a higher overall inaccuracy than that which is unlikely to occur. Further work should incorporate this additional parameter into the hybrid fault simulation algorithm.

In order to evaluate the effect of the fault model resistance value on the results, the experiment was repeated using 500 Ω in place of 1 Ω in the short fault model for Monte Carlo simulations. It was found that the maximum difference in probability of detection for any one fault was 22%; the average over all 79 short faults was however less than 2%. Thus in this case the effect of higher resistance fault models is minimal on the overall fault test quality.

8. Conclusions

This paper has described the principle of an automatic test generation and verification technique for analog circuits. It has been shown to be both effective and easy to implement (suitable for test automation). The approach is directed specifically at the generation of stimuli for structural tests in order to detect catastrophic faults in analog circuits, using RMS supply current monitoring, but is not restricted to supply current tests. Tests for sampled circuits could be derived if they were first converted to the continuous time domain and the appropriate fault models employed [14].

The stimulus is generated by choosing the frequency and DC offset of a sinusoid that has the highest sensitivity to faulty behavior but a low susceptibility to process parameter change. The test is then verified with fault simulation, using an initial low accuracy simulation followed by a very accurate Monte Carlo simulation for those faults that are marginal cases. Thus, excessive fault simulation effort is avoided whilst still retaining accurate results and generating optimum tests. For each fault considered, a measure of detectability is calculated based on probability theory that takes into account the likely variation in supply current due to process parameter deviations. Using a mixture of fault simulation approaches (hybrid fault simulation) has reduced simulation time to the point where it is feasible without significant loss of accuracy.

Although in this case the fault coverage figures were not high for either resistance of fault model employed, all faults which were classed as undetectable were found to have little effect on the functionality of the circuit, passing a specification test. Those faults that were classed as partially detected, mostly in the opamp would need other tests, perhaps measuring the RMS of the output voltage. Further work needs to be done to automatically derive such tests. +An alternative is to modify the circuit, to reduce the masking effect of the attenuators.

Further work should focus on the application of the test algorithm to sampled circuits and other structural test methodologies. In addition, further automation of the test stimulus generation technique is required to include circuits that have multiple inputs. Furthermore to increase confidence in the results, the entire spectrum of bridging resistances should be considered within the fault simulation scheme. Clearly, as this approach relies on the sensitivity calculations, the circuit under consideration must be operating in a linear region. Highly nonlinear circuits cannot be analyzed using this approach and therefore may need to be partitioned. Again, this is a subject for further work.

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