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Single, double and surround gate vertical MOSFETs with reduced parasitic capacitance

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Abstract

The vertical MOSFET structure is one of the solutions for reducing the channel length of transistors under 50 nm. Surround gates can be easily realised in vertical MOSFETs which offer increased channel width per unit silicon area. In this paper, a low overlap capacitance, surround gate, vertical MOSFET technology is presented. A new process that uses spacer or fillet local oxidation is developed to reduce the overlap capacitance between the gate and the source/drain electrodes. Electrical characteristics of surround gate n-MOSFETs are presented and compared with characteristics from single gate and double gate devices on the same wafer. Transistors with channel length down to 100 nm have been realised. They show good symmetry between the source on top and source on bottom configuration and subthreshold slope down to 100 mV. The short channel effects of the surround gate MOSFETs are investigated.

Keywords: Vertical MOSFETs; Parasitic capacitance; FILOX; Surround gate; Double gate

1. Introduction

Surround gate vertical MOS transistors built on the sidewalls of vertical pillars [1–7] have been developed for four main reasons:

- surround gate or double gate structures allow more channel width per unit of silicon area; this leads to an increase of the drive current per unit area;
- the better control of the substrate depletion region in thin, fully depleted pillars reduces the short channel effects;
- the gate length is controlled by non-lithographic methods; this allows the realisation of shorter channel lengths than using photolithography;
- the gate length is decoupled from the packing density; for RAM applications, long channel transistors (with lower off currents) can be produced without decreasing the number of devices per unit area.

One of the main problems inherent to the vertical layout is the overlap capacitance associated with the gate contact as shown in Fig. 1. In vertical MOSFETs the contact is created via a polysilicon track that overlaps onto the top of the pillar and onto the bottom electrode. This results in large overlap capacitances between the gate track and the source–drain electrodes, which are only separated by a thin gate oxide in the traditional vertical layout (Fig. 1A).

Several solutions to this problem have been proposed. In one approach the pillar was selectively grown by epitaxial deposition in a well etched in a previously deposited oxide/polysilicon/oxide stack. The channel length was defined by epitaxy. The gate oxide was grown

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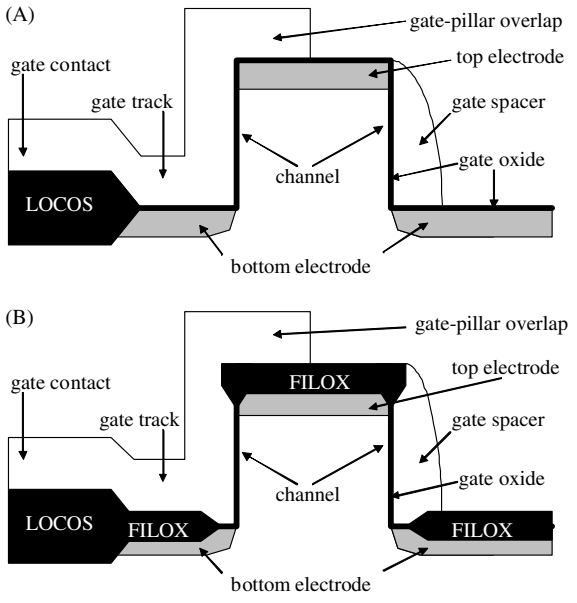

Fig. 1. Cross-section of a ion implanted vertical MOSFET. (A) The overlap between the gate track and the electrode, due to alignment tolerance, gives rise to parasitic capacitance in the traditional structure. (B) The FILOX process allows to reduce the overlap capacitance.

either before or after the epitaxial deposition [8,9]. Another solution is the vertical replacement gate transistor, in which the source/drain electrodes are defined by solid state diffusion after epitaxial growth of the substrate. The gate oxide was grown before [10] or after [11] the epitaxial deposition of the channel.

The main disadvantage of the above epitaxial approaches is that they are not CMOS compatible. Ion implanted vertical MOSFETs [12] use non-lithographic methods to define the channel length and are CMOS compatible. Unfortunately in these devices it is very difficult to reduce the gate/source–drain overlap capacitance because the gate must be deposited and patterned after the source–drain implant. One way to overcome this problem is the amorphisation of the silicon surface by a high dose and low energy implant which increases the oxidation rate on planar surfaces [13]. However this process only gives a small increase in oxide thickness.

We have developed a fully CMOS compatible self-aligned second oxidation process, called spacer of fillet local oxidation (FILOX) that allows to reduce gate overlap capacitance in ion implanted vertical MOS transistors (Fig. 1B) [14]. A similar process has been applied in the past to the fabrication of planar transistors [15]. In this case the objective was a reduction of the source/drain junction capacitance in planar MOSFETs.

In this paper we shortly describe the FILOX process and focus on the electrical characterisation of NMOS vertical transistors with channel length down to 100 nm. A comparison is made between transistors with a surround gate, a double gate and a single gate fabricated on the same wafer. Short channel effects of the surround gate vertical NMOS transistors are analysed.

2. Spacer or fillet local oxidation

2.1. Process

Fig. 2 shows a schematic of the process steps in the FILOX process [16]. After etching of the pillar or trench of the vertical MOSFET, a thin stress relief oxide is grown over the structure. A nitride layer is deposited over the pillar by chemical vapor deposition (Fig. 2A). First the nitride layer and then the stress relief oxide are anisotropically etched to expose the silicon substrate on the horizontal surfaces, while leaving nitride fillets on the sidewalls of the pillar (Fig. 2B). A subsequent local oxidation will result in the growth of an oxide layer on all exposed planar surfaces, except on the protected vertical channel area (Fig. 2C). After the removal of the nitride fillets by wet etch, the grown oxide covers the active area, while the vertical sidewalls of the pillar only contain the thinner original stress relief oxide which doubles up as sacrificial oxide. After removal of the stress relief oxide by wet etch and growth of a thin gate oxide the extra oxide in the trench and on top of the pillar will reduce the

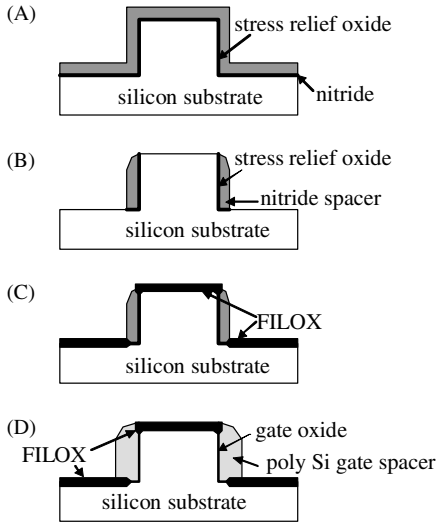

Fig. 2. Principle of the fabrication of vertical MOSFETs with the FILOX process: (A) stress relief oxide and nitride deposition; (B) nitride and oxide anisotropic etch to leave nitride spacers on the sidewalls of the pillar; (C) growth of thick oxide on all planar surfaces; (D) wet etch of nitride fillets and pad oxide, gate oxidation, gate polysilicon deposition and patterning.

parasitic capacitance by a factor equal to the ratio of the gate oxide and the FILOX oxide.

A concept similar to the FILOX was developed independently by Oh [17]. In that case were fabricated test structures in which the LOCOS oxidation was extended up to the nitride spacer. The use of a second thinner oxidation (FILOX) in our process enables the fabrication of vertical NMOS transistors.

2.2. FILOX process characterisation

A separate study was performed in order to characterise the formation of the FILOX oxide and its interaction with the nitride spacer with the consequent formation of bird's beaks on the sidewall and on the bottom of the pillar. Test structures were fabricated by reactive ion etching of Si pillars. A 5 nm stress relief oxide was grown, followed by a 70 nm Si_3N_4 layer. The spacer or FILOX was a 40 nm wet oxide grown at 1000 °C. Fig. 3 shows a TEM micrograph of a pillar capacitor just after the fillet oxidation. The original pillar height before oxidation was derived from profilometer measurements and its height of 215 nm is shown as a dashed line in the figure. It can be seen that the nitride fillet is slightly over etched by 25 nm with regard to the original pillar height. The figure shows clearly the influence of the FILOX oxidation on the oxide thickness. At the bottom of the pillar the nitride fillet protects the Si channel very well against oxide encroachment and no bird's beak is visible. However, at the top of the pillar significant oxide encroachment has caused an increase of the oxide thickness on the sidewall extending almost to the bottom of the pillar.

2.3. Process simulations

To investigate the oxide encroachment, the FILOX process was simulated using Silvaco's package "ATHENA". The oxidation process took place at 1000 °C which is a high enough temperature to allow viscous flow of the oxide, and this flag was switched on in the simulations. Using the default parameters for the nitride viscosity [18,19] (3.8×10^{16} g cm^{-1} s^{-1}), the experimental results shown in Fig. 3 could not be reproduced; it results in a similar encroachment of the oxide at the top of the pillar as on the bottom. However, by reducing the nitride viscosity slightly (1.64×10^{16} g cm^{-1} s^{-1}), the experimental results could be reproduced. These results can be understood by realizing that the thickness of the nitride spacer perpendicular to the oxide–nitride interface is much larger at the bottom of the pillar than at the top of the pillar. When the nitride viscosity is reduced to allow oxidation at the interface, the oxidation will in the first instance only happen at the top of the pillar where it is easier for the oxide to bend the nitride spacer [20]. The experimental results correspond almost exactly with the maximum achievable difference in encroachment between the top and bottom oxide. More details on the simulations of the FILOX process and on the effects of mechanical stress on the nitride spacer can be found in [14].

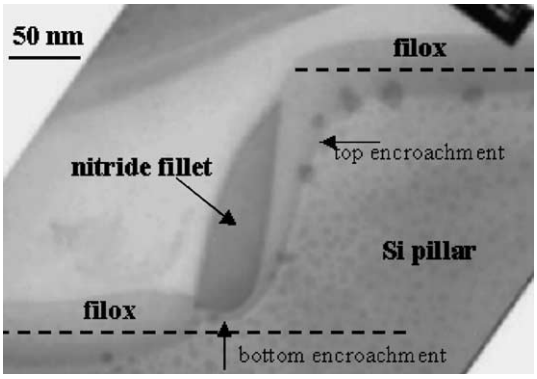

Fig. 3. TEM cross-section of the FILOX process directly after the oxidation (see text for details).

3. Transistor fabrication

3.1. Process

Single, double and surround gate vertical NMOS transistors incorporating the FILOX process were fabricated. Boron-doped (10–33 Ω cm) (1 0 0) wafers served as the starting material. A p-type body was formed with boron implantation (5×10^{14} cm^{-2}, 50 keV), followed by dry etch of the Si pillars to a height of about 300 nm. A 20 nm stress relief oxide was thermally grown at 900 °C to relieve the stress between the ensuing nitride layer and the silicon. Silicon nitride was deposited to a thickness of 130 nm at 740 °C (Fig. 2A). The active area was defined by patterning the nitride layer using an anisotropic dry etch. Then the field oxide was created with a standard LOCOS process, thermally growing a 600 nm thick oxide layer at 1000 °C.

At this stage the FILOX process took place. The nitride layer and the stress relief oxide were dry etched; this resulted in the formation of 130 nm wide nitride spacers on the sidewalls of the pillar (Fig. 2B). Subsequently an oxide layer 60 nm thick was thermally grown at 1000 °C (Fig. 2C). The area protected by the nitride spacers was not affected by the oxide growth; thus a thick oxide layer was formed on the whole active area and on the top of the pillar. A substrate contact was created with boron implantation (5×10^{15} cm^{-2}, 47 keV). Self-aligned source/drain electrodes were implanted (arsenic, 6×10^{15} cm^{-2}, 150 keV). This was followed by a selective wet etch in orthophosphoric acid at 160 °C in

order to remove the nitride fillets. Another wet etch in HF was performed to remove the stress relief oxide; a precise etch timing removes all stress relief oxide, leaving an approximately 40 nm thick FILOX oxide. A 3 nm gate oxide was thermally grown on the sidewall of the pillar at 900 °C. Then a 200 nm in-situ doped (arsenic, 5×10^{19} cm^{-3}) polysilicon layer was deposited by LPCVD and patterned by dry etch. In this way polysilicon spacers were created all around the pillar (Fig. 2(D)).

The polysilicon track connecting the polysilicon spacers to the gate contact was protected from the etch by a resist mask. Fig. 4 shows that mask alignment tolerances and minimum feature dimension of the lithography node prevent a reduction of the overlapping surface of the gate track.

Another mask was used to selectively remove by isotropic dry etch the remaining polysilicon spacers, creating single, double and surround gate devices on the same wafer (Fig. 5). A 600 nm thick oxide isolation layer was then deposited and an RTA at 1100 °C for 10 s was performed for dopant activation. Finally contacts were etched and metal deposited and patterned. A photograph of the fabricated surround gate vertical transistor is shown in Fig. 6.

3.2. Structural characterisation

The FILOX process provides a gate overlap capacitance that is lower than in the standard process. The reduction in overlap capacitance is achieved by the approximately 40 nm thick FILOX oxide layer that is grown on all planar surfaces instead of the 3 nm thick gate oxide. The SEM cross-section in Fig. 7 shows the active transistor area of the fabricated MOSFETs.

Several factors contribute to reduce the gate overlap capacitance. First, the thick FILOX oxide reduces the gate/source overlap capacitance between the gate track and the active area at the bottom of the pillar. Second, the nitride spacer used in the FILOX process was much thinner than the gate spacer, which allows the FILOX oxide to extend beneath the gate and reduce the gate/source overlap capacitance. Third, the FILOX oxide on top of the pillar reduces the gate/drain overlap capacitance where the gate track overlaps onto the top of the pillar. Fourth, both the nitride spacer and the polysilicon gate spacer were over-etched, which reduces the gate/drain overlap capacitance on the side of the pillar.

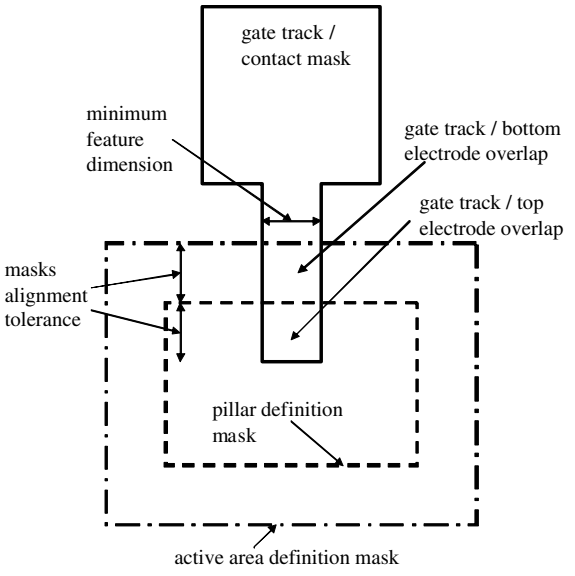

Fig. 4. Mask layout showing the gate track/top and bottom electrode overlap. The reduction of the overlapping surface is limited by mask alignment tolerance and minimum feature dimension.

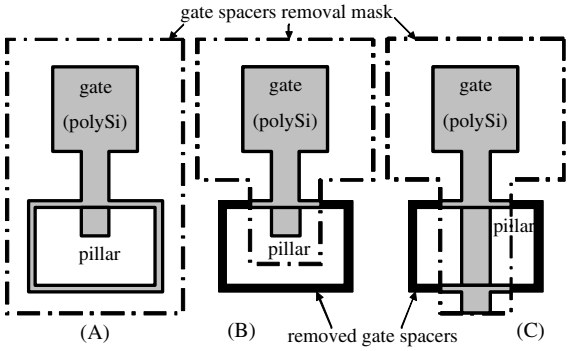

Fig. 5. Mask layout showing the utilization of the gate spacers removal mask in order to obtain surround gate (A), single gate (B) and double gate (C) vertical MOS transistors.

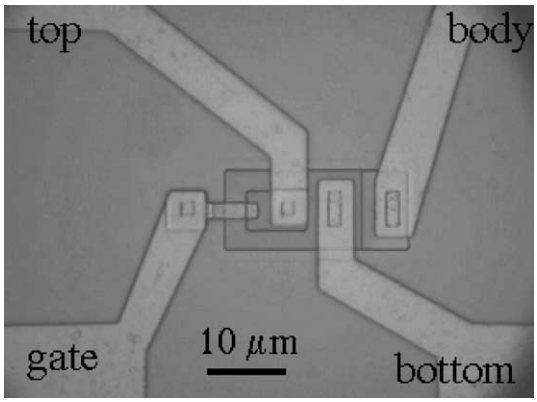

Fig. 6. Top view of a surround gate ion-implanted vertical NMOS transistor showing the overlap of the gate track with active area and pillar. The total channel width of the depicted transistor is 24 μm.

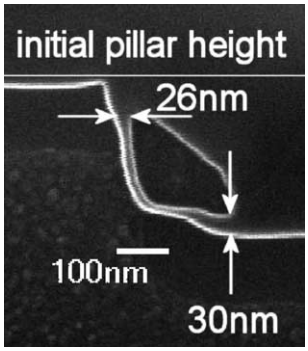

Fig. 7. Field emission SEM cross-section of a surround gate ion-implanted vertical NMOS transistor fabricated with the FILOX process. Both pillar top and bottom show a thick FILOX oxide visible under the gate electrode.

Finally, the FILOX bird's beaks reduce the gate/drain overlap capacitance on the pillar sidewall and the gate/source overlap capacitance at the bottom of the pillar.

4. Electrical characteristics

4.1. Transistors electrical characterisation

The transistors were characterised by a HP4155A semiconductor analyser. Figs. 8–10 show the transfer characteristics of surround, double and single gate transistors with estimated channel length of 125 nm respectively. Fig. 11 shows the output characteristic of the surround gate transistors. All results show measurements in both configurations: source on top and source on bottom of the pillar.

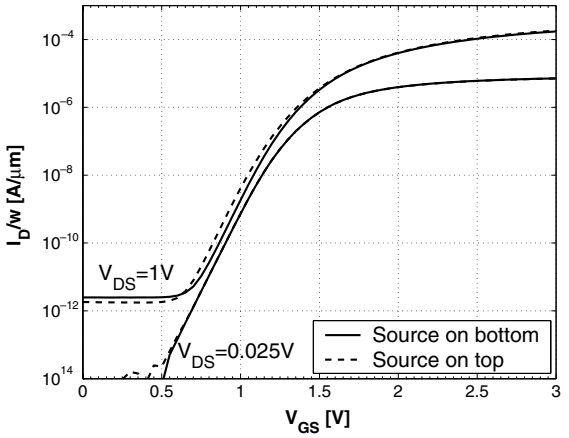

Fig. 8. Transfer characteristic of a surround gate vertical NMOS transistor with channel width = 24 μm and approximate channel length = 125 nm; $V_S = V_B = 0$ V.

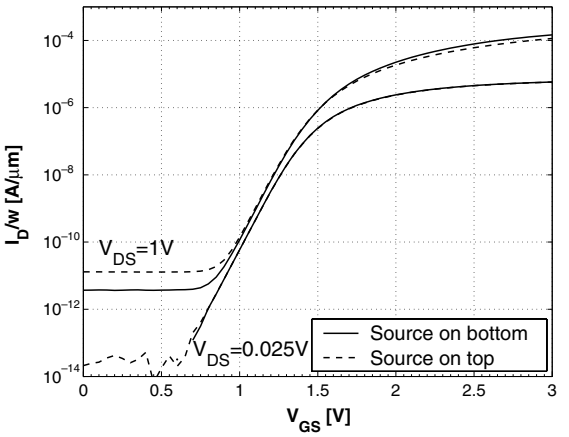

Fig. 9. Transfer characteristic of a double gate vertical NMOS transistor with channel width = 9 μm and approximate channel length = 125 nm; $V_S = V_B = 0$ V.

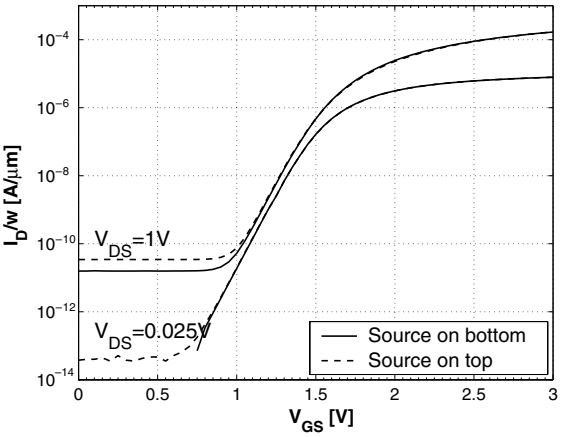

Fig. 10. Transfer characteristic of a single gate vertical NMOS transistor with channel width = 4.5 μm and approximate channel length = 125 nm; $V_S = V_B = 0$ V.

Very little asymmetry is observed, due to the low series resistances of both electrodes. This is due to the high percentage of activation of the dopants implanted to form the source and drain contact and to the transistor layout that minimizes source and drain series resistances.

Van der Pauw sheet resistance measurements [21] have been performed on test structures implanted with the same dose as the source/drain electrodes. An average value of 49 Ω/□ has been measured, which constitutes and acceptable value for MOSFET devices [22].

In the off-state operation mode the transistors show a drain leakage current which is independent of the gate voltage, but increases with increasing drain voltage. The off-state leakage current is less than 10^{-14} A/μm for $V_{DS} = 0.025$ V and increases to about 10^{-12} A/μm for

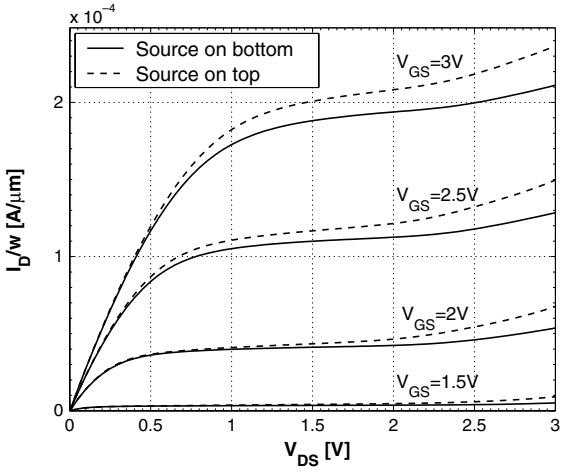

Fig. 11. Output characteristic of a surround gate vertical NMOS transistor with channel width = 24 μm and approximate channel length = 125 nm; $V_S = V_B = 0$ V.

$V_{DS} = 1$ V for the surround gate NMOS transistors (Fig. 8). To find the origin of this leakage, the currents from all electrodes of the devices have been measured simultaneously. This shows that the leakage current origins from the reverse biased drain-substrate diode.

The best electrical results in terms of subthreshold slope and leakage current minimization are achieved with the surround gate transistor (Table 1). This is because in this device the gate fillets cover the whole side of the pillar and the gate controls the substrate depletion region throughout the pillar perimeter. On the contrary, in the double and single gate transistors the areas where the fillets have been removed (Fig. 5) are not controlled by the gate during the off-state operation of the transistors. This gives rise to enhanced source–drain leakage currents and to subthreshold slope degradation in the short-channel devices.

MOSFETs with various channel widths have been fabricated. Measurements were performed in order to evaluate the precision of the transfer of the channel width drawn on the mask on the real devices fabricated. With this objective the on-state drain current with constant gate voltage overdrive ($V_{GS} - V_t = 1$ V, $V_{DS} = 1$ V) has been measured and plotted as a function of the layout channel width for surround, single and double gate MOSFETs (Fig. 12). In this way it is possible to directly correlate measured electrical parameters with the mask layout of the MOSFETs. Fig. 12 shows that the on-state drain current varies approximately linearly with the channel width, as expected, within transistors with the same structure. If a comparison between single, double and surround gate transistors is attempted, the direct proportionality between the two parameters is not perfect due to the process differences in the fabrication of the devices. Nevertheless, the linear relation between on-state drain current and channel width is still approximately valid. Table 1 shows the values of important electrical parameters measured on vertical NMOS transistors with single, double and surround gate and approximate channel length of 125 nm.

4.2. Short channel effects of surround gate vertical NMOS transistors

Due to non-uniformity of the dry etch during the pillar definition, a distribution of pillar heights has been

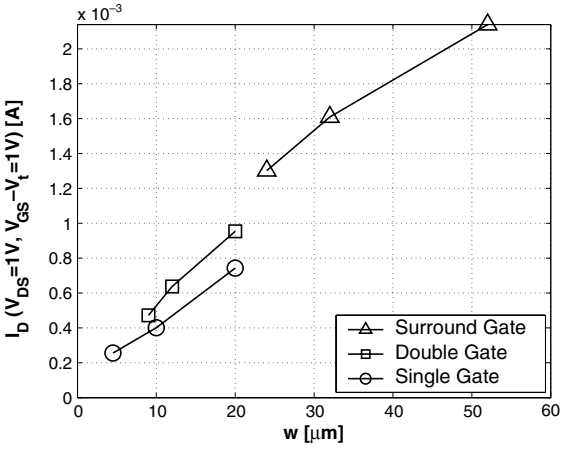

Fig. 12. On-state drain current as a function of the channel width (obtained from the mask layout) of single, double and surround gate NMOS transistors with approximate channel length of 130 nm; $V_S = V_B = 0$ V.

Table 1
Measured parameters of typical transistors with estimated channel length = 125 nm (w = channel width; S = subthreshold slope; V_t = threshold voltage; $I_{D,on}$ = on-state drain current for $V_{GS} - V_t = 1$ V; $I_{D,off}$ = off-state drain current for $V_{GS} = 0$ V)

	w (μm)	V_{DS} (V)	S (mV)	V_t (V)	$I_{D,on}$ (A/μm)	$I_{D,off}$ (A/μm)
Surround gate	24	0.025	107	1.36	6.13×10^{-6}	$<10^{-14}$
Surround gate	24	1	109	1.20	7.68×10^{-5}	2.49×10^{-12}
Double gate	9	0.025	113	1.54	4.69×10^{-6}	$<10^{-14}$
Double gate	9	1	111	1.44	7.20×10^{-5}	3.68×10^{-12}
Single gate	4.5	0.025	114	1.59	6.55×10^{-6}	$<10^{-14}$
Single gate	4.5	1	117	1.44	8.22×10^{-5}	1.57×10^{-11}

obtained (profilometer measurements). This results in a variation between 100 and 130 nm of the channel length of the devices fabricated. A rough analysis of the short channel effects [22] of the devices has thus been possible.

Fig. 13 shows the measured threshold voltage for the surround gate layout as a function of the channel length. The threshold voltage has been calculated using the linear drain current extrapolation method both for low ($V_{DS} = 0.025$ V) and high ($V_{DS} = 1$ V) drain voltages. The results show a decrease in the value of the threshold voltage with decreasing channel length. The difference between the high-V_{DS} and low-V_{DS} behaviour increases for the shortest channel lengths. This is expected, because for short channel lengths the gate loses control of the substrate depletion region. This short channel effect increases with the drain–source voltage, because of drain induced barrier lowering (DIBL).

A comparison of transfer characteristics of surround gate NMOS transistors with different channel length for $V_{DS} = 0.025$ V is shown in Fig. 14. DIBL values comprised between 200 mV (100 nm channel length) and 50 mV (130 nm channel length) were measured for $V_{DS} = 1$ V and 0.025 V. This results show good control of short channel effects for devices down to 100 nm channel length. This is achieved through a high boron body doping concentration of about 10^{19} cm^{-3}.

The drawback of this simple approach to reduce short channel effects by increasing the body doping are fairly high subthreshold swing values, because of the high body-effect coefficient [22] of the transistors. The subthreshold swing varies between 100 and 120 mV/dec (Table 1), values far from the ideal MOSFET subthreshold swing (60 mV/dec). The conservative gate oxide thickness used in the experiments (3 nm) further degrades this parameter by increasing the body-effect coefficient of the devices.

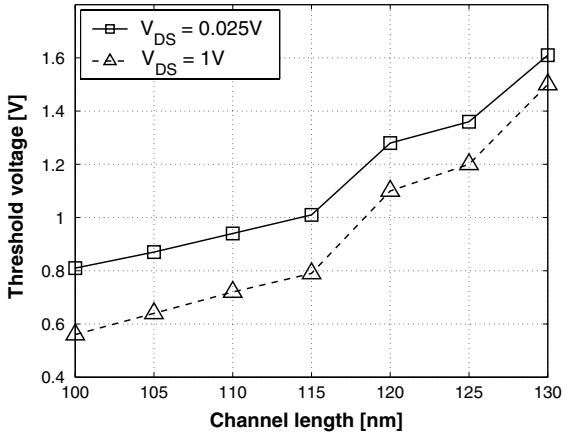

Fig. 13. Threshold voltage of a surround gate vertical NMOS transistor with channel width of 24 μm as a function of the estimated channel length; $V_S = V_B = 0$ V.

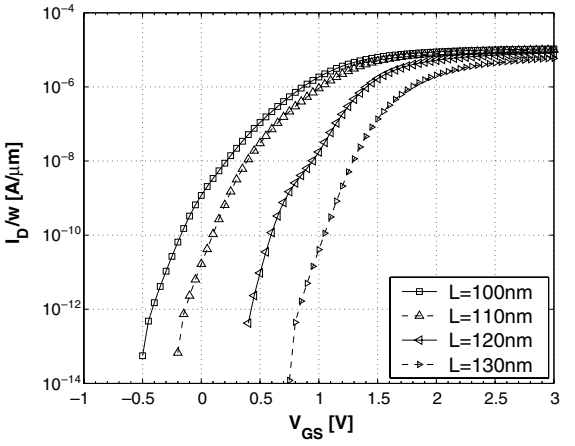

Fig. 14. Transfer characteristics of a surround gate vertical NMOS transistor with channel width = 24 μm and approximate channel lengths down to 100 nm. The applied drain voltage is 0.025 V; $V_S = V_B = 0$ V.

In Fig. 15 the measured on-state drain current for the surround gate vertical NMOS transistor has been plotted as a function of the channel length. The values have been measured both with a constant gate voltage ($V_{GS} = 3$ V) and with a constant gate voltage overdrive ($V_{GS} - V_t = 1$ V). All measurements show a strong dependence of the on-state drain current on channel length, both when the gate voltage is maintained constant and when the gate voltage overdrive is kept constant.

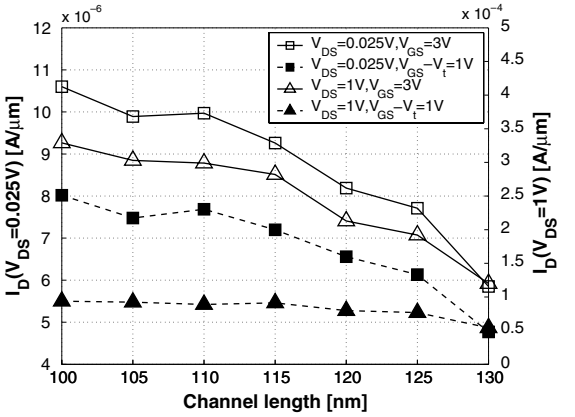

Fig. 15. On-state drain current of a surround gate vertical NMOS transistor with channel width of 24 μm as a function of the estimated channel length; $V_S = V_B = 0$ V; the squares show the values measured for $V_{DS} = 0.025$ V (left axis) while the triangles represent the measurements obtained applying $V_{DS} = 1$ V (right axis).

4.3. Evaluation of capacitance reduction due to the FILOX process

As shown in the previous sections, the FILOX process does not alter the transistor operation, indicating that the gate oxide is not degraded by the FILOX oxidation. Although direct probing of the intrinsic capacitance of the transistors is impossible due to their small size, calculations based on SEM micrographs, and process and device simulations have been used to give an estimate of the expected capacitance reduction. This takes place both below the gate track and below the gate spacers and is strongly dependent on the nitride spacer thickness and on the lithography node.

A quantitative comparison was made of a planar MOSFET, a standard vertical MOSFET and a vertical MOSFET with FILOX. The comparison was done for a state of the art 100 nm industrial planar MOSFET technology with a 20 nm source/drain extensions junction depth, a 40 nm HDD junction depth, a 2 nm gate oxide, a 60 nm channel length, a 100 nm minimum feature size and a 50 nm alignment tolerance. For the vertical MOSFETs, the source/drain junction depth was scaled to 40 nm, the nitride spacer thickness to 40 nm, the polysilicon gate thickness to 60 nm and the FILOX was 40 nm thick. The components of overlap capacitance were assumed to be in the same proportion as those in Fig. 7. An STI field oxide was used for consistency with the 100 nm technology, as illustrated in Fig. 16. To normalize the results, all devices had channels 1 μm wide.

The results of the calculations are summarised in Fig. 17. As the vertical MOSFETs are not symmetrical, the source on bottom configuration was chosen to compare the devices. Comparing the two vertical transistors, the FILOX process reduces the drain overlap capacitance by a factor of 2.6 from 5.2×10^{-16} to 2×10^{-16} F and the source overlap capacitance by a factor of 3.3 from 1.5×10^{-15} to 4.5×10^{-16} F. Comparing the vertical FILOX transistor with the lateral transistor, the FILOX vertical MOSFET has a 1.7 times lower drain capacitance and a 1.3 higher source capacitance than the lateral MOSFET. Thus the FILOX process allows to fabricate vertical MOSFETs with overlap capacitance values much lower than the traditional vertical devices and similar to the lateral technology. A further reduction in source capacitance could be obtained by reducing the thickness of the nitride fillet in the FILOX process.

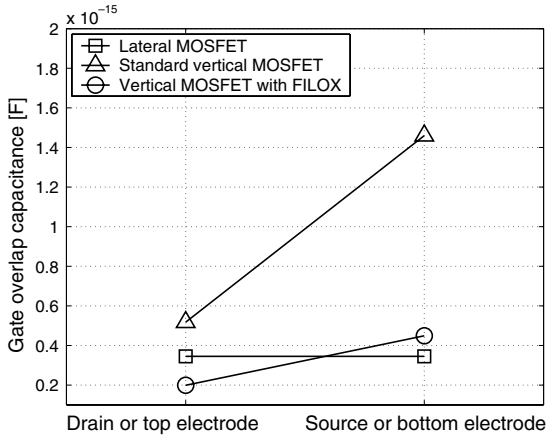

Fig. 17. Gate/source and gate/drain overlap capacitances calculated on the simplified MOSFETs shown in Fig. 17 with a 100 nm industrial technology design rules.

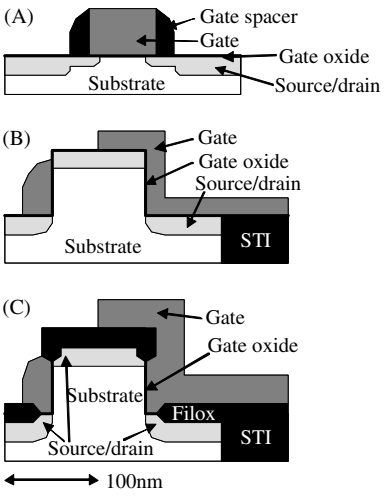

Fig. 16. Simplified cross-sections of MOSFETs using a 100 nm industrial technology to compare gate overlap capacitance: (A) planar MOSFET, (B) standard vertical MOSFET, (C) vertical MOSFET with FILOX.

5. Conclusions

For the first time surround, single and double gate vertical MOSFETs have been fabricated on a single wafer using a new spacer or FILOX process. Channel lengths down to 100 nm with a gate oxide 3 nm thick have been realised. The process uses implanted sources and drains and hence is CMOS-compatible.

Electrical results for single, double and surround gate transistors have been presented. They show good symmetry between source on top and source on bottom of the pillar configuration, low leakage current and a subthreshold slope down to 100 mV/dec. The short channel effects of the surround gate vertical MOSFET have been analysed and plots of measured threshold voltage and on-state drain current as a function of the channel length shown. Devices with various channel widths have been fabricated and electrically characterised, showing that a

good control of the channel width has been achieved in all transistor structures fabricated.

A quantitative comparison has been made of the overlap capacitance of the FILOX vertical MOSFET and a conventional lateral MOSFET using a 100 nm baseline technology. The drain overlap capacitance of the vertical MOSFET is a factor of 1.7 times lower and the source overlap capacitance a factor of just 1.3 times higher than in the lateral MOSFET. These results demonstrate the effectiveness of the FILOX process in reducing gate overlap capacitance in vertical MOSFETs.

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